LINEAR INTEGRATED CIRCUITS

TYPES TL091M, TL091I, TL091C, TL092M, TL092I, TL092C, ~~TL094M, TL094I, TL094C~~ JFET-INPUT OPERATIONAL AMPLIFIERS

D2585, OCTOBER 1981—REVISED MAY 1982

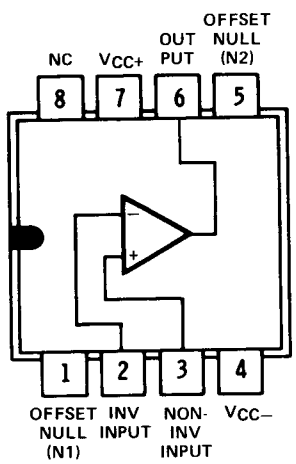
- Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies
- Class AB Output Stage
- High-Impedance N-Channel-JFET Input Stage . . . 10^{12} Ω typical
- Internal Frequency Compensation
- Short-Circuit Protection
- Input Common-Mode Range Includes V_{CC-}
- Low Input Offset Current . . . 50 pA typical
- Low Input Bias Current . . . 200 pA typical

description

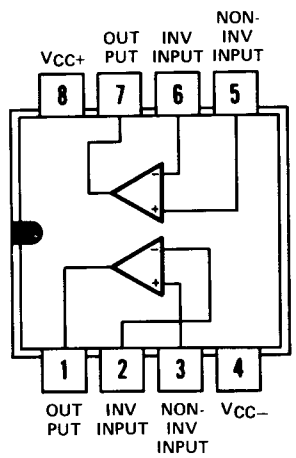
The TL091 JFET input operational amplifier family is similar in performance to the MC3403 family but with much higher input impedance derived from a FET input stage. The N-channel-JFET input stage provides a typical input impedance of 10^{12} ohms, a typical input offset current of 50 picoamperes, a typical input bias current of 200 picoamperes, and allows a common-mode input voltage range that includes the negative supply voltage. The TL091 family is designed to operate from a single supply over a range of 3 to 36 volts. Operation from split supplies is also possible provided the difference between the two supplies is 3 to 36 volts. Output voltage range is typically from V_{CC-} to 1.7 volts less than V_{CC+} with a 10-kilohm load resistor to V_{CC-}.

Device types with an "M" suffix are characterized for operation over the ~~full military~~ temperature range of −55 °C to 125 °C, those with an "I" suffix are characterized for operation from −25 °C to 85 °C, and those with a "C" suffix are characterized for operation from 0 °C to 70 °C.

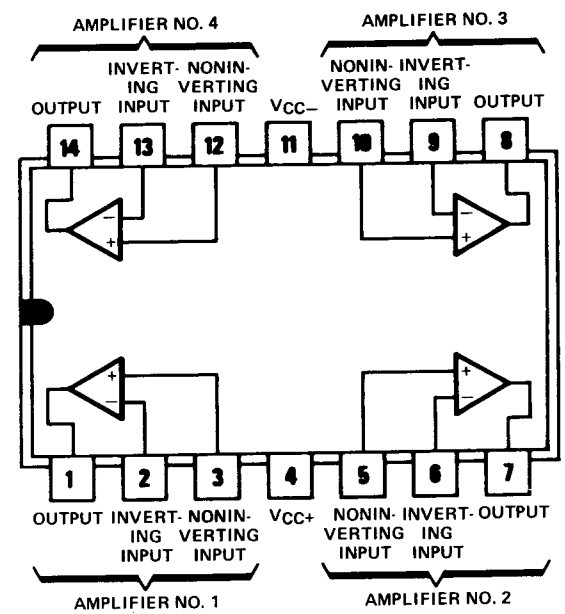
TL091
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



TL092
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



TL094
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



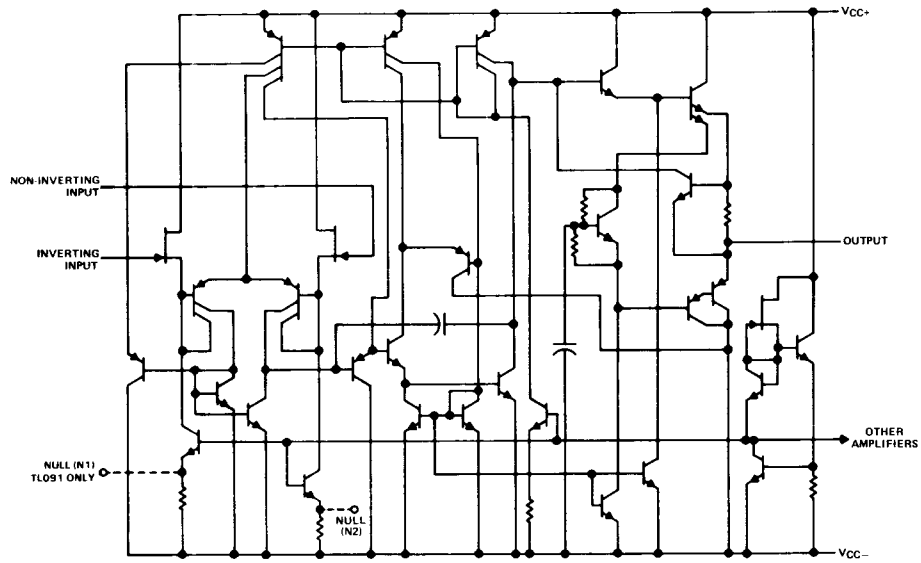
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582

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL091M TL092M TL094M	TL091I TL092I TL094I	TL091C TL092C TL094C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	36	V
Differential input voltage (see Note 2)		±36	±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	±18	V
Continuous total dissapation at (or below) 25°C free-air temperature (see Note 4)	J Package	1375	1025	1025	mW
	JG Package	1050	825	825	
	N Package		1150	1150	
	P Package		1000	1000	
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	J or JG Package	300	300	300	°C
Lead temperature 1/16 inch (,6 mm) from case for 10 seconds	N or P Package		260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-} minus 0.3 V.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J and JG packages. TL09_M chips are alloy-mounted; TL09_I and TL09_C chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1375 mW	11.0 mW/°C	25°C
J (Glass-Mounted Chip)	1025 mW	8.2 mW/°C	25°C
JG (Alloy-Mounted Chip)	1050 mW	8.4 mW/°C	25°C
JG (Glass-Mounted Chip)	825 mW	6.6 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL091M TL092M TL094M			TL091I TL092I TL094I			TL091C TL092C TL094C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	T_A = 25°C, $R_S \leq 50\ \Omega$			5	9		5	9		5	15	mV
		T_A = full range, $R_S \leq 50\ \Omega$				15			15			20	
αV_{IO}	Temperature coefficient of input offset voltage	T_A = 25°C			10			10			10		μV/°C
I_{IO}	Input offset current§	T_A = 25°C			50	200		50	200		50	200	pA
		T_A = full range				20			10			5	nA
I_{IB}	Input bias current§	T_A = 25°C			200	400		200	400		200	400	pA
		T_A = full range				50			20			10	nA
V_{ICR}	Common-mode input voltage range‡	T_A = 25°C		V_{CC-} to 12	V_{CC-} to 13		V_{CC-} to 12	V_{CC-} to 13		V_{CC-} to 12	V_{CC-} to 13		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L = 2 kΩ,	T_A = 25°C	±10	±13		±10	±13		±10	±13		
		R_L = 2 kΩ,	T_A = full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	T_A = 25°C	50	200		20	200		20	200		V/mV
			T_A = full range	25			15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%	R_L = 2 kΩ, T_A = 25°C,		9			9			9		kHz
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C	V_O = 50 mV,		1			1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, T_A = 25°C	R_L = 2 kΩ,		60°			60°			60°		
r_i	Input resistance	f = 20 Hz,	T_A = 25°C		10^{12}			10^{12}			10^{12}		Ω
r_o	Output resistance	f = 20 Hz,	T_A = 25°C		75			75			75		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, $V_{IC} = V_{ICR}$	T_A = 25°C	70	90		70	90		70	90		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	R_S = 50 Ω, V_{CC} = ±2.5 V to ±15 V	T_A = 25°C	75	90		75	90		75	90		dB
I_{OS}	Short-circuit output current	T_A = 25°C	$V_O = V_{CC+}$		65			65			65		mA
			$V_O = V_{CC-}$		−30			−30			−30		
I_{CC}	Total supply current per amplifier	No load, T_A = 25°C	V_O = 0 V,		1.5	2.5		1.5	2.5		1.5	2.5	mA

†All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL094M; −40°C to 85°C for TL094I, and 0°C to 70°C for TL094C.

‡The V_{ICR} limits are directly linked volt-for-volt to supply voltage, i.e., the positive limit is 3 volts less than V_{CC+}.

§Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL091M, TL092M, TL094M			TL091I, TL092I, TL094I			TL091C, TL092C, TL094C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, $R_S \leq 50\ \Omega$		5	9		5	9		5	15	mV
I_{IO}	Input offset current§	V_O = 2.5 V		50	200		50	200		50	200	pA
I_{IB}	Input bias current§	V_O = 2.5 V		200	400		200	400		200	400	pA
V_{OM}	Peak output voltage swing¶	R_L = 10 kΩ to gnd	3.3	3.5		3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ to gnd, V_{CC} = 5V to 30V	$V_{CC+}-1.7$			$V_{CC+}-1.7$			$V_{CC+}-1.7$			
A_{VD}	Large-signal differential voltage amplification	ΔV_O = 1.6 V, R_L = 2 kΩ	20	200		20	200		20	200		V/mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	R_S = 50 Ω, V_{CC} = ±3 V to ±15 V	75			75			75			dB
I_{CC}	Supply current (per amplifier)	V_O = 2.5 V, No load		1.5	2.5		1.5	2.5		1.5	2.5	mA
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz		120			120			120		dB

†All characteristics are specified under open-loop conditions.

§Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

¶The output will swing essentially to ground provided that the load resistor, R_L, is connected from the output to ground.

operating characteristics: V_{CC+} = ±15 V, T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, See Figure 1	C_L = 100 pF,	R_L = 2 kΩ,		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, See Figure 1	C_L = 100 pF,	R_L = 2 kΩ,		0.2		μs
t_f	Fall time					0.2		μs
	Overshoot factor					20%		
	Crossover distortion	V_{IPP} = 30 mV,	V_{OPP} = 2 V,	f = 10 kHz		1%		
V_n	Equivalent input Noise voltage	R_s = 100 Ω,	f = 1 kHz			34		$nV/\sqrt{Hz}$

PARAMETER MEASUREMENT INFORMATION

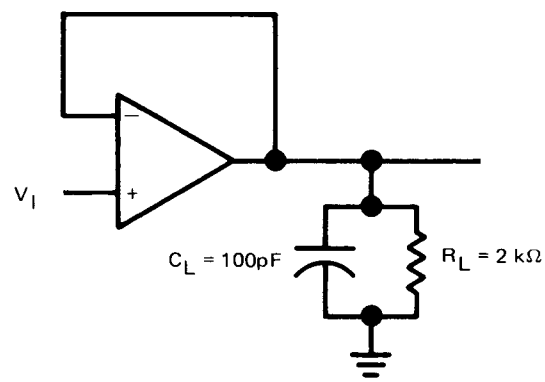


FIGURE 1–UNITY-GAIN AMPLIFIER

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