DATA SHEET

CBT6820

20-bit bus switch with precharged outputs and Schottky undershoot protection for live insertion

Product specification

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Philips
Semiconductors

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20-bit bus switch with precharged outputs and Schottky undershoot protection for live insertion

CBT6820

FEATURES

- TTL compatible inputs and outputs
- 5Ω switch connection between two port A and port B
- Thin shrink small outline (TSSOP)
- Undershoot protection included to prevent shoot through level changes
- Bias voltage pre-charges the outputs to minimize signal distortion during live insertion

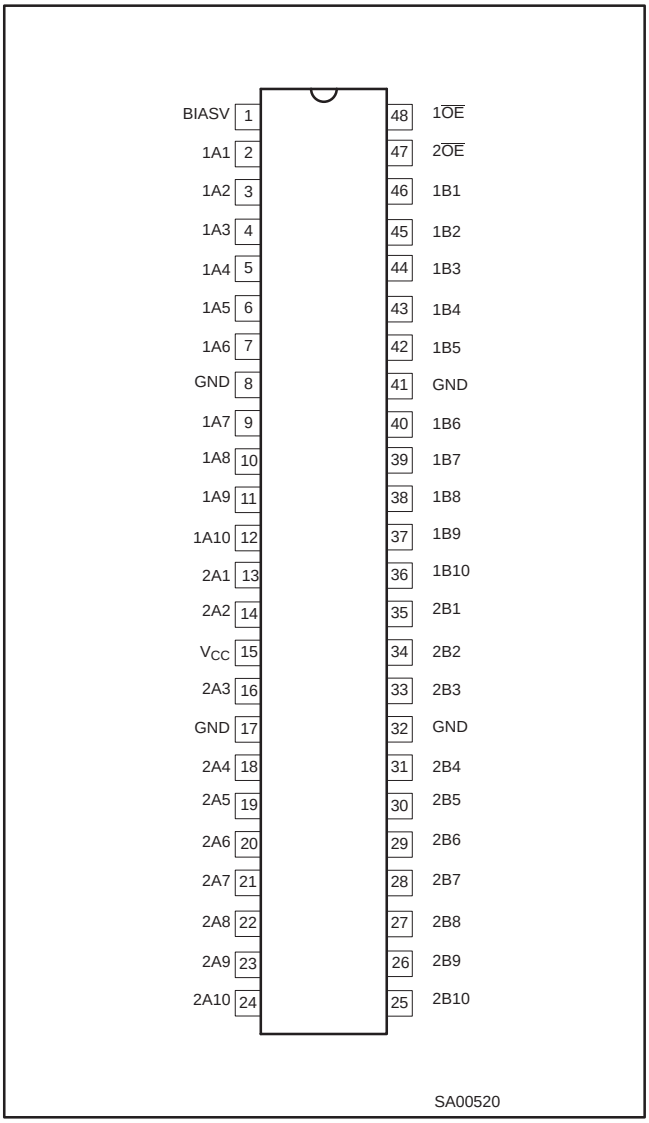
DESCRIPTION

The CBT6820 provides twenty bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bi-directional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as two 10-bit switch with individual enable (OE) input. When OE is low, the switch is on and port A is connected to port B. When OE is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

Special clamp circuitry and Schottky diode clamps to ground are used to prevent an under voltage on the A side (Vin < GND) from causing the B side precharge voltage to drop below the "1" state.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH}/t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF, V_{CC} = 5 V	0.25	ns
C_{IN}	Input capacitance		4.5	pF
$C_{I/O}$	Input/output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	9.5	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic TSSOP Type II	–40°C to +85°C	CBT6820 DGG	CBT6820 DGG	SOT362–1

PIN DESCRIPTION

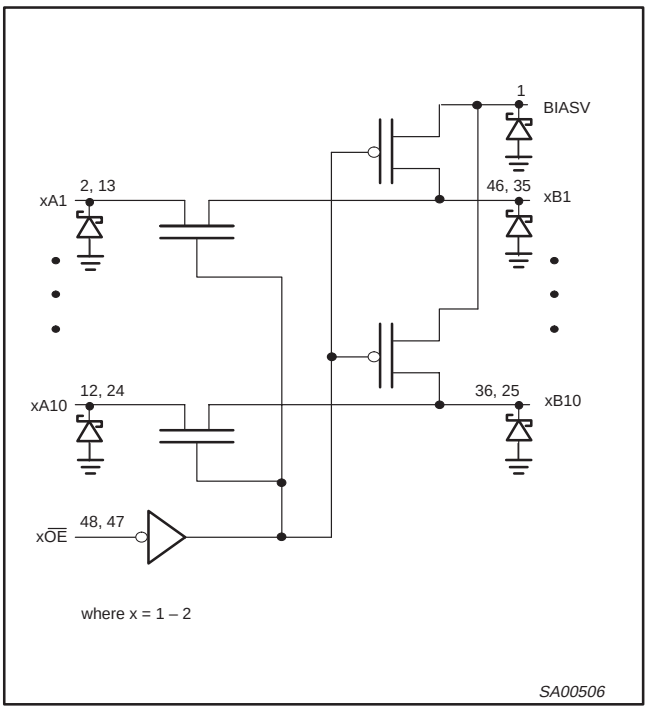
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	BIASV	Bias voltage
2, 3, 4, 5, 6, 7, 9, 10, 11,12	1A1–1A10	Port 1A1 to Port 1A10
8, 17, 32, 41	GND	Ground (V)
13, 14, 16, 18, 19, 20, 21, 22, 23, 24	2A1–2A10	Port 2A1 to Port 2A10
15	V_{CC}	Positive supply voltage
35, 34, 33, 31, 30, 29, 28, 27, 26, 25	2B1–2B10	Port 2B1 to Port 2B10
46, 45, 44, 43, 42, 40, 39, 38, 37, 36	1B1–1B10	Port 1B1 to Port 1B10
48, 47	$1\overline{OE}$, $2\overline{OE}$	Switch enables

FUNCTION TABLE

$\overline{OE}$	STATE
L	A Port = B Port
H	A Port = Z
H	B Port = BIASV

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC clamp diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[1]		–0.5 to +7.0	V
I_{SW}	DC continuous channel current	V_O = 0 to V_{CC}	±128	mA
V_{BIASV}	DC bias voltage		–0.5 to +7.0	V
T_{stg}	Storage temperature range		–65 to 150	°C
øJA	Plastic thin shrink small outline package (TSSOP)		104	°C/W

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.0	5.5	V
BIASV	DC supply voltage	1.3	V_{CC}	V
V_{IH}	High-level input voltage (control pin)	2.0		V
V_{IL}	Low-level Input voltage (control pin)		0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = –40°C to +85°C			
			Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_I = –18mA			–1.2	V
I_I	Input leakage current (control pin)	V_{CC} = 5.5V; V_I = GND or 5.5V			±5	µA
I_O	Output bias current (B pins)	V_{CC} = 4.5V; BiasV = 2.4V; V_O = 0, $\overline{OE}$ = V_{CC}			–0.25	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; I_O = 0, V_I = V_{CC} or GND			2.5	mA
ΔI_{CC}	Control pins[2]	V_{CC} = 5.5V, one input at 3.4V, other inputs at V_{CC} or GND			2.5	mA
C_I	Input capacitance per $\overline{OE}$ pin	V_I= 3V or 0		4.5		pF
$C_{O(OFF)}$	Capacitance per port (OFF-state)	V_O = 3V or 0; switch off		9.5		pF
r_{on}[3]	On-resistance	V_{CC} = 4.5V; V_I = 0V; I_I = 64mA		5	7	Ω
		V_{CC} = 4.5V; V_I = 0V; I_I = 30mA		5	7	
		V_{CC} = 4.5V; V_I = 2.4V; I_I = –15mA		10	15	
V_P	Pass voltage	V_{IN} = V_{CC} = 4.5V; I_{out} = –100µA	3.4	3.6	3.9	V
I_{USP}	Undershoot static current protection[4]	V_{CC} = 5.0V, V_{Bias} = V_{CC} I_B = –5µA, $V_B \geq$ 3.0V		–10		mA

NOTES:
1. All typical values are at VCC = 5V, TA = 25 C
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On–state resistance is determined by the lowest voltage of the two (A or B) terminals.
4. Force I_{USP}, measure $V_B \geq 3V$

AC CHARACTERISTICS FOR V_{CC} = 5.0V ±0.5V RANGE

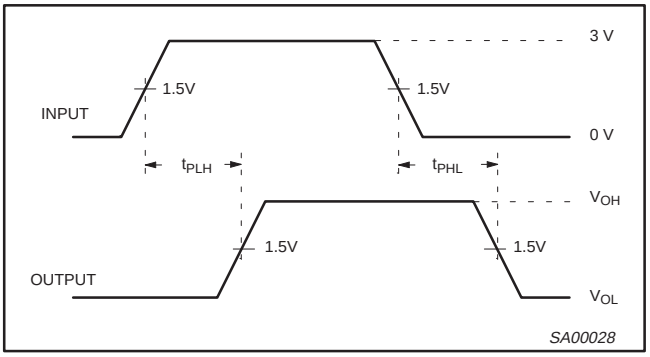
GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = –40 to +85°C			
			MIN	TYP[1]	MAX	
t_{pd}	Propagation delay; An to Bn; Bn to An[2]	1			0.25	ns
t_{PZH}	3-State output enable time OE to An; OE to Bn; BIASV = GND	2	1.3	3.1	5.3	ns
t_{PZL}	3-State output enable time OE to An; OE to Bn; BIASV = 3.0V	2	1.4	2.9	4.6	ns
t_{PHZ}	3-State output enable time $\overline{OE}$ to An; $\overline{OE}$ to Bn; BIASV = GND	2	1.7	2.8	4.5	ns
t_{PLZ}	3-State output enable time $\overline{OE}$ to An; $\overline{OE}$ to Bn; BIASV = 3.0V	2	2.8	4.4	6.6	ns

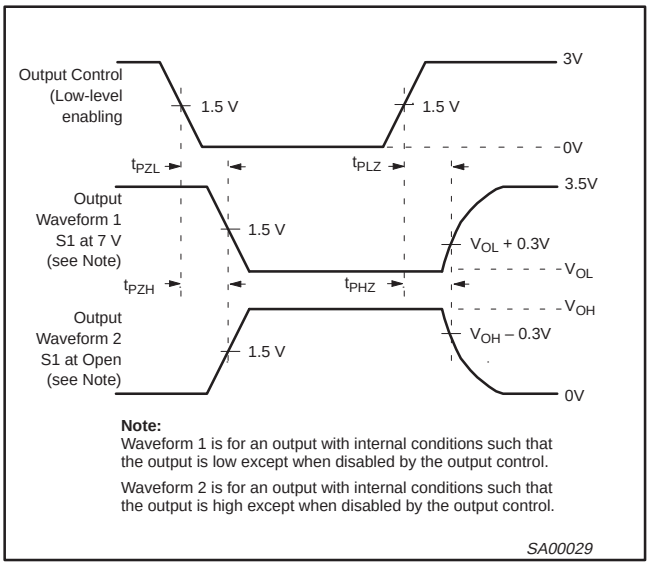
NOTE:
1. All typical values are measured at T_{amb} = 25°C and V_{CC} = 5.0V
2. Warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50pF, when driven by an ideal voltage source (zero output impedance)

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

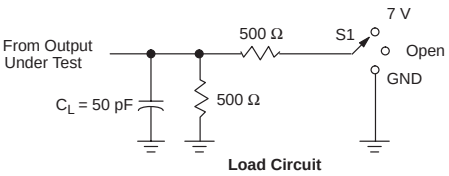


Waveform 1. Waveforms Showing the Input (An) to Output (Bn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

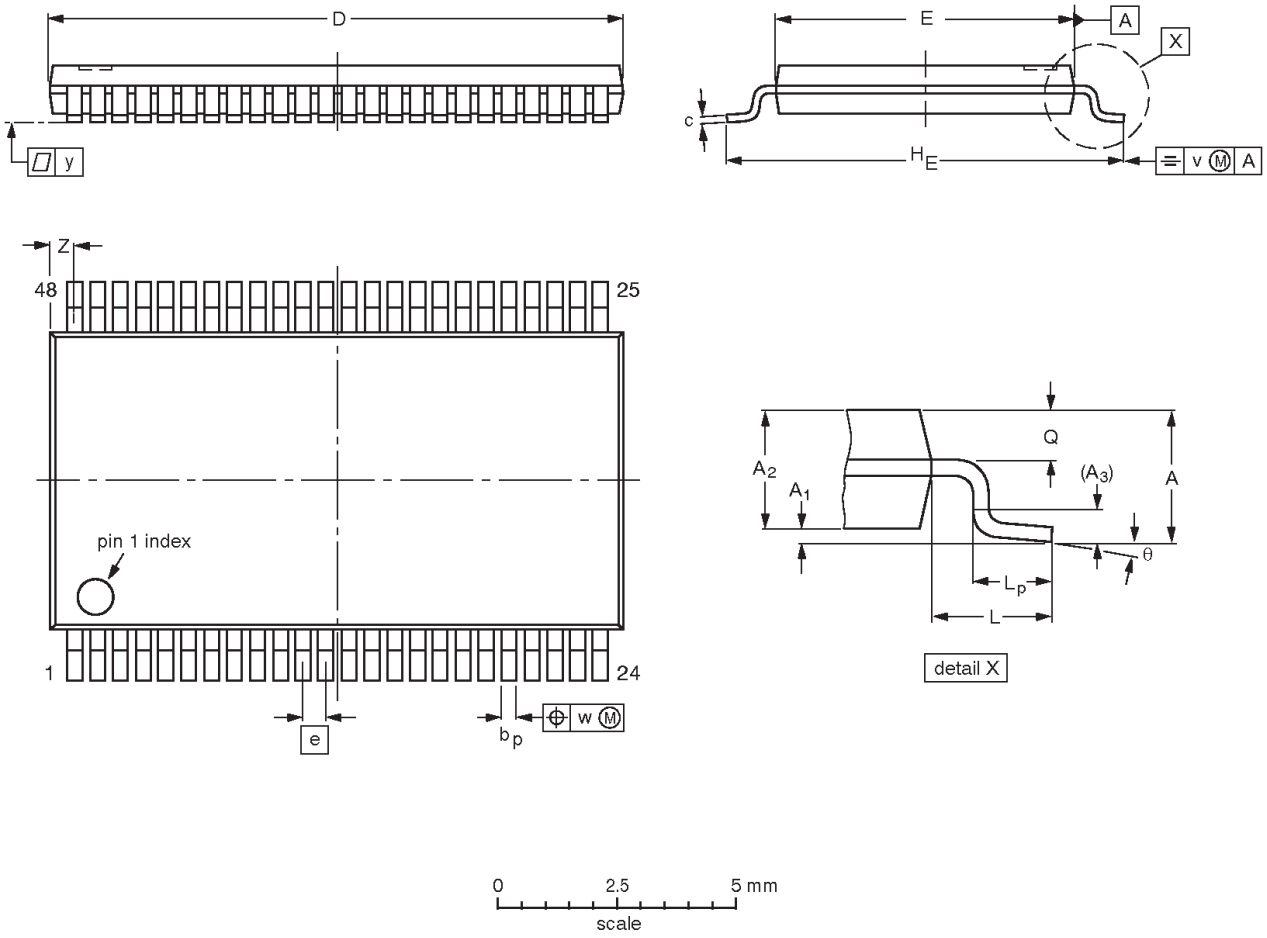
DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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