National Semiconductor

February 21, 2008

ADC12DS105
Dual 12-Bit, 105 MSPS A/D Converter with Serial LVDS Outputs

General Description

The ADC12DS105 is a high-performance CMOS analog-to-digital converter capable of converting two analog input signals into 12-bit digital words at rates up to 105 Mega Samples Per Second (MSPS). The digital outputs are serialized and provided on differential LVDS signal pairs. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. The ADC12DS105 may be operated from a single +3.0V or 3.3V power supply. A power-down feature reduces the power consumption to very low levels while still allowing fast wake-up time to full operation. The differential inputs accept a 2V full scale differential input swing. A stable 1.2V internal voltage reference is provided, or the ADC12DS105 can be operated with an external 1.2V reference. The selectable duty cycle stabilizer maintains performance over a wide range of clock duty cycles. A serial interface allows access to the internal registers for full control of the ADC12DS105's functionality. The ADC12DS105 is available in a 60-lead LLP package and operates over the industrial temperature range of −40°C to +85°C

Features

- Clock Duty Cycle Stabilizer
- Single +3.0 or 3.3V supply operation
- Serial LVDS Outputs
- Serial Control Interface
- Overrange outputs
- 60-pin LLP package, (9x9x0.8mm, 0.5mm pin-pitch)

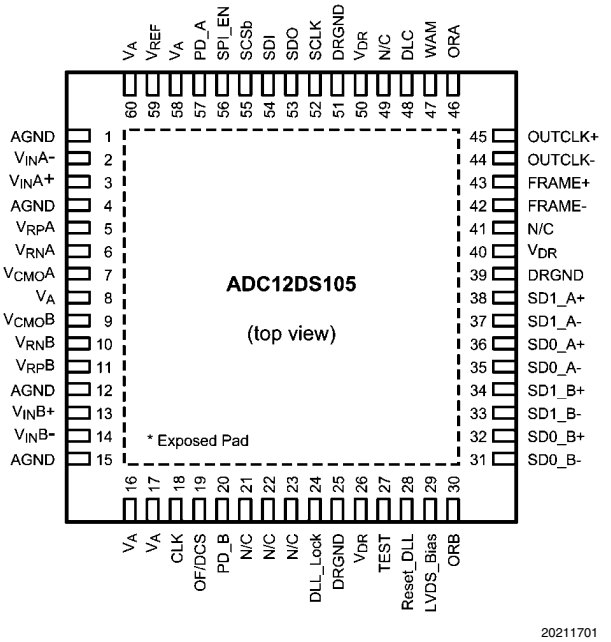
Key Specifications

Resolution	12 Bits
Conversion Rate	105 MSPS
SNR (f_{IN} = 240 MHz)	68.5 dBFS (typ)
SFDR (f_{IN} = 240 MHz)	83 dBFS (typ)
Full Power Bandwidth	1 GHz (typ)
Power Consumption	1 W (typ)

Applications

- High IF Sampling Receivers
- Wireless Base Station Receivers
- Test and Measurement Equipment
- Communications Instrumentation
- Portable Instrumentation

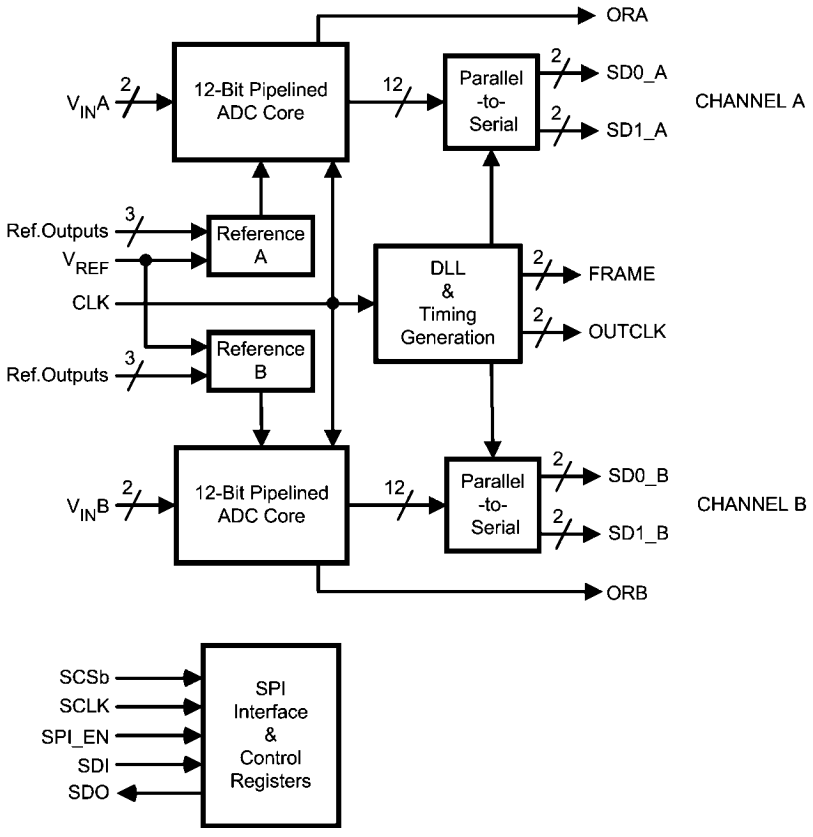
Connection Diagram



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Block Diagram

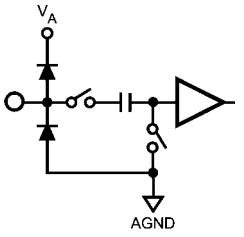
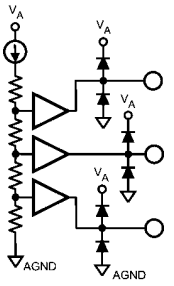
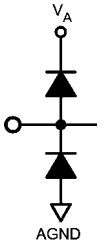
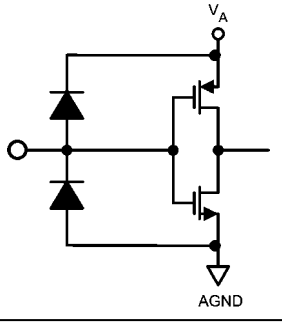
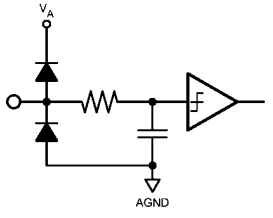


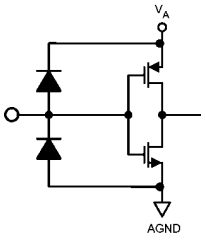
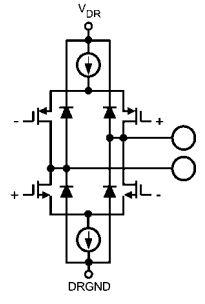
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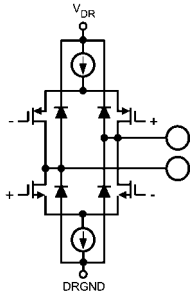
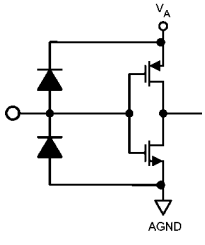
Ordering Information

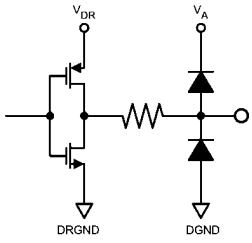
Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC12DS105CISQ	60 Pin LLP
ADC12DS105LFEB	Evaluation Board for Input Frequency < 70 MHz

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
3 13	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. The differential full-scale input signal level is $2V_{P-P}$ with each input pin signal centered on a common mode voltage, V_{CM}.
2 14	$V_{IN}A-$ $V_{IN}B-$		
5 11	$V_{RP}A$ $V_{RP}B$		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. An 0201 size 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 1 µF capacitor should be placed in parallel. V_{RP} and V_{RN} should not be loaded. V_{CMO} may be loaded to 1mA for use as a temperature stable 1.5V reference. It is recommended to use V_{CMO} to provide the common mode voltage, V_{CM}, for the differential analog inputs.
7 9	$V_{CMO}A$ $V_{CMO}B$		
6 10	$V_{RN}A$ $V_{RN}B$		
59	V_{REF}		Reference Voltage. This device provides an internally developed 1.2V reference. When using the internal reference, V_{REF} should be decoupled to AGND with a 0.1 µF and a 1µF, low equivalent series inductance (ESL) capacitor. This pin may be driven with an external 1.2V reference voltage. This pin should not be used to source or sink current.
29	LVDS_Bias		LVDS Driver Bias Resistor is applied from this pin to Analog Ground. The nominal value is 3.6KΩ
DIGITAL I/O			
18	CLK		The clock input pin. The analog inputs are sampled on the rising edge of the clock input.
28	Reset_DLL		Reset_DLL input. This pin is normally low. If the input clock frequency is changed abruptly, the internal timing circuits may become unlocked. Cycle this pin high for 1 microsecond to re-lock the DLL. The DLL will lock in several microseconds after Reset_DLL is asserted.
19	OF/DCS		This is a four-state pin controlling the input clock mode and output data format. OF/DCS = V_A, output data format is 2's complement without duty cycle stabilization applied to the input clock OF/DCS = AGND, output data format is offset binary, without duty cycle stabilization applied to the input clock. OF/DCS = (2/3)*V_A, output data is 2's complement with duty cycle stabilization applied to the input clock OF/DCS = (1/3)*V_A, output data is offset binary with duty cycle stabilization applied to the input clock. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.

Pin No.	Symbol	Equivalent Circuit	Description
57 20	PD_A PD_B		This is a two-state input controlling Power Down. PD = V_A, Power Down is enabled and power dissipation is reduced. PD = AGND, Normal operation. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
27	TEST		Test Mode. When this signal is asserted high, a fixed test pattern (101001100011 msb->lsb) is sourced at the data outputs. With this signal deasserted low, the device is in normal operation mode. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
47	WAM		Word Alignment Mode. In single-lane mode this pin must be set to logic-0. In dual-lane mode only, when this signal is at logic-0 the serial data words are offset by half-word. With this signal at logic-1 the serial data words are aligned with each other. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
48	DLC		Dual-Lane Configuration. The dual-lane mode is selected when this signal is at logic-0. With this signal at logic-1, all data is sourced on a single lane (SD1_x) for each channel. Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.
45 44	OUTCLK+ OUTCLK-		Serial Clock. This pair of differential LVDS signals provides the serial clock that is synchronous with the Serial Data outputs. A bit of serial data is provided on each of the active serial data outputs with each falling and rising edge of this clock. This differential output is always enabled while the device is powered up. In power-down mode this output is held in logic-low state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
43 42	FRAME+ FRAME-		Serial Data Frame. This pair of differential LVDS signals transitions at the serial data word boundaries. The SD1_A+/- and SD1_B+/- output words always begin with the rising edge of the Frame signal. The falling edge of the Frame signal defines the start of the serial data word presented on the SD0_A+/- and SD0_B+/- signal pairs in the Dual-Lane mode. This differential output is always enabled while the device is powered up. In power-down mode this output is held in logic-low state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.

Pin No.	Symbol	Equivalent Circuit	Description
38 37	SD1_A+ SD1_A-		Serial Data Output 1 for Channel A. This is a differential LVDS pair of signals that carries channel A ADC's output in serialized form. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode each sample's output is provided in succession. In Dual-Lane mode every other sample output is provided on this output. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
34 33	SD1_B+ SD1_B-		Serial Data Output 1 for Channel B. This is a differential LVDS pair of signals that carries channel B ADC's output in serialized form. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode each sample's output is provided in succession. In Dual-Lane mode every other sample output is provided on this output. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
36 35	SD0_A+ SD0_A-		Serial Data Output 0 for Channel A. This is a differential LVDS pair of signals that carries channel A ADC's alternating samples' output in serialized form in Dual-Lane mode. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode this differential output is held in high impedance state. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
32 31	SD0_B+ SD0_B-		Serial Data Output 0 for Channel B. This is a differential LVDS pair of signals that carries channel B ADC's alternating samples' output in serialized form in Dual-Lane mode. The serial data is provided synchronous with the OUTCLK output. In Single-Lane mode this differential output is held in high impedance state. This differential output is always enabled while the device is powered up. In power-down mode this output holds the last logic state. A 100-ohm termination resistor must always be used between this pair of signals at the far end of the transmission line.
56	SPI_EN		SPI Enable: The SPI interface is enabled when this signal is asserted high. In this case the direct control pins have no effect. When this signal is deasserted, the SPI interface is disabled and the direct control pins are enabled.
55	SCSb		Serial Chip Select: While this signal is asserted SCLK is used to accept serial data present on the SDI input and to source serial data on the SDO output. When this signal is deasserted, the SDI input is ignored and the SDO output is in tri-state mode.
52	SCLK		Serial Clock: Serial data are shifted into and out of the device synchronous with this clock signal.
54	SDI		Serial Data-In: Serial data are shifted into the device on this pin while SCSb signal is asserted.

Pin No.	Symbol	Equivalent Circuit	Description
53	SDO		Serial Data-Out: Serial data are shifted out of the device on this pin while SCSb signal is asserted. This output is in tri-state mode when SCSb is deasserted.
46 30	ORA ORB		Overrange. These CMOS outputs are asserted logic-high when their respective channel's data output is out-of-range in either high or low direction.
24	DLL_Lock		DLL_Lock Output. When the internal DLL is locked to the input CLK, this pin outputs a logic high. If the input CLK is changed abruptly, the internal DLL may become unlocked and this pin will output a logic low. Cycle Reset_DLL (pin 28) to re-lock the DLL to the input CLK.
ANALOG POWER			
8, 16, 17, 58, 60	V_A		Positive analog supply pins. These pins should be connected to a quiet source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins.
1, 4, 12, 15, Exposed Pad	AGND		The ground return for the analog supply.
DIGITAL POWER			
26, 40, 50	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source and be bypassed to DRGND with a 0.1 µF capacitor located close to the power pin.
25, 39, 51	DRGND		The ground return for the digital output driver supply. This pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's AGND pins.

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	−0.3V to 4.2V
Voltage on Any Pin (Not to exceed 4.2V)	−0.3V to (V_A +0.3V)
Input Current at Any Pin other than Supply Pins (Note 4)	±5 mA
Package Input Current (Note 4)	±50 mA
Max Junction Temp (T_J)	+150°C
Thermal Resistance (θ_{JA})	30°C/W
ESD Rating	
Human Body Model (Note 6)	2500V
Machine Model (Note 6)	250V
Storage Temperature	−65°C to +150°C
Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 7)	

Operating Ratings (Notes 1, 3)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A=V_{DR})	+2.7V to +3.6V
Clock Duty Cycle	
(DCS Enabled)	30/70 %
(DCS disabled)	45/55 %
V_{CM}	1.4V to 1.6V
|AGND-DRGND|	≤100mV

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for T_{MIN} ≤ T_A ≤ T_{MAX}.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity			±0.5	**2** **-2**	LSB (max) LSB (min)
DNL	Differential Non Linearity			±0.3	**0.8** **-0.8**	LSB (max) LSB (min)
PGE	Positive Gain Error			0.15	**±1**	%FS (max)
NGE	Negative Gain Error			0.07	**±1**	%FS (max)
TC PGE	Positive Gain Error Tempco	−40°C ≤ T_A ≤ +85°C				ppm/°C
TC NGE	Negative Gain Error Tempco	−40°C ≤ T_A ≤ +85°C				ppm/°C
V_{OFF}	Offset Error			0.03	**±0.55**	%FS (max)
TC V_{OFF}	Offset ErrorTempco	−40°C ≤ T_A ≤ +85°C				ppm/°C
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CMO}	Common Mode Output Voltage			1.5	**1.4** **1.6**	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage			1.5	1.4 1.6	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND) (Note 11)	V_{IN} = 1.5 Vdc ± 0.5 V	(CLK LOW)	8.5		pF
			(CLK HIGH)	3.5		pF
V_{REF}	Internal Reference Voltage			1.18	1.17 1.21	V (min) V (max)
TC V_{REF}	Internal Reference Voltage Tempco	−40°C ≤ T_A ≤ +85°C		18		ppm/°C
V_{RP}	Internal Reference Top			2.0		V
V_{RN}	Internal Reference Bottom			1.0		V

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Internal Reference Accuracy	(V_{RP}-V_{RN})	0.97	0.89 1.06	V (min) V (max)
EXT V_{REF}	External Reference Voltage		1.2	1.176 1.224	V (min) V (max)

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin, . Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.0		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	71		dBFS
		f_{IN} = 70 MHz	70		dBFS
		f_{IN} = 240 MHz	68.5	**67.4**	dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	88		dBFS
		f_{IN} = 70 MHz	85		dBFS
		f_{IN} = 240 MHz	83	**76.5**	dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.5		Bits
		f_{IN} = 70 MHz	11.3		Bits
		f_{IN} = 240 MHz	11	**10.7**	Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	–86		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–80	**-74**	dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	–90		dBFS
		f_{IN} = 70 MHz	–88		dBFS
		f_{IN} = 240 MHz	–83	**-76.5**	dBFS
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	–88		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–83	**-76.5**	dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	70.8		dBFS
		f_{IN} = 70 MHz	69.9		dBFS
		f_{IN} = 240 MHz	68.2	**66.5**	dBFS
IMD	Intermodulation Distortion	f_{IN} = 19.5 and 20.5 MHz, each -7dBFS	-82		dBFS

Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD_A,PD_B,SCSb,SPI_EN,SCLK,SDI,TEST,WAM,DLC)					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	–10		µA

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (ORA,ORB,SDO,DLL_Lock)					
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA		**1.2**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	−10		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Operation	240	**270**	mA (max)
I_{DR}	Digital Output Supply Current	Full Operation	70	**80**	mA
	Power Consumption		1000	**1130**	mW (max)
	Power Down Power Consumption	Clock disabled	33		mW

Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Maximum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**65** **105**	MHz (max)
	Minimum Clock Frequency	In Single-Lane Mode In Dual-Lane Mode		**25** **52.5**	MHz (min)
t_{CONV}	Conversion Latency	Single-Lane Mode Dual-Lane, Offset Mode Dual-Lane, Word Aligned Mode		**7.5** **8** **9**	Clock Cycles
t_{AD}	Aperture Delay		0.6		ns
t_{AJ}	Aperture Jitter		0.1		ps rms

Serial Control Interface Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = 3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
f_{SCLK}	Serial Clock Frequency	f_{SCLK} = f_{CLK}/10		10.5	MHz (max)
t_{PH}	SCLK Pulse Width - High	% of SCLK Period		40 60	% (min) % (max)
t_{PL}	SCLK Pulse Width - Low	% of SCLK Period		40 60	% (min) % (max)
t_{SU}	SDI Setup Time			5	ps (min)
t_H	SDI Hold Time			5	ns (min)
t_{ODZ}	SDO Driven-to-Tri-State Time		40	50	ns (max)
t_{OZD}	SDO Tri-State-to-Driven Time		15	20	ns (max)
t_{OD}	SDO Output Delay Time		15	20	ns (max)
t_{CSS}	SCSb Setup Time		5	10	ns (min)
t_{CSH}	SCSb Hold Time		5	10	ns (min)
t_{IAG}	Inter-Access Gap	Minimum time SCSb must be deasserted between accesses	3		Cycles of SCLK

LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
LVDS DC CHARACTERISTICS					
V_{OD}	Output Differential Voltage (SDO+) - (SDO-)	R_L = 100Ω	350	250 450	mV (min) mV (max)
delta V_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω		±25	mV (max)
V_{OS}	Offset Voltage	R_L = 100Ω	1.25	1.125 1.375	V (min) V (max)
delta V_{OS}	Offset Voltage Unbalance	R_L = 100Ω		±25	mV (max)
IOS	Output Short Circuit Current	DO = 0V, V_{IN} = 1.1V,	-10		mA (max)
LVDS OUTPUT TIMING AND SWITCHING CHARACTERISTICS					
t_{DP}	Output Data Bit Period	Dual-Lane Mode	1.59		ns
t_{HO}	Output Data Edge to Output Clock Edge Hold Time(Note 12)	Dual-Lane Mode	750	**450**	ps
t_{SUO}	Output Data Edge to Output Clock Edge Set-Up Time(Note 12)	Dual-Lane Mode	800	**500**	ps
t_{FP}	Frame Period	Dual-Lane Mode	19.05		ns
t_{FDC}	Frame Clock Duty Cycle(Note 12)		50	45 55	% (min) % (max)
t_{DFS}	Data Edge to Frame Edge Skew	50% to 50%	15		ps
t_{ODOR}	Output Delay of OR output	From rising edge of CLK to ORA/ORB valid	4		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: This parameter is specified in units of dBFS - indicating the value that would be attained with a full-scale input signal.

Note 3: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

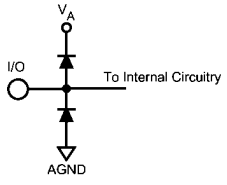
Note 4: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 5: The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 6: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω

Note 7: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 8: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



20211711

Note 9: With a full scale differential input of $2V_{P-P}$, the 12-bit LSB is 488 µV.

Note 10: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 11: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 12: This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

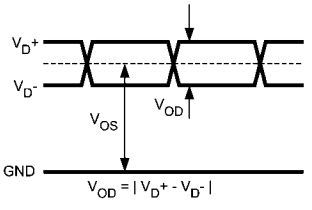
It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.



LVDS Differential Output Voltage (V_{OD}) is the absolute value of the difference between the differential output pair voltages (V_D+ and V_D-), each measured with respect to ground.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}-)] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

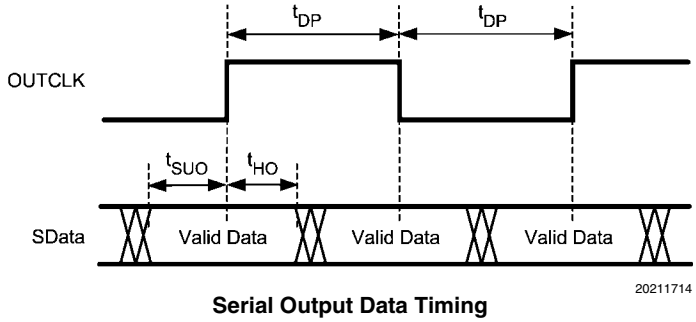
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_7^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_7 are the RMS power of the first six harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagrams



Serial Output Data Timing

FIGURE 1.

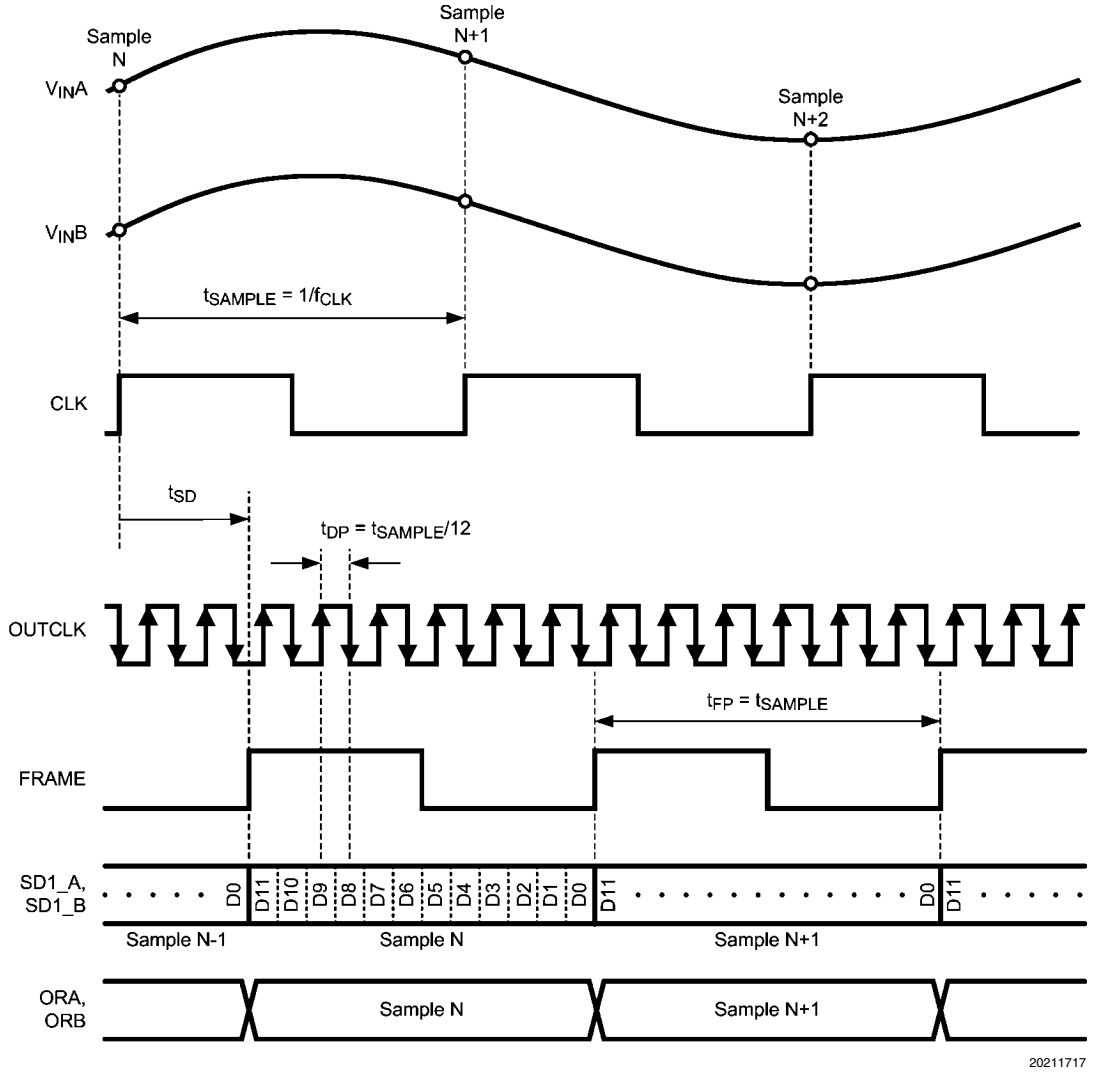


FIGURE 2. Serial Output Data Format in Single-Lane Mode

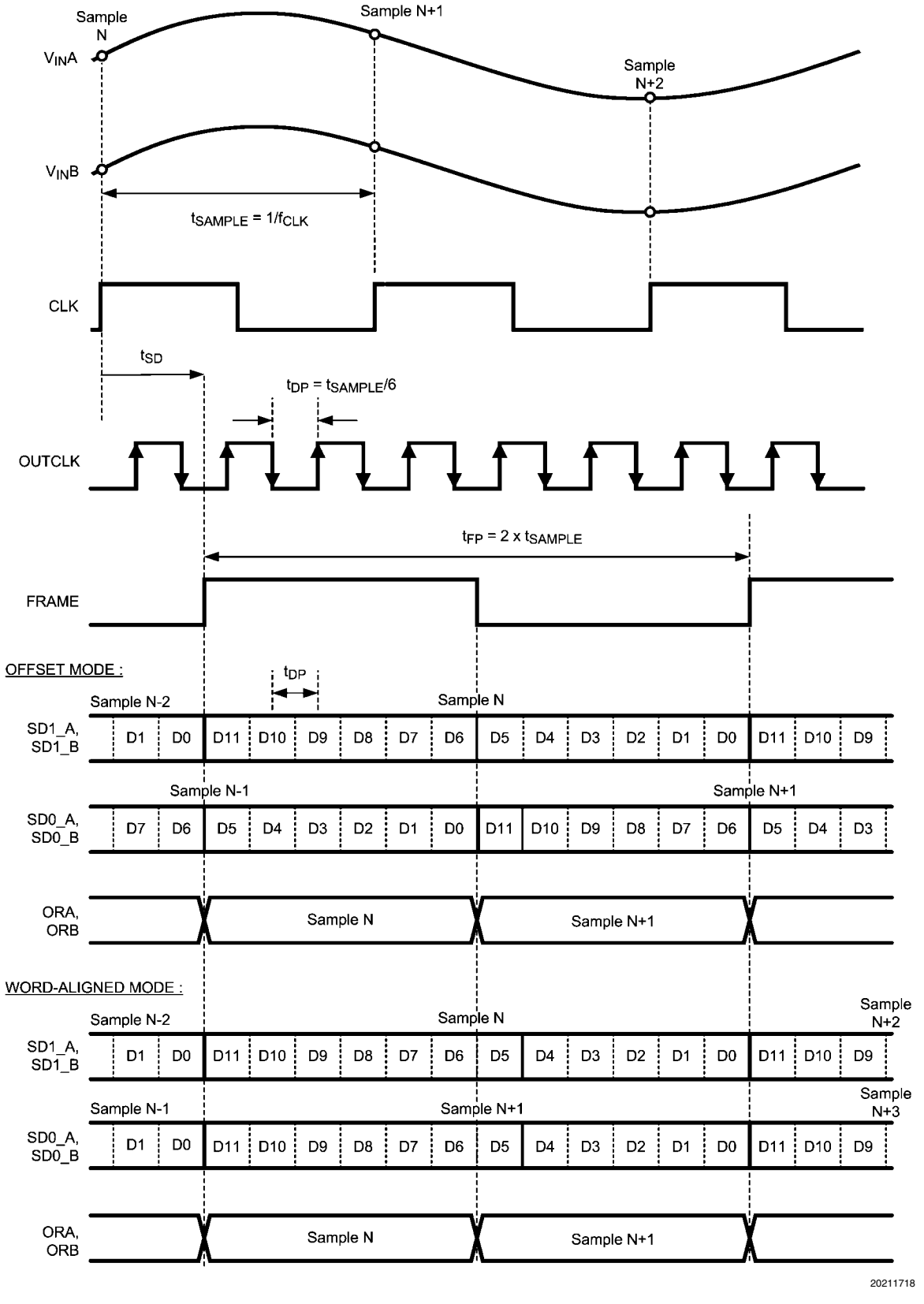


FIGURE 3. Serial Output Data Format in Dual-Lane Mode

Transfer Characteristic

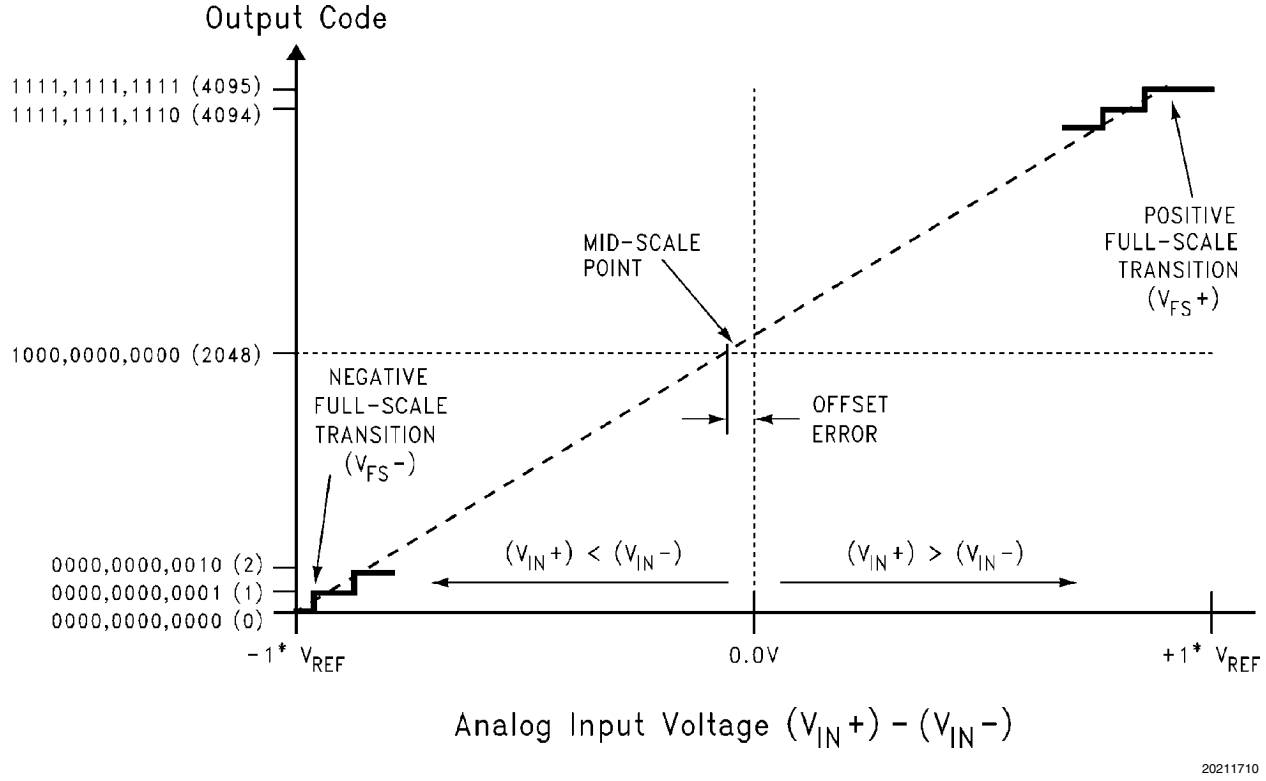
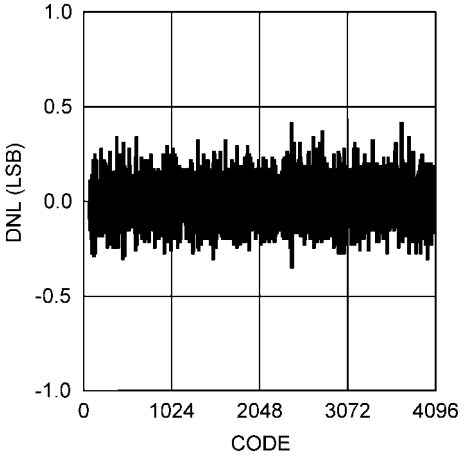


FIGURE 4. Transfer Characteristic

Typical Performance Characteristics DNL, INL

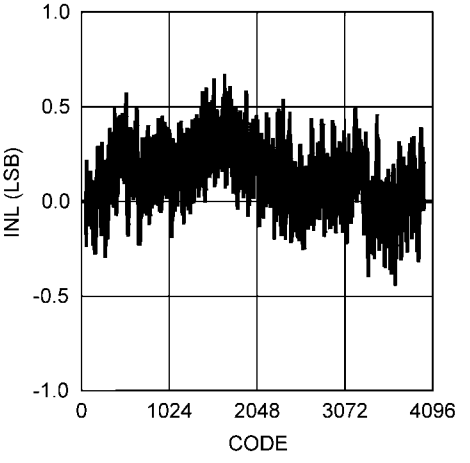
Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, 50% Duty Cycle, DCS disabled, $V_{CM} = V_{CMO}$, T_A = 25°C.

DNL



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INL

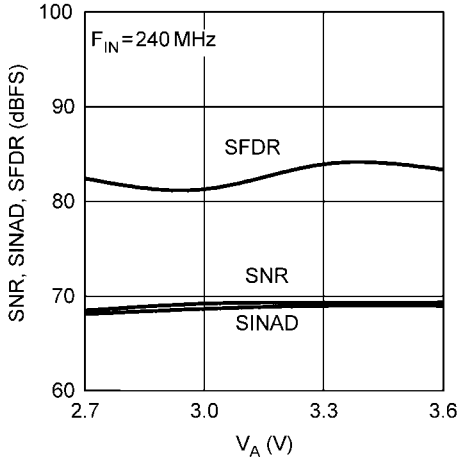


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Typical Performance Characteristics

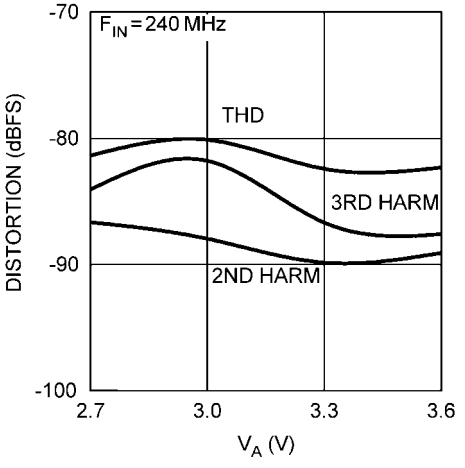
Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +3.0V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, 50% Duty Cycle, DCS disabled, V_{CM} = V_{CMO}, f_{IN} = 10 MHz, T_A = 25°C.

SNR, SINAD, SFDR vs. V_A



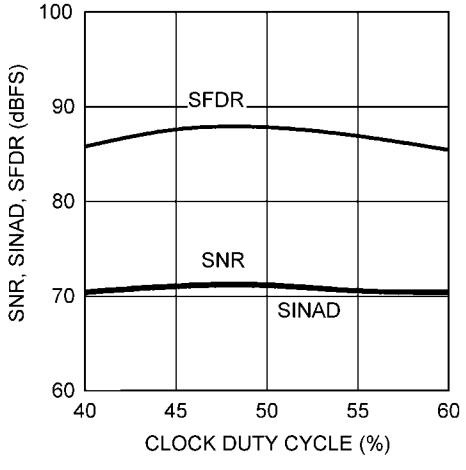
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Distortion vs. V_A



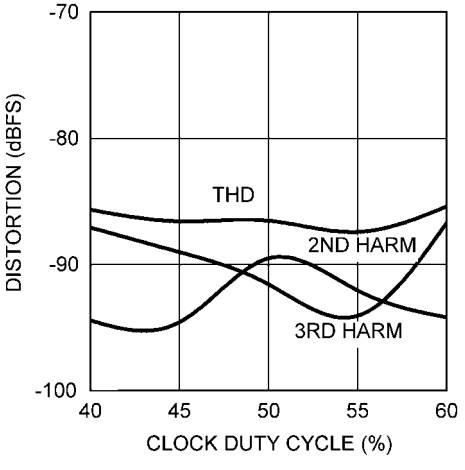
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SNR, SINAD, SFDR vs. Clock Duty Cycle



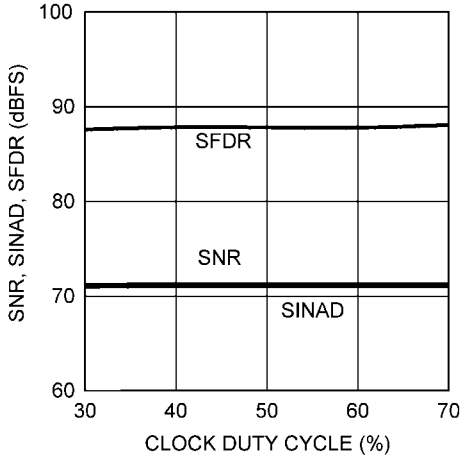
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Distortion vs. Clock Duty Cycle



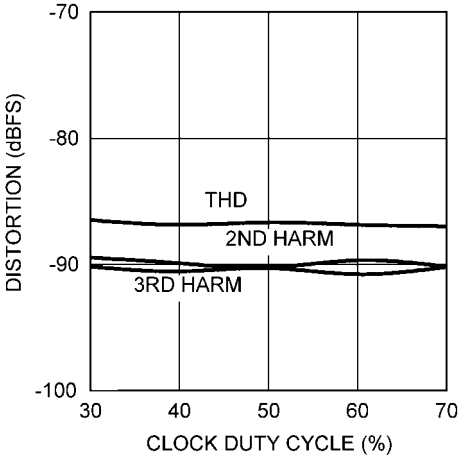
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SNR, SINAD, SFDR vs. Clock Duty Cycle, DCS Enabled



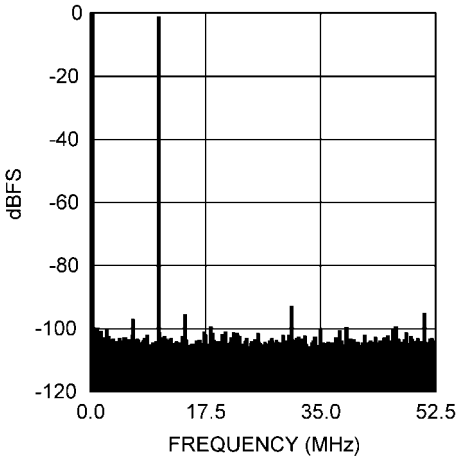
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Distortion vs. Clock Duty Cycle, DCS Enabled



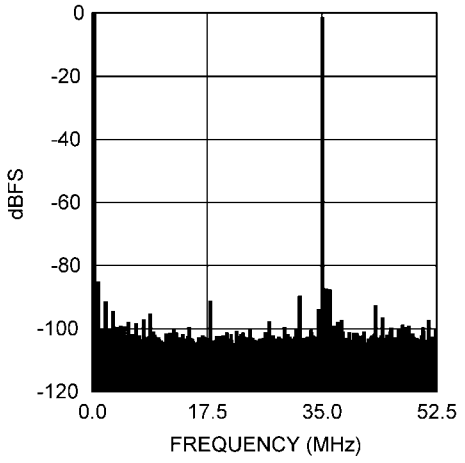
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Spectral Response @ 10 MHz Input



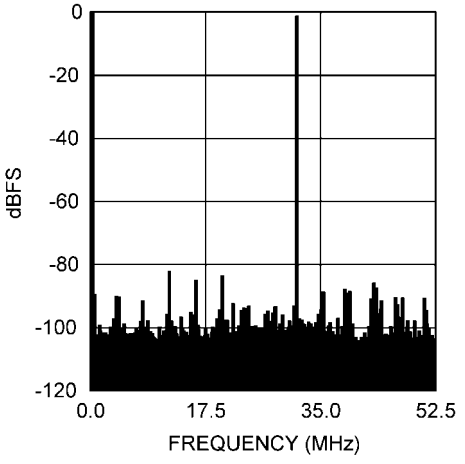
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Spectral Response @ 70 MHz Input



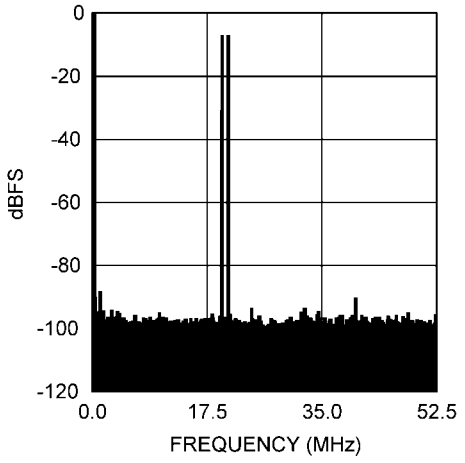
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Spectral Response @ 240 MHz Input



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IMD, $f_{IN}1$ = 20 MHz, $f_{IN}2$ = 21 MHz



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Functional Description

Operating on a single +3.3V supply, the ADC12DS105 digitizes two differential analog input signals to 12 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance. The user has the choice of using an internal 1.2V stable reference, or using an external 1.2V reference. Any external reference is buffered on-chip to ease the task of driving that pin. Duty cycle stabilization and output data format are selectable using the quad state function OF/DCS pin (pin 19). The output data can be set for offset binary or two's complement.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12DS105:

$2.7V \leq V_A \leq 3.6V$

$2.7V \leq V_{DR} \leq V_A$

$25\ MHz \leq f_{CLK} \leq 105\ MHz$

1.2V internal reference

V_{REF} = 1.2V (for an external reference)

V_{CM} = 1.5V (from V_{CMO})

2.0 ANALOG INPUTS

2.1 Signal Inputs

2.1.1 Differential Analog Input Pins

The ADC12DS105 has a pair of analog signal input pins for each of two channels. V_{IN}+ and V_{IN}– form a differential input pair. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

Figure 5 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be 1.5V. Using V_{CMO} (pins 7,9) for V_{CM} will ensure the proper input common mode level for the analog input signal. The positive peaks of the individual input signals should each never exceed 2.6V. Each analog input pin of the differential pair should have a maximum peak-to-peak voltage of 1V, be 180° out of phase with each other and be centered around V_{CM}.The peak-to-peak voltage swing at each analog input pin should not exceed the 1V or the output data will be clipped.

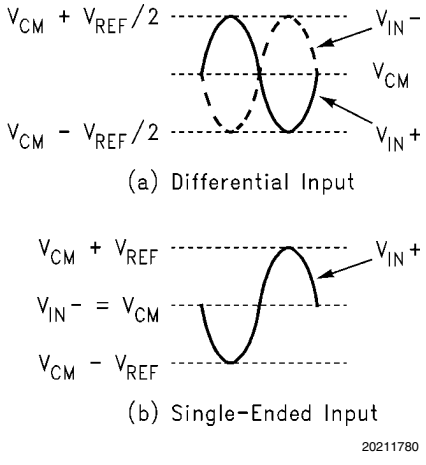


FIGURE 5. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately

$$E_{FS} = 4096 (1 - \sin (90° + dev))$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see *Figure 6*). For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

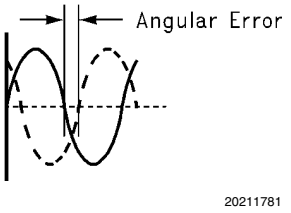


FIGURE 6. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

It is recommended to drive the analog inputs with a source impedance less than 100Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 1 indicates the input to output relationship of the ADC12DS105.

TABLE 1. Input to Output Relationship

V_{IN+}	V_{IN-}	Binary Output	2's Complement Output	
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000	1000 0000 0000	Negative Full-Scale
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000	1100 0000 0000	
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000	Mid-Scale
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000	0100 0000 0000	
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111	0111 1111 1111	Positive Full-Scale

2.1.2 Driving the Analog Inputs

The V_{IN}+ and the V_{IN}– inputs of the ADC12DS105 have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier.

Figure 7 and *Figure 8* show examples of single-ended to differential conversion circuits. The circuit in *Figure 7* works well for input frequencies up to approximately 70MHz, while the circuit in *Figure 8* works well above 70MHz.

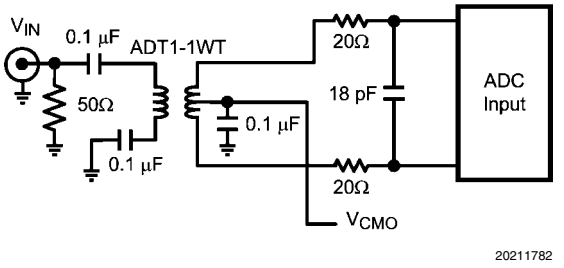


FIGURE 7. Low Input Frequency Transformer Drive Circuit

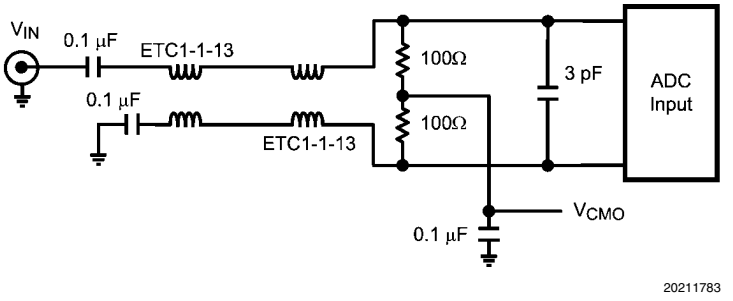


FIGURE 8. High Input Frequency Transformer Drive Circuit

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

2.1.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 1.4V to 1.6V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than 2.6V. It is recommended to use V_{CMO} (pins 7,9) as the input common mode voltage.

2.2 Reference Pins

The ADC12DS105 is designed to operate with an internal or external 1.2V reference. The internal 1.2 Volt reference is the default condition when no external reference input is applied to the V_{REF} pin. If a voltage is applied to the V_{REF} pin, then that voltage is used for the reference. The V_{REF} pin should always be bypassed to ground with a 0.1 µF capacitor close to the reference input pin.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins (V_{RP}, V_{CMO}, and V_{RN}) for channels A and B are made available for bypass purposes. These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 1 µF capacitor should be placed in parallel. This configuration is shown in *Figure 9*. It is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. V_{CMO} may be loaded to 1mA for use as a temperature stable 1.5V reference. The remaining pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in de-

graded noise performance. Loading any of these pins, other than V_{CMO} may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

V_{CMO} = 1.5 V

V_{RP} = 2.0 V

V_{RN} = 1.0 V

2.3 OF/DCS Pin

Duty cycle stabilization and output data format are selectable using this quad state function pin. When enabled, duty cycle stabilization can compensate for clock inputs with duty cycles ranging from 30% to 70% and generate a stable internal clock, improving the performance of the part. With OF/DCS = V_A the output data format is 2's complement and duty cycle stabilization is not used. With OF/DCS = AGND the output data format is offset binary and duty cycle stabilization is not used. With OF/DCS = (2/3)*V_A the output data format is 2's complement and duty cycle stabilization is applied to the clock. If OF/DCS is (1/3)*V_A the output data format is offset binary and duty cycle stabilization is applied to the clock. While the sense of this pin may be changed "on the fly," doing this is not recommended as the output data could be erroneous for a few clock cycles after this change is made.

Note: This signal has no effect when SPI_EN is high and the serial control interface is enabled.

3.0 DIGITAL INPUTS

Digital CMOS compatible inputs consist of CLK, and PD_A, PD_B, Reset_DLL, DLC, TEST, WAM, SPI_EN, SCSb, SCLK, and SDI.

3.1 Clock Input

The CLK controls the timing of the sampling process. To achieve the optimum noise performance, the clock input should be driven with a stable, low jitter clock signal in the range indicated in the Electrical Table. The clock input signal should also have a short transition region. This can be achieved by passing a low-jitter sinusoidal clock source through a high speed buffer gate. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The clock signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC clock pins only drive that pin. However, if that source is used to drive other devices, then each driven pin should be AC terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12DS105 has a Duty Cycle Stabilizer.

3.2 Power-Down (PD_A and PD_B)

The PD_A and PD_B pins, when high, hold the respective channel of the ADC12DS105 in a power-down mode to conserve power when that channel is not being used. The channels may be powered down individually or together. The data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the components on the reference bypass pins (V_{RP}, V_{CMO} and V_{RN}). These capacitors lose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

Note: This signal has no effect when SPI_EN is high and the serial control interface is enabled.

3.3 Reset_DLL

This pin is normally low. If the input clock frequency is changed abruptly, the internal timing circuits may become unlocked. Cycle this pin high for 1 microsecond to re-lock the DLL. The DLL will lock in several microseconds after Reset_DLL is asserted.

3.4 DLC

This pin sets the output data configuration. With this signal at logic-1, all data is sourced on a single lane (SD1_x) for each channel. When this signal is at logic-0, the data is sourced on dual lanes (SD0_x and SD1_x) for each channel. This simplifies data capture at higher data rates.

Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.

3.5 TEST

When this signal is asserted high, a fixed test pattern (101001100011 msb->lsb) is sourced at the data outputs. When low, the ADC is in normal operation. The user may specify a custom test pattern via the serial control interface.

Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.

3.6 WAM

In dual-lane mode only, when this signal is at logic-0 the serial data words are offset by half-word. With this signal at logic-1 the serial data words are aligned with each other. In single lane mode this pin must be set to logic-0.

Note: This signal has no effect when SPI_EN is high and the SPI interface is enabled.

3.7 SPI_EN

The SPI interface is enabled when this signal is asserted high. In this case the direct control pins (OF/DCS, PD_A, PD_B, DLC, WAM, TEST) have no effect. When this signal is de-asserted, the SPI interface is disabled and the direct control pins are enabled.

3.8 SCSb, SDI, SCLK

These pins are part of the SPI interface. See Section 5.0 for more information.

4.0 DIGITAL OUTPUTS

Digital outputs consist of six LVDS signal pairs (SD0_A, SD1_A, SD0_B, SD1_B, OUTCLK, FRAME) and CMOS logic outputs ORA, ORB, DLL_Lock, and SDO.

4.1 LVDS Outputs

The digital data for each channel is provided in a serial format. Two modes of operation are available for the serial data format. Single-lane serial format (shown in *Figure 2*) uses one set of differential data signals per channel. Dual-lane serial format (shown in *Figure 3*) uses two sets of differential data signals per channel in order to slow down the data and clock frequency by a factor of 2. At slower rates of operation (typically below 65 MSPS) the single-lane mode may be the most efficient to use. At higher rates the user may want to employ the dual-lane scheme. In either case DDR-type clocking is used. For each data channel, an overrange indication is also provided. The OR signal is updated with each frame of data.

4.2 ORA, ORB

These CMOS outputs are asserted logic-high when their respective channel's data output is out-of-range in either high or low direction.

4.3 DLL_Lock

When the internal DLL is locked to the input CLK, this pin outputs a logic high. If the input CLK is changed abruptly, the internal DLL may become unlocked and this pin will output a logic low. Cycle Reset_DLL to re-lock the DLL to the input CLK.

4.4 SDO

This pin is part of the SPI interface. See Section 5.0 for more information.

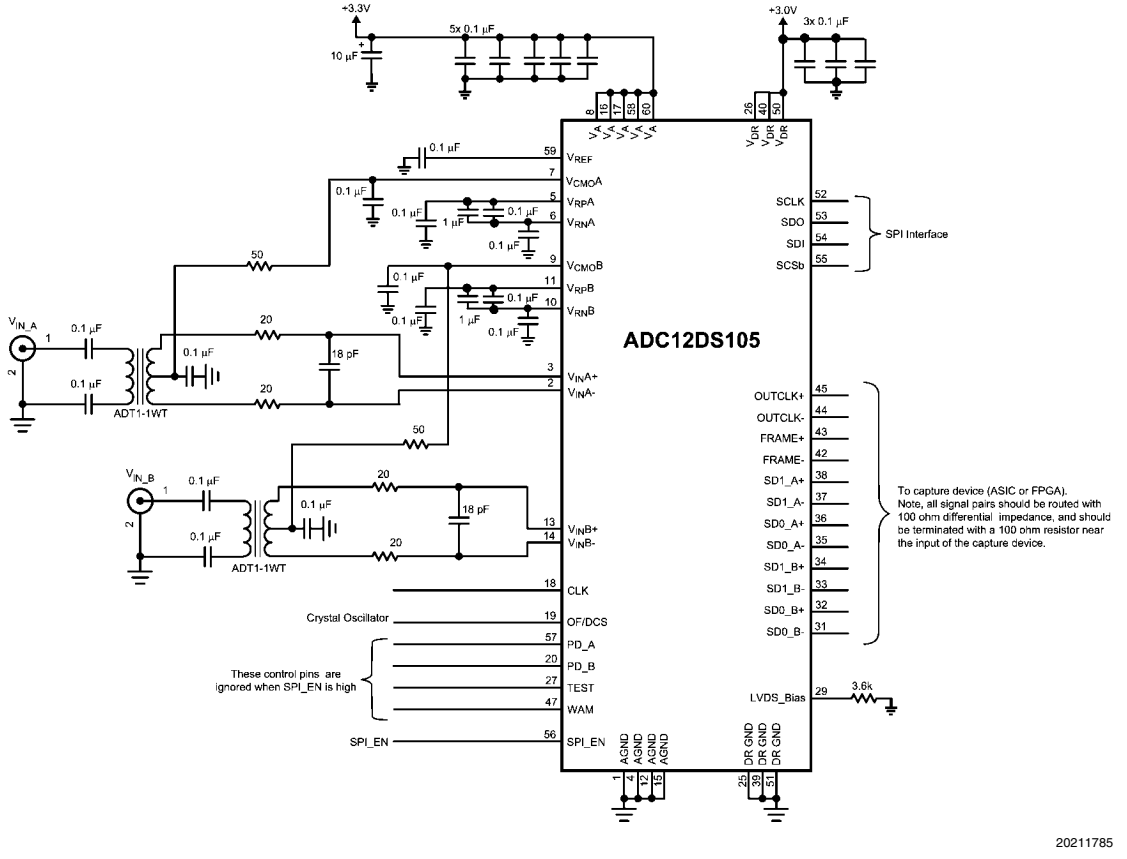


FIGURE 9. Application Circuit

5.0 Serial Control Interface

The ADC12DS105 has a serial interface that allows access to the control registers. The serial interface is a generic 4-wire synchronous interface that is compatible with SPI type interfaces that are used on many microcontrollers and DSP controllers.

The ADC's input clock must be running for the Serial Control Interface to operate. It is enabled when the SPI_EN (pin 56) signal is asserted high. In this case the direct control pins (OF/DCS, PD_A, PD_B, DLC, WAM, TEST) have no effect. When this signal is deasserted, the SPI interface is disabled and the direct control pins are enabled.

Each serial interface access cycle is exactly 16 bits long. *Figure 10* shows the access protocol used by this interface. Each signal's function is described below. The Read Timing is shown in *Figure 11*, while the Write Timing is shown in *Figure 12*

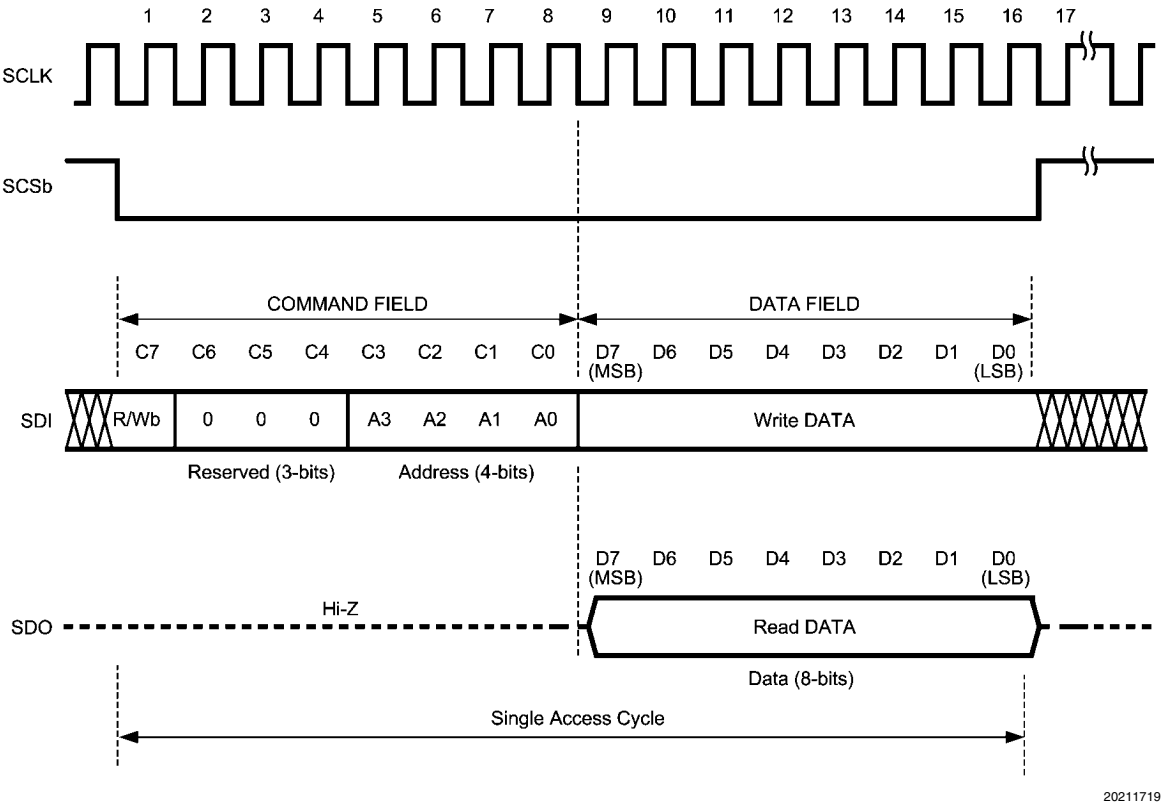


FIGURE 10. Serial Interface Protocol

SCLK: Used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. User may disable clock and hold it in the low-state, as long as clock pulse-width min spec is not violated when clock is enabled or disabled.

SCSb: Serial Interface Chip Select. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the SCSb is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the deasserted pulse - which is specified in the Electrical Specifications section.

SDI: Serial Data. Must observe setup/hold requirements with respect to the SCLK. Each cycle is 16-bits long.

R/Wb:	A value of '1' indicates a read operation, while a value of '0' indicates a write operation.
Reserved:	Reserved for future use. Must be set to 0.
ADDR:	Up to 3 registers can be addressed.
DATA:	In a write operation the value in this field will be written to the register addressed in this cycle when SCSb is deasserted. In a read operation this field is ignored.

SDO: This output is normally at TRI-STATE and is driven only when SCSb is asserted. Upon SCSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h.

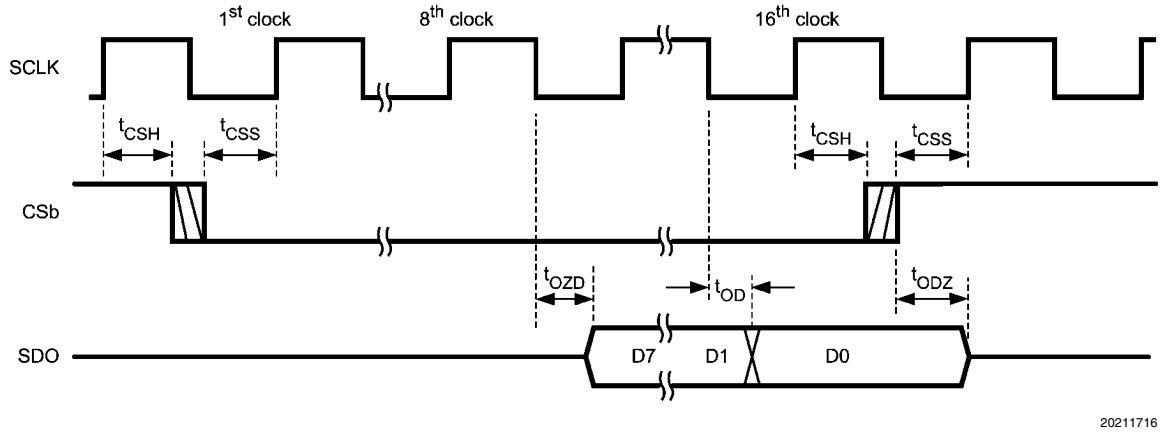


FIGURE 11. Read Timing

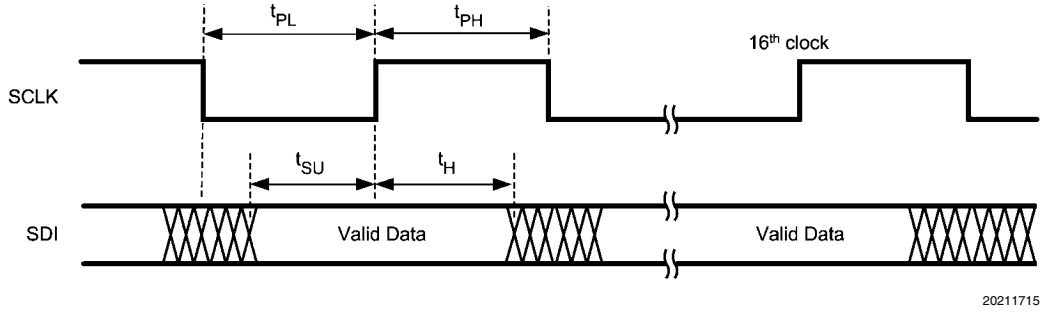


FIGURE 12. Write Timing

Device Control Register, Address 0h

7 6	5	4	3	2	1	0
OM	DLC	DCS	OF	WAM	PD_A	PD_B

Reset State : 08h

Bits (7:6) Operational Mode

0 0 Normal Operation.

0 1 Test Output mode. A fixed test pattern (1010011000111msb->lsb) is sourced at the data outputs.

1 0 Test Output mode. Data pattern defined by user in registers 01h and 02h is sourced at data outputs.

1 1 Reserved.

Bit 5 Data Lane Configuration. When this bit is set to '0', the serial data interface is configured for dual-lane mode where the data words are output on two data outputs (SD1 and SD0) at half the rate of the single-lane interface. When this bit is set to ‘1’, serial data is output on the SD1 output only and the SD0 outputs are held in a high-impedance state

Bit 4 Duty Cycle Stabilizer. When this bit is set to '0' the DCS is off. When this bit is set to ‘1’, the DCS is on.

Bit 3 Output Data Format. When this bit is set to ‘1’ the data output is in the “twos complement” form. When this bit is set to ‘0’ the data output is in the “offset binary” form.

Bit 2 Word Alignment Mode.
This bit must be set to '0' in the single-lane mode of operation.
In dual-lane mode, when this bit is set to '0' the serial data words are offset by half-word. This gives the least latency through the device. When this bit is set to '1' the serial data words are in word-aligned mode. In this mode the serial data on the SD1 lane is additionally delayed by one CLK cycle. (Refer to *Figure 3*).

Bit 1 Power-Down Channel A. When this bit is set to '1', Channel A is in power-down state and Normal operation is suspended.

Bit 0 Power-Down Channel B. When this bit is set to '1', Channel B is in power-down state and Normal operation is suspended.

User Test Pattern Register 0, Address 1h

7	6	5	4	3	2	1	0
Reserved		User Test Pattern (13:6)					

Reset State : 00h

Bits (7:6) Reserved. Must be set to '0'.

Bits (5:0) User Test Pattern. Most-significant 6 bits of the 12-bit pattern that will be sourced out of the data outputs in Test Output Mode.

User Test Pattern Register 1, Address 2h

7	6	5	4	3	2	1	0
User Test Pattern (5:0)						Reserved	

Reset State : 00h

Bits (7:2) User Test Pattern. Least-significant 6 bits of the 12-bit pattern that will be sourced out of the data outputs in Test Output Mode.

Bits (1:0) Reserved. Must be set to '0'.

6.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 0.1 µF capacitor and with a 100 pF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12DS105 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

7.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12DS105 between these areas, is required to achieve specified performance.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane area.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should *not* be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC12DS105 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

8.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must have a sharp transition region and be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 13*. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

As mentioned in Section *7.0 LAYOUT AND GROUNDING*, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

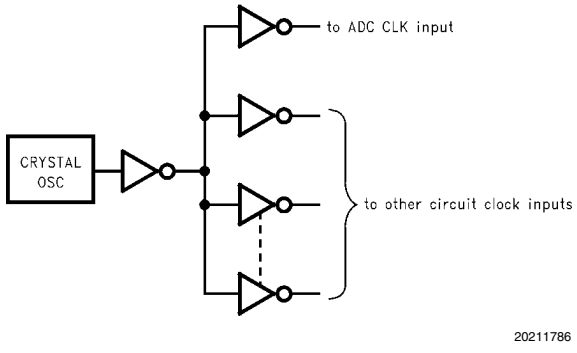
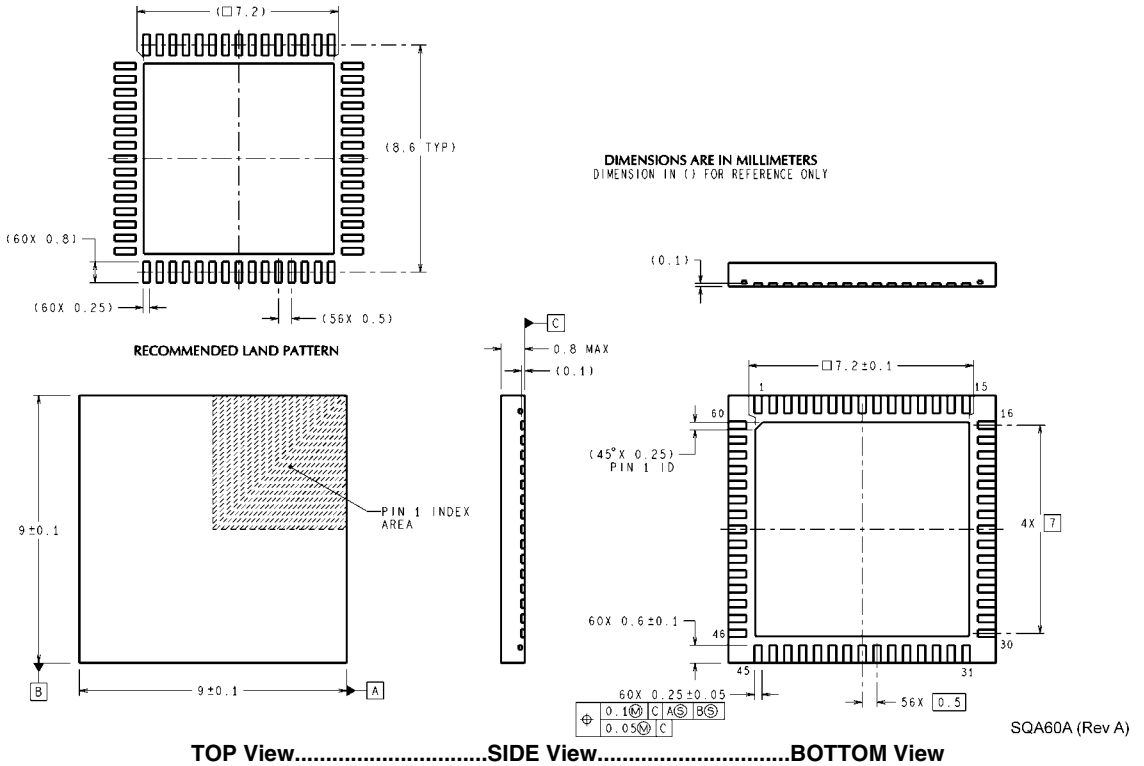


FIGURE 13. Isolating the ADC Clock from other Circuitry with a Clock Tree

Physical Dimensions inches (millimeters) unless otherwise noted



SQA60A (Rev A)

TOP View.....SIDE View.....BOTTOM View
60-Lead LLP Package
Ordering Numbers:
ADC12DS105CISQ
NS Package Number SQA60A

Notes

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
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