DATASHEET

ISL6569A

Multi-Phase PWM Controller

FN9092
Rev 2.00
Dec 29, 2004

The ISL6569A provides core-voltage regulation by driving two interleaved synchronous-rectified buck-converter channels in parallel. Interleaving the channel timing results in increased ripple frequency which reduces input and output ripple currents. The reduction in ripple results in lower component cost, reduced dissipation, and a smaller implementation area.

The ISL6569A uses cost and space-saving $r_{DS(ON)}$ sensing for channel current balance, active voltage positioning, and over-current protection. Output voltage is monitored by an internal differential remote sense amplifier. A high-bandwidth error amplifier drives the output voltage to match the programmed 5-bit DAC reference voltage. The resulting compensation signal guides the creation of pulse width modulated (PWM) signals to control companion Intersil MOSFET drivers. The OFS pin allows direct offset of the DAC voltage from 0V to 50mV using a single external resistor. The reference and amplifiers are trimmed to ensure a system accuracy of ±0.5% over temperature.

Outstanding features of this controller IC include Dynamic VID™ technology allowing seamless on-the-fly VID changing without the need of any external components. Output voltage “droop” or active voltage positioning is optional. When employed, it allows the reduction in size and cost of the output capacitors required to support load transients. A threshold-sensitive enable input allows the use of an external resistor divider for start-up coordination with Intersil MOSFET drivers or any other devices powered from a separate supply.

Superior over-voltage protection is achieved by gating on the lower MOSFET of all phases to crowbar the output voltage. An optional second crowbar on V_{IN}, formed with an external MOSFET or SCR gated by the OVP pin, is triggered when an over-voltage condition is detected. Under-voltage conditions are detected, but PWM operation is not disrupted. Over-current conditions cause a hiccup-mode response as the controller repeatedly tries to restart. After a set number of failed startup attempts, the controller latches off. A power good logic signal indicates when the converter output is between the UV and OV thresholds.

Features

- Multi-Phase Power Conversion
  - 2 Phase Operation
- Active Channel Current Balancing
- Precision $r_{DS(ON)}$ Current Sharing
  - Lossless
  - Low Cost
- Input Voltage: 12V or 5V Bias
- Precision CORE Voltage Regulation
  - ±0.5% System Accuracy Over Temperature
  - Differential Remote Output Voltage Sensing
  - Programmable Reference Offset
- Microprocessor Voltage Identification Input
  - 5-Bit VID Input
  - 0.800V to 1.550V in 25mV Steps
  - Dynamic VID™ Technology
- Programmable Droop Voltage
- Fast Transient Recovery Time
- Over Current Protection
- Digital Soft Start
- Threshold Sensitive Enable Input
- High Ripple Frequency (160kHz to 2MHz)
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Available (RoHS Compliant)

Applications

- AMD Hammer Family Processor Voltage Regulator
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

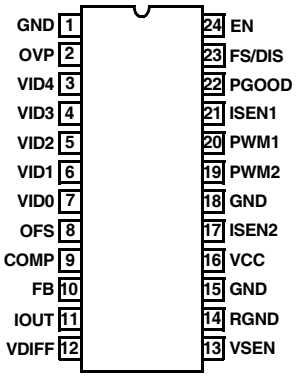
Ordering Information

PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6569ACB	0 to 70	24 Ld SOIC	M24.3
ISL6569ACBZ (Note)	0 to 70	24 Ld SOIC (Pb-free)	M24.3
ISL6569ACR	0 to 85	32 Ld 5x5 QFN	L32.5x5
ISL6569ACRZ (Note)	0 to 85	32 Ld 5x5 QFN (Pb-free)	L32.5x5

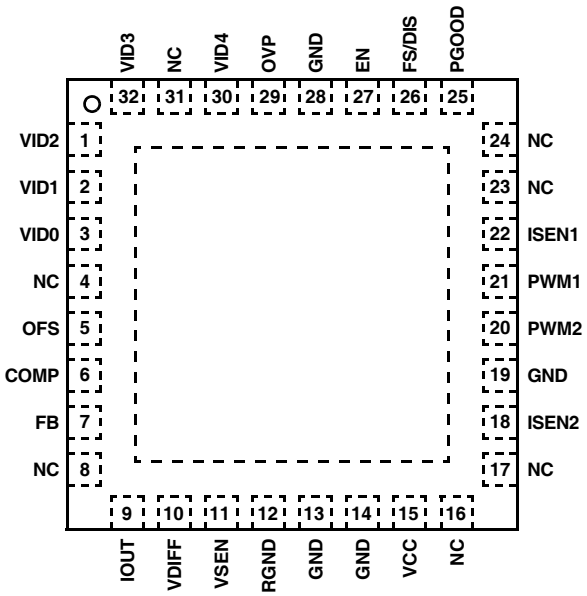
Add “-T” suffix for tape and reel.
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

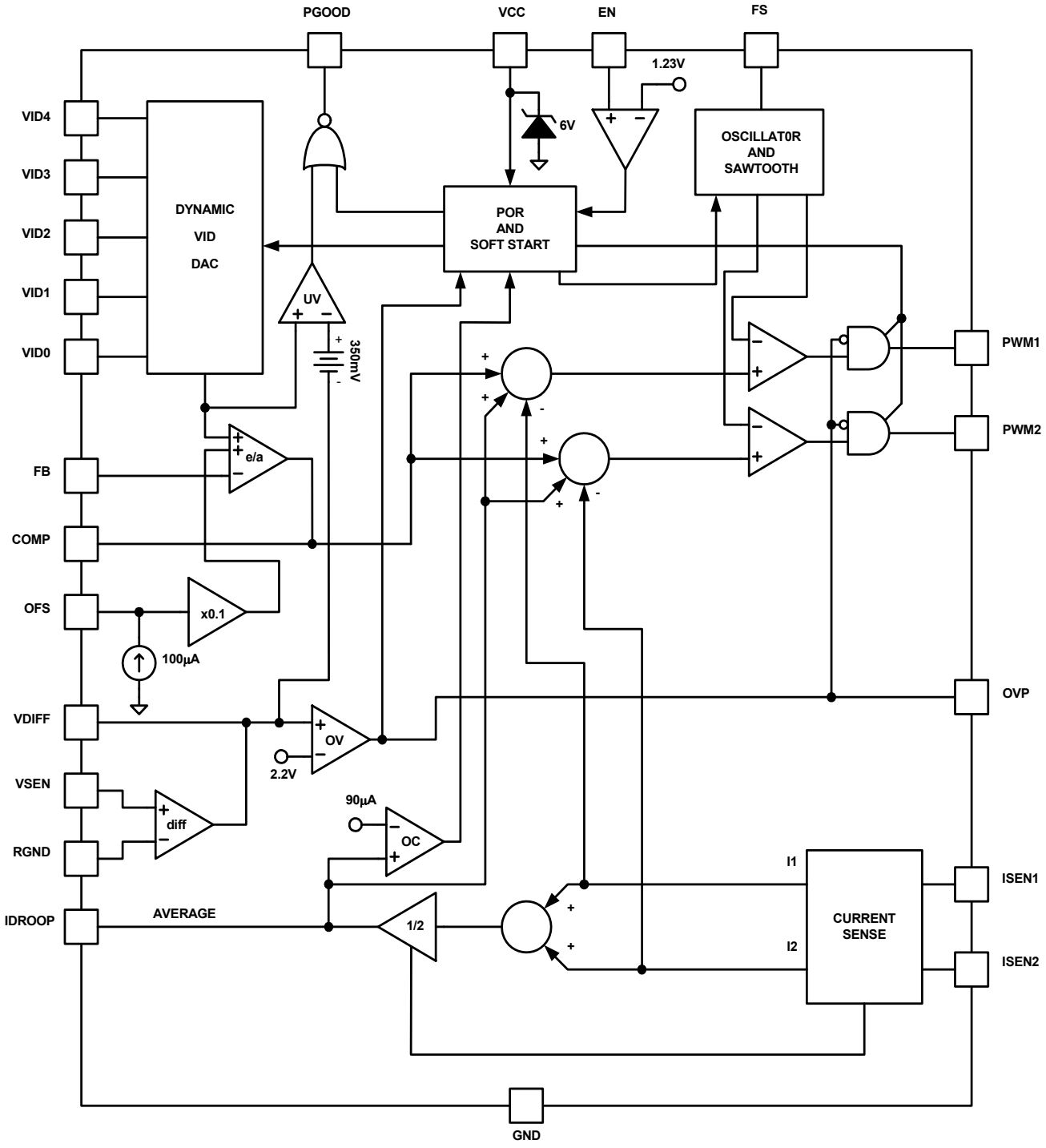
ISL6569ACB (24 LD SOIC)
TOP VIEW



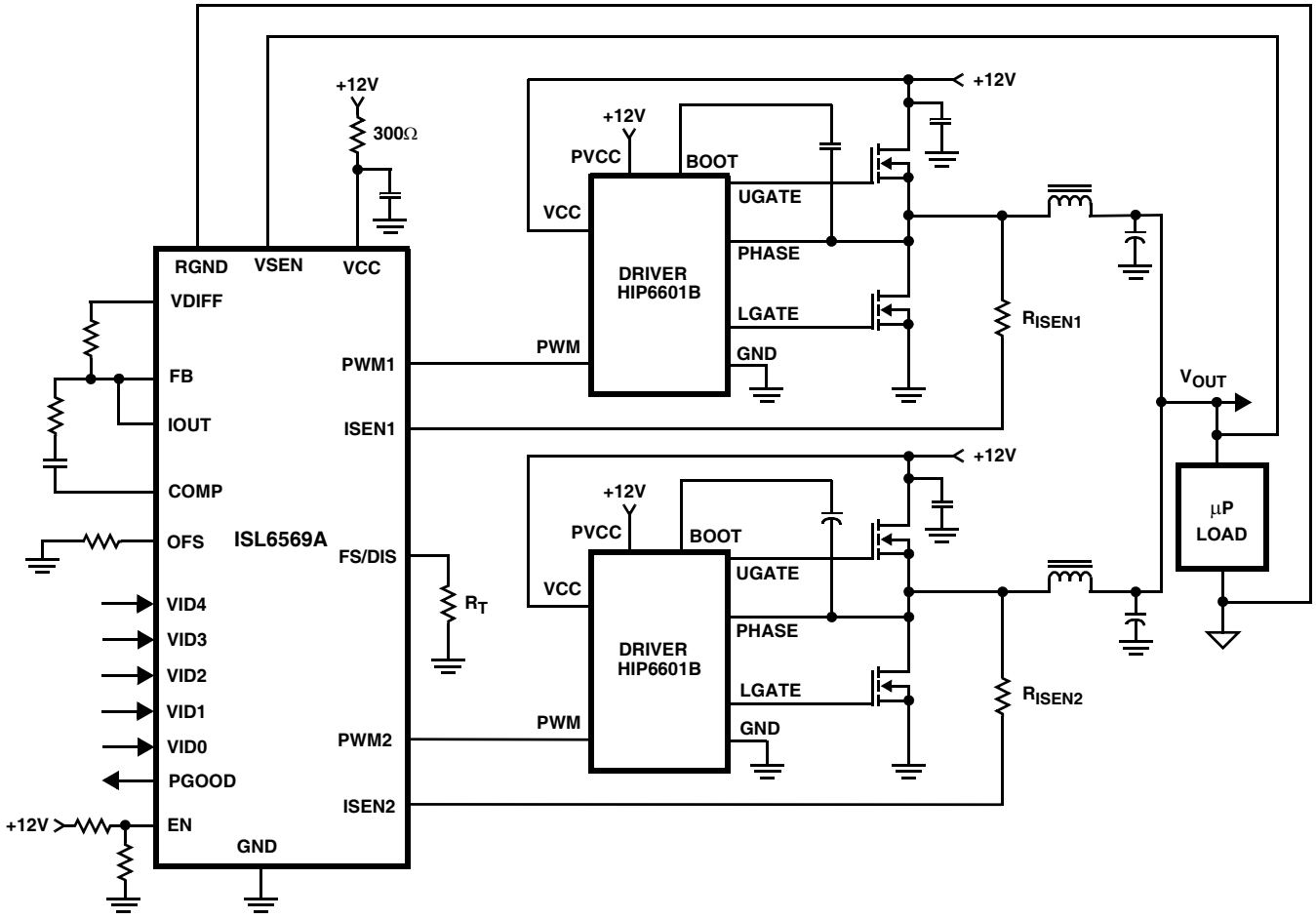
ISL6569ACR (32 LD 5x5 QFN)
TOP VIEW



Block Diagram



Typical Application - 2 Phase Converter



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . +7V
Input, Output, or I/O Voltage. . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 3kV

Operating Conditions

Supply Voltage, VCC . . . . . +5V ±5%
Ambient Temperature. . . . . 0^oC to 70^oC
Junction Temperature. . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package (Note 1)	63	N/A
QFN Package (Notes 2, 3).	32	4

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature. . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, $T_A = 0^o$ C to 70^oC. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R_T = 100 kΩ ±1%	8.0	10.8	14.0	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R_T = 100 kΩ ±1%	8.0	10.3	13.0	mA
SHUNT REGULATOR					
VCC Voltage	VCC tied to 12VDC thru 300Ω resistor, R_T = 100kΩ	5.63	5.8	5.97	V
VCC Sink Current	VCC tied to 12VDC thru 300Ω resistor, R_T = 100kΩ	15	20	25	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC Rising	4.25	4.35	4.50	V
	VCC Falling	3.75	3.85	4.00	V
ENABLE Threshold	EN Rising	1.205	1.23	1.255	V
	Hysteresis	86	92	98	mV
REFERENCE VOLTAGE AND DAC					
Reference Voltage		0.792	0.8	0.808	V
System Accuracy	(Note 4)	-0.5	-	0.5	%VID
VID on Fly Step Size	R_T = 100kΩ	-	25	-	mV
VID Pull Up		-	-20	-	µA
VID Input Low Level		-		0.8	V
VID Input High Level		-	1.36	1.6	V
PIN-ADJUSTABLE OFFSET					
OFS Current		-	100	-	µA
Offset Accuracy	ROFS = 5.00kΩ ±1%	47.0	50.0	53.0	mV
OSCILLATOR					
Accuracy		-10	-	10	%
Adjustment Range		0.08	-	1.0	MHz

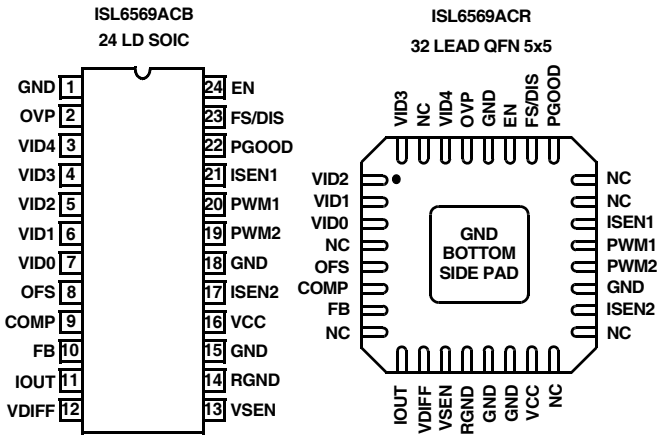
Electrical Specifications Operating Conditions: VCC = 5V, $T_A = 0^o$ C to 70^oC. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Disable Voltage	$I_{FS/DIS}$ = 1mA	0.8	1.0	1.2	V
Sawtooth Amplitude		-	1.37	-	V
Max Duty Cycle		-	75	-	%
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	-	72	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, Load = ±400mA	-	7.1	11	V/µs
Maximum Output Voltage	R_L = 10kΩ to ground	3.6	4.5	-	V
Source Current		3.0	7.0	9.0	mA
Sink Current		1.6	3.0	5.4	mA
REMOTE-SENSE AMPLIFIER					
Input Impedance		-	80	-	kΩ
Bandwidth		-	20	-	MHz
Slew Rate		-	6	-	V/µs
SENSE CURRENT					
IOUT Accuracy	ISEN1 = ISEN2 = 50µA	-5	-	5	%
ISEN Offset Voltage		-	6	-	mV
Over-Current Trip Level		72	90	108	µA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
Under-Voltage Offset From VID	VSEN Falling	320	350	420	mV
Over-Voltage Threshold	VSEN Rising	2.08	2.13	2.20	V
OVP Voltage	I_{OVP} = 100mA, VCC = 5V	2.2	3.28	4.0	V

NOTE:

4. These parts are designed and adjusted for accuracy within the system tolerance.

Functional Pin Description



GND

Bias and reference ground for the IC.

OVP

Over-voltage protection pin. This pin is pulled to VCC and is latched when an over-voltage condition is detected. Connect this pin to the gate of an SCR or MOSFET tied across V_{IN} and ground. A fuse must be placed upstream to open the input supply rail and prevent damage to the load device.

VID4, VID3, VID2, VID1, VID0

The state of these five inputs program the internal DAC, which provides the reference voltage for output regulation. Connect these pins to either open-drain or active pull-up type outputs. Pulling these pins above 2.9V can cause a reference offset inaccuracy.

OFS

Connecting a resistor between this pin and ground creates a positive offset voltage which is added to the DAC voltage, allowing easy implementation of load-line regulation. For no offset, simply tie this pin to ground.

FB and COMP

The internal error amplifier inverting input and output respectively. Connect the external R-C feedback compensation network of the regulator to these pins.

IOUT

The current carried out of this pin is proportional to output current and can be used to incorporate output voltage droop and/or load sharing. The scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$. If droop is desired, connect this pin to FB. When not used for droop or load sharing, simply leave this pin open.

VSEN, RGND, VDIFF

VSEN and RGND are the inputs to the differential remote-sense amplifier. Connect these pins to the sense points of the remote load. Connect an appropriately sized feedback resistor, R_{FB}, between VDIFF and FB.

VCC

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply or through a series 255Ω resistor to a +12V supply.

ISEN1, ISEN2

Current sense inputs. A resistor connected between these pins and their respective phase nodes sets a current proportional to the current in the lower MOSFET during it's conduction interval. This current is used as a reference for channel balancing, load sharing, protection, and load-line droop.

PWM1, PWM2

Pulse-width modulating outputs. Connect these pins to the individual HIP660x driver PWM input pins. These logic outputs command the driver IC(s) in switching the half-bridge configuration of MOSFETs.

PGOOD

Power good is an open-drain logic output that changes to a logic low when the voltage at VDIFF is 350mV below the VID setting or above 2.2V.

FS/DIS

A dual function pin for setting the switching frequency and disabling the controller. Place a resistor from this pin to ground to set the switching frequency between 25kHz and 1MHz. Pulling this pin below 0.8V disables the controller.

EN

Threshold sensitive enable input of the controller. Transition this pin above 1.23V (typical enable threshold) to initiate a soft-start cycle. Pull this pin below 1.14V, taking into account the enable hysteresis, to disable the controller once in operation. Connect a resistor divider to this pin to set the power-on voltage level for proper coordination with Intersil MOSFET drivers. If this function is not required, simply tie this pin to VCC.

Multi-Phase Control

Microprocessor load current profiles have increased to the point where the multi-phase power conversion advantage is pronounced. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6569A controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram in Figure 1 provides a top level view of multi-phase power conversion using the ISL6569A controller.

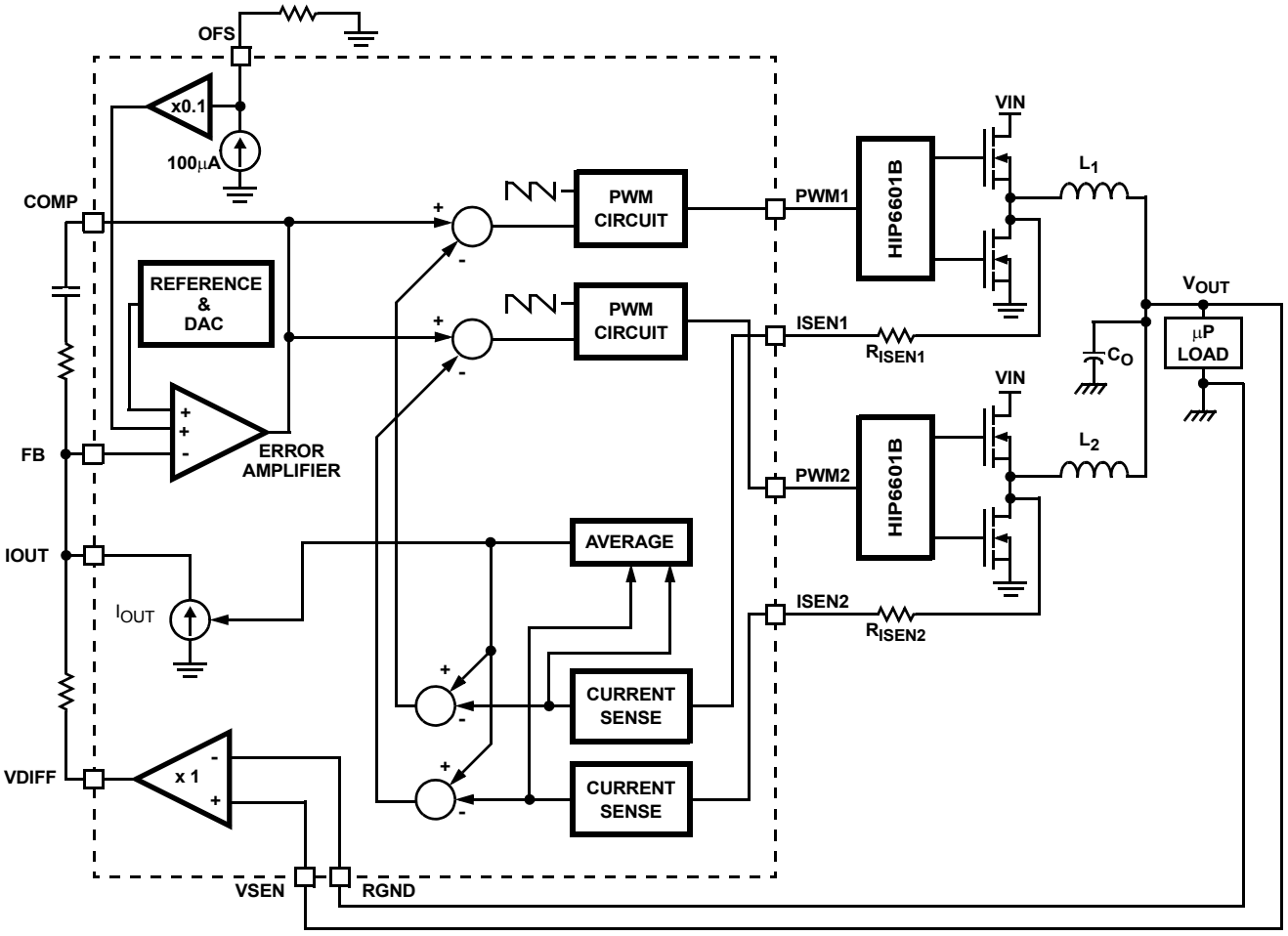


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF A ISL6569A CONVERTER

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with the other channel. In a 2-phase converter, channel-2 switches half a cycle after channel-1. As a result, the converter has a ripple frequency twice that of either phase. Figure 2 illustrates the multiplicative effect on output ripple frequency. The two channel currents (IL1 and IL2), combine to form the AC ripple current and the DC load current. The ripple component has twice the ripple frequency of either channel current. Each PWM pulse is terminated half of a cycle, or 2.0µs, after the PWM pulse of the previous phase. The peak-to-peak current waveform for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

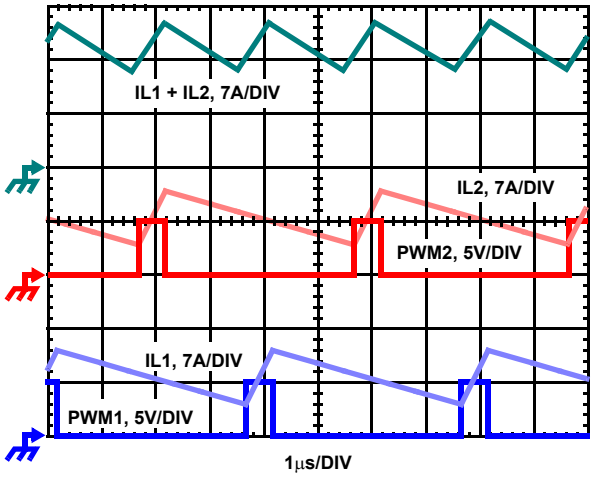


FIGURE 2. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 2-PHASE CONVERTER

In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases. To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of two symmetrically phase-shifted inductor currents in Equation 2.

$$I_{C,PP} = \frac{(V_{IN} - 2V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 2)}$$

Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 3 illustrates input currents from a two-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 3 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 8.6A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter input capacitor bank must support 38% more RMS current than an equivalent 2-phase converter.

Figure 16 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle. It is provided as an aid in determining the optimal input capacitor solution.

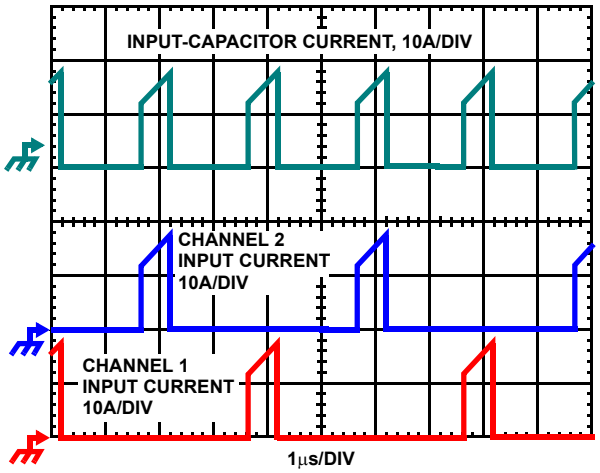


FIGURE 3. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

PWM Operation

One switching cycle is defined as the time between PWM1 pulse termination signals. The pulse termination signal is an internally generated clock signal which triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS/DIS pin and ground. Each cycle begins when the clock signal commands the channel-1 PWM output to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. The PWM2 pulse terminates 1/2 of a cycle after PWM1.

Once a PWM signal transitions low, it is held low for a minimum of 1/4 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 1. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

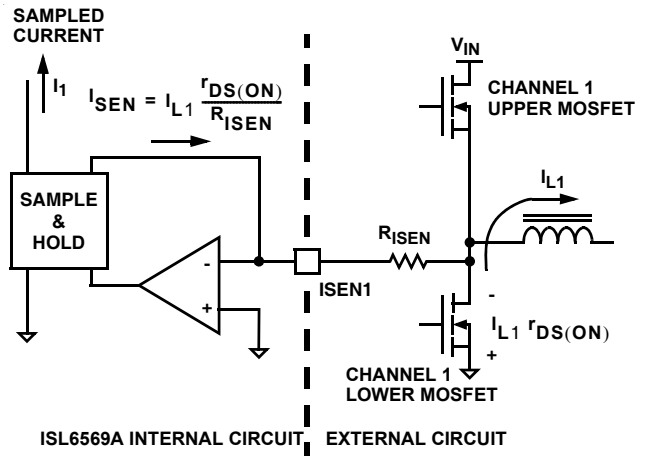


FIGURE 4. CHANNEL 1 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

Current Sensing

During the forced off time following a PWM transition low, the controller senses channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$. A ground-referenced amplifier, internal to the ISL6569A, connects to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is then sampled and held after sufficient settling time every switching cycle. The sampled current is used for channel-current balance, load-line regulation, overcurrent protection, and module current sharing.

The circuitry shown in Figure 4 represents channel-1 of a two channel converter. This circuitry is repeated for channel-2 of the converter. From Figure 4, the following equation for channel-1 sampled current, I_1, is derived

$$I_1 = I_{L1} \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 3)}$$

where I_{L1} is half of the total load current.

If $r_{DS(ON)}$ sensing is not desired, an independent current-sense resistor in series with the lower MOSFET source can serve as a sense element.

Channel-Current Balance

The sampled current from both channels, I_1 and I_2, is used to gauge both overall load current and the relative channel current carried in each leg of the converter. The individual sample currents are averaged. The resulting average current, I_{AVG}, provides a measure of the total load current demand on the converter and the appropriate level of channel current. Using Figures 4 and 6, the average current is defined as:

$$I_{AVG} = \frac{I_1 + I_2}{2} \quad \text{(EQ. 4)}$$

$$I_{AVG} = \frac{I_{OUT}}{2} \frac{r_{DS(ON)}}{R_{ISEN}}$$

where I_{OUT} is the total load current.

The average current is then subtracted from the individual channel sample currents. The resulting error current, I_{ER}, is then filtered before it adjusts V_{COMP}. The modified V_{COMP} signal is compared to a sawtooth ramp signal and produces a pulse width which corrects for any unbalance and drives the error current toward zero. Figure 6 illustrates Intersil's patented current balance method as implemented on one channel of a multi-phase converter.

Two considerations designers face are MOSFET selection and inductor design. Both are significantly improved when channel currents track at any load level. The need for complex drive schemes for multiple MOSFETs, exotic magnetic materials, and expensive heat sinks is avoided. Resulting in a cost-effective and easy to implement solution relative to single-phase conversion. Channel current balance insures the thermal advantage of multi-phase conversion is realized. Heat dissipation is spread over multiple channels and a greater area than single phase approaches.

In some circumstances, it may be necessary to deliberately design some channel-current unbalance into the system. In a highly compact design, one channel may be able to cool more effectively than the other due to nearby air flow or heat sinking components. The other channel may have more difficulty cooling with comparatively less air flow and heat sinking. The hotter channel may also be located close to other heat-generating components tending to drive it's temperature even higher. In these cases, the proper selection of the current sense resistors (R_{ISEN} in Figure 4) introduces channel current unbalance into the system. Increasing the value of R_{ISEN} in the cooler channel and decreasing it in the hotter channel moves both channels into thermal balance at the expense of current balance.

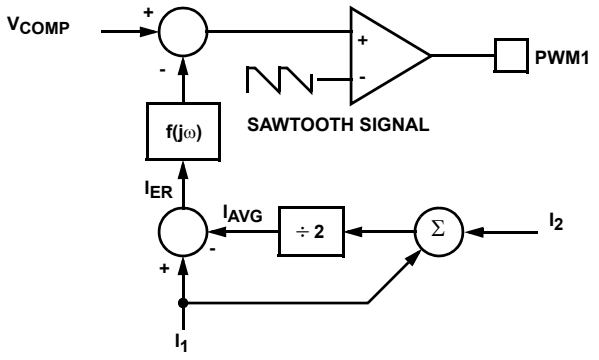


FIGURE 5. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Voltage Regulation

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to modulate the pulse width of the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. Three distinct inputs to the error amplifier determine the voltage level of V_{COMP}. The internal and external circuitry which control voltage regulation is illustrated in Figure 6.

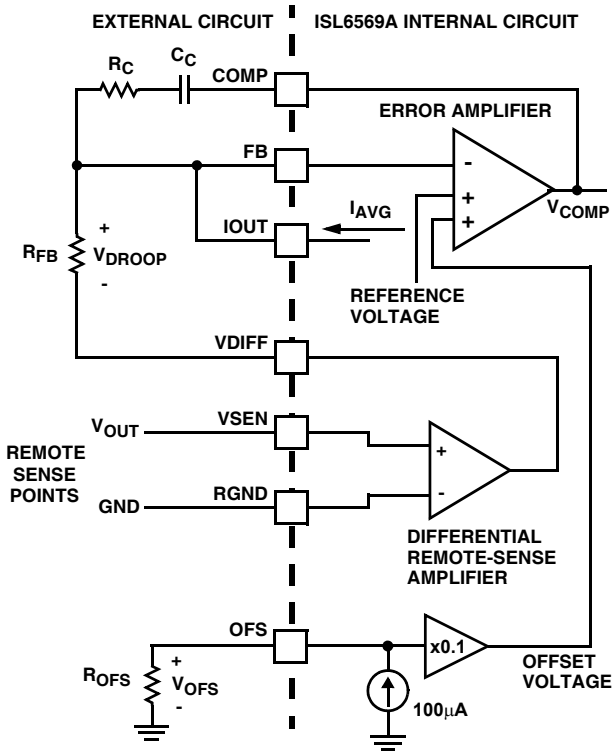


FIGURE 6. OUTPUT-VOLTAGE AND LOAD-LINE REGULATION

Most multi-phase controllers simply have the output voltage fed back to the inverting input of the error amplifier through a resistor. The ISL6569A features an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense amplifier output, V_{DIFF}, is then tied through an external resistor to the inverting input of the error amplifier.

A digital to analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID4 through VID0. The DAC decodes the a 5-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 20µA pull-up to an internal 2.5V source for use with open-drain outputs. External pull-up resistors or active-high output stages can augment the pull-up current sources, but a slight accuracy error can occur if they are pulled above 2.9V. The DAC-selected reference voltage is connected to the non-inverting input of the error amplifier.

The ISL6569A features a second non-inverting input to the error amplifier which allows the user to directly offset the DAC reference voltage in the positive direction only. The offset voltage is created by an internal current source which feeds out the OFS pin into a user selected external resistor to ground. The resulting voltage across the resistor, V_{OFS}, is internally divided down by ten to create the offset voltage. This method of offsetting the DAC voltage is more accurate than external methods of level-shifting the FB pin.The integrating compensation network shown in Figure 6 assures that the steady-state error in the output voltage is limited to the error in the reference voltage (output of the DAC) plus offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6569A to include all variations in current sources, amplifiers and the reference so that the output voltage remains within the specified system tolerance of ±0.5% over temperature.

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925

TABLE 1. VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	DAC
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

LOAD-LINE REGULATION

Microprocessor load current demands change from near no-load to full load often during operation. The resulting sizable transient current slew rate causes an output voltage spike since the converter is not able to respond fast enough to the rapidly changing current demands. The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. In order to drive the cost of the output capacitor solution down, one commonly accepted approach is active voltage positioning. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works against the voltage spike.

The average current of all the active channels, I_{AVG}, flows out IOUT, see Figure 6. IOUT is connected to FB through a load-line regulation resistor, R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as

$$V_{DROOP} = I_{AVG} R_{FB} \quad \text{(EQ. 5)}$$

In most cases, each channel uses the same R_{ISEN} value to sense current. A more complete expression for V_{DROOP} is derived by combining Equations 4 and 5.

$$V_{DROOP} = \frac{I_{OUT}}{2} \frac{r_{DS(ON)}}{R_{ISEN}} R_{FB} \quad \text{(EQ. 6)}$$

Droop is an optional feature of the ISL6569A. If active voltage positioning is not required, simply leave the IOUT pin open.

REFERENCE OFFSET

Typical microprocessor tolerance windows are centered around a nominal DAC set point. Implementing a load-line requires offsetting the output voltage above this nominal DAC set point; centering the load-line within the static specification window. The ISL6569A features an internal 100µA current source which feeds out the OFS pin. Placing a resistor from OFS and ground allows the user to set the amount of positive offset desired directly to the reference voltage. The voltage developed across the OFS resistor, R_{OFS}, is divided down internally by a factor of 10 and directly counters the DAC voltage at the error amplifier non-inverting input. Select the resistor value based on the voltage offset desired, V_{OFS}, using Equation 7

$$R_{OFS} = \frac{V_{OFS} \cdot 10}{100\mu A} \quad \text{(EQ. 7)}$$

DYNAMIC VID

Next generation microprocessors can change VID inputs at any time while the regulator is in operation. The power management solution is required to monitor the DAC inputs and respond to VID voltage transitions, or 'on-the-fly' VID changes, in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption.

The ISL6569A checks the five VID inputs at the beginning of each channel-1 switching cycle. If the VID code has changed, the controller waits one complete switching cycle to validate the new code. If the VID code is stable for this entire switching cycle, then the controller will begin executing the output voltage change. The controller begins incrementing the reference voltage by making 25mV steps every two switching cycles until it reaches the new VID code.

The total time required for a VID change, t_{DV}, is dependent on the switching frequency (f_S), the size of the change (ΔVID), and the time before the next switching cycle begins. Since the ISL6569A recognizes VID-code changes only at the beginning of switching cycles, up to one full cycle may pass before a VID change registers. This is followed by a one-cycle wait before the output voltage begins to change. The one-cycle uncertainty in Equation 8 is due to the possibility that the VID code change may occur up to one full cycle before being recognized.

$$\frac{1}{f_S}\left(\frac{2\Delta VID}{0.025} - 1\right) < t_{DV} \leq \frac{1}{f_S}\left(\frac{2\Delta VID}{0.025}\right) \quad \text{(EQ. 8)}$$

The time required for a converter running with f_S = 500kHz to make a 1.2V to 1.4V reference-voltage change is between 30µs and 32µs as calculated using Equation 8. This example is also illustrated in Figure 7.

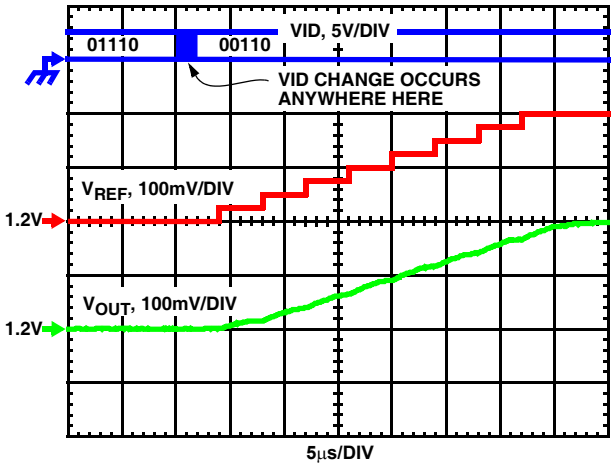


FIGURE 7. DYNAMIC-VID WAVEFORMS FOR 500kHz ISL6569A BASED MULTI-PHASE BUCK CONVERTER

Operation Initialization

Before converter operation is initialized, proper conditions must exist on the enable and disable inputs. Once these conditions are met, the controller begins a soft-start interval. Once the output voltage is within the proper window of operation, the PGOOD output changes state to update an external system monitor.

Enable and Disable

The PWM outputs are held in a high-impedance state to assure the drivers remain off while in shutdown mode. Four separate input conditions must be met before the ISL6569A is released from shutdown mode.

First, the bias voltage applied at VCC must reach the internal power-on reset (POR) circuit rising threshold. Once this threshold is met, the EN input signal becomes the gate for soft-start initialization. Hysteresis between the rising and falling thresholds insures that once enabled, the ISL6569A will not inadvertently turn off unless the bias voltage drops substantially. See *Electrical Specifications* for specifics on POR rising and falling thresholds.

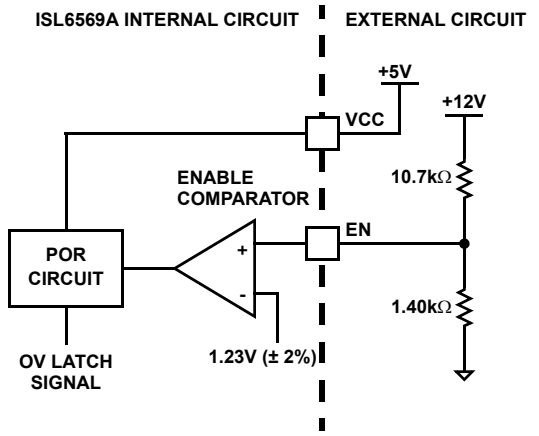


FIGURE 8. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

Second, the ISL6569A features an enable input (EN) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6569A in shutdown until the voltage at EN rises above 1.23V. The enable comparator has about 90mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the ISL6569A becomes enabled. The schematic in Figure 8 demonstrates sequencing the ISL6569A with the HIP660X family of Intersil MOSFET drivers which require 12V bias.

Third, the frequency select/disable input (FS/DIS) will shutdown the converter when pulled to ground. Under this condition, the internal oscillator is disabled. The oscillator resumes operation upon release of FS/DIS and a soft-start sequence is initiated.

Finally, the 11111 VID code is reserved as a signal to the controller that no load is present. The controller will enter shutdown mode after receiving this code and will start up upon receiving any other code.

To enable the controller, VCC must be greater than the POR threshold; the voltage on EN must be greater than 1.23V; FS/DIS must not be grounded; and VID cannot be equal to 11111. Once these conditions are true, the controller immediately initiates a soft-start sequence.

Soft-Start

The soft-start time, t_{SS}, is determined by an 11-bit counter that increments with every pulse of the phase clock. For example, a converter switching at 250kHz per phase has a soft-start time of

$$T_{SS} = \frac{2048}{f_{SW}} = 8.3\text{ms} \quad \text{(EQ. 9)}$$

During the soft-start interval, the soft-start voltage, V_{RAMP}, increases linearly from zero to 140% of the programmed DAC voltage. At the same time a current source, I_{RAMP}, is decreasing from 160µA down to zero. These signals are connected as shown in Figure 9 (I_{OUT} may or may not be connected to FB depending on the particular application).

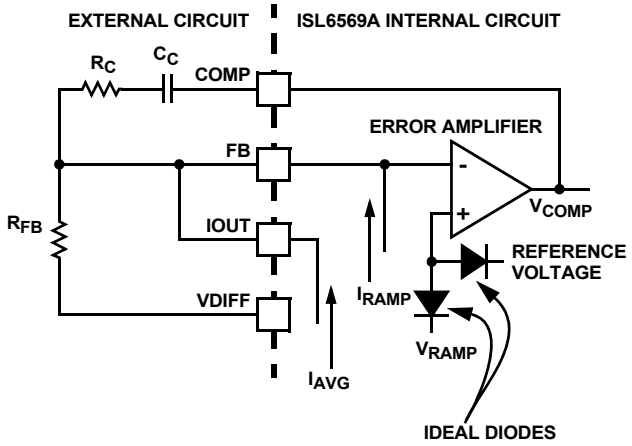


FIGURE 9. RAMP CURRENT AND VOLTAGE FOR REGULATING SOFT-START SLOPE AND DURATION

The ideal diodes in Figure 9 assure that the controller tries to regulate its output to the lower of either the reference voltage or V_{RAMP}. Since I_{RAMP} creates an initial offset across R_{FB} (R_{FB} x 160µA), the first PWM pulse will not be seen until V_{RAMP} is greater than the $R_{FB}I_{RAMP}$ offset. This produces a delay after the ISL6569A enables before the output voltage starts moving. For example, if VID = 1.5V, R_{FB} = 1kΩ and T_{SS} = 8.3ms, the delay time can be expressed using Equation 10.

$$t_{DELAY} = \frac{T_{SS}}{1 + \frac{1.4\,(VID)}{R_{FB}160 \times 10^{-6}}} = 560\mu\text{s} \quad \text{(EQ. 10)}$$

Following the delay, the soft start ramps linearly until V_{RAMP} reaches VID. For the system described above, this first linear ramp will continue for approximately

$$t_{RAMP1} = \frac{T_{SS}}{1.4} - t_{DELAY} \quad \text{(EQ. 11)}$$
$$= 5.27ms$$

The final portion of the soft-start sequence is the time remaining after V_{RAMP} reaches VID and before I_{RAMP} gets to zero. This is also characterized by a slight change in the slope of the output voltage ramp which, for the current example, exists for a time of

$$t_{RAMP2} = T_{SS} - t_{RAMP1} - t_{DELAY} \quad \text{(EQ. 12)}$$
$$= 2.34ms$$

This behavior is seen in the example in Figure 10 of a converter switching at 500kHz. For this converter, R_{FB} is set to 2.67kΩ leading to T_{SS} = 4.0ms, t_{DELAY} = 700ns, t_{RAMP1} = 2.23ms, and t_{RAMP2} = 1.17ms.

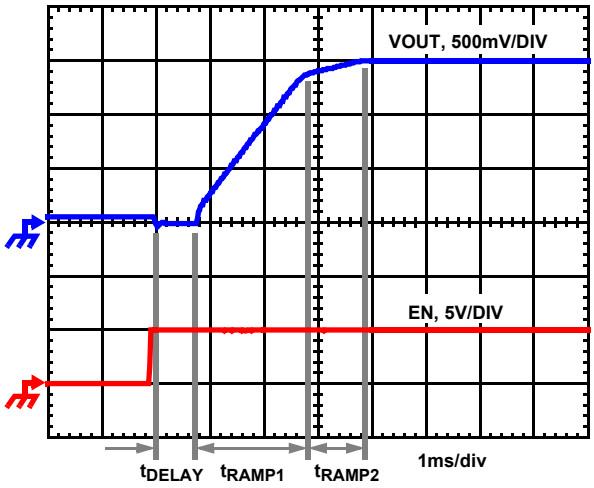


FIGURE 10. SOFT-START WAVEFORMS FOR ISL6569A BASED MULTI-PHASE BUCK CONVERTER

NOTE: Switching frequency 500kHz and R_{FB} = 2.67kΩ

Fault Monitoring and Protection

The ISL6569A actively monitors voltage and current feedback to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indication signal is provided for linking to external system monitors. The schematic in Figure 11 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output which indicates that the converter is operating properly and the output voltage is within a set window. The under-voltage (UV) and over-voltage (OV) comparators create the output voltage window. The controller also takes advantage of current feedback to detect output over-current (OC)

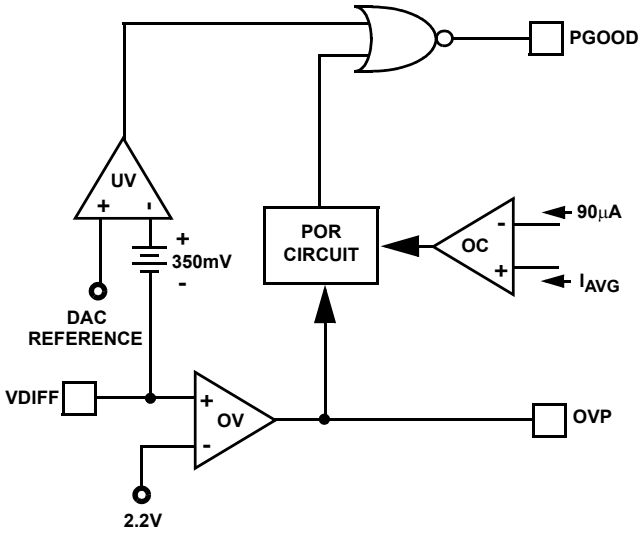


FIGURE 11. POWER GOOD AND PROTECTION CIRCUITRY

conditions. PGOOD pulls low during shutdown and releases high during soft-start once the output voltage exceeds the UV threshold. Once high, PGOOD will only transition low when the controller is disabled or a fault condition is detected. It will return high under certain circumstances once a fault clears.

Under-Voltage Protection

The voltage on V_{DIFF} is internally offset by 350mV before it is compared with the DAC reference voltage. By positively offsetting the output voltage, an UV threshold is created which moves relative to the VID code. During soft-start, the slow rising output voltage eventually exceeds the UV threshold. Assuming the POR leg of the PGOOD NOR gate has not detected an OC fault, the PGOOD signal will go high.

If a fault condition arises during operation and the output voltage drops below the UV threshold, PGOOD will immediately pull low, but converter operation will continue. PGOOD will return high once the output voltage surpasses the UV threshold.

If the ISL6569A is disabled during operation, the PGOOD signal will not pull low until the output voltage decays below the UV threshold.

Over-Voltage Protection

When the output of the differential amplifier (VDIFF) reaches 2.2V, PGOOD immediately goes low indicating a fault. Two protective actions are taken by the ISL6569A to protect the microprocessor load.

First, all PWM outputs are commanded low. Directing the Intersil drivers to turn on the lower MOSFETs; shunting the output to ground preventing any further increase in output voltage. The PWM outputs remain low until VDIFF falls to the programmed DAC level at which time they go into a high-

impedance state. The Intersil drivers respond by turning off both upper and lower MOSFETs. If the over-voltage condition reoccurs, the ISL6569A will again command the lower MOSFETs to turn on. The ISL6569A will continue to protect the load in this fashion as long as the over-voltage repeats.

Second, the OVP pin pulls to VCC and can deliver 100mA into the gate of either a MOSFET or SCR placed on the input rail (V_{IN}) or V_{OUT}. Turning on the MOSFET or SCR collapses the power rail and causes a fuse placed further up stream to blow. The fuse must be sized such that the MOSFET or SCR will not overheat before the fuse blows.

Once an over-voltage condition is detected, normal PWM operation ceases and PGOOD remains low until the ISL6569A is reset. Cycling the voltage on EN below 1.23V or the bias to VCC below the POR-falling threshold will reset the controller.

Over-Current Protection

The ISL6569A takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an over-current condition. See the *Channel-Current Balance* section for more detail on how the average current is created. The average current is continually compared with a constant 90µA reference current. Once the average current exceeds the reference current, the comparator triggers the converter to shutdown. The POR circuit places all PWM signals in a high-impedance state which commands the drivers to turn off both upper and lower MOSFETs. PGOOD pulls low and the system remains in this state while the controller counts 2048 phase clock cycles. This is followed by a soft-start attempt (see *Soft-Start*).

During the soft-start interval, the over-current protection circuitry remains active. As the output voltage ramps up, if an over-current condition is detected, the ISL6569A immediately places all PWM signals in a high-impedance state. The ISL6569A repeats the 2048-cycle wait period and follows with another soft-start attempt, as shown in Figure 12. This hiccup mode of operation repeats up to seven times. On the eighth soft-start attempt, the part latches off. Once latched off, the ISL6559 can only be reset when the voltage on EN is brought below 1.23V or VCC is brought below the POR falling threshold. Upon completion of a successful soft-start attempt, operation will continue as normal, PGOOD will return high, and the over-current latch counter will reset.

During VID-on-the-fly transitions, the OC comparator output is blanked. The quality and mix of output capacitors used in different applications leads to a wide output capacitance range. Depending upon the magnitude and direction of the VID change, the change in voltage across the output capacitors could result in significant current flow. Summing this instantaneous current with the load current already present could drive the average current above the reference current level and cause an OC trip during the transition. By blanking the OC comparator during the VID-on-the-fly transition, nuisance tripping is avoided.

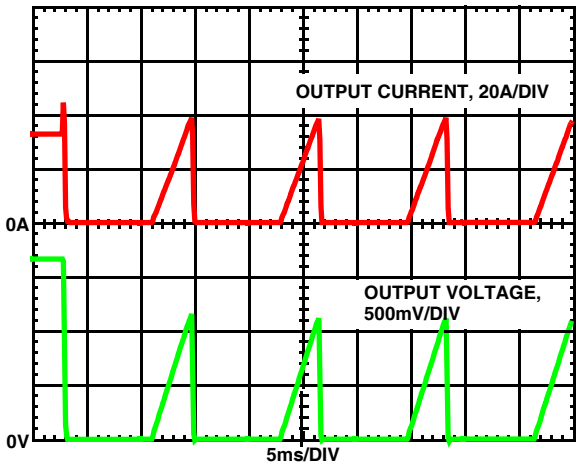


FIGURE 12. OVERCURRENT BEHAVIOR IN HICCUP MODE

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power-supply circuitry. Generally speaking, the most economical solutions are those where each phase handles between 15 and 20A. All surface-mount designs will tend toward the lower end of this current range and, if through-hole MOSFETs can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 30A per phase, but these designs require heat sinks and forced air to cool the MOSFETs.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 13, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor

current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_L = r_{DS(ON)}\left[\left(\frac{I_M}{2}\right)^2(1-d) + \frac{I_{L,PP}^2(1-d)}{12}\right] \quad \text{(EQ. 13)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_S; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_D = V_{D(ON)} f_S\left[\left(\frac{I_M}{2} + \frac{I_{PP}}{2}\right) t_{d1} + \left(\frac{I_M}{2} - \frac{I_{PP}}{2}\right) t_{d2}\right] \quad \text{(EQ. 14)}$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of P_L and P_D.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 15, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{2} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right) f_S \quad \text{(EQ. 15)}$$

The upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 16, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{2} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right) f_S \quad \text{(EQ. 16)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$ and is approximately

$$P_{UP,3} \approx V_{IN} Q_{rr} f_S \quad \text{(EQ. 17)}$$

Finally, the resistive part of the upper MOSFET's dissipation is given in Equation 18 as $P_{UP,4}$.

$$P_{UP,4} = r_{DS(ON)}\left[\left(\frac{I_M}{2}\right)^2 d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 18)}$$

In this case, of course, $r_{DS(ON)}$ is the on resistance of the upper MOSFET.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 15, 16, 17 and 18. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process that involves repetitively solving the loss equations for different MOSFETs and different switching frequencies until converging upon the best solution.

Current Sensing

The ISEN pins are denoted ISEN1 and ISEN2. The resistors connected between these pins and their respective phase nodes determine the gain in the load-line regulation loop and the channel-current balance loop. Select the values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full-load operating current, I_{FL}; according to Equation 19 (see also Figure 4).

$$R_{ISEN} = \frac{r_{DS(ON)}}{50 \times 10^{-6}} \frac{I_{FL}}{2} \quad \text{(EQ. 19)}$$

In certain circumstances, it may be necessary to adjust the value of one or both of the ISEN resistors. This can arise when the components of one channel are inhibited from dissipating their heat so that the affected channel runs hotter than desired (see the section entitled *Channel-Current Balance*). In this case, chose a new, smaller value of R_{ISEN} for the affected phase. Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 20)}$$

In Equation 20, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 20 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve perfect thermal balance between both channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 6. Its value depends on the desired full-load droop voltage (V_{DROOP} in Figure 6). If Equation 19 is used to select each ISEN resistor, the load-line regulation resistor is as shown in Equation 21.

$$R_{FB} = \frac{V_{DROOP}}{50 \times 10^{-6}} \quad \text{(EQ. 21)}$$

If one or both of the ISEN resistors was adjusted for thermal balance, as in Equation 20, the load-line regulation resistor should be selected according to Equation 22. Where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the n^{th} ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL}\, r_{DS(ON)}} \sum_{n} R_{ISEN(n)} \quad \text{(EQ. 22)}$$

Output Filter Design

The output inductors and the output capacitor bank together form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy during the interval of time after the beginning of the transient until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response leaving the output capacitor bank to supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 23)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance, but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR)\frac{\left(V_{IN} - 2V_{OUT}\right)V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \quad \text{(EQ. 24)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limits on inductance.

$$L \leq \frac{4CV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \quad \text{(EQ. 25)}$$

$$L \leq \frac{(2.5)C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right]\left(V_{IN} - V_O\right) \quad \text{(EQ. 26)}$$

Equation 26 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 25 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, and C is the total output capacitance.

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in *Load-Line Regulation*, there are two distinct methods for achieving these goals.

COMPENSATING LOAD-LINE REGULATED CONVERTER

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

Since the system poles and zero are effected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator by compensating the L-C poles and the ESR zero of the voltage-mode approximation yields a solution that is always stable with very close to ideal transient performance.

The feedback resistor, R_{FB}, has already been chosen as outlined in *Load-Line Regulation Resistor*. Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the three cases which follow, there is a separate set of equations for the compensation components.

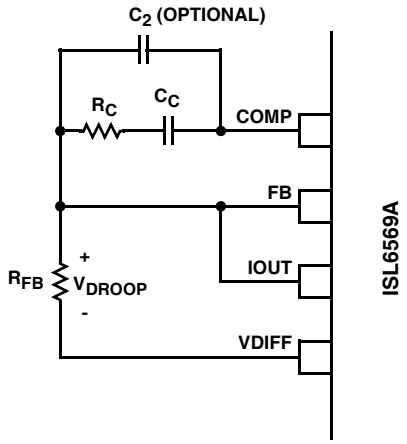


FIGURE 13. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6569A CIRCUIT

In Equations 27, L is the per-channel filter inductance divided by 2 (the number of active channels); C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 6 and *Electrical Specifications*.

Case 1:

$$\frac{1}{2\pi\sqrt{LC}} > f_0$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}\sqrt{LC}}{0.75V_{IN}}$$

$$C_C = \frac{0.75V_{IN}}{2\pi V_{PP} R_{FB} f_0}$$

Case 2:

$$\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.75\,V_{IN}} \qquad \text{(EQ. 27)}$$

$$C_C = \frac{0.75V_{IN}}{(2\pi)^2 f_0^2 V_{PP} R_{FB}\sqrt{LC}}$$

Case 3:

$$f_0 > \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp} L}{0.75\,V_{IN}(ESR)}$$

$$C_C = \frac{0.75V_{IN}(ESR)\sqrt{C}}{2\pi V_{PP} R_{FB} f_0\sqrt{L}}$$

Once selected, the compensation values in Equations 27 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equations 27 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 13). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any trailing edge jitter problem is noted.

Compensation without load-line regulation

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type-III controller, as shown in Figure 14, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to chose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

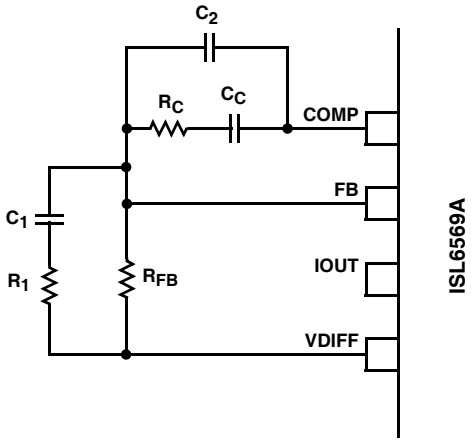


FIGURE 14. COMPENSATION CIRCUIT FOR ISL6569A BASED CONVERTER WITHOUT LOAD-LINE REGULATION

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equations 28, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equations 28.

$$R_1 = R_{FB}\frac{C(ESR)}{\sqrt{LC} - C(ESR)}$$

$$C_1 = \frac{\sqrt{LC} - C(ESR)}{R_{FB}}$$

$$C_2 = \frac{0.75V_{IN}}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}} \quad \text{(EQ. 28)}$$

$$R_C = \frac{V_{PP}(2\pi)^2 f_0 f_{HF} LCR_{FB}}{0.75V_{IN}\left[\left(2\pi f_{HF}\sqrt{LC} - 1\right)\right]}$$

$$C_C = \frac{0.75V_{IN}\left(2\pi f_{HF}\sqrt{LC} - 1\right)}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}}$$

In Equations 28, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 6 and *Electrical Specifications*.

Input Supply Voltage Selection

The VCC input of the ISL6569A can be connected to either a +5V supply directly or through a current limiting resistor to a +12V supply. An integrated 5.8V shunt regulator maintains the voltage on the VCC pin when a +12V supply is used. A 300Ω resistor is suggested for limiting the current into the VCC pin to approximately 20mA.

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Input Supply Voltage Selection*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

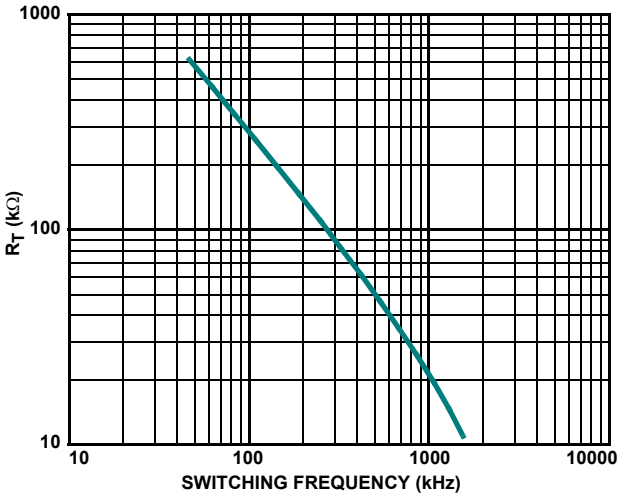


FIGURE 15. R_T vs SWITCHING FREQUENCY

Switching frequency is determined by the selection of the frequency-setting resistor, RT (see the figure *Typical Application* on page 4). Figure 15 and Equation 29 are provided to assist in the selecting the correct value for R_T.

$$R_T = 10^{[11.09 - 1.13\log(f_S)]} \quad \text{(EQ. 29)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

For a two phase design, use Figure 16 to determine the input-capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the combined peak-to-peak inductor current ($I_{C,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

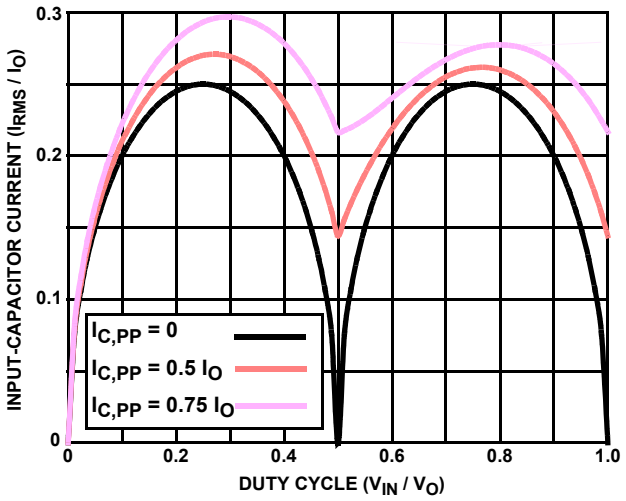


FIGURE 16. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

Layout Considerations

The following multi-layer printed circuit board layout strategies minimize the impact of board parasitics on converter performance. The following sections highlight some important practices which should not be overlooked during the layout process.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they switch large amounts of energy and tend to generate large amounts of noise. How the switching components are placed should also take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil HIP660X drivers as close as possible to the MOSFETs they control to reduce the parasitics due to trace length between critical driver input and output signals. If possible, duplicate the same placement of switching components for each phase.

Next, place the input and output capacitors. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains results in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity around the microprocessor socket.

The ISL6569A can be placed off to one side or centered relative to the individual phase switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the ISEN resistors, R_T resistor, feedback resistor, and compensation components.

Bypass capacitors for the ISL6569A and HIP660X driver bias supplies must be placed next to their respective pins. Stray trace parasitics will reduce their effectiveness.

Plane Allocation and Routing

Dedicate one solid layer, usually a middle layer, for a ground plane. Make all critical component ground connections with vias to this plane. Dedicate one additional layer for power planes; breaking the plane up into smaller islands of common voltage. Use the remaining layers for small signal wiring.

Route PHASE planes of copper filled polygons on the top and bottom once the switching component placement is set. Size the trace width between the driver gate pins and the MOSFET gates to carry 1A of current. When routing components in the switching path, use short wide traces to reduce the associated parasitics.

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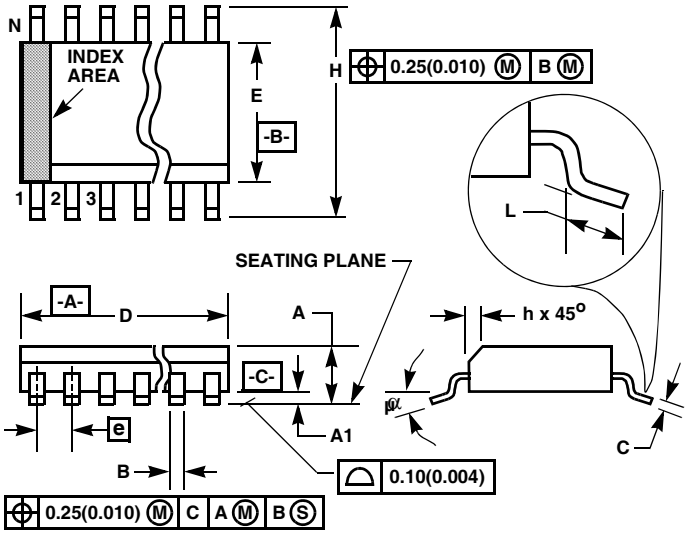
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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

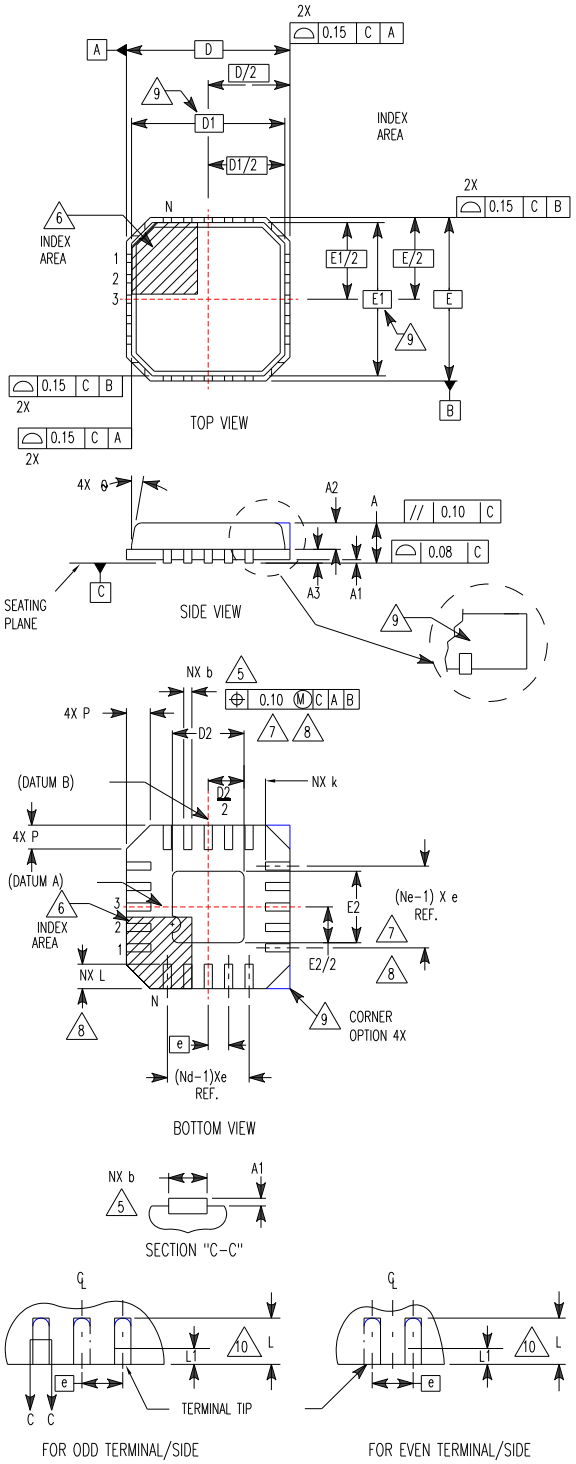
M24.3 (JEDEC MS-013-AD ISSUE C)

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.