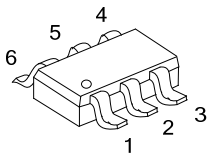
U74LVC2G07

CMOS IC

BUFFERS WITH OPEN-DRAIN OUTPUTS



SOT-363

■ DESCRIPTION

The **U74LVC2G07** provides two non-inverting buffers with open-drain output and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

This device has power-down protective circuit to preventing device from destruction when it is powered down.

■ FEATURES

* Wide Supply Voltage Range From 1.65V To 5.5V.
* Inputs Can Be Driven From Either 3.3V or 5V Devices.
* Low Power Dissipation: Ptot =300mW(Max)
* -24mA Output Drive(V_{CC}=3.0V)
* Power Down Protection
* Latch-Up Performance Exceeds 250mA.
* High Noise Immunity
* Direct Interface With TTL Levels

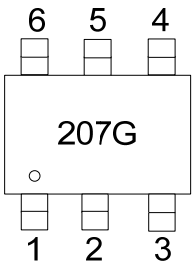
■ ORDERING INFORMATION

Ordering Number	Package	Packing
U74LVC2G07G-AL6-R	SOT-363	Tape Reel

U74LVC2G07G-AL6-R
- (1)Packing Type
- (2)Package Type
- (3)Halogen Free

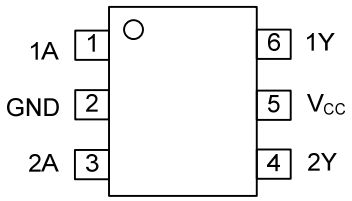
(1) R: Tape Reel
(2) AL6: SOT-363
(3) G: Halogen Free

■ MARKING



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■ PIN CONFIGURATION

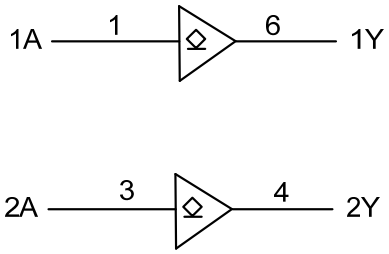


■ FUNCTION TABLE (Each Gate)

INPUT(nA)	OUTPUT(nY)
H	Z
L	L

Note: H = HIGH voltage level
L = LOW voltage level
Z = High-impedance OFF-state

■ LOGIC DIAGRAM (Positive Logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage(Active Mode)	V_{OUT}	-0.5~6.5	V
Output Voltage(Power-Down Mode)	V_{OUT}	-0.5~6.5	V
Input Clamp Current(V_{IN}<0)	I_{IK}	-50	mA
Output Clamp Current(V_{OUT}<0)	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Operating Ambient Temperature	T_{OPR}	-40 ~ +125	℃
Storage Temperature	T_{STG}	-65 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. When V_{CC} =0V(Power-Down Mode),the output voltage can be 5.5V in normal operation.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	1.65		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage	Active Mode	V_{OUT}	0		Vcc	V
	Vcc=0V; Power-Down Mode		0		5.5	

■ STATIC CHARACTERISTICS (T_{OPR} =-40℃ to +85℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC} =1.65V~1.95V	0.65*V_{CC}			V
		V_{CC} =2.3V~2.7V	1.7			
		V_{CC} =3.0V~3.6V	2.0			
		V_{CC} =4.5V~5.5V	0.7* V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} =1.65V~1.95V			0.35* V_{CC}	V
		V_{CC} =2.3V~2.7V			0.7	
		V_{CC} =3.0V~3.6V			0.8	
		V_{CC} =4.5V~5.5V			0.3* V_{CC}	
Low-Level Output Voltage	V_{OL}	V_{CC} =1.65V ~ 5.5V, I_{OL}=100μA			0.1	V
		V_{CC} =1.65V, I_{OL}=4mA			0.45	
		V_{CC} =2.3V, I_{OL}=8mA			0.3	
		V_{CC} =2.7V, I_{OL}=12mA			0.4	
		V_{CC} =3.0V, I_{OL}=24mA			0.55	
		V_{CC} =4.5V, I_{OL}=32mA			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC} =1.65V ~ 5.5V, V_{IN}=5.5V or 0		±0.1	±5	μA
Power OFF Leakage Current	I_{OFF}	V_{CC} =0V, V_{IN} or Vo=5.5V		±0.1	±10	μA
Quiescent Supply Current	I_Q	V_{CC} =5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0		0.1	10	μA
Additional Quiescent Supply Current per pin	ΔI_Q	V_{CC} =2.3V ~ 5.5V, V_{IN}=Vcc-0.6V, Io=0A		5	500	μA
Output OFF-state current	I_{OZ}	V_{CC} =5.5V, V_{IN}=V_{IH} or V_{IL} Vo = V_{CC} or GND		±0.1	±10	μA

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{OPR}=-40℃ to +85℃(note)						
Propagation delay from input (nA) to output(nY)	t_{PLZ}/t_{PZL}	V_{CC} = 1.65 ~ 1.95	1.0	3.5	6.7	ns
		V_{CC} = 2.3 ~ 2.7	0.5	2.4	4.3	
		V_{CC} = 2.7	1.0	2.3	4.3	
		V_{CC} = 3.0 ~ 3.6	0.5	2.6	3.7	
		V_{CC} = 4.5 ~ 5.5	0.5	1.5	2.9	

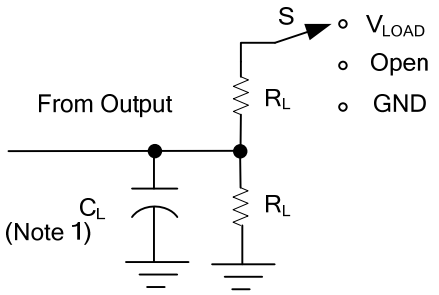
Note: All typical values are measured at T_{OPR} =25℃ and at Vcc=1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively.

■ OPERATING CHARACTERISTICS （T_A=25℃）

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power Dissipation Capacitance Per Gate	C_{PD}	V_{CC}=3.3V (Notes 1, 2)	6.5	pF
Input Capacitance	C_I		2.5	pF

Notes: 1. C_{PD} is used to determine the dynamic power dissipation (PD in μW).
PD = C_{PD} * Vcc2 * fi * N + Σ（CL *Vcc2* fo）where:
fi = Input Frequency in MHz;
fo= Output Frequency in MHz;
C_L= Output Load Capacitance in PF;
V_{CC} = Supply Voltage in Volts;
N= Total Load Switching Outputs.
Σ(C_L * Vcc2 * fo)= Sum of Outputs.
2. The Condition is V_{IN} = GND to Vcc.

■ TEST CIRCUIT AND WAVEFORMS

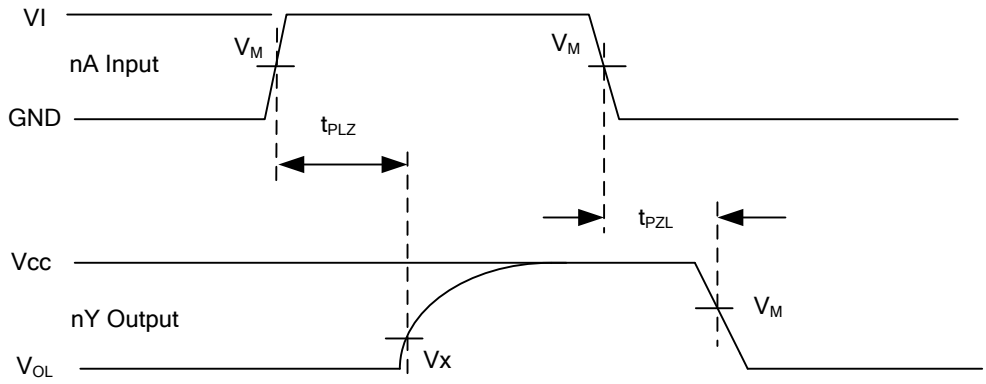


TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

Note 1: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R / t_F	V_M	V_{LOAD}	C_L	R_L	Vx
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	1KΩ	V_{OL} + 0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	500Ω	V_{OL} + 0.15V
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	V_{OL} + 0.3V
3.3V±0.3V	3 V	≤2.5ns	1.5V	6V	50pF	500Ω	V_{OL} + 0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2* V_{CC}	50pF	500Ω	V_{OL} + 0.3V

Note: VΔ= Vx - VOL



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