XX1001-QK

Doubler and Power Amplifier 18.0-21.0/36.0-42.0 GHz

Rev. V1

Mimix Broadband

Features

- Integrated Doubler and Power Amplifier
- Excellent Saturated Output Stage
- +25.0 dBm Output Power
- 50.0 dBc Fundamental Suppression
- RoHS* Compliant and 260°C Reflow Compatible

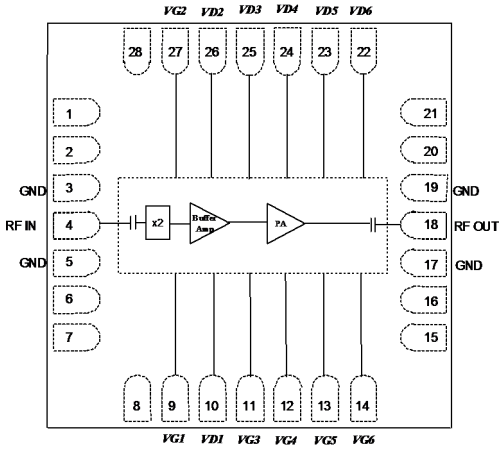
Description

M/A-COM Tech's 18.0-21.0/36.0-42.0 GHz GaAs doubler integrates a doubler, a buffer amplifier and 4 -stage power amplifier. The device provides better than +25.0 dBm output power and has excellent fundamental rejection. The device comes in a 7x7mm QFN package that is RoHS compliant. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XX1001-QK-0N00	bulk quantity
XX1001-QK-0N0T	tape and reel
XX1001-QK-EV1	evaluation board

Functional Block Diagram



Pin Configuration

Pin No.	Function	Pin No.	Function
3	Ground	17	Ground
4	RF Input	18	Output RF
5	Ground	19	Ground
9	Gate Bias (Doubler)	22	Drain Bias (PA)
10	Drain Bias (Doubler)	23	Drain Bias (PA)
11	Gate Bias (Buffer Amplifier)	24	Drain Bias (PA)
12	Gate Bias (PA)	25	Drain Bias (PA)
13	Gate Bias (PA)	26	Drain Bias (Buffer Amplifier)
14	Gate Bias (PA)	27	Gate Bias (PA)

Absolute Maximum Ratings[1]

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	800 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (RF Pin)	TBD
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to MTTF Table[1]
Channel Temperature (Tch)	MTTF Table[1]
Moisture Sensitivity Level	MSL3

(1) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

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• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
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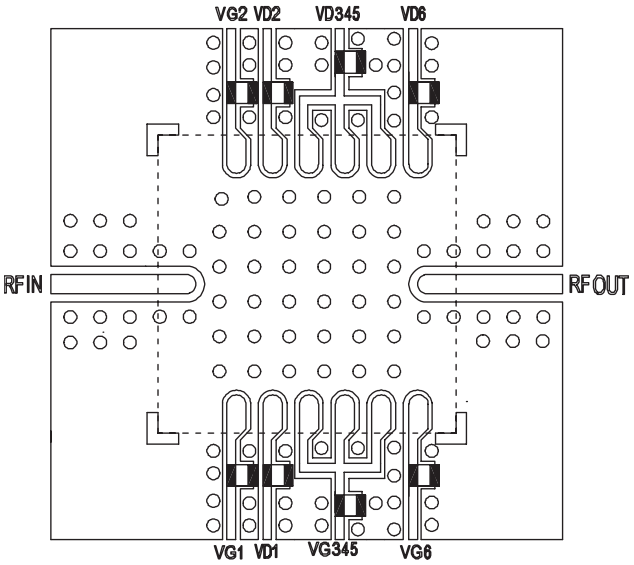
Electrical Specifications: 18-21 GHz (fin) (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Output Frequency Range (fout)	GHz	36.0	-	42.0
Input Return Loss (S11)	dB	-	TBD	-
Output Return Loss (S22)	dB	-	12.0	-
Fundamental Rejection	dBc	-	50.0	-
RF Input Power (RF Pin)	dBm	-	0.0	-
Output Power at 0.0 dBm Pin (Pout)	dBm	-	+26.0	-
Drain Supply Voltage (Vd1) Doubler	V	-	2.5	3.0
Drain Supply Voltage (Vd2) Buffer Amplifier	V	-	3.0	4.0
Drain Supply Voltage (Vd3,4,5,6) Power Amplifier	V	-	4.5	5.5
Gate Supply Voltage (Vg1) Doubler	V	-	-1.2	-
Drain Supply Current (Id1) Doubler	mA	-	<1.0	-
Drain Supply Current (Id2) Buffer Amplifier	mA	-	20	25
Drain Supply Current (Id3,4,5,6) (Vg=-0.7V Typical) Power Amplifier	mA	-	530	600

Recommended Layout



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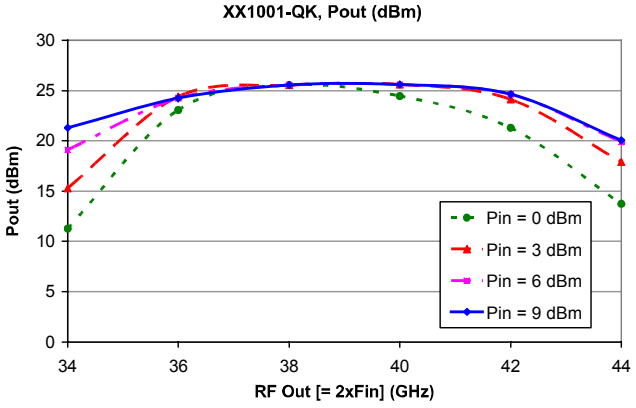
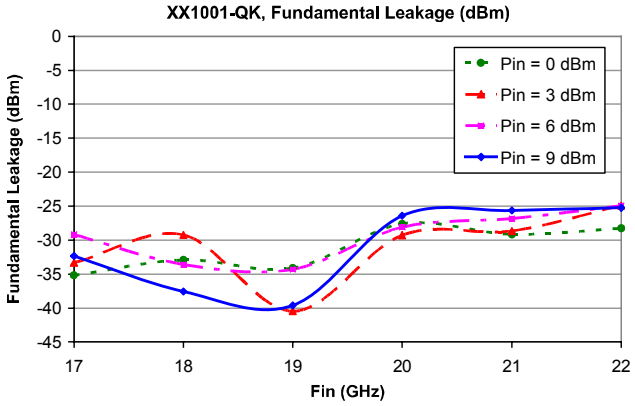
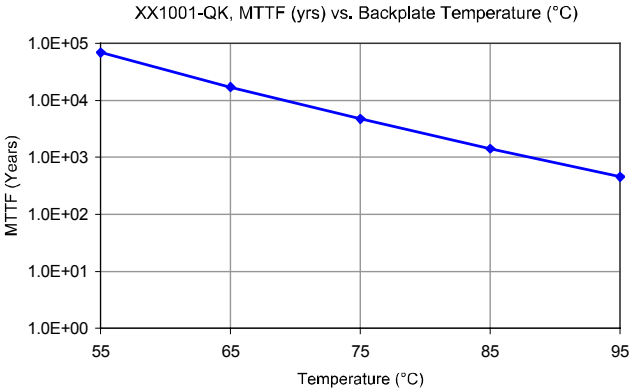
Typical Performance Curves (Measured at Nominal Conditions)





MTTF

MTTF is calculated from accelerated life-time data of single devices and assumes an isothermal back-plate.



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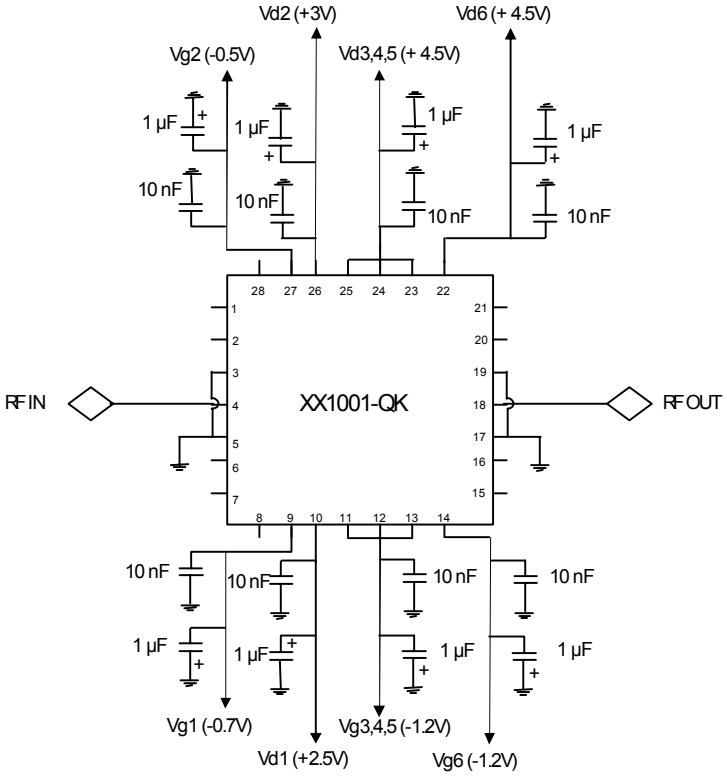
App Note [1] Biasing - Please refer to the application diagram below for recommended biasing information. The table below shows the recommended drain currents for each stage.

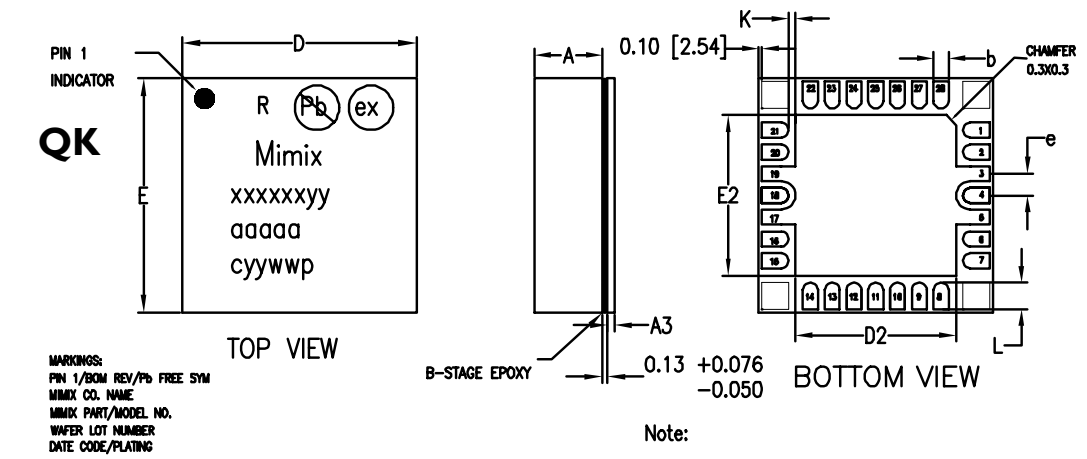
Pin	Voltage (V)	Current (mA)	Comment
VD1	2.5	<1	Drain Bias (Doubler)
VD2	3.0	20	Drain Bias (Buffer Amplifier)
VD3,4,5	4.5	260	Drain Bias (Power Amplifier)
VD6	4.5	270	Drain Bias (Power Amplifier—final stage)

It is possible to bias each stage separately for greater bias control with the following conditions: Id1<1mA, Id2=20mA, Id3=40mA, Id4=70mA, Id5=150mA, Id6=270mA. It is recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.7V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Bias Application Schematic



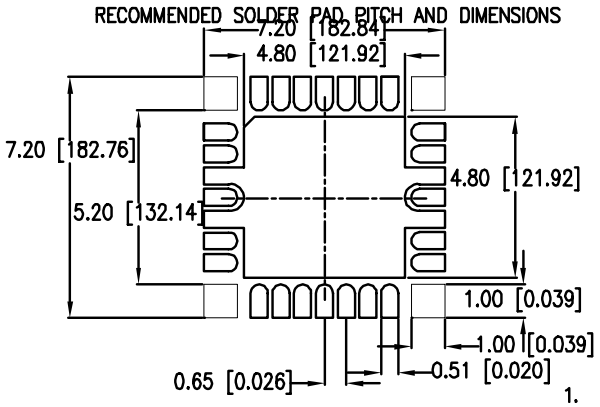
Lead-Free Package Dimensions/Layout



Note:

1. ALL DIMENSIONS ARE IN mm.

	MIN	TYP	MAX
A	1.20	1.25	1.30
A3		0.10 – 0.20 REF	
b	0.40	0.45	0.50
K	0.20	–	–
D		7.00 BSC	
E		7.00 BSC	
e		0.65	
D2	4.75	4.80	4.85
E2	4.75	4.80	4.85
L	0.75	0.80	0.85



1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.