3.2 mm x 2.5 mm Ceramic Package SMD Oscillator,
LVMOS / LVPECL / LVDS

ISM67 Series

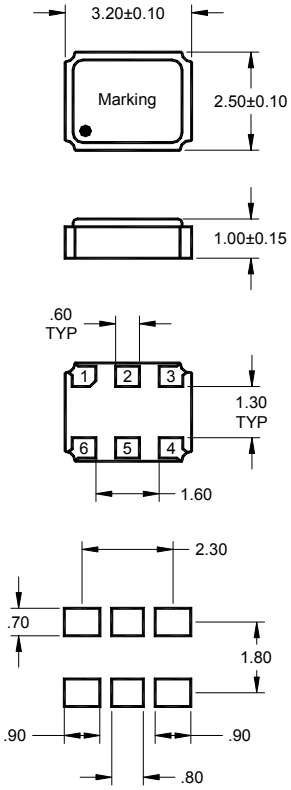
Product Features

Small Surface Mount Package
Fast Sample Delivery
Fast Sample Delivery
Pb Free/ RoHS Compliant
Leadfree Processing

Applications

xDSL
Broadcast Video
Wireless Base Stations
Sonet /SDH
WiMAX/WLAN
Server and Storage
Ethernet/LAN/WAN
Optical modules
Clock and data recovery
FPGA/ASIC
Backplanes
GPON

Frequency	
LVCMOS	10.000MHz to 250.000MHz
LVPECL	10.000MHz to 1500.000MHz
LVDS	10.000MHz to 1500.000MHz
Output Level	
LVCMOS	Logic "0" = 10% of Vcc max, Logic "1" = 90% of Vcc min
LVPECL	Logic "0"= Vcc-1.62V max., Logic "1" = 1.02 V min
LVDS	VOD=(Diff. Output) 350mV Typ.
Duty Cycle	
LVMOS	50% ±5% @ 50% of Vcc
LVPECL	50% ±5% @ 50%*
LVDS	50% ±5% @ 50%*
Rise / Fall Time	
LVCMOS	2.0 ns max. (10% to 90%)*
LVPECL	0.8 ns max. (20% to 80%)*
LVDS	0.8 ns max. (20% to 80%)*
Output Load	
LVCMOS	15pF
LVPECL	50 Ω to Vcc - 2.0 VDC
LVDS	RL=100 Ω/CL= 5pF
Frequency Stability	See Table Below
Supply Voltage (Vcc)	+3.30 VDC ± 5%, +2.50 VDC ± 5%
Aging	±3.0 ppm max per year
Current	HCMOS = 45 mA max LVPECL = 90 mA max LVDS = 35 mA max
Phase Jitter (RMS) (12kHz to 20MHz)	0.9 ps typical
Operating Temp. Range	See Table Below
Storage Temp. Range	-40° C to +85° C



Suggested Land Pattern

PIN CONNECTIONS	
PIN 1	Enable/Disable or N/C
PIN 2	Enable/Disable or N/C
PIN 3	Ground
PIN 4	Output
PIN 5	Comp. Output or N/C
PIN 6	Voltage Supply

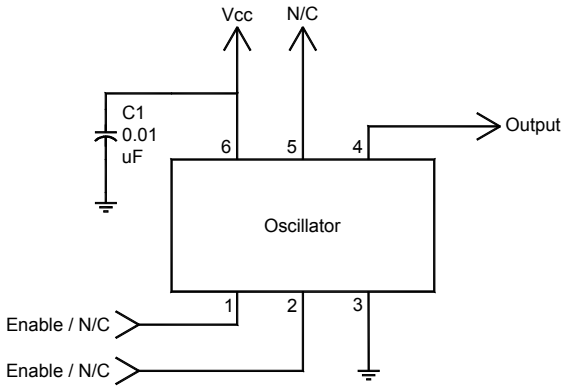
Dimension Units: mm

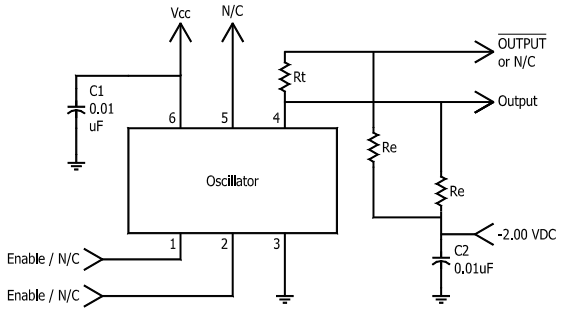
Part Number Guide **Sample Part Number: ISM67–31A9H2–155.520**

Package	Input Voltage	Operating Temperature	Stability (in ppm)	Output	Enable / Disable	Complimentary Ouput (Pin 5) **	Frequency
ISM67	3 = 3.3V	1 = 0° C to +70° C	F = ±20	3 = LVCMOS	H = Enable (Pin 1)	1 = N.C.	-155.520 MHz
	6 = 2.5V	2 = -40° C to +85° C	A = ±25	8 = LVDS	K = Enable (Pin 2)	2 = Output	
		3 = -20° C to +70° C	B = ±50	9 = LVPECL			

NOTE: A 0.01 µF bypass capacitor is recommended between V_{DD} (pin 6) and GND (pin 3) to minimize power supply noise. * Measured as percent of waveform. ** Available on LVDS and LVPECL ouput only.

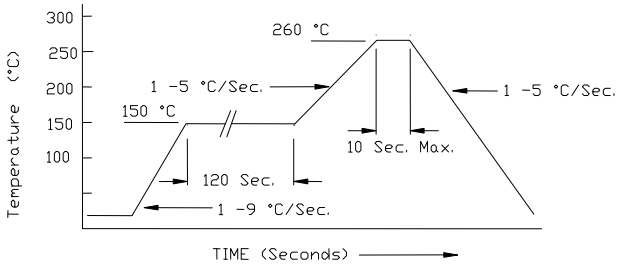
Typical Application:





Notes;
1. LVPECL Load = Use Re and -2.0 VDC Source.
2. LVDS Load = Omit Re and use Rt.

Pb Free Solder Reflow Profile:

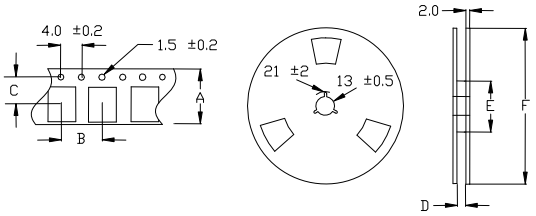


*Units are backward compatible with 240C reflow processes

Package Information:

MSL = N.A. (package does not contain plastic, storage life is unlimited under normal room conditions).
Termination = e4 (Au over Ni over W base metallization).

Tape and Reel Information:



Quantity per Reel	1000
A	16 +/-.3
B	8 +/-.2
C	7.5 +/-.2
D	17.5 +/-1
E	50 / 60 / 80
F	180 / 250

Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10-8 atm cc/s
Solvent Resistance	MIL-STD-202, Method 215

Marking

Line 1: ILSI and Date Code (YWW)
Line 2: Frequency