iPOWIR™ TECHNOLOGY

Synchronous Buck Multiphase Optimized BGA Power Block

Integrated Power Semiconductors, Drivers & Passives

Features:

- Output current 30A continuous with no derating up to T_{PCB} = 90°C and T_{CASE} = 90°C
- Operating frequency up to 1MHz
- Dual sided heatsink capable
- Very small 11mm x 11mm x 2.6mm profile
- iP2001 footprint compatible
- Internal features minimize layout sensitivity *
- Optimized for very low power losses

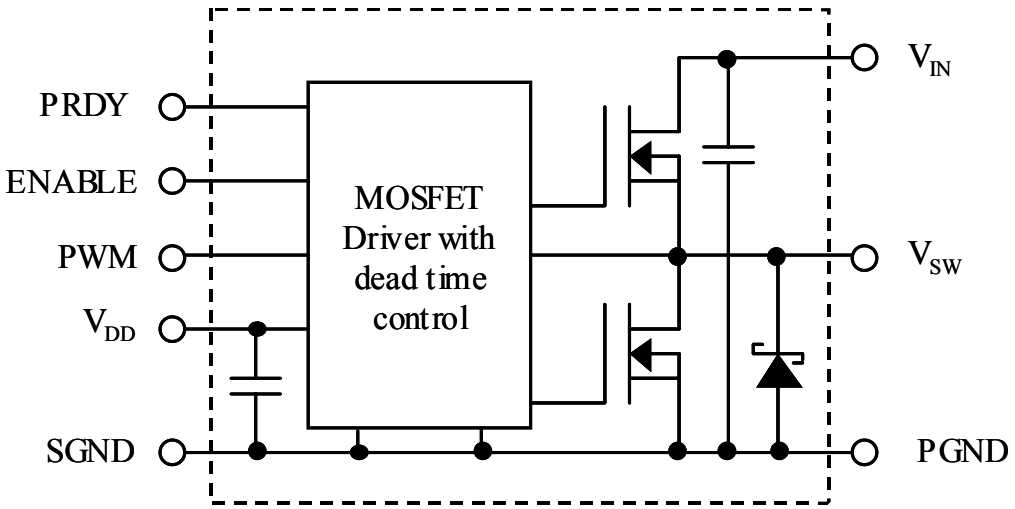
iP2002 Power Block

Description

The iP2002 is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 11mm x 11mm x 2.6mm BGA power block. The only additional components required for a complete multiphase converter are a PWM IC, the external inductors, and the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP2002 Internal Block Diagram



* All of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR Block. There are no concerns about double pulsing, unwanted shutdown, or other malfunctions which often occur in switching power supplies. The iPOWIR Block will function normally without any additional input power supply bypass capacitors. However, for reliable long term operation it is recommended that at least four 10uF ceramic input decoupling capacitors are provided to the V_{IN} pin of each power block. No additional bypassing is required on the V_{DD} pin.

Absolute Maximum Ratings :

Parameter	Min	Typ	Max	Units	Conditions
V_{IN} to PGND	-	-	16	V	
V_{DD} to SGND	-	-	6.0	V	
PWM to SGND	-0.3	-	V_{DD}+0.3	V	not to exceed 6.0V
Enable to SGND	-0.3	-	V_{DD}+0.3	V	not to exceed 6.0V
Output RMS Current	-	-	30	A	
Block Temperature	-40	-	125	°C	

Recommended Operating Conditions :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.6	5.0	5.5	V	
Input Voltage Range	V_{IN}	3.0	-	13.2	V	see Figs. 2 & 3
Output Voltage Range	V_{OUT}	0.9	-	3.3	V	see Figs. 2, 4 & 8
Output Current Range	I_{OUT}	-	-	30	A	see Fig. 2
Operating Frequency	fsw	150	-	1000	kHz	see Figs. 2 & 5
Operating Duty Cycle	D	-	-	85	%	

Electrical Specifications @ V_{DD} = 5V (unless otherwise specified) :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Block Power Loss ①	P_{BLK}	-	7.2	8.9	W	V_{IN} = 12V, V_{OUT} = 1.3V,
Turn On Delay ②	$t_{d(on)}$	-	63	-	ns	I_{OUT} = 30A, f_{SW} = 1MHz
Turn Off Delay ②	$t_{d(off)}$	-	26	-		
V_{IN} Quiescent Current	I_{Q-VIN}	-	-	1.0	mA	Enable = 0V, V_{IN} = 12V
V_{DD} Quiescent Current	I_{Q-VDD}	-	-	10	µA	Enable = 0V, V_{DD} = 5V
Under-Voltage Lockout	UVLO					
Start Threshold	V_{START}	4.2	4.4	4.5	V	
Hysteresis	$V_{Hys-UVLO}$	-	.05	-		
Enable	Enable					
Input Voltage High	V_{IH}	2.0	-	-	V	
Input Voltage Low	V_{IL}	-	-	0.8		
Power Ready	PRDY					
Logic Level High	V_{OH}	4.5	4.6	-	V	V_{DD} = 4.6V, I_{Load} = 10mA
Logic Level Low	V_{OL}	-	0.1	0.2		V_{DD} < UVLO Threshold, I_{Load} = 1mA
PWM Input	PWM					
Logic Level High	V_{OH}	2.0	-	-	V	
Logic Level Low	V_{OL}	-	-	0.8		

① Measurement were made using four 10uF (TDK C3225X7R1C106M or equiv.) capacitors across the input (see Fig. 8).

② Not associated with the rise and fall times. Does not affect Power Loss (see Fig. 9).

Pin Description Table

Pin Name	Ball Designator	Pin Function
V_{DD}	A1 – A3, B1 – B3	Supply voltage for the internal circuitry.
V_{IN}	A5 – A12, B5 – B12, C5 - C10	Input voltage for the DC-DC converter.
PGND	C11, C12, D11, D12, E11, E12, F6, F7, F12, G6, G7, G12, H6, H7, H12, J6, J7, J12, K5 – K7, K12, L5, L6, L12, M5 – M7, M12	Power Ground - connection to the ground of bulk and filter capacitors.
V_{SW}	D5 – D10, E5 – E10, F8 – F11, G8 – G11, H8 – H11, J8 – J11, K8 – K11, L8 – L11, M8 – M11	Switching Node - connection to the output inductor.
SGND	C1 – C3, D1 –D3, E1 –E3	Signal Ground.
ENABLE	F1	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the PRDY pin is forced low, the Control and Sychronous switches are turned off, and the supply current is less than 10µA.
PRDY	K1	Power Ready - This pin indicates the status of ENABLE or V_{DD}. This output will be driven low when ENABLE is logic low or when V_{DD} is less than 4.4V (typ.). When ENABLE is logic high and V_{DD} is greater than 4.4V (typ.), this output is driven high. This output has a 10mA source and 1mA sink capability.
PWM	H1	TTL-level input signal to MOSFET drivers.
NC	B4, C4, D4, E4, F2 – F4, G2 – G4, H2 – H4, J1, J2 – J4, K3, L1, L2, M1 – M4	This pin is not for electrical connection. It should be attached only to dead copper.

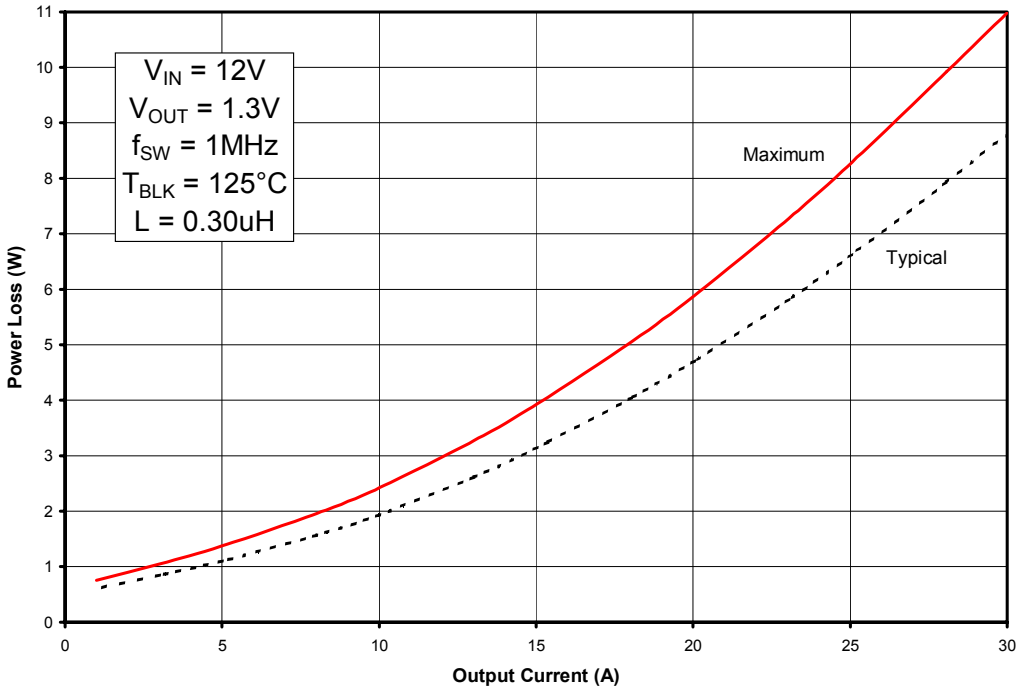


Fig. 1: Power Loss vs. Current

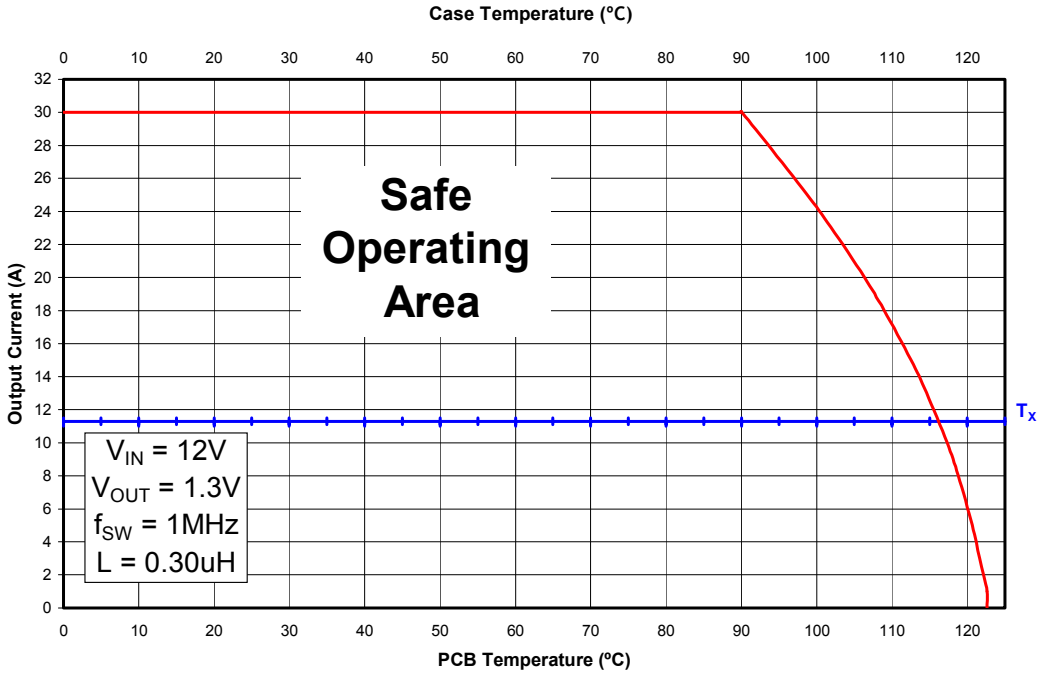


Fig. 2: Safe Operating Area (SOA) vs. T_{PCB} & T_{CASE}

Typical Performance Curves

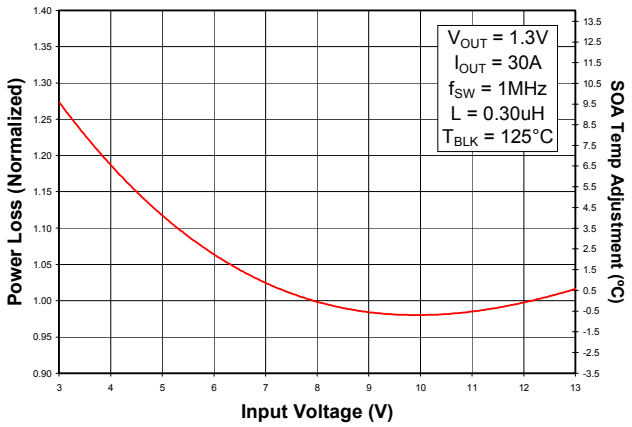


Fig. 3: Normalized Power Loss vs. V_{IN}

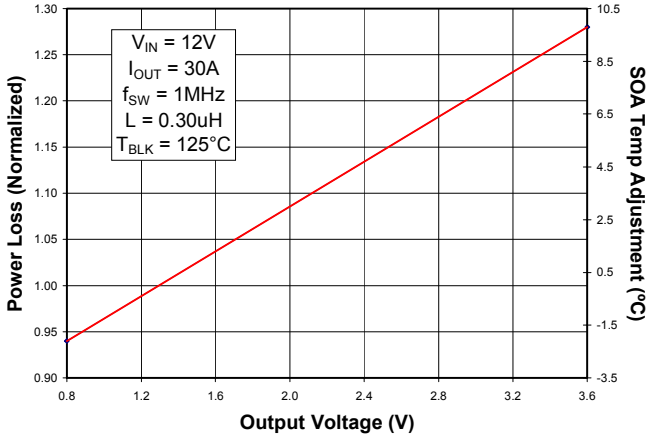


Fig. 4: Normalized Power Loss vs. V_{OUT}

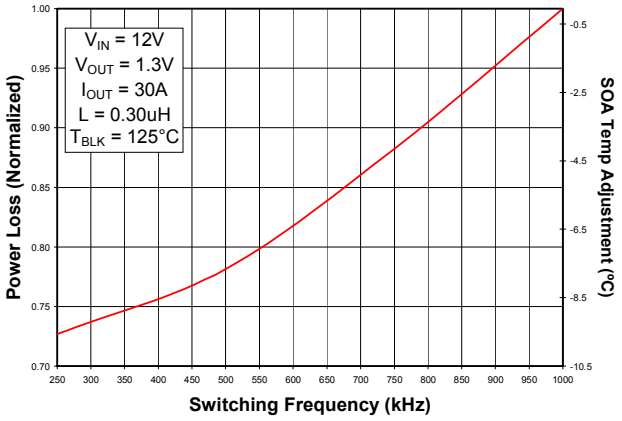


Fig. 5: Normalized Power Loss vs. Frequency

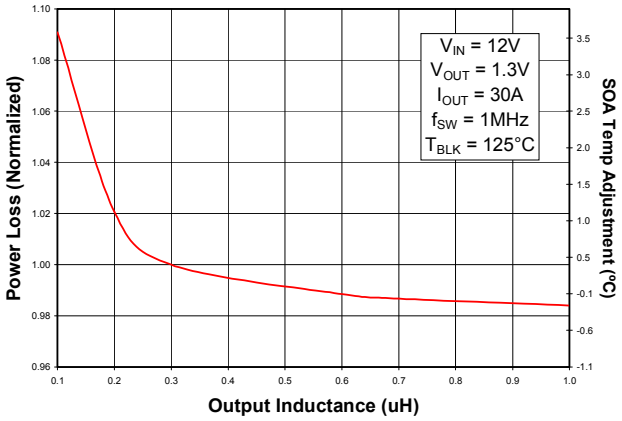


Fig. 6: Normalized Power Loss vs. Inductance

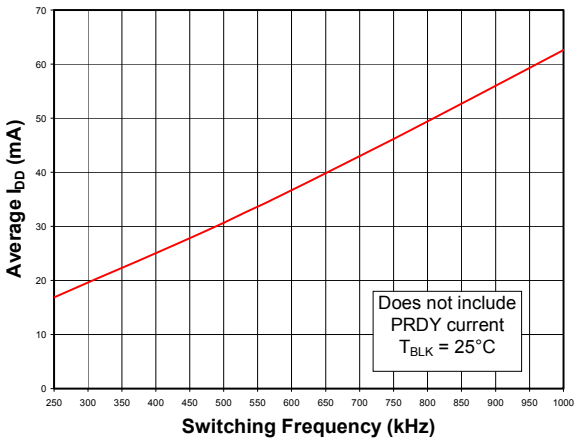


Fig. 7: I_{DD} vs. Frequency

Applying the Safe Operating Area (SOA) Curve

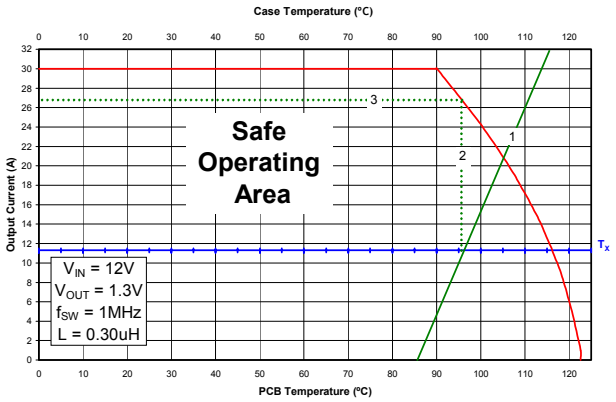
The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case.

Procedure

1) Draw a line from Case Temp axis at T_{CASE} to the PCB Temp axis at T_{PCB}.

2) Draw a vertical line from the T_X axis intercept to the SOA curve.

3) Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y axis. The point at which the horizontal line meets the y-axis is the SOA current.



Adjusting the Power Loss and SOA curves for different operating conditions

To make adjustments to the power loss curves in Fig. 1, multiply the normalized value obtained from the curves in Figs. 3, 4, 5 or 6 by the value indicated on the power loss curve in Fig. 1. If multiple adjustments are required, multiply all of the normalized values together, then multiply that product by the value indicated on the power loss curve in Fig. 1. The resulting product is the final power loss based on all factors. See example no. 1.

To make adjustments to the SOA curve in Fig. 2, determine your maximum PCB Temp & Case Temp at the maximum operating current of each iP2002. Then, add the correction temperature from the normalized curves in Figs. 3, 4, 5 or 6 to the T_X axis intercept (see procedure no. 2 above) in Fig. 2. When multiple adjustments are required, add all of the temperatures together, then add the sum to the T_X axis intercept in Fig. 2. See example no. 2.

Operating Conditions for the following examples:

Output Current = 30A	Input Voltage = 10V	Inductor = 0.2uH
Output Voltage = 3.3V	Sw Freq= 900kHz	

Example 1) Adjusting for Maximum Power Loss:

(Fig. 1) Maximum power loss = 11W
(Fig. 3) Normalized power loss for input voltage ≈ 0.98
(Fig. 4) Normalized power loss for output voltage ≈ 1.24
(Fig. 5) Normalized power loss for frequency ≈ 0.95
(Fig. 6) Normalized power loss for inductor value ≈ 1.02

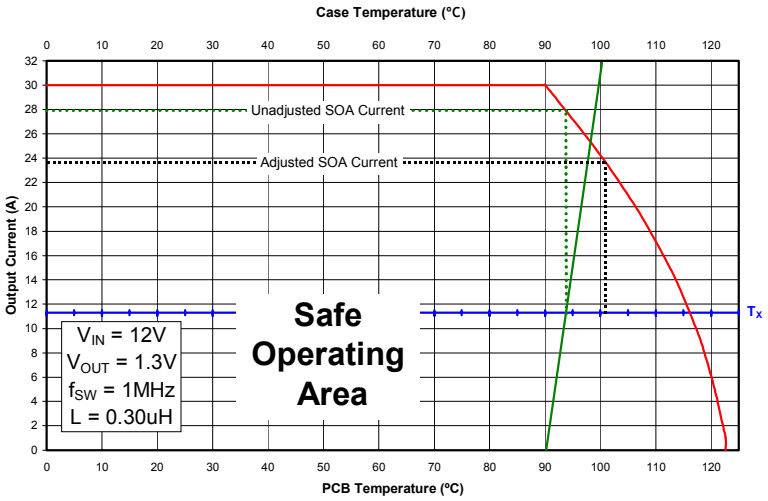
Adjusted Power Loss = 11W x 0.98 x 1.24 x 0.95 x 1.02 ≈ 12.95W

Example 2) Adjusting for SOA Temperature:

(Fig. 3) Normalized SOA Temperature for input voltage ≈ -0.6°C
(Fig. 4) Normalized SOA Temperature for output voltage ≈ 8.4°C
(Fig. 5) Normalized SOA Temperature for frequency ≈ -1.8°C
(Fig. 6) Normalized SOA Temperature for inductor value ≈ 1.1°C

T_X axis intercept temp adjustment = - 0.6°C + 8.4°C - 1.8°C + 1.1°C ≈ 7.1°C

Assuming T_{CASE} = 100°C & T_{PCB} = 90°C:
The following example shows how the SOA current is adjusted for a T_X increase of 7.1°C.



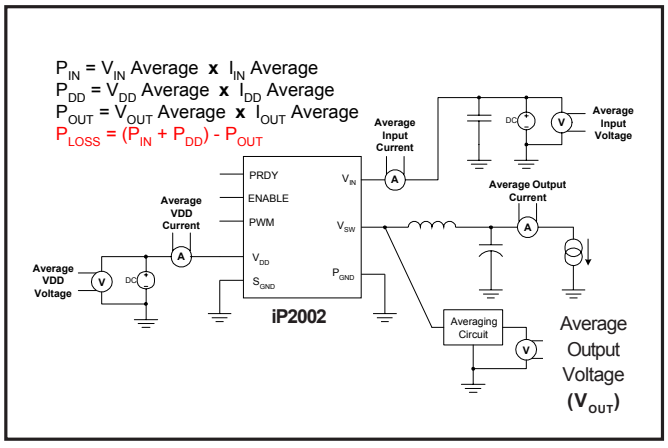


Fig 8. Power Loss Test Circuit

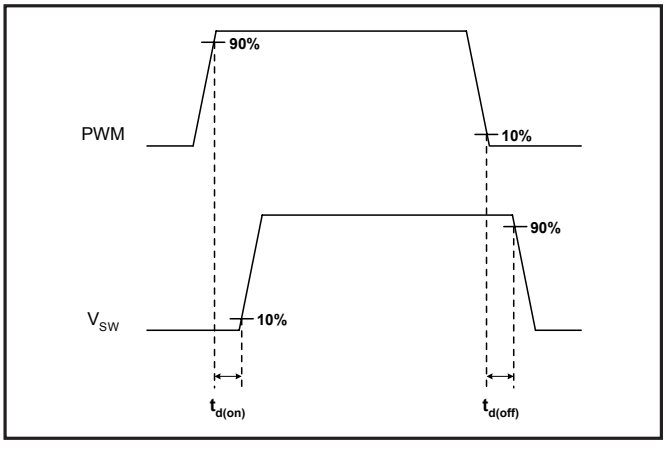
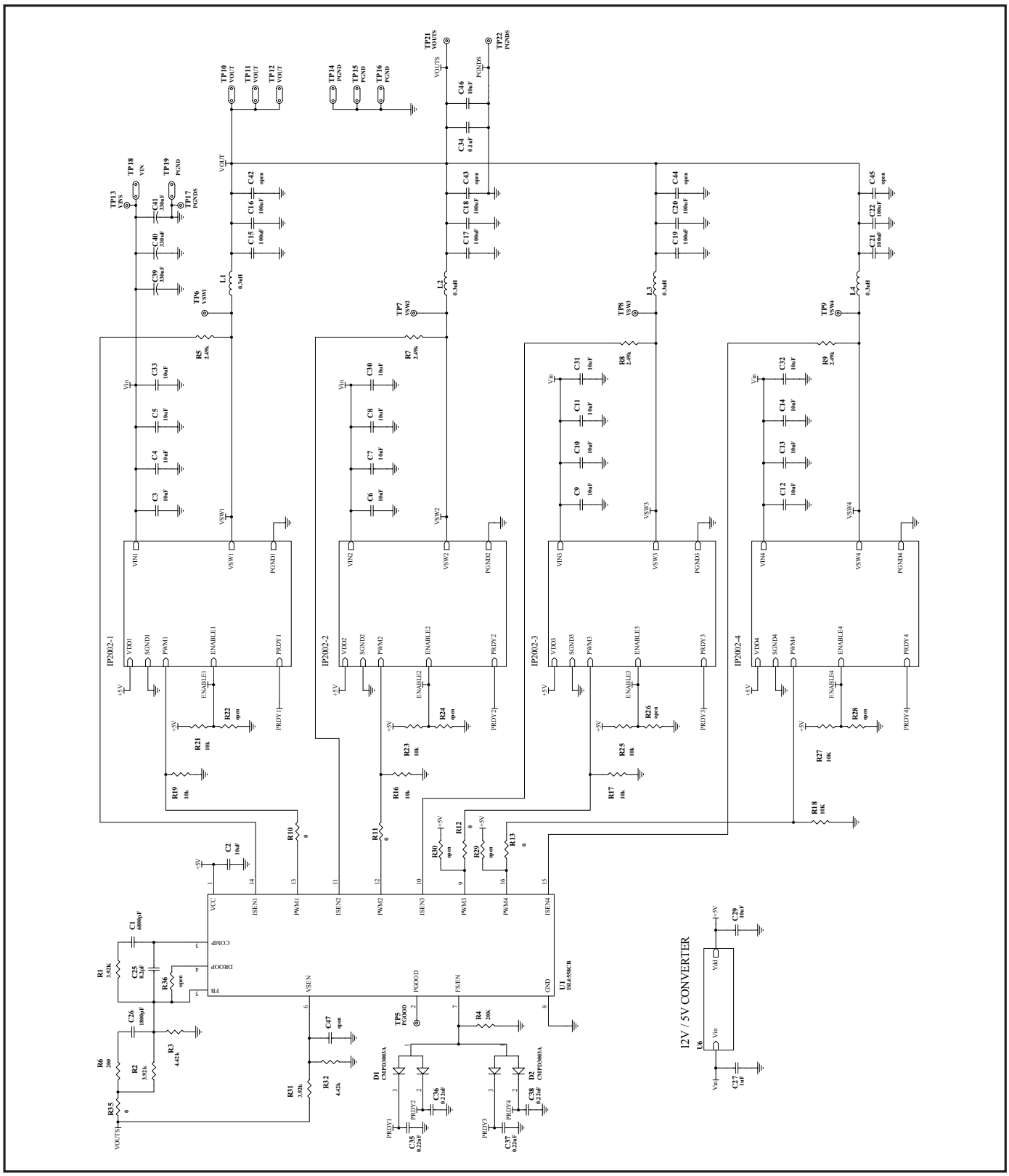


Fig 9. Timing Diagram



4-Phase Reference Design Schematic

Quantity	Designator	Value 1	Value 2	Type 2	Tolerance	Package	Mfr.	Mfr. Part No.
1	C1	6800pF	50V	X7R	10%	0805	PHICOMP	08052R682K9BB0
17	C10 C11 C12 C13 C14 C3 C30 C31 C32 C33 C4 C46 C5 C6 C7 C8 C9	10.0uF	16V	X5R	10%	1206	Murata	GRM31CR61C106KC31B
8	C15 C16 C17 C18 C19 C20 C21 C22	100uF	6.3V	X5R	20%	1210	TDK	C3225X5R0J107M
2	C2 C29	10.0uF	6.3V	X5R	10%	1206	TDK	C3216X5R0J106K
1	C25	8.20pF	50V	NPO	3%	0805	PHICOMP	0805CG829C9BB0
1	C26	1800pF	50V	X7R	10%	0805	PHICOMP	08052R182K9BB0
1	C27	1.00uF	16V	X7R	10%	0805	MuRata	GRM40X7R105K016
1	C28	0.010uF	50V	X7R	10%	0805	TDK	C2012X7R1H103KT
1	C34	0.100uF	50V	X7R	10%	0805	ROHM	MCH215C104KP
4	C35 C36 C37 C38	0.22uF	6.3V	X5R	10%	0603	TDK	C1608X5R0J224K
3	C39 C40 C41	330uF	16V	WA series	20%	SMD	Panasonic	EEF-WA1C331P
5	C42 C43 C44 C45 C47	Open	-	-	-	-	-	-
3	R1 R2 R31	3.92K	1/8W	thin film	0.10%	0805	BC Component	2312-241-73922
5	R10 R11 R12 R13 R35	0	1/8W	thick film	<50m	0805	ROHM	MCR10EZHJ000
9	R16 R17 R18 R19 R21 R23 R25 R27 R34	10.0K	1/8W	thick film	1%	0805	KOA	RK73H2A1002F
2	R3 R32	4.42K	1/8W	thin film	0.10%	0805	BC Component	2312-241-74422
1	R33	30.1K	1/8W	thick film	1%	0805	KOA	RK73H2A3012F
1	R4	20.0K	1/8W	thick film	1%	0805	KOA	RK73H2A2002F
4	R5 R7 R8 R9	2.49K	1/8W	thick film	1%	0805	KOA	RK73H2A2491F
1	R6	200	1/8W	thick film	1%	0805	KOA	RK73H2A2000F
7	R22 R24 R26 R28 R29 R30 R36	Open	-	-	-	-	-	-
2	D1 D2	30V	200mA	schottky	-	sot23	Central	CMPD3003A
1	D5	40V	2.1A	schottky	-	D-64	IRF	10MQ040N
1	D6	30V	100mA	schottky	-	sot23	Central	CMPSH-3
4	L1 L2 L3 L4	0.3uH	36A	ferrite	20%	SMT	Panasonic	ETQP2H0R3BFA
1	L5	15uH	0.70A	ferrite	20%	SMT	Coilcraft	1008PS-153M
1	U1	4.5 - 5.5V	0.8 - 5V	PWM controller	0 - 70°C	16 Ld SOIC	Intersil	ISL6558CB
4	U2 U3 U4 U5	30A	-	Power Block	-	11mm x 11mm	International Rect	iP2002
1	U6	4.7 - 25V	1.8 - 5V	PWM controller	-40 to +85°C	S6	Linear Technology	LT1616

4-Phase Reference Design Bill of Materials

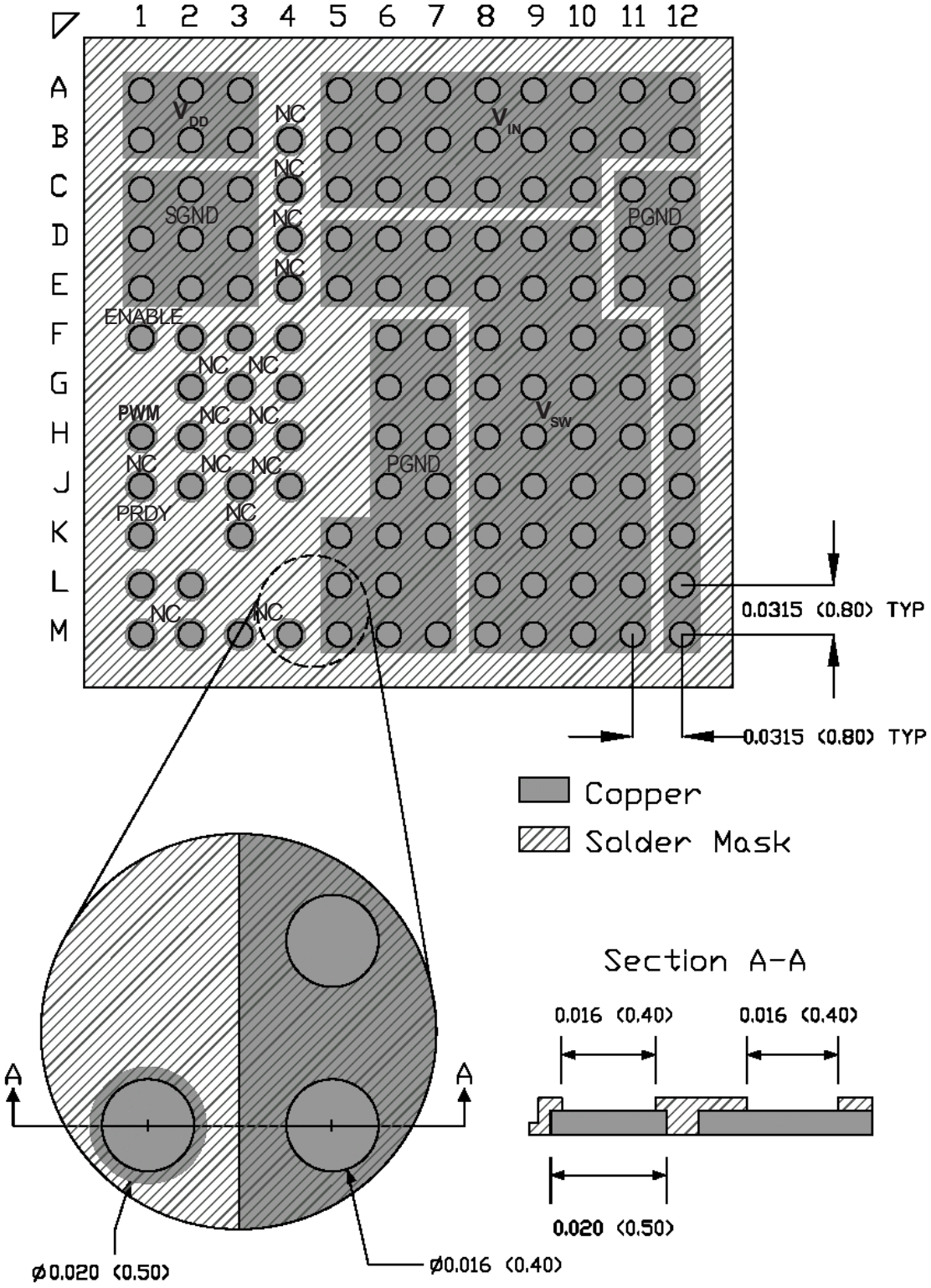
Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

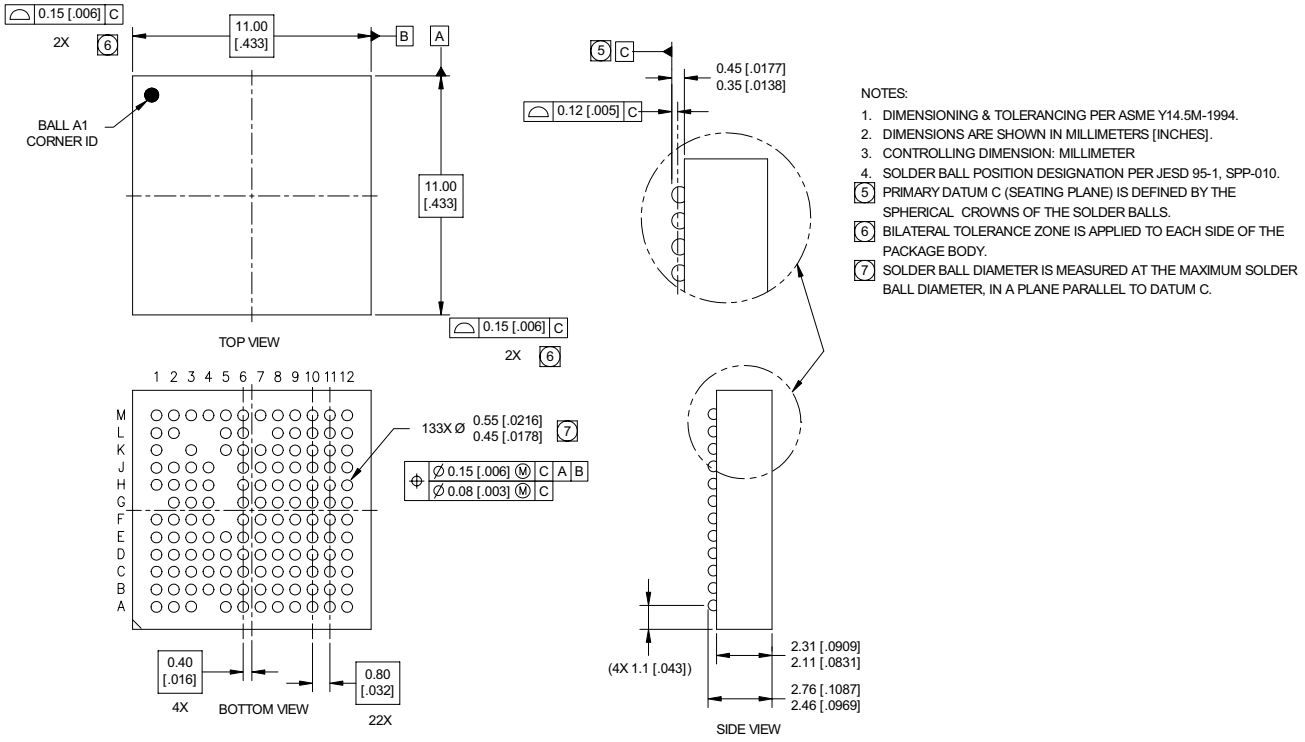
AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1047: Graphical solution for two branch heatsinking Safe Operating Area
Detailed explanation of the dual axis SOA graph and how it is derived.

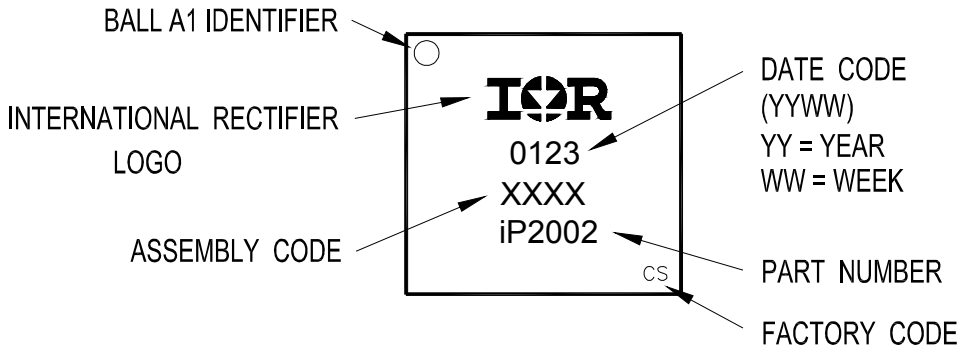


Dimensions shown in inches (millimeters)

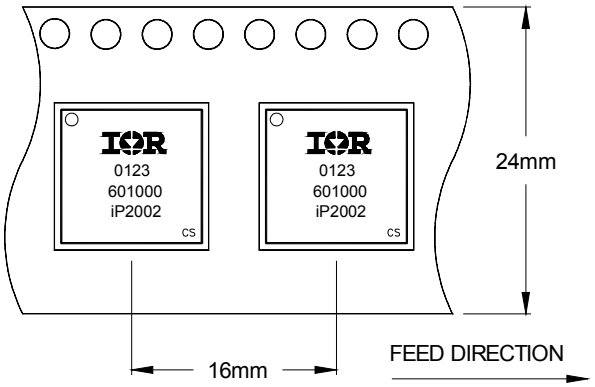
Recommended PCB Footprint (Top View)



Mechanical Drawing

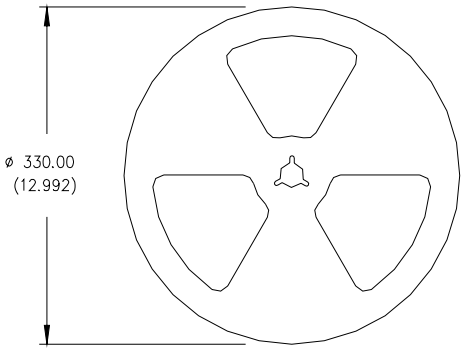


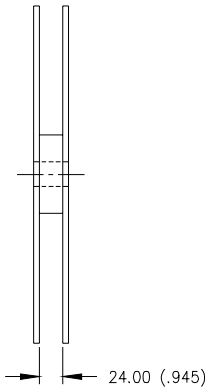
Part Marking



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.





NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Tape & Reel Information

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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