MAX14802/MAX14803/ MAX14803A

Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

General Description

The MAX14802/MAX14803/MAX14803A provide high-voltage switching on 16 channels for ultrasonic imaging and printer applications. The devices utilize HVCMOS process technology to provide 16 high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 16-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The MAX14802/MAX14803/MAX14803A operate with a wide range of high-voltage supplies including V_{PP}/V_{NN} = +100V/-100V, +200V/0V, or +40V/-160V. The digital interface operates from a separate +2.7V to +5.5V V_{DD} supply. Digital inputs DIN, CLK, $\overline{LE}$, and CLR operate on the V_{DD} supply voltage.

The MAX14803/MAX14803A provide integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads. The MAX14802/MAX14803/MAX14803A provide integrated clamping diodes for overvoltage protection against positive overshoot.

The MAX14802 is available in a 48-pin LQFP package and is specified for commercial 0°C to +70°C and extended -40°C to +85°C temperature ranges.

The MAX14803 is available in a 48-pin LQFP package and is specified for the commercial 0°C to +70°C temperature range.

The MAX14803A is available in the 110-bump wafer level package (WLP) and is specified at the -40°C to +85°C temperature range.

Applications

- Ultrasound Imaging
- Printers

Features

- Integrated Overvoltage Protection
- 20MHz Serial Interface (5V)
- HVCMOS Technology for High Performance
- Individually Programmable High-Voltage Analog Switches
- Very Low 5µA (typ) Quiescent Current
- DC-to-20MHz Low-Voltage Analog Signal Frequency Range
- 2.7V to 5.5V Logic Supply Voltage
- Low-Charge Injection, Low-Capacitance R_L Switches
- -77dB (typ) Off-Isolation at 5MHz (R_L = 50Ω)
- Daisy-Chainable Serial Interface
- Flexible High-Voltage Supplies (V_{PP} - V_{NN} = 250V)

***Ordering Information/Selector Guide* appear at end of data sheet.**

19-4484; Rev 5; 2/21

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{DD} Logic-Supply Voltage.....-0.3V to +7V
V_{PP} - V_{NN} Supply Voltage
(MAX14802CCM+, MAX14803CCM+).....260V
(MAX14802ECM+, MAX14803AEWZ+).....230V
V_{PP} Positive-Supply Voltage.....-0.3V to +220V
V_{NN} Negative-Supply Voltage.....-0.3V to -220V
Logic Inputs ($\overline{LE}$, CLR, CLK, DIN, DOUT).....-0.3V to +7V
COM_, NO_..... (-0.3V + V_{NN}) to the minimum of [(V_{NN} + 220V) or (V_{PP} + 0.3V)]
Peak Analog Signal Current Per Channel.....3A
Continuous Power Dissipation (T_A = +70°C)
48-Pin LQFP (derate 22.7mW/°C above +70°C) 1818mW
110-Bump WLP (derate 37mW°C above +70°C).....2960mW
Operating Temperature Range (Commercial).....0°C to +70°C
Operating Temperature Range (Extended)..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 48 LQFP	
Package Code	C48+6
Outline Number	**21-0054**
Land Pattern Number	**90-0093**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	44°C/W
Junction to Case (θ_{JC})	10°C/W

PACKAGE TYPE: 110 WLP	
Package Code	W1105B5+1
Outline Number	**21-0494**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +2.7V to +5.5V, V_{PP} = +40V to V_{NN} + 250V, V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
V_{DD} Supply Voltage	V_{DD}			+2.7		+5.5	V
V_{PP} Supply Voltage	V_{PP}	MAX14802ECM+, MAX14803AEWZ+		+40	+100	V_{NN} + 200	V
		MAX14802CCM+, MAX14803CCM+		+40	+100	V_{NN} + 250	
V_{NN} Supply Voltage	V_{NN}			-160	-100	0	V
V_{DD} Supply Quiescent Current	I_{DDQ}					5	µA
V_{DD} Supply Dynamic Current	I_{DD}	V_{DD} = +5V, $V_{\overline{LE}}$ = +5V, f_{CLK} = 5MHz				0.5	mA
V_{PP} Supply Quiescent Current	I_{PPQ}	All switches remain on or off, $I_{COM\_}$ = 5mA			0	10	µA
V_{PP} Supply Dynamic Current (All Channel Switching Simultaneously)	I_{PP}	V_{PP} = +40V, V_{NN} = -160V, $f_{COM\_}$ = 50kHz				4	mA
		V_{PP} = +100V, V_{NN} = -100V, $f_{COM\_}$ = 50kHz			3.4	6	
		V_{PP} = +160V, V_{NN} = -40V, $f_{COM\_}$ = 50kHz				8	
V_{NN} Supply Quiescent Current	I_{NNQ}	All switches remain on or off, $I_{COM\_}$ = 5mA			0	10	µA
V_{NN} Supply Dynamic Current (All Channel Switching Simultaneously)	I_{NN}	V_{PP} = +40V, V_{NN} = -160V, $f_{COM\_}$ = 50kHz				5	mA
		V_{PP} = +100V, V_{NN} = -100V, $f_{COM\_}$ = 50kHz			2.3	4	
		V_{PP} = +160V, V_{NN} = -40V, $f_{COM\_}$ = 50kHz				3	
ANALOG SWITCH							
COM_, NO_ Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$	(Note 2)		V_{NN}		min of (V_{NN} + 200V) or (V_{PP} - 10V)	V
Small-Signal Switch On-Resistance	R_{ONS}	V_{PP} = +40V, V_{NN} = -160V, $V_{COM\_}$ = 0V	$I_{COM\_}$ = 5mA		26	48	Ω
			$I_{COM\_}$ = 200mA		22	32	
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0V	$I_{COM\_}$ = 5mA		22	30	
			$I_{COM\_}$ = 200mA		18	27	
		V_{PP} = +160V, V_{NN} = -40V, $V_{COM\_}$ = 0V	$I_{COM\_}$ = 5mA		20	30	
			$I_{COM\_}$ = 200mA		16	27	
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0V, $I_{COM\_}$ = 5mA			5		%
Large-Signal Switch On-Resistance	R_{ONL}	$V_{COM\_}$ = V_{PP} - 10V, $I_{COM\_}$ = 1A			15		Ω
Shunt Resistance	R_{INT}	NO_ or COM_ to GND (MAX14803/MAX14803A), switch off		30	40	50	KΩ

Electrical Characteristics (continued)

(V_{DD} = +2.7V to +5.5V, V_{PP} = +40V to V_{NN} + 250V, V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch-Off Leakage	$I_{COM\_(OFF)}$, $I_{NO\_(OFF)}$	$V_{COM\_}$, $V_{NO\_}$ = +100V or unconnected		0	2	µA
Switch-Off DC Offset		R_L = 100kΩ	-30		+30	mV
Switch-Output Peak Current		100ns pulse width, 0.1% duty cycle (Note 3)		3		A
Switch-Output COM_ Isolation Diode Current		300ns pulse width, 2% duty cycle (Note 3)		500		mA
SWITCH DYNAMIC CHARACTERISTICS						
Turn-On Time	t_{ON}	$V_{NO\_}$ = +100V, R_L = 10kΩ, V_{NN} = -100V		2	3.5	µs
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = +100V, R_L = 10kΩ, V_{NN} = -100V		2	3.5	µs
Output Switching Frequency	f_{SW}	Duty cycle = 50%			50	kHz
Maximum $V_{COM\_}$, $V_{NO\_}$ Slew Rate	dV/dt	(Note 3)	20			V/ns
Off-Isolation	V_{ISO}	f = 5MHz, R_L = 1kΩ, C_L = 15pF		-50		dB
		f = 5MHz, R_L = 50Ω		-77		
Crosstalk	V_{CT}	f = 5MHz, R_L = 50Ω		-80		dB
COM_, NO_ Off-Capacitance	$C_{COM\_(OFF)}$, $C_{NO\_(OFF)}$	$V_{COM\_}$ = 0V, $V_{NO\_}$ = 0V, f = 1MHz (Note 3)	4	11	18	pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	$V_{COM\_}$ = 0V, f = 1MHz (Note 3)	20	36	56	pF
Output-Voltage Spike	V_{SPK}	R_L = 50Ω (Note 3)	-150		+150	mV
Small-Signal Analog Bandwidth	f_{BW}	V_{PP} = +100V, V_{NN} = -100V, C_L = 200pF		20		MHz
Charge Injection	Q	V_{PP} = +40V, V_{NN} = -160V, $V_{COM\_}$ = 0V		820		pC
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0V		600		
		V_{PP} = +160V, V_{NN} = -40V, $V_{COM\_}$ = 0V		350		
LOGIC LEVELS						
Logic-Input Low Voltage	V_{IL}				0.75	V
Logic-Input High Voltage	V_{IH}		V_{DD} - 0.75			V
Logic-Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 0.75mA	V_{DD} - 0.5			V
Logic-Input Capacitance	C_{IN}	(Note 3)			10	pF
Logic-Input Leakage	I_{IN}		-1		+1	µA

Timing Characteristics

(V_{DD} = +2.7V to +5.5V, V_{PP} = +40V to V_{NN} + 200V, V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

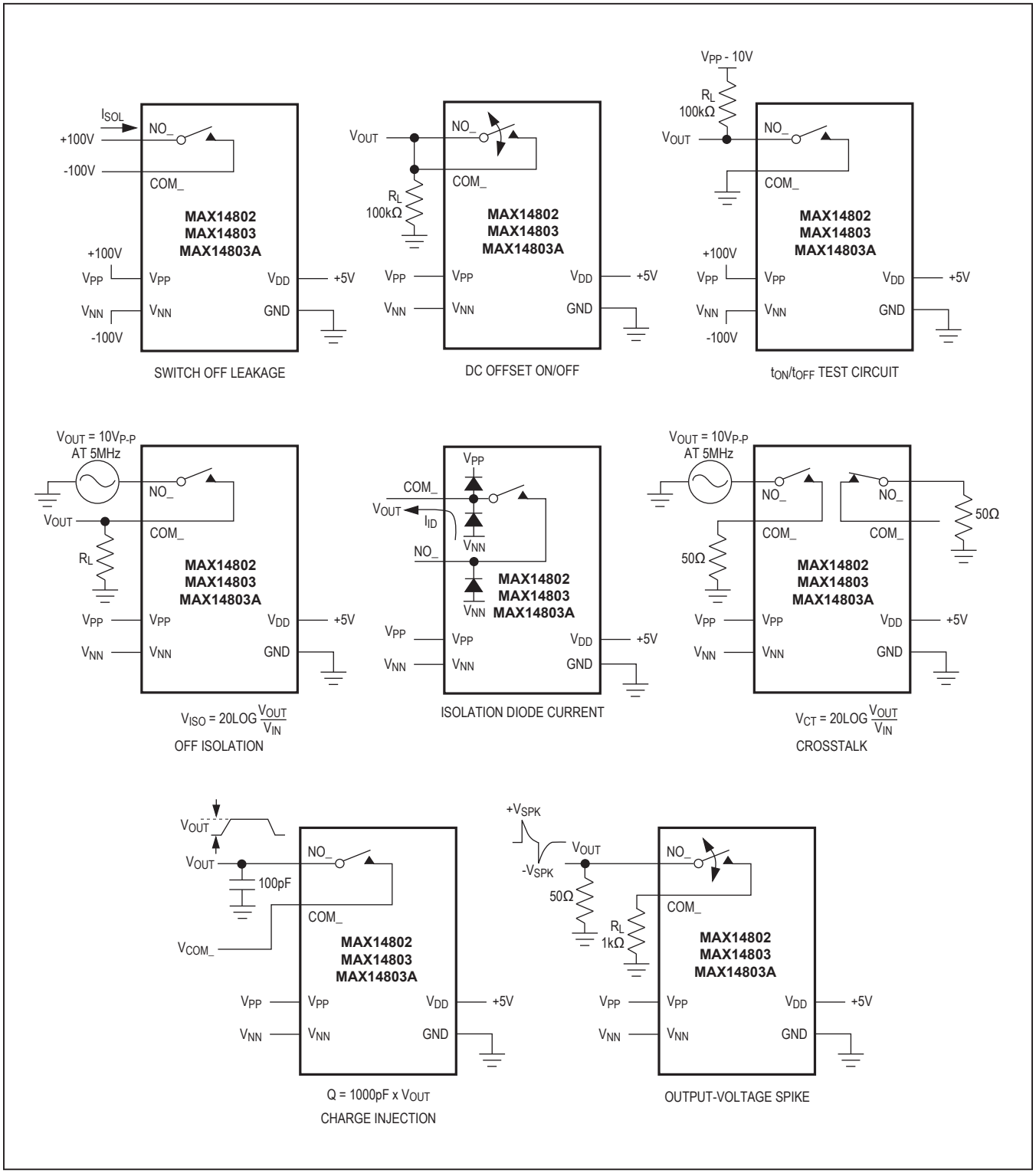
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC TIMING (Figure 1)						
CLK Frequency	f_{CLK}	V_{DD} = +5V ±10%			20	MHz
		V_{DD} = +3V ±10%			10	
DIN to CLK Setup Time	t_{DS}	V_{DD} = +5V ±10%	10			ns
		V_{DD} = +3V ±10%	16			
DIN to CLK Hold Time	t_{DH}	V_{DD} = +5V ±10%	3			ns
		V_{DD} = +3V ±10%	3			
CLK to $\overline{LE}$ Setup Time	t_{CS}	V_{DD} = +5V ±10%	36			ns
		V_{DD} = +3V ±10%	65			
$\overline{LE}$ Low-Pulse Width	t_{WL}	V_{DD} = +5V ±10%	14			ns
		V_{DD} = +3V ±10%	22			
CLR High-Pulse Width	t_{WC}	V_{DD} = +5V ±10%	20			ns
		V_{DD} = +3V ±10%	40			
CLK Rise and Fall Times	t_R, t_F	V_{DD} = +5V ±10%			50	ns
		V_{DD} = +3V ±10%			50	
CLK to DOUT Delay	t_{DO}	V_{DD} = +5V ±10%	6		42	ns
		V_{DD} = +3V ±10%	12		80	

Note 1: All devices are 100% tested at T_A = +70°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 2: The analog signal input $V_{COM\_}$ and $V_{NO\_}$ must satisfy $V_{NN} \le (V_{COM\_}, V_{NO\_}) \le V_{PP}$, or remain unconnected during power-up and power-down.

Note 3: Guaranteed by characterization; not production tested.

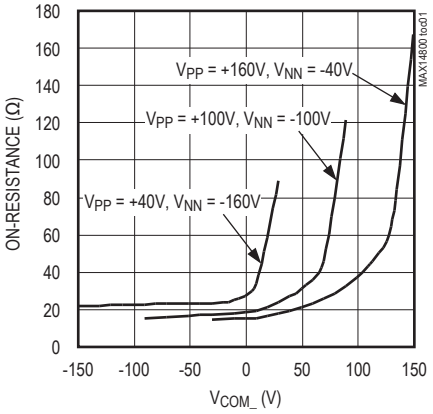
Test Circuits



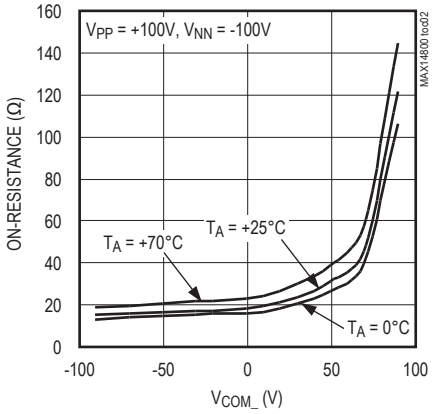
Typical Operating Characteristics

(V_{DD} = +3V, V_{PP} = +100V, V_{NN} = -100V, T_A = +25°C, unless otherwise noted.)

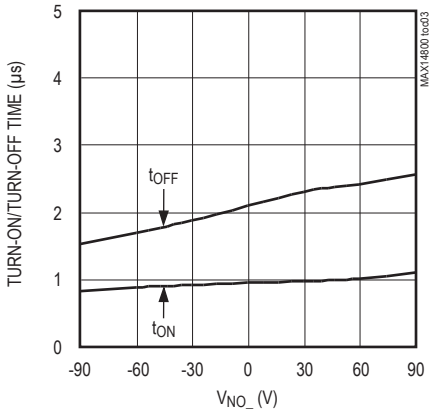
ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



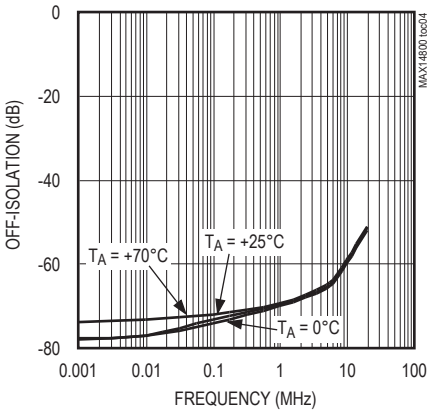
ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



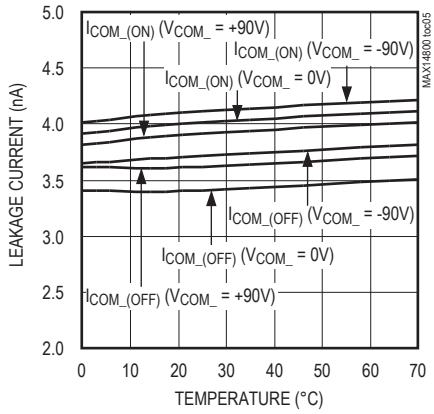
TURN-ON/TURN-OFF TIME vs. ANALOG SIGNAL VOLTAGE



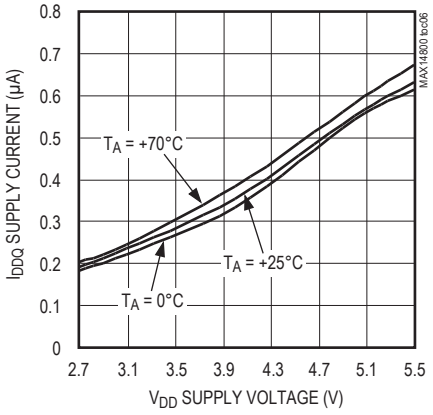
OFF-ISOLATION vs. FREQUENCY



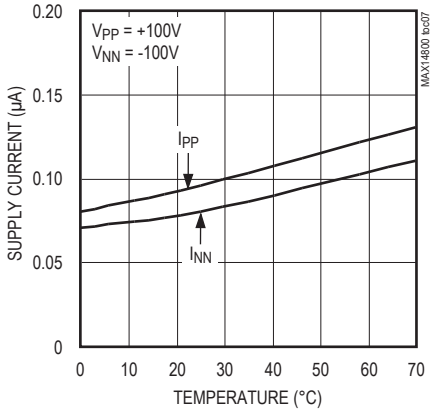
LEAKAGE CURRENT vs. TEMPERATURE



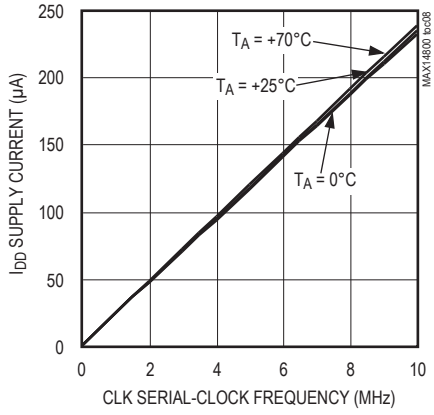
LOGIC SUPPLY CURRENT vs. SUPPLY VOLTAGE



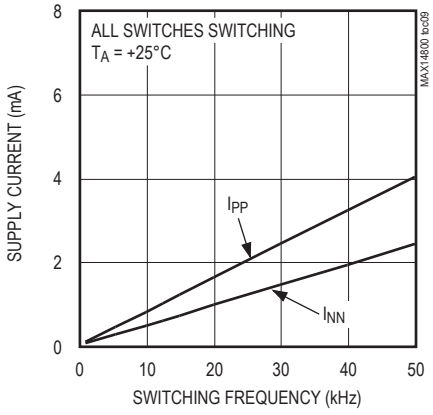
HIGH-VOLTAGE SUPPLY CURRENT vs. TEMPERATURE



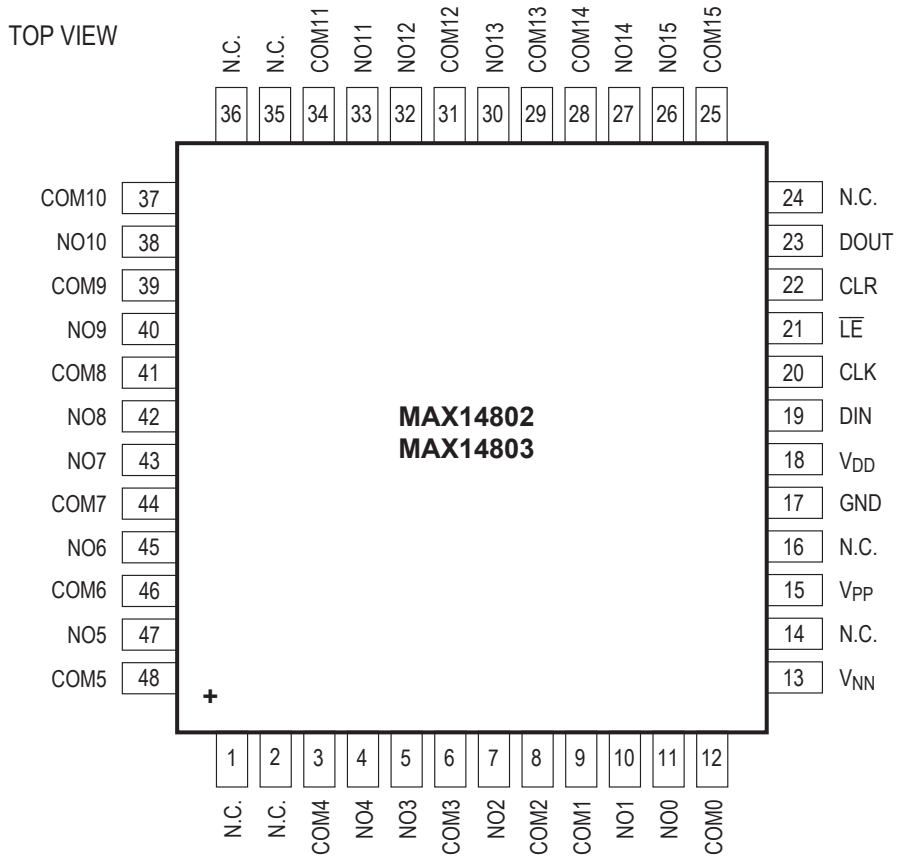
LOGIC SUPPLY CURRENT vs. SERIAL-CLOCK FREQUENCY



HIGH-VOLTAGE SUPPLY CURRENT vs. SWITCHING FREQUENCY



Pin Configurations

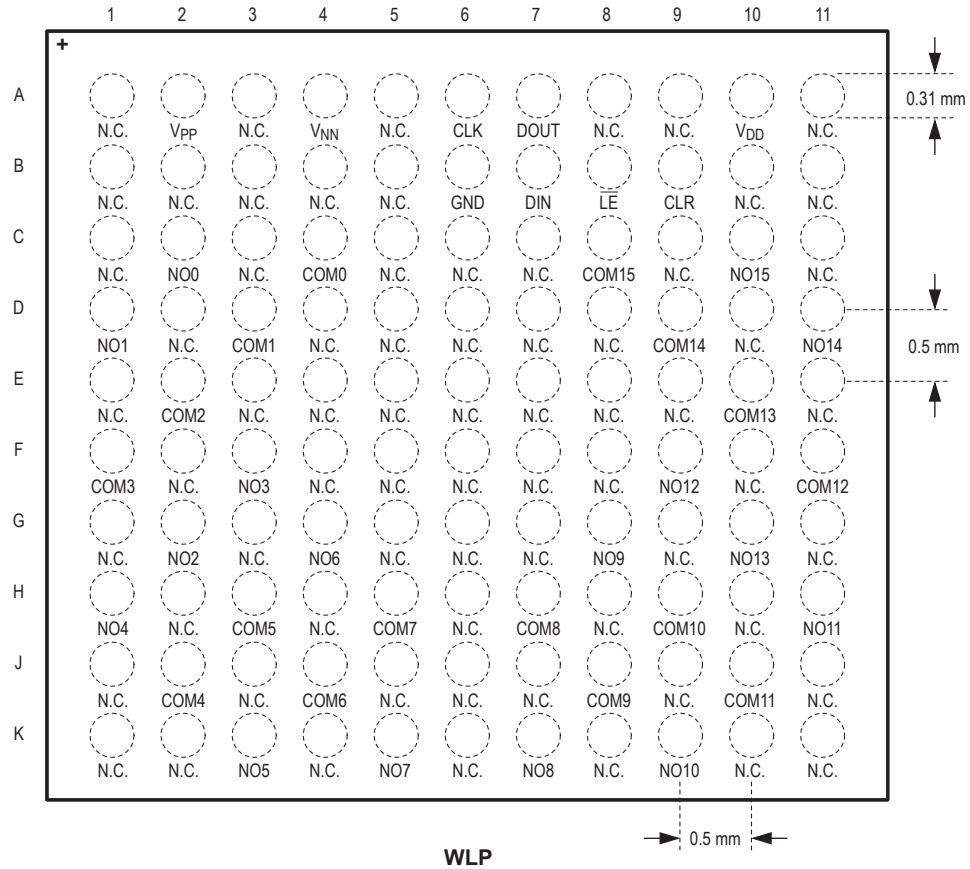


LQFP
(7mm x 7mm)

Pin Configurations (continued)

TOP VIEW
(BUMPS ON BOTTOM)

MAX14803A



WLP
(5.81mm x 5.43mm)

Pin Description

PIN		NAME	FUNCTION
LQFP	WLP		
1, 2, 14, 16, 24, 35, 36	A1, A3, A5, A8, A9, A11, B1–B5, B10, B11, C1, C3, C5, C6, C7, C9, C11, D2, D4–D8, D10, E1, E3–E9, E11, F2, F4–F8, F10, G1, G3, G5, G6, G7, G9, G11, H2, H4, H6, H8, H10, J1, J3, J5, J6, J7, J9, J11, K1, K2, K4, K6, K8, K10, K11	N.C.	No Connection. Not internally connected.
3	J2	COM4	Analog Switch 4—Common Terminal
4	H1	NO4	Analog Switch 4—Normally-Open Terminal
5	F3	NO3	Analog Switch 3—Normally-Open Terminal
6	F1	COM3	Analog Switch 3—Common Terminal
7	G2	NO2	Analog Switch 2—Normally-Open Terminal
8	E2	COM2	Analog Switch 2—Common Terminal
9	D3	COM1	Analog Switch 1—Common Terminal
10	D1	NO1	Analog Switch 1—Normally-Open Terminal
11	C2	NO0	Analog Switch 0—Normally-Open Terminal
12	C4	COM0	Analog Switch 0—Common Terminal
13	A4	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
15	A2	V_{PP}	Positive High-Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
17	B6	GND	Ground
18	A10	V_{DD}	Digital Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
19	B7	DIN	Serial-Data Input
20	A6	CLK	Serial-Clock Input
21	B8	$\overline{LE}$	Active-Low, Latch-Enable Input
22	B9	CLR	Latch Clear Input
23	A7	DOUT	Serial-Data Output
25	C8	COM15	Analog Switch 15—Common Terminal
26	C10	NO15	Analog Switch 15—Normally-Open Terminal
27	D11	NO14	Analog Switch 14—Normally-Open Terminal
28	D9	COM14	Analog Switch 14—Common Terminal
29	E10	COM13	Analog Switch 13—Common Terminal
30	G10	NO13	Analog Switch 13—Normally-Open Terminal
31	F11	COM12	Analog Switch 12—Common Terminal

Pin Description (continued)

PIN		NAME	FUNCTION
LQFP	WLP		
32	F9	NO12	Analog Switch 12—Normally-Open Terminal
33	H11	NO11	Analog Switch 11—Normally-Open Terminal
34	J10	COM11	Analog Switch 11—Common Terminal
37	H9	COM10	Analog Switch 10—Common Terminal
38	K9	NO10	Analog Switch 10—Normally-Open Terminal
39	J8	COM9	Analog Switch 9—Common Terminal
40	G8	NO9	Analog Switch 9—Normally-Open Terminal
41	H7	COM8	Analog Switch 8—Common Terminal
42	K7	NO8	Analog Switch 8—Normally-Open Terminal
43	K5	NO7	Analog Switch 7—Normally-Open Terminal
44	H5	COM7	Analog Switch 7—Common Terminal
45	G4	NO6	Analog Switch 6—Normally-Open Terminal
46	J4	COM6	Analog Switch 6—Common Terminal
47	K3	NO5	Analog Switch 5—Normally-Open Terminal
48	H3	COM5	Analog Switch 5—Common Terminal

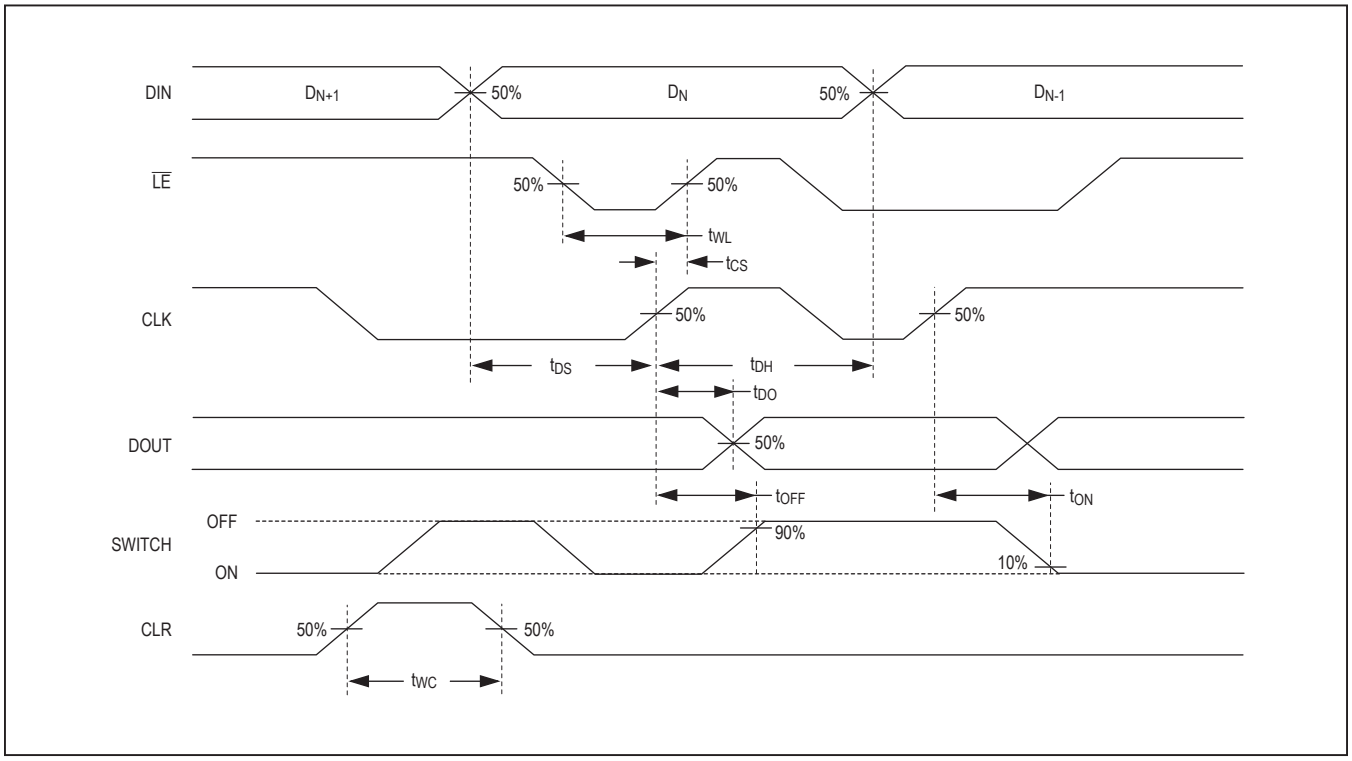
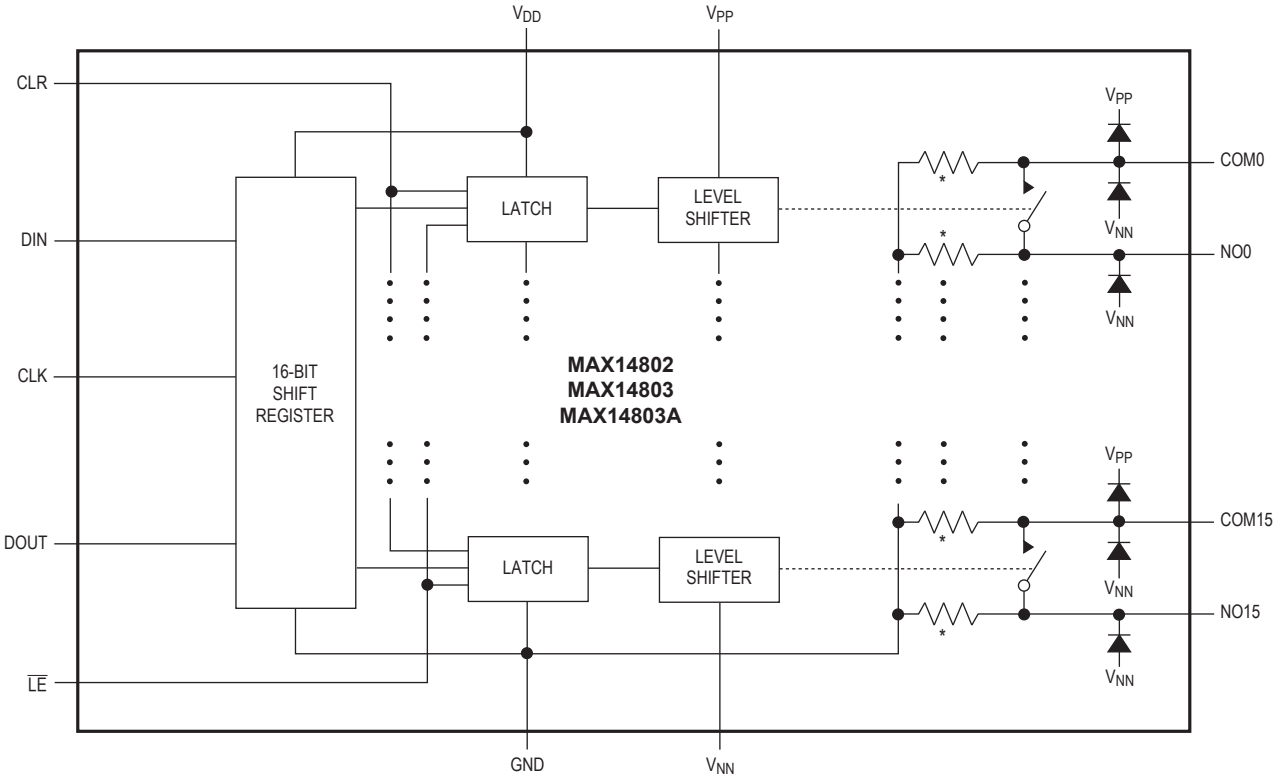


Figure 1. Serial Interface Timing

Functional Diagram



*BLEED RESISTORS AVAILABLE ON THE MAX14803/MAX14803A ONLY.

Detailed Description

The MAX14802/MAX14803/MAX14803A provide high-voltage switching on 16 channels for ultrasound imaging and printer applications. The devices utilize HVCMOS process technology to provide 16 high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 16-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on-reset function ensures that all switches are open on power-up.

The MAX14802/MAX14803/MAX14803A operate with a wide range of high-voltage supplies including: V_{PP}/V_{NN} = +100V/-100V, +200V/0V, or +40V/-160V. The digital interface operates from a separate +2.7V to +5.5V V_{DD} supply. Digital inputs DIN, CLK, $\overline{LE}$, and CLR operate on the V_{DD} supply voltage. The MAX14803/MAX14803A provide integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads. The MAX14802/MAX14803/MAX14803A feature clamping diodes (at the COM_). These clamping diodes provide overvoltage protection against positive overshoot.

Analog Switch

The MAX14802/MAX14803/MAX14803A allow a peak-to-peak analog signal range from V_{NN} to the minimum of either V_{NN} + 200V or (V_{PP} - 10V). Analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM\_}, V_{NO\_}) \le V_{PP}$ during power-up and power-down.

High-Voltage Supplies

The MAX14802/MAX14803/MAX14803A allow a wide range of high-voltage supplies. The devices operate with V_{NN} from -160V to 0 and V_{PP} from +40V to V_{NN} +250V. When V_{NN} is connected to GND (single-supply applications), the devices operate with V_{PP} up to +200V. The V_{PP} and V_{NN} high-voltage supplies are not required to be symmetrical, but the voltage difference (V_{PP} - V_{NN}) must not exceed 250V.

Bleed Resistors (MAX14803/MAX14803A)

The MAX14803/MAX14803A feature integrated 35kΩ bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to GND with a bleed resistor.

Overvoltage Protection

The MAX14802/MAX14803/MAX14803A feature clamping diodes (at the COM_). These clamping diodes provide overvoltage protection against positive overshoot.

Serial Interface

The MAX14802/MAX14803/MAX14803A are controlled by a serial interface with a 16-bit serial shift register and transparent latch. Each of the 16 data bits controls a single analog switch (Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 16 clock cycles (Figures 1 and 2).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 2). Drive $\overline{LE}$ logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

Latch Clear (CLR)

The MAX14802/MAX14803/MAX14803A feature a latch clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch.

Power-On Reset

The MAX14802/MAX14803/MAX14803A feature a power-on-reset circuit to ensure all switches are open at power-on. The internal 16-bit serial shift register and latch are set to zero on power-up.

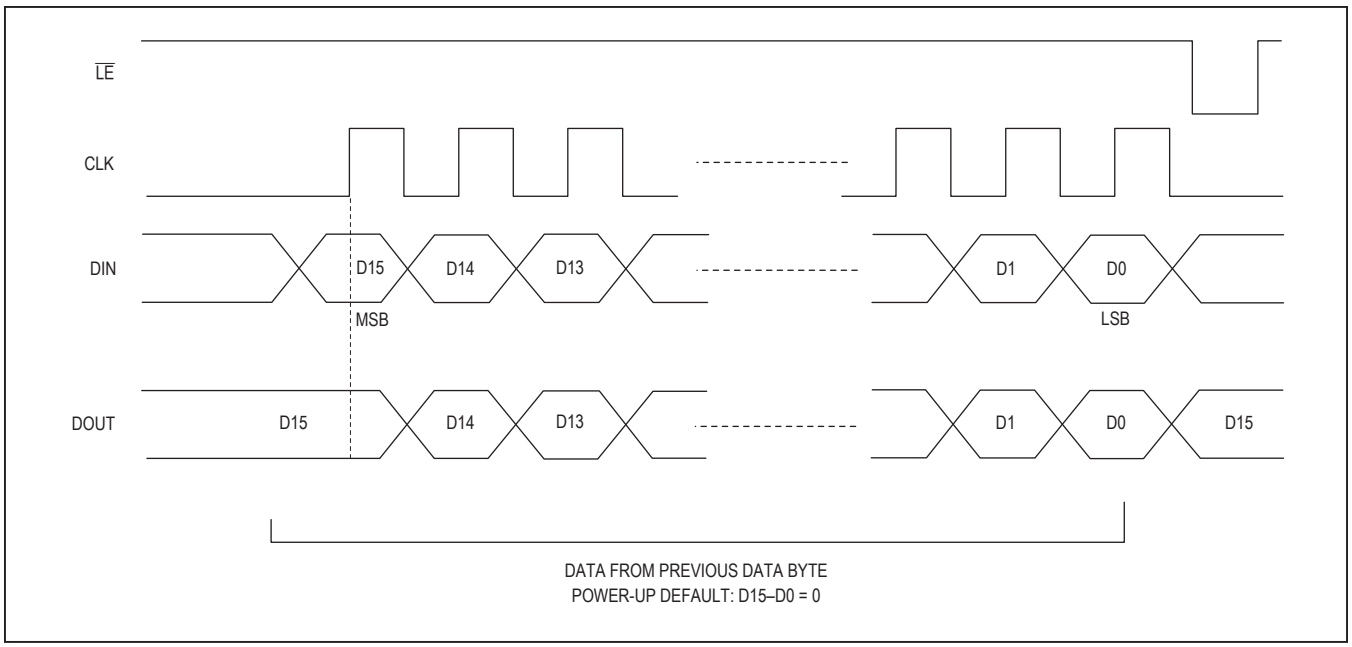


Figure 2. Latch Enable Interface Timing

Table 1. Serial Interface Programming (Notes 4–9)

DATA BITS								CONTROL BITS		FUNCTION							
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Table 1. Serial Interface Programming (Notes 4–9) (continued)

DATA BITS								CONTROL BITS		FUNCTION							
D8	D9	D10	D11	D12	D13	D14	D15 (MSB)	$\overline{LE}$	CLR	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care.

Note 4: The 16 switches operate independently.
Note 5: Serial data is clocked in on the rising edge of CLK.
Note 6: The switches go to a state retaining their present condition on the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
Note 7: DOUT is high when switch 15 is on.
Note 8: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
Note 9: The CLR input overrides all other inputs.

Applications Information

For medical ultrasound applications, see Figures 4, 5, and 6.

Logic Levels

The MAX14802/MAX14803/MAX14803A digital interface inputs CLK, DIN, $\overline{LE}$, and CLR operate on the V_{DD} supply voltage.

Daisy-Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple MAX14802/MAX14803/MAX14803A devices by daisy-chaining (Figure 3). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, and CLR inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers can be included anywhere in series with the MAX14802/MAX14803/MAX14803A data chain.

Supply Sequencing and Bypassing

The MAX14802/MAX14803/MAX14803A do not require special sequencing of the V_{DD}, V_{PP}, and V_{NN} supply voltages; however, analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM\_}, V_{NO\_}) \le V_{PP}$ during power-up and power-down. Bypass V_{DD}, V_{PP}, and V_{NN} to GND with a 0.1µF ceramic capacitor as close as possible to the device.

Application Diagrams

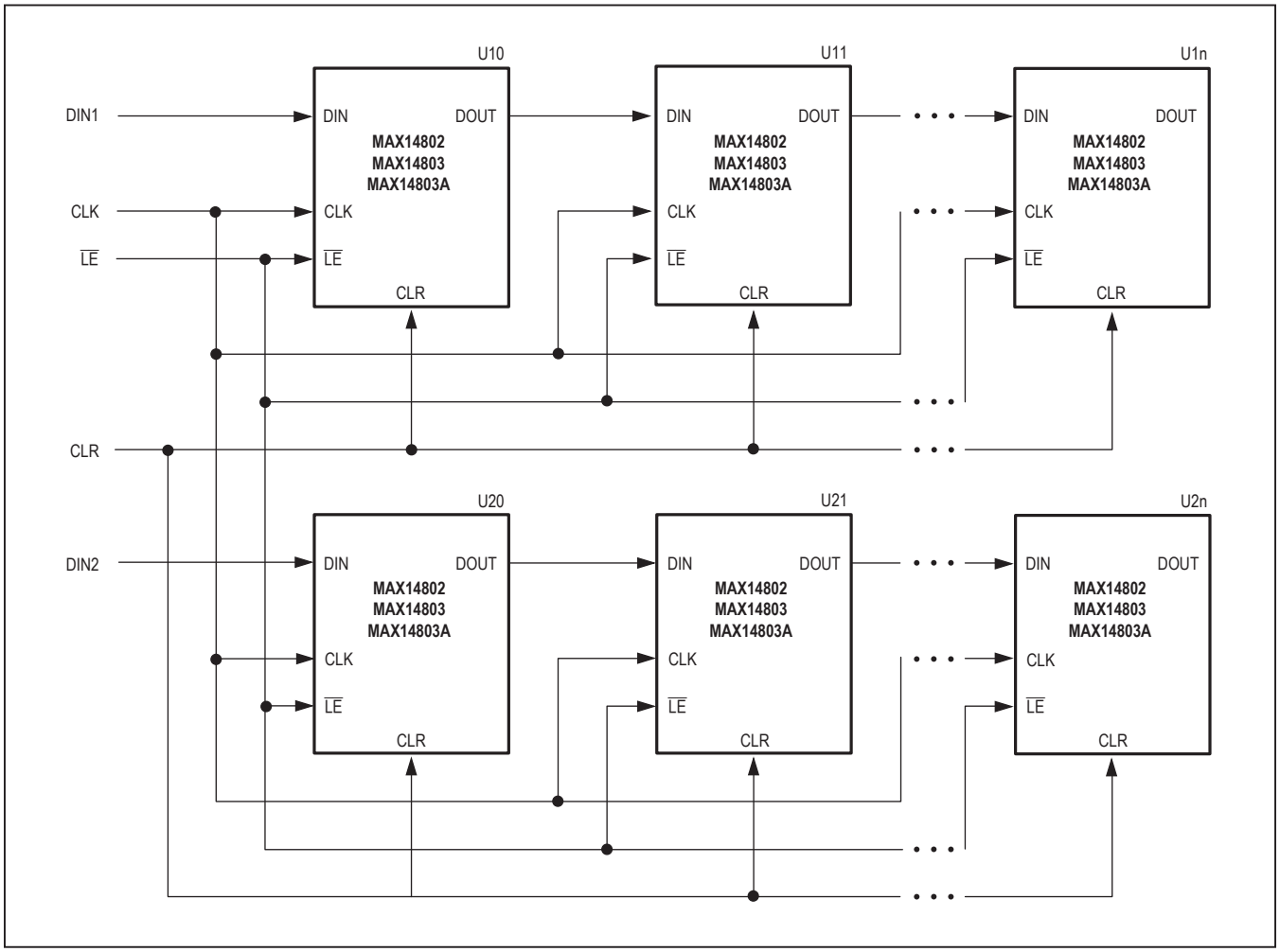


Figure 3. Interfacing Multiple Devices by Daisy-Chaining

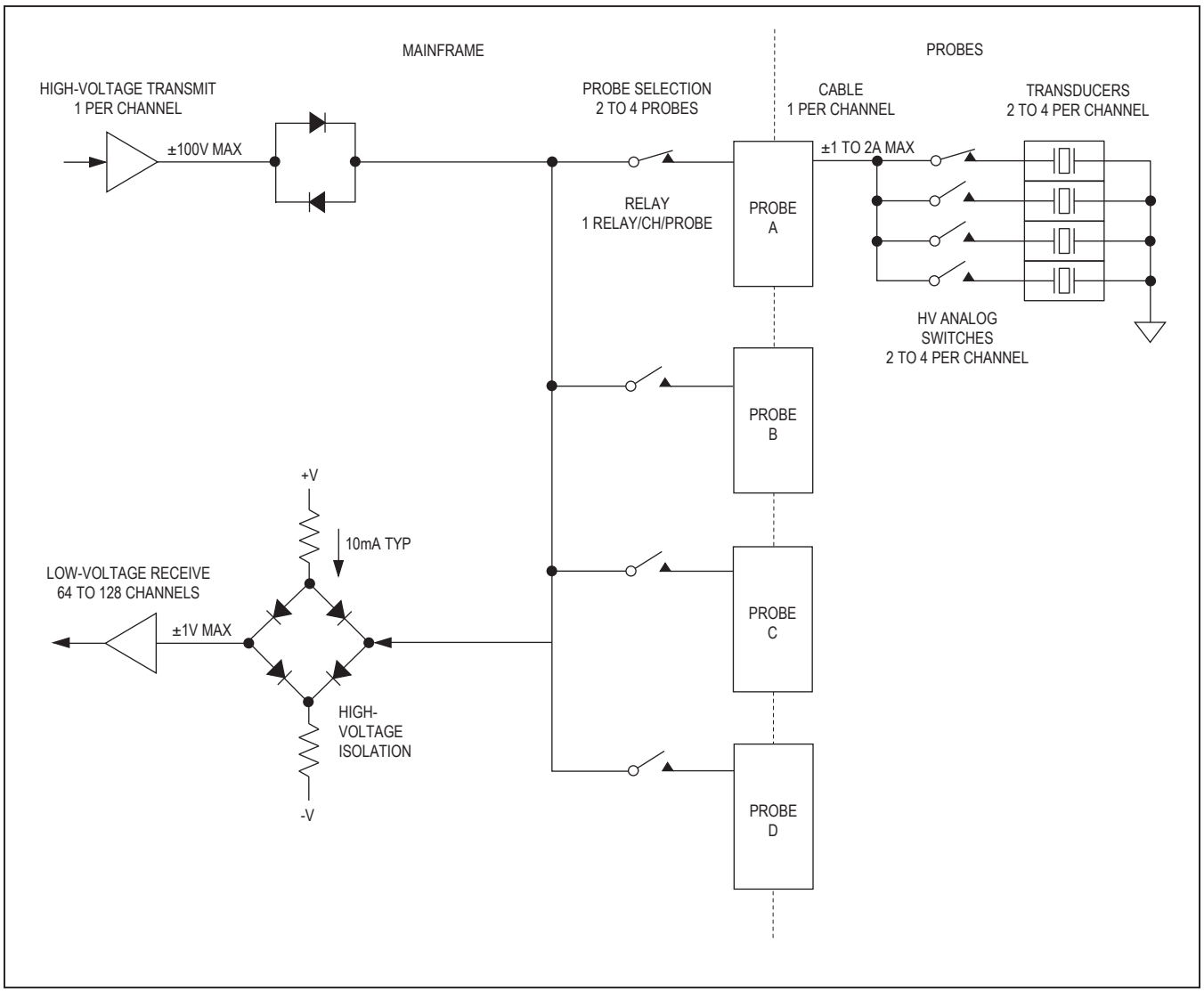


Figure 4. Medical Ultrasound Application—High-Voltage Analog Switches in Probe

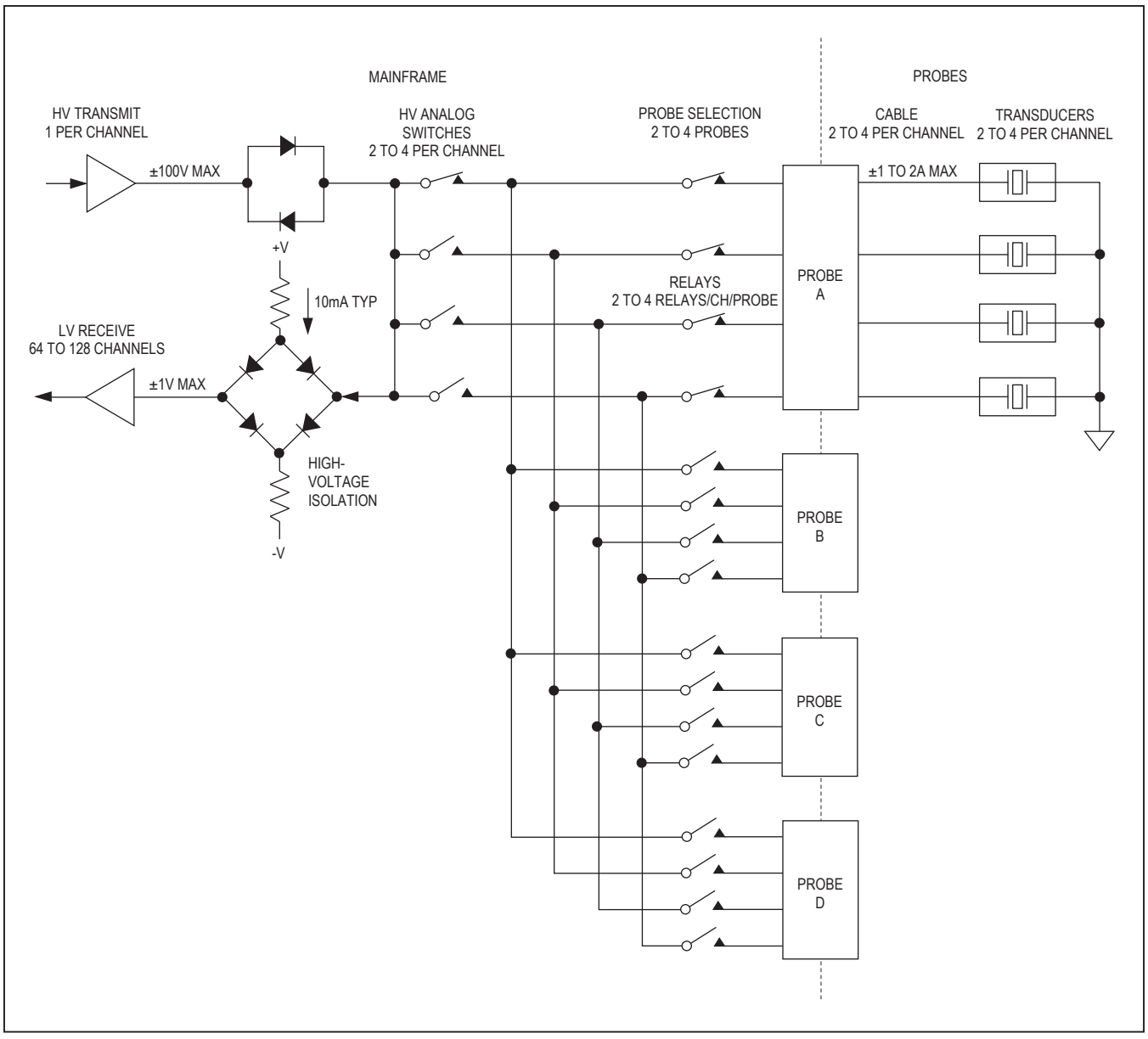


Figure 5. Medical Ultrasound Application—High-Voltage Analog Switches in Mainframe

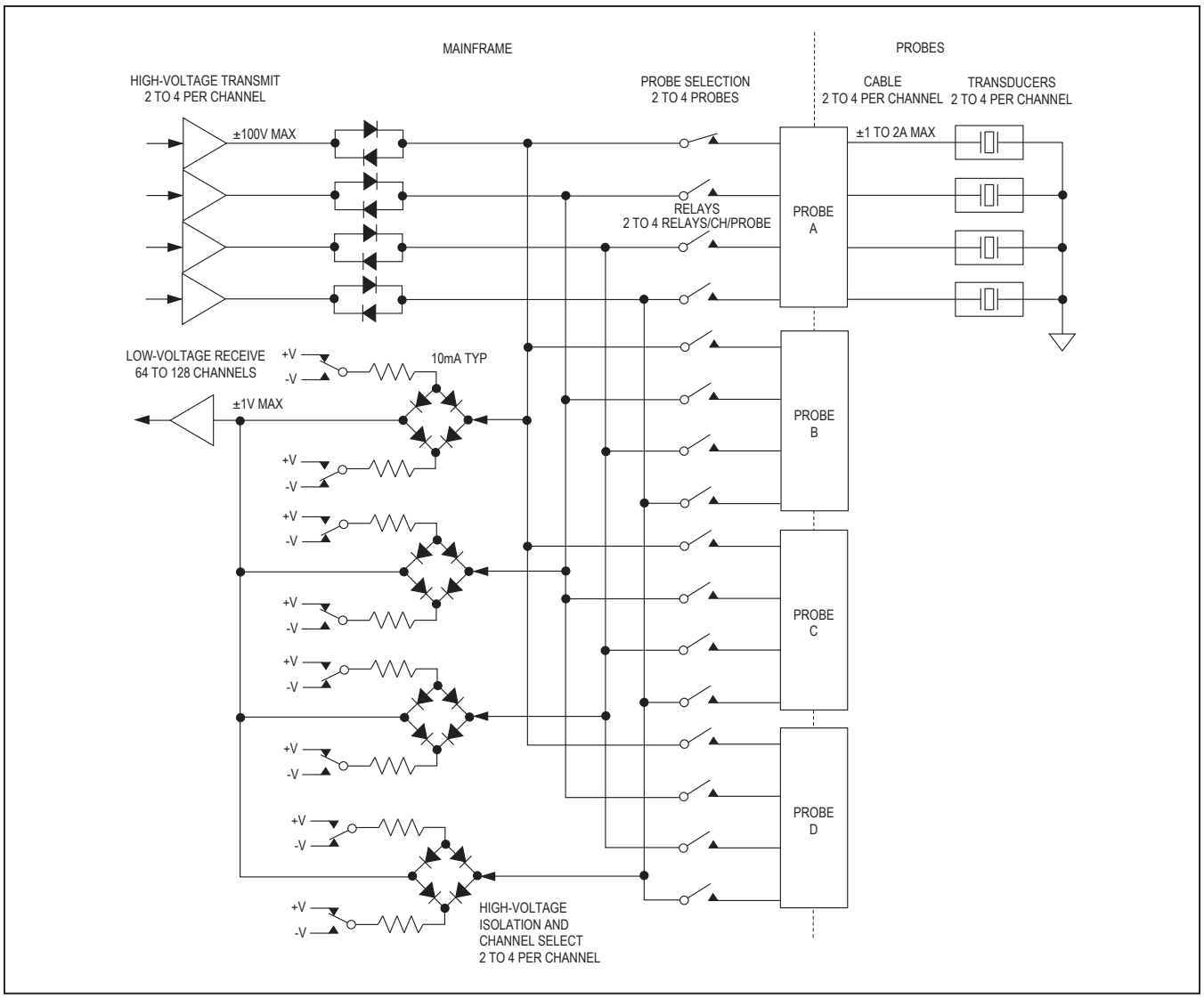


Figure 6. Medical Ultrasound Application—Multiple Transmit and Isolation per Receiver Channel

Ordering Information/Selector Guide

PART	SWITCH CHANNELS	BLEED RESISTOR	OVP	PIN-PACKAGE	TEMP RANGE
MAX14802CCM+	16	No	Yes	48 LQFP	0°C to +70°C
MAX14802ECM+	16	No	Yes	48 LQFP	-40°C to +85°C
MAX14803CCM+	16	Yes	Yes	48 LQFP	0°C to +70°C
MAX14803AEWZ+	16	Yes	Yes	110 WLP	-40°C to +85°C

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Initial release	—
1	9/09	Corrected two specifications in the *Absolute Maximum Ratings* section, changed the minimum of the peak-to-peak analog signal range to “either V_{NN} + 200V or (V_{PP} – 10V)”	2, 9
2	11/10	Deleted the MAX14800/MAX14801 from the entire data sheet and added the MAX14803A; added the WLP part to the *Ordering Information*, *Pin Configurations*, *Pin Descriptions*, and *Package Information* sections	1–19
3	8/11	Added extended temperature information; added MAX14802ECM+ to data sheet	1
4	6/13	Updated *Absolute Maximum Ratings* and *Operating Supply Voltages*	1, 2
5	2/21	Updated the *General Description, Absolute Maximum Ratings, Pin Configuration, Pin Description, Package Thermal Characteristics, Package Information,* and *Ordering Information* sections	1–2, 8–9, 18–19