1 PRODUCT OVERVIEW

The KS57C01502/C01504 single-chip CMOS microcontroller has been designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

The KS57P01504 is the microcontroller which has 4 Kbyte one-time-programmable ROM and the functions are the same to KS57C01502/C01504. With a four-channel comparator, eight LED direct drive pins, serial I/O interface, and its versatile 8-bit timer/counter, the KS57C01502/C01504 offers an excellent design solution for a wide variety of general-purpose applications.

Up to 24 pins of the 30-pin SDIP package can be dedicated to I/O. Five vectored interrupts provide fast response to internal and external events. In addition, the KS57C01502/C01504's advanced CMOS technology provides for very low power consumption and a wide operating voltage range — all at a very low cost.

FEATURES SUMMARY

Memory

- 512 × 4-bit data memory (RAM)
- 2048 × 8-bit program memory (ROM):KS57C01502
  4096 × 8-bit program memory (ROM):KS57C01504

24 I/O Pins

- I/O: 18 pins, including 8 high current pins
- Input only: 6 pins

Comparator

- 4-channel mode:
  Internal reference (4-bit resolution)
  16-step variable reference voltage
- 3-channel mode:
  External reference
  150 mV resolution (worst case)

8-bit Basic Timer

- Programmable interval timer
- Watch-dog timer

8-bit Timer/Counter 0

- Programmable interval timer
- External event counter function
  Timer/counter clock output to TCLO0 pin

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- 4 frequency outputs to BUZ pin

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive-only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Interrupts

- Two external interrupt vectors
- Three internal interrupt vectors
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode: Only CPU clock stops
- Stop mode: System clock stops

OSCILLATION SOURCES

- Crystal, Ceramic for system clock
- Crystal/ceramic: 0.4 - 6.0 MHz
- CPU clock divider circuit (by 4. 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 0.67, 1.33, 10.7 µs at 6.0 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 30 SDIP, 32 SOP

FUNCTION OVERVIEW

SAM47 CPU

All KS57-series microcontrollers have the advanced SAM47 CPU core. The SAM47 CPU can directly address up to 32 K bytes of program memory. The arithmetic logic unit (ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle and most 8-bit arithmetic and logical operations in two cycles.

CPU REGISTERS

Program Counter

A 11-bit program counter (PC) stores addresses for instruction fetch during program execution. Usually, the PC is incremented by the number of bytes of the instruction being fetched. An exception is the 1-byte instruction REF which is used to reference instructions stored in a look-up table in the ROM. Whenever a reset operation or an interrupt occurs, bits PC11 through PC0 are set to the vector address. Bit PC13–12 is reserved to support future expansion of the device's ROM size.

Stack Pointer

An 8-bit stack pointer (SP) stores addresses for stack operations. The stack area is located in the general-purpose data memory bank 0. The SP is read or written by 8-bit instructions and SP bit 0 must always be set to logic zero.

During an interrupt or a subroutine call, the PC value and the program status word (PSW) are saved to the stack area in RAM. When the service routine has completed, the values referenced by the stack pointer are restored. Then, the next instruction is executed.

The stack pointer can access the stack regardless of data memory access enable flag status. Since the reset value of the stack pointer is not defined in firmware, it is recommended that the stack pointer be initialized to 00H by program code. This sets the first register of the stack area to data memory location 0FFH.

PROGRAM MEMORY

In its standard configuration, the 4096 × 8-bit ROM is divided into three functional areas:

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 1920-byte general purpose area (KS57C01502)

— 3968-byte general purpose area (KS57C01504)

The vector address area is used mostly during reset operations and interrupts. These 16 bytes can also be used as general-purpose ROM.

The REF instruction references 2 × 1-byte and 2-byte instructions stored in locations 0020H–007FH. The REF instruction can also reference 3-byte instructions such as JP or CALL. In order for REF to be able to reference these instructions, however, JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name. Unused locations in the instruction reference area can be allocated to general-purpose use.

DATA MEMORY

Overview

Data memory is organized into three areas:

— 32 × 4-bit working registers

— 224 × 4-bit general-purpose area in bank 0

— 256 × 4-bit general-purpose area in bank 1

— 128 × 4-bit area in bank 15 for memory-mapped I/O addresses

Data stored in data memory can be manipulated by 1-, 4-, and 8-bit instructions.

Data memory is organized into two memory banks — bank 0, bank 1 and bank 15. The select memory bank instruction (SMB) selects the bank to be used as working data memory. After power-on reset operation, initialization values for data memory must be redefined by code.

Data Memory Addressing Modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0, 1 or 15.

When the EMB flag is logic zero, restricted area can be accessed. When the EMB flag is set to logic one, all two data memory banks can be accessed according to the current SMB value. The EMB = "0" addressing mode is used for normal program execution, whereas the EMB = "1" mode is commonly used for interrupts, subroutines, mapped I/O, and repetitive access of specific RAM addresses.

Working Registers

The RAM's working register area in data memory bank 0 is further divided into four *register* banks. Each register bank has eight 4-bit registers that are addressable either by 1-bit or 4-bit instructions. Paired 4-bit registers can be addressed as double registers by 8-bit instructions.

Register A is the 4-bit accumulator and double register EA is the 8-bit extended accumulator. Double registers WX, WL, and HL are used as data pointers for indirect addressing. Unused working registers can be used as general-purpose memory.

To limit the possibility of data corruption due to incorrect register bank addressing, register bank 0 is usually used for the main program and banks 1, 2, and 3 for interrupt service routines.

CONTROL REGISTERS

Program Status Word

The 8-bit program status word (PSW) controls ALU operations and instruction execution sequencing. It is also used to restore a program's execution environment when an interrupt has been serviced. Program instructions can always address the PSW regardless of the current value of data memory enable flags.

Before an interrupt or subroutine is processed, the PSW values are pushed onto the stack in data memory bank 0. When the service routine is completed, the PSW values are restored.

IS1	IS0	EMB	ERB
C	SC2	SC1	SC0

Interrupt status flags (IS1, IS0), the enable memory bank and enable register bank flags (EMB, ERB), and the carry flag (C) are 1- and 4-bit read/write or 8-bit read-only addressable. You can address the skip condition flags (SC0–SC2) using 8-bit read instructions only.

Select Bank (SB) Register

Two 4-bit registers store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

'SMB n' instruction selects a data memory bank (0 or 15) and stores the upper four bits of the 12-bit data memory address in the SMB register. To select register bank 0, 1, 2, or 3, and store the address data in the SRB, you can use the instruction 'SRB n'.

The instructions "PUSH SB" and "POP SB" move SRB and SMB values to and from the stack for interrupts and subroutines.

CLOCK CIRCUITS

System oscillation circuit generates the internal clock signals for the CPU and peripheral hardware.

The system clock can use a crystal, or ceramic oscillation source, or an externally-generated clock signal. To drive KS57C01502/C01504 using an external clock source, the external clock signal should be input to X_{in}, and its inverted signal to X_{out}.

4-bit power control register controls the oscillation on/off, and select the CPU clock. The internal system clock signal (fx) can be divided internally to produce three CPU clock frequencies — fx/4, fx/8, or fx/64.

INTERRUPTS

Interrupt requests may be generated internally by on-chip processes (INTB, INTT0, and INTS) or externally by peripheral devices (INT0 and INT1). There are two quasi-interrupts: INTK and INTW. INTK (KS0–KS2) detects falling edges of incoming signals and INTW detects time intervals of 0.5 seconds or 3.91 milliseconds. The following components support interrupt processing:

— Interrupt enable flags

— Interrupt request flags

— Interrupt priority registers

— Power-down termination circuit

POWER-DOWN

To reduce power consumption, there are two power-down modes: idle and stop. The IDLE instruction initiates idle mode; the STOP instruction initiates stop mode.

In idle mode, the CPU clock stops while peripherals continue to operate normally. In stop mode, system clock oscillation stops completely, halts all operations except for a few basic peripheral functions. A power-down is terminated either by a RESET or by an interrupt (with exception of the external interrupt INT0).

RESET

When RESET is input during normal operation or during power-down mode, a reset operation is initiated and the CPU enters idle mode. When the standard oscillation stabilization time interval (31.3 ms at 4.19 MHz) has elapsed, normal CPU operation resumes.

I/O PORTS

The KS57C01502/C01504 has seven I/O ports. Pin addresses for all I/O ports are mapped to locations FF0H–FF6H in bank 15 of the RAM. There are 6 input pins and 18 configurable I/O pins including 8 high current I/O pins for a total of 24 I/O pins. The contents of I/O port pin latches can be read, written, or tested at the corresponding address using bit manipulation instructions.

TIMERS and TIMER/COUNTER

The timer function has three main components: an 8-bit basic timer, an 8-bit timer/counter, and a watch timer.

The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected internal clock frequency.

The programmable 8-bit timer/counter is used for counting events, modifying internal clock frequencies, and dividing external clock signals. The 8-bit timer/counter generates a clock signal (SCK) for the serial I/O interface.

The watch timer consists of an 8-bit watch timer mode register, a clock selector, and a frequency divider circuit. Its functions include real-time, watch-time measurement, and clock generation for frequency output for buzzer sound.

SERIAL I/O INTERFACE

The serial I/O interface supports the transmission or reception of 8-bit serial data with an external device. The serial interface has the following functional components:

— 8-bit mode register
— Clock selector circuit
— 8-bit buffer register
— 3-bit serial clock counter

The serial I/O circuit can be set to transmit-and-receive, or to receive-only mode. MSB-first or LSB-first transmission is also selectable.

The serial interface can operate with an internal or an external clock source, or using the clock signal generated by the 8-bit timer/counter. Transmission frequency can be modified by setting the appropriate bits in the SIO mode register.

BIT SEQUENTIAL CARRIER

The bit sequential carrier (BSC) is a 16-bit register that can be manipulated using 1-, 4-, and 8-bit instructions.

Using 1-bit indirect addressing, addresses and bit locations can be specified sequentially. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register. BSC data can also be manipulated using direct addressing.

COMPARATOR

The KS57C01502/C01504 contains a 4-channel comparator which can be multiplexed to normal input port.

— Conversion time: 15.2 µs, 121.6 µs at 4.19 MHz

— Two operation modes:

  Three channels for analog input and one channel for external reference voltage input

  Four channels for analog input and internal reference voltage level

— 16-level internal reference voltage generator

— 150 mV accuracy for input voltage level difference detection (maximum)

— Comparator enable and disable

The comparison results are read from the 4-bit CMPREG register after the specified conversion time.

BLOCK DIAGRAM

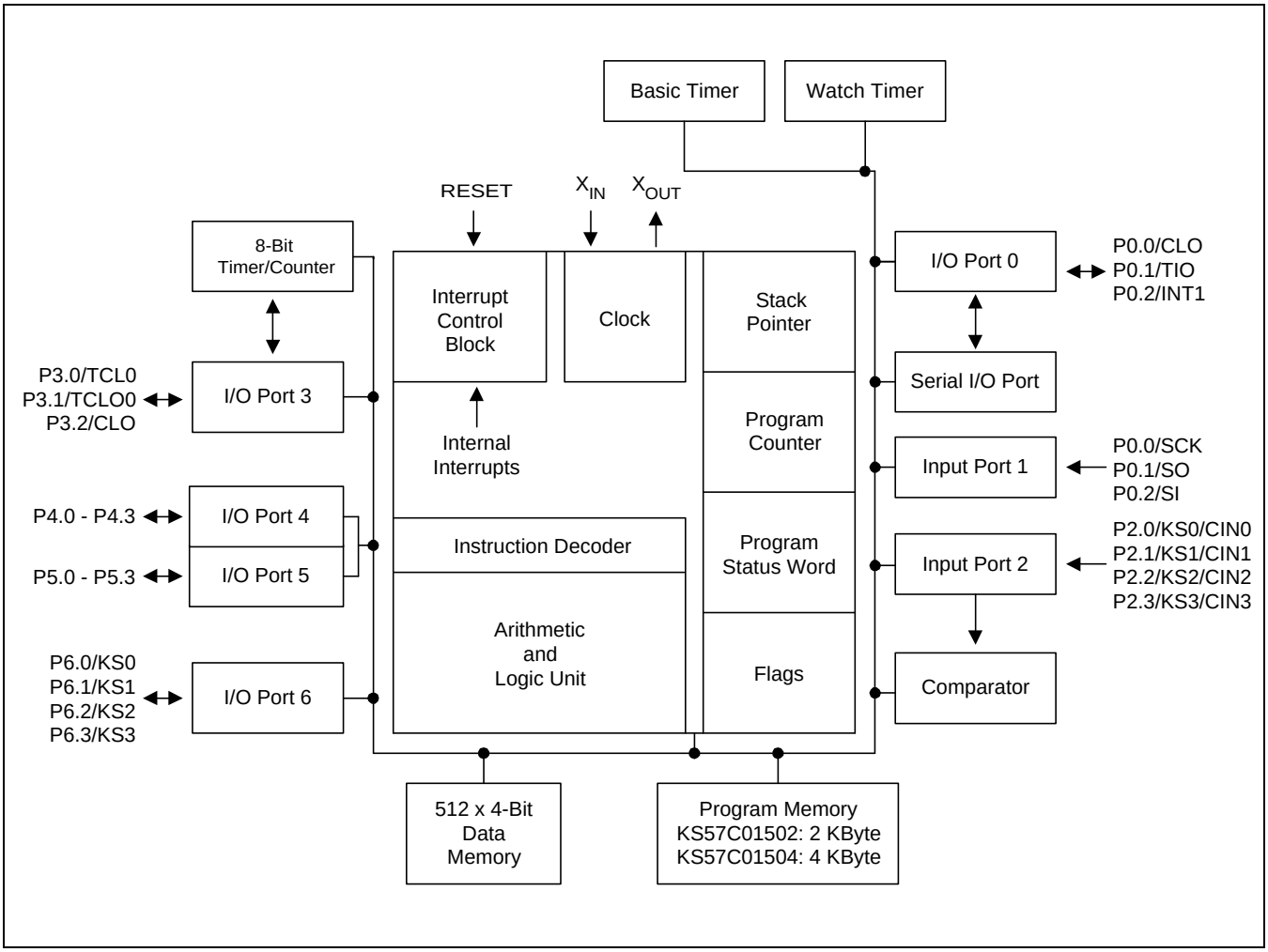
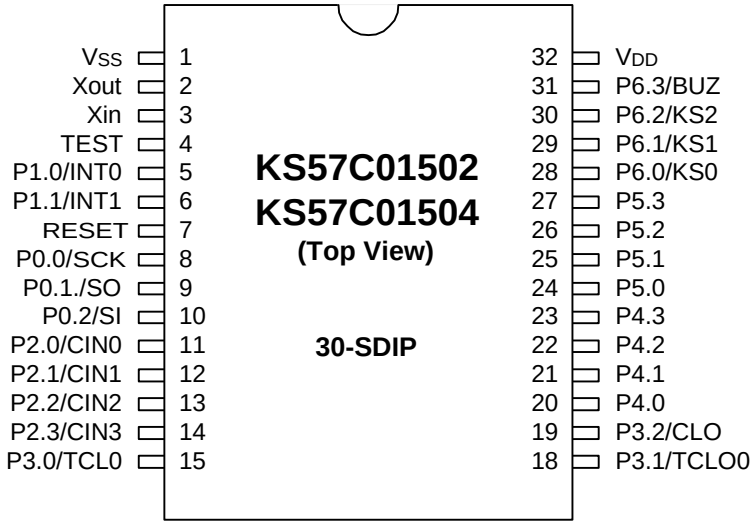


Figure 1-1. KS57C01502/C01504 Simplified Block Diagram

Pin Assignments



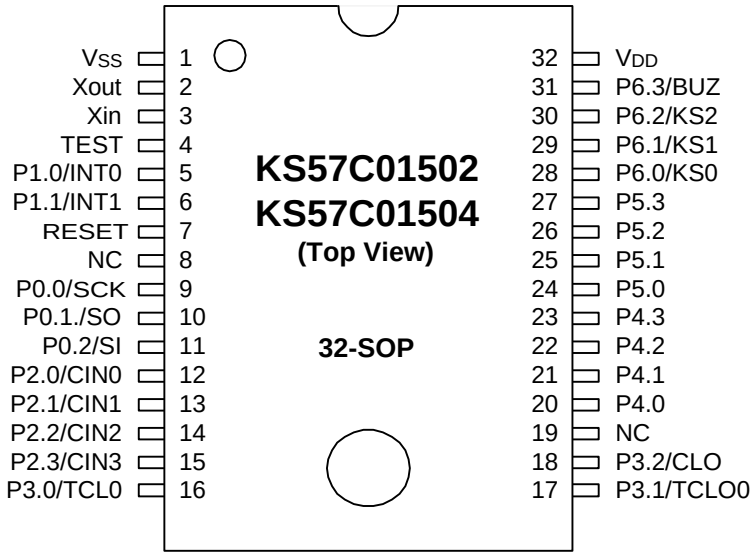


Figure 1-2. KS57C01502/C01504 Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. KS57C01502/C01504 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test are possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	8(9) 9(10) 10(11)	SCK SO SI
P1.0 P1.1	I	2-bit input port. 1-bit or 2-bit read and test are possible. Pull-up resistors are assignable by software.	5(5) 6(6)	INT0 INT1
P2.0–P2.3	I	4-bit input port. 1-bit or 4-bit read and test are possible.	11-14 (12-15)	CIN0–CIN3
P3.0 P3.1 P3.2	I/O	Same as port 0	15(16) 16(17) 17(18)	TCL0 TCLO0 CLO
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-, or 8-bit read/write and test are possible. Pins are individually configurable as input or output. 4-bit pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. The N-channel open-drain or push-pull output can be selected by software (1-bit unit)	18-21(20-23) 22-25(24-27)	–
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test are possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	26(28) 27(29) 28(30) 29(31)	KS0 KS1 KS2 BUZ
INT0	I	External interrupts with detection of rising and falling edges	5(5)	P1.0
INT1	I	External interrupts with detection of rising or falling edges	6(6)	P1.1
CIN0–CIN3	I	4-channel comparator input. CIN0–CIN2: comparator input only. CIN3: comparator input or external reference input	11-14(12-15)	P2.0–P2.3
SCK	I/O	Serial interface clock signal	8(9)	P0.0
SO	I/O	Serial data output	9(10)	P0.1
SI	I/O	Serial data input	10(11)	P0.2
TCL0	I/O	External clock input for timer/counter	15(16)	P3.0
TCLO0	I/O	Timer/counter clock output	16(17)	P3.1
CLO	I/O	CPU clock output	17(18)	P3.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	29(31)	P6.3

NOTE: Pn numbers shown in parentheses '( )' are for 32-pin SOP package; other pin numbers are for the 30-pin SDIP.

Table 1-1. KS57C01502/C01504 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
		Quasi-interrupt input with falling edge detection	26-28(28-30)	P6.0–P6.2
V_{DD}	—	Main power supply	30(32)	—
V_{SS}	—	Ground	1(1)	—
RESET	I	Reset signal	7(7)	—
TEST	I	Test signal input (must be connected to V_{SS})	4(4)	—
X_{in}, X_{out}	—	Crystal or ceramic oscillator signal for system clock	3,2(3,2)	—

NOTE: Pin numbers shown in parentheses '( )' are for 32-pin SOP package; other pin numbers are for the 30-pin SDIP.

Table 1-2. Overview of KS57C01502/C01504 Pin Data

SDIP Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1	V_{SS}	—	—	—	—
2,3	Xout, Xin	—	—	—	—
4	TEST	—	I	—	—
5,6	P1.0, P1.1	INT0, INT1	I	Input	A-3
7	RESET	—	I	—	B
8-10	P0.0 - P0.2	SCK, SO, SI	I/O	Input	D-1
11-14	P2.0 - P2.3	CIN0 - CIN3	I	Input	F-1, F-2 (note)
15-17	P3.0 - P3.2	TCL0, TCLO0, CLO	I/O	Input	D-1
18-21	P4.0 - P4.3	—	I/O	Input	E
22-25	P5.0 - P5.3	—	I/O	Input	E
26-29	P6.0 - P6.3	KS0, KS1, KS2, BUZ	I/O	Input	D-1
30	V_{DD}	—	—	—	—

NOTE: I/O circuit type F-2 is implemented for P2.3 only.

PIN CIRCUIT DIAGRAMS

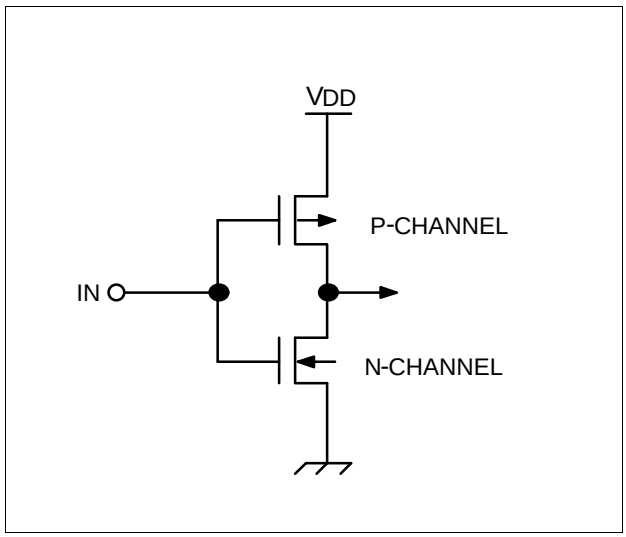


Figure 1-3. Pin Circuit Type A

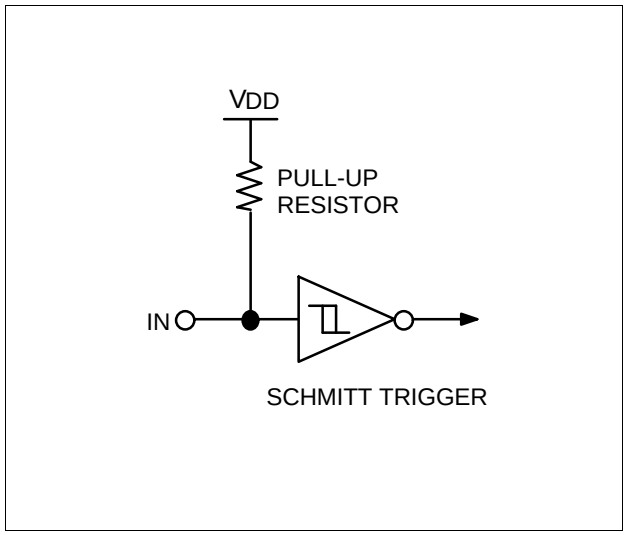


Figure 1-5. Pin Circuit Type B

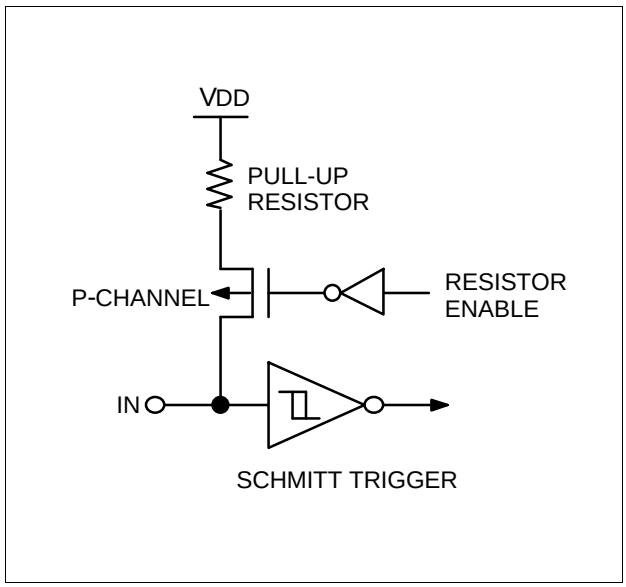


Figure 1-4. Pin Circuit Type A-3

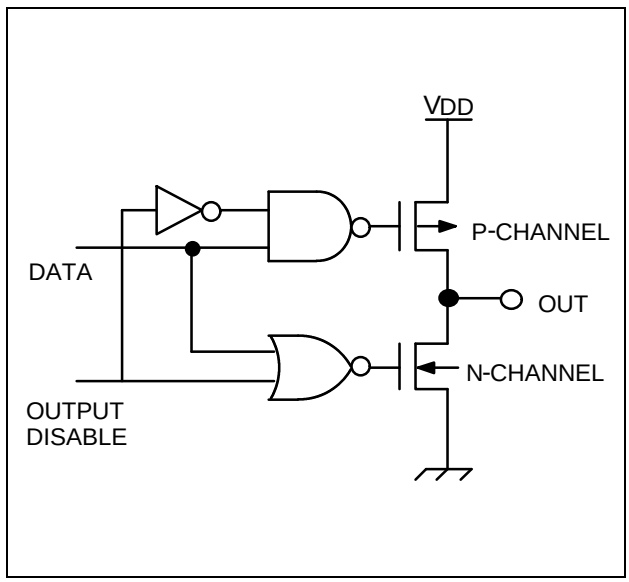


Figure 1-6. Pin Circuit Type C

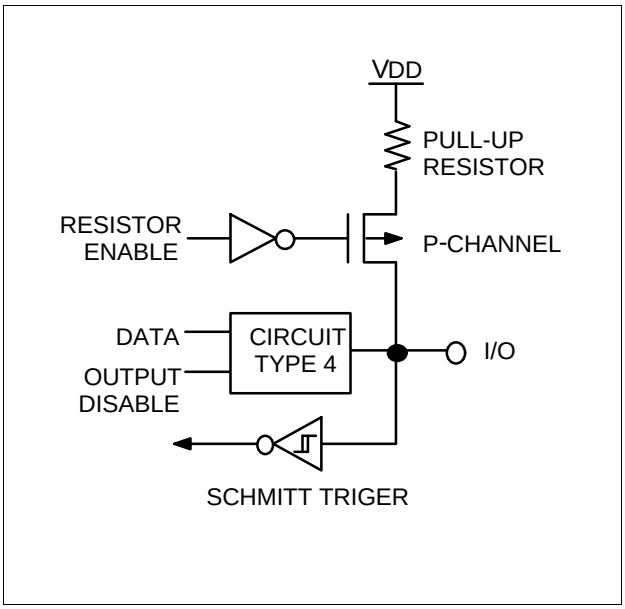


Figure 1-7. Pin Circuit Type D-1

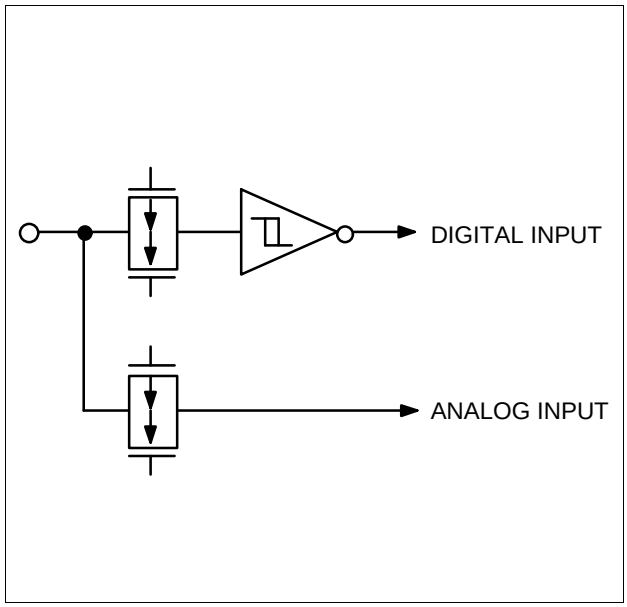


Figure 1-9. Pin Circuit Type F-1

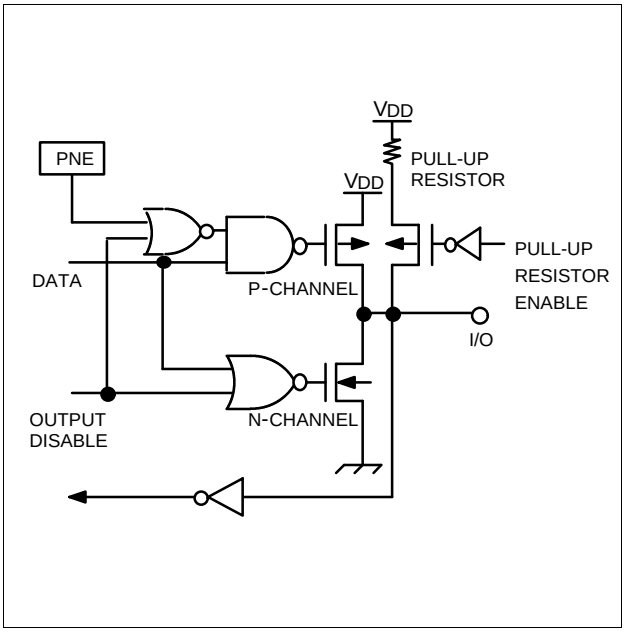


Figure 1-8. Pin Circuit Type E

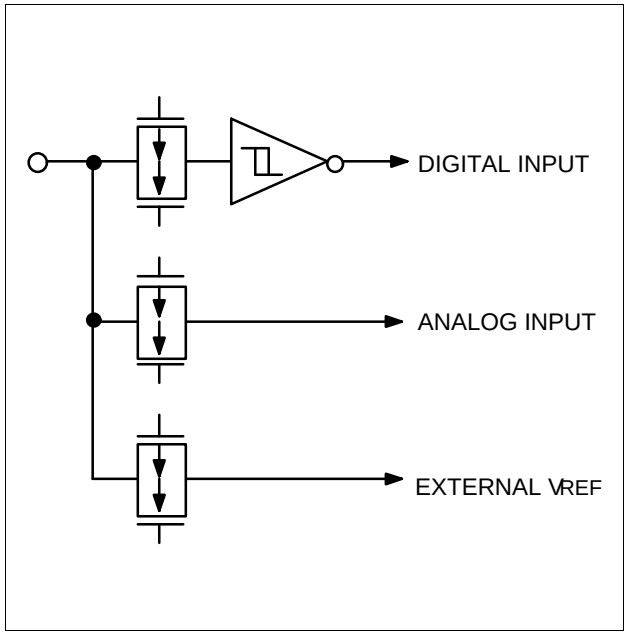


Figure 1-10. Pin Circuit Type F-2

14 ELECTRICAL DATA

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 5	mA
		All I/O ports active	– 15	
Output Current Low	I_{OL}	Ports 0, 3, and 6	5	mA
		Ports 4 and 5	30	
		All ports, total	+ 100	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 4 and 5	$0.7V_{DD}$	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 3, 6, and RESET	$0.8V_{DD}$	–	V_{DD}	
	V_{IH3}	X_{in} and X_{out}	V_{DD} – 0.1	–	V_{DD}	
Input Low Voltage	V_{IL1}	Ports 4 and 5	–	–	$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 2, 3, 6, and RESET			$0.2V_{DD}$	
	V_{IL3}	X_{in} and X_{out}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 3, 4, 5, 6	V_{DD} - 1.0	–	–	V

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4, 5	–	–	2	V
		V_{DD} = 4.5V to 5.5 V I_{OL} = 4.0mA All output pins except Ports 4, 5		–	2	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{in} and X_{out}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{in} and X_{out}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{in}, X_{out} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{in} and X_{out}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V	–	–	– 3	µA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V Port 0, 1, 3, 4, 5, 6	25	50	100	kΩ
		V_{DD} = 3 V	50	100	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	250	400	
		V_{DD} = 3 V	200	500	800	

Table 14-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.0	8.0	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		2.0	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.3	4.0	
			4.19MHz		1.0	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	0.8	2.5	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		0.6	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.6	1.5	
			4.19MHz		0.4	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.5	3.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.3	2.0	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistor, output port drive currents and comparator.
2. The supply current assumes a CPU clock of fx/4.

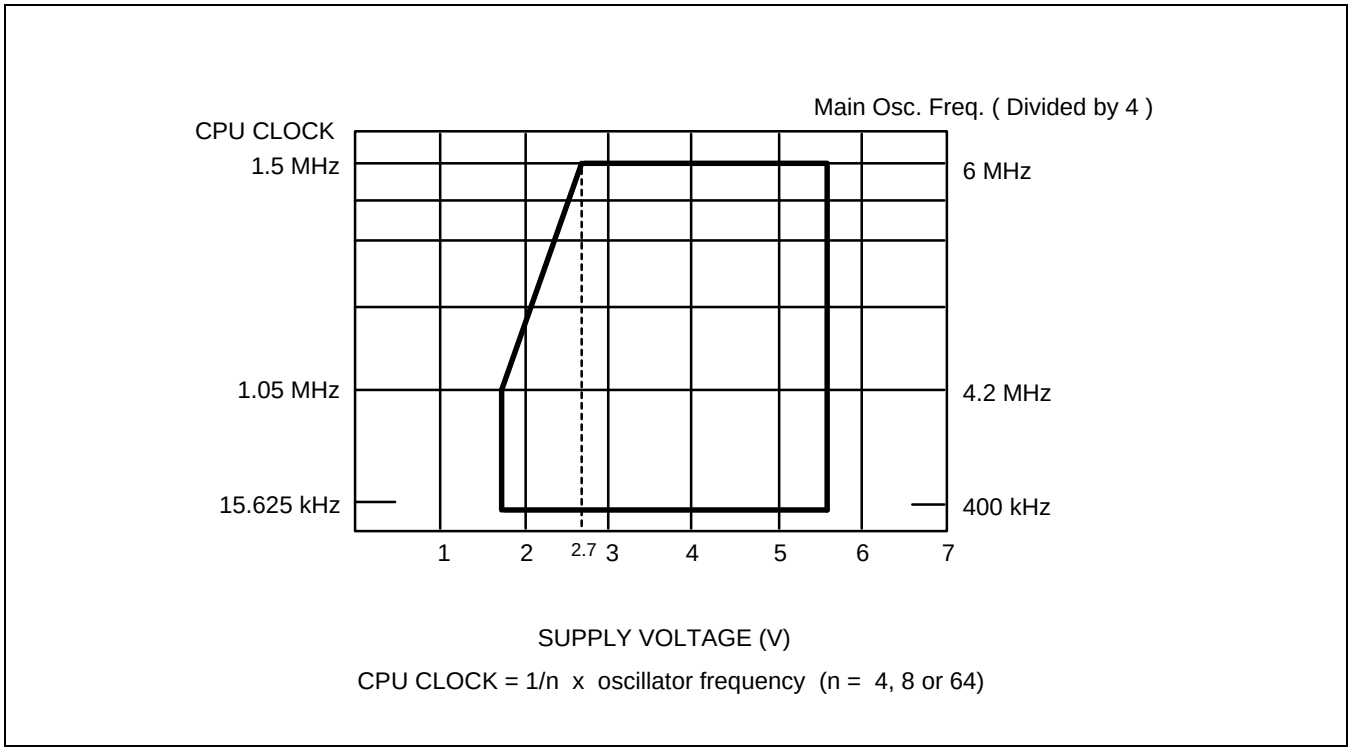
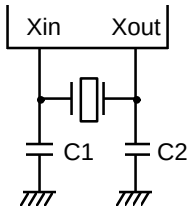
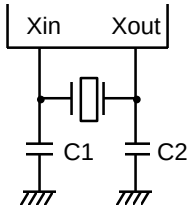
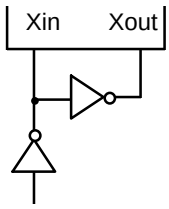


Figure 14-1. Standard Operating Voltage Range

Table 14-3. Oscillators Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{in} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}				15	pF
I/O Capacitance	C_{IO}				15	pF

Table 14-5. Comparator Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.5V, V_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	–	–	0	–	V_{DD}	V
Reference Voltage Range	V_{REF}	–	0	–	V_{DD}	V
Input Voltage Accuracy	V_{CIN}	–	–	–	±150	mV
Input Leakage Current	I_{CIN}, I_{REF}	–	– 3	–	3	µA

Table 14-6. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	0.95			
TCL0 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	670			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			

Table 14-6. A.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	ns
		Internal SCK source	$t_{KCY}/2 - 50$			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 - 150$			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 1.8 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 1.8 V to 5.5 V External SCK source	600			
		Internal SCK source	500			
Output Delay for SCK to SO	t_{KSO} (1)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, KS0–KS2	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES:

1. R (1 Kohm) and C (100 pF) are the load resistance and load capacitance of the SO output line.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

Table 14-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

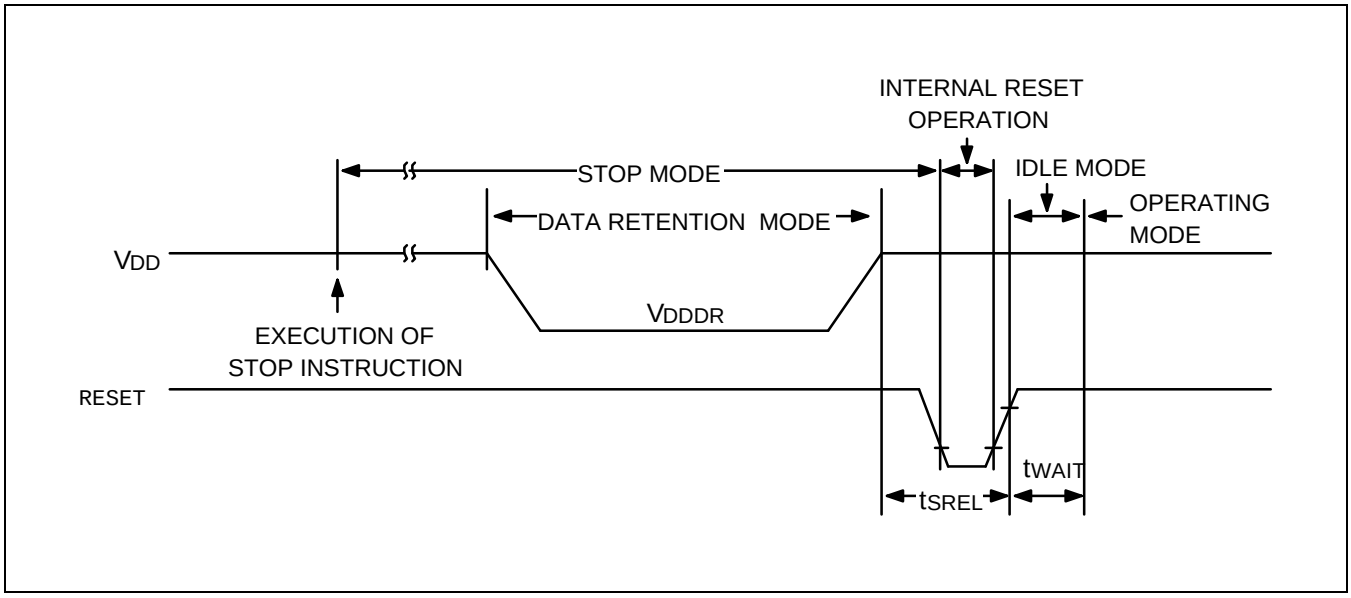


Figure 14-2. Stop Mode Release Timing When Initiated by RESET

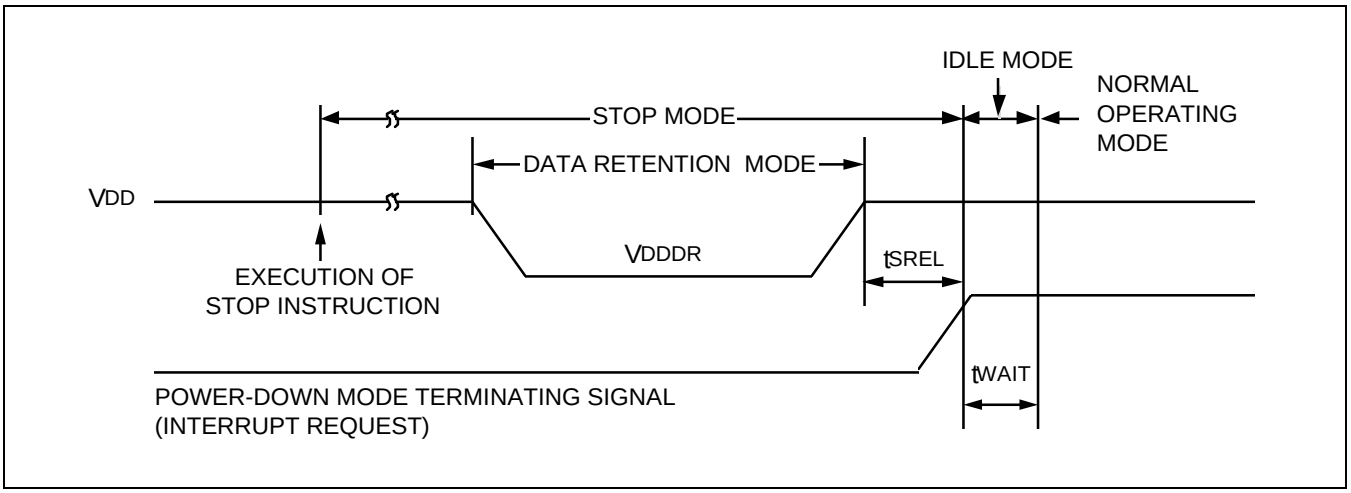


Figure 14-3. Stop Mode Release Timing When Initiated By Interrupt Request

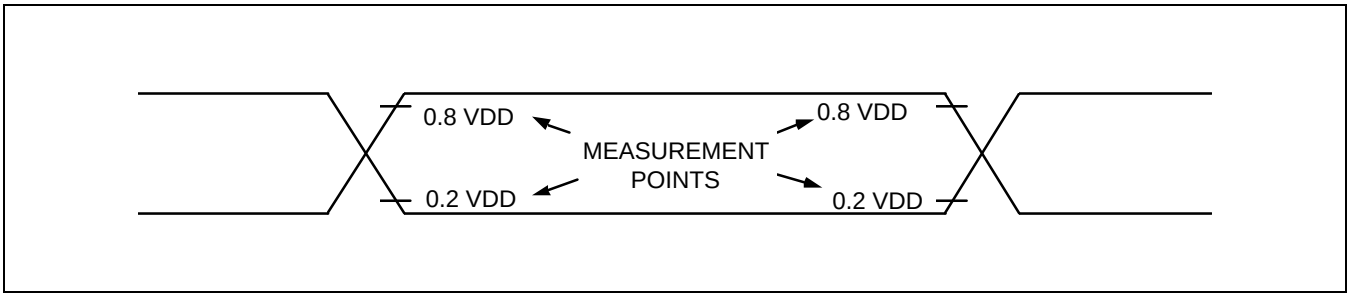


Figure 14-4. A.C. Timing Measurement Points (Except for X_{in})

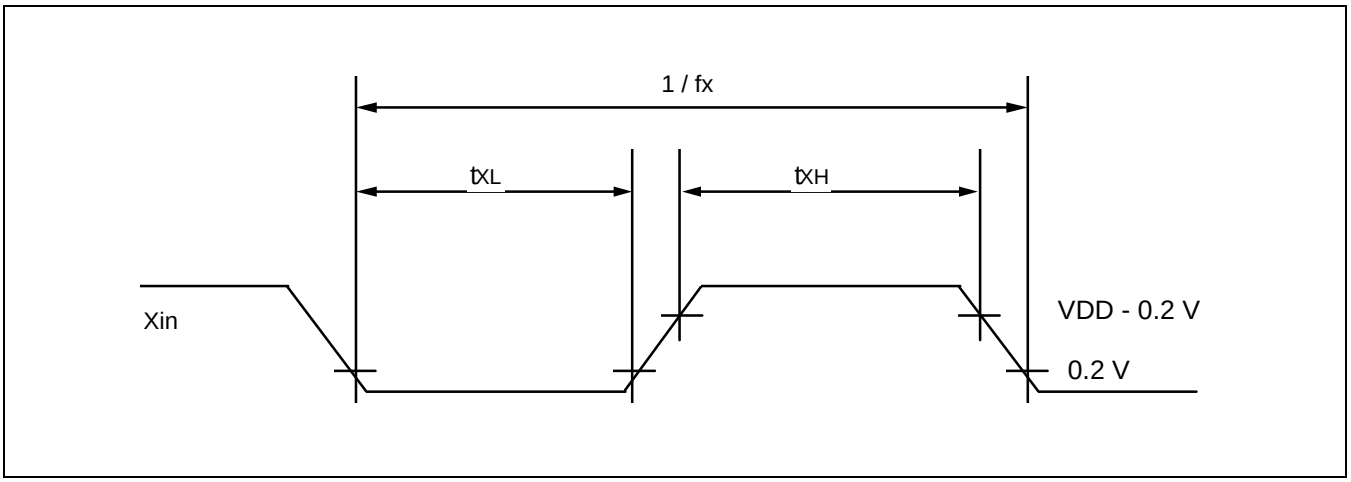


Figure 14-5. Clock Timing Measurement at X_{in}

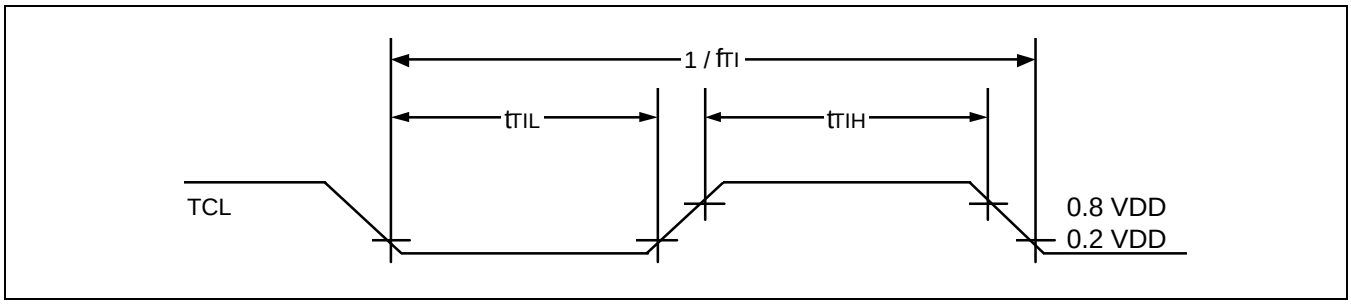


Figure 14-6. TCL Timing

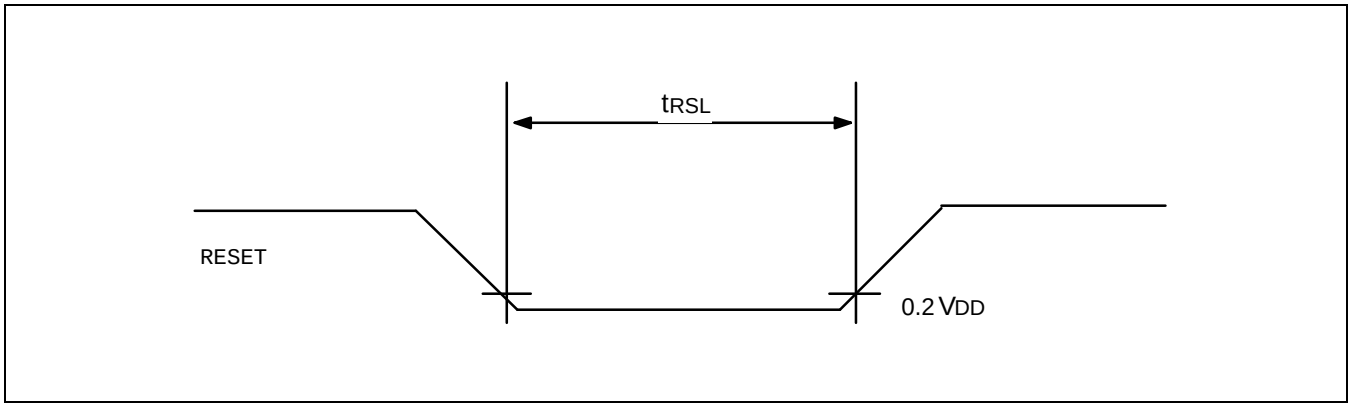


Figure 14-7. Input Timing for RESET Signal

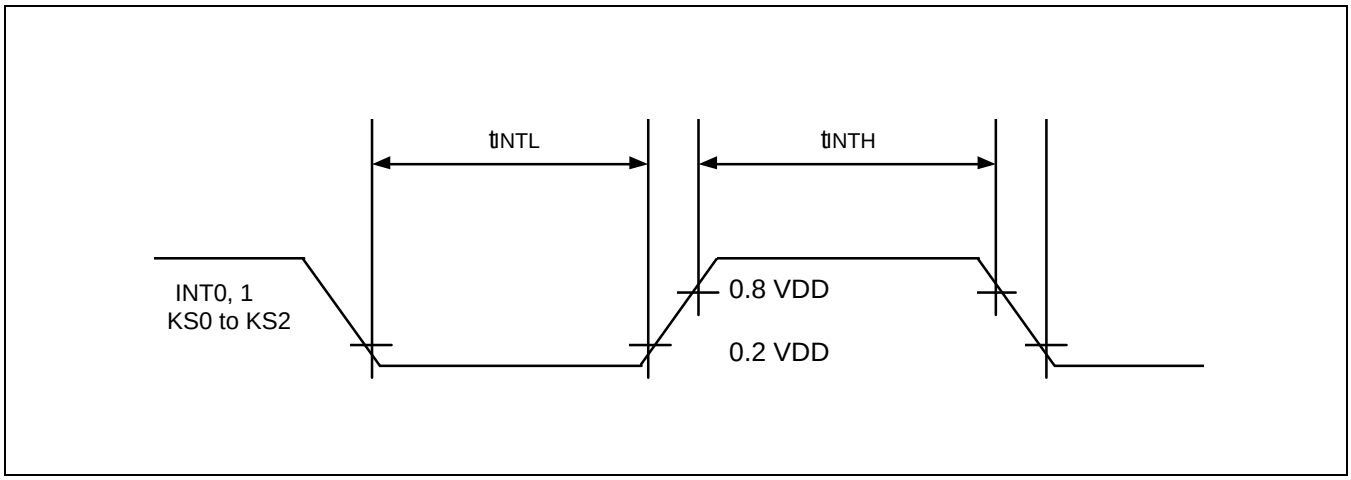


Figure 14-8. Input Timing for External Interrupts

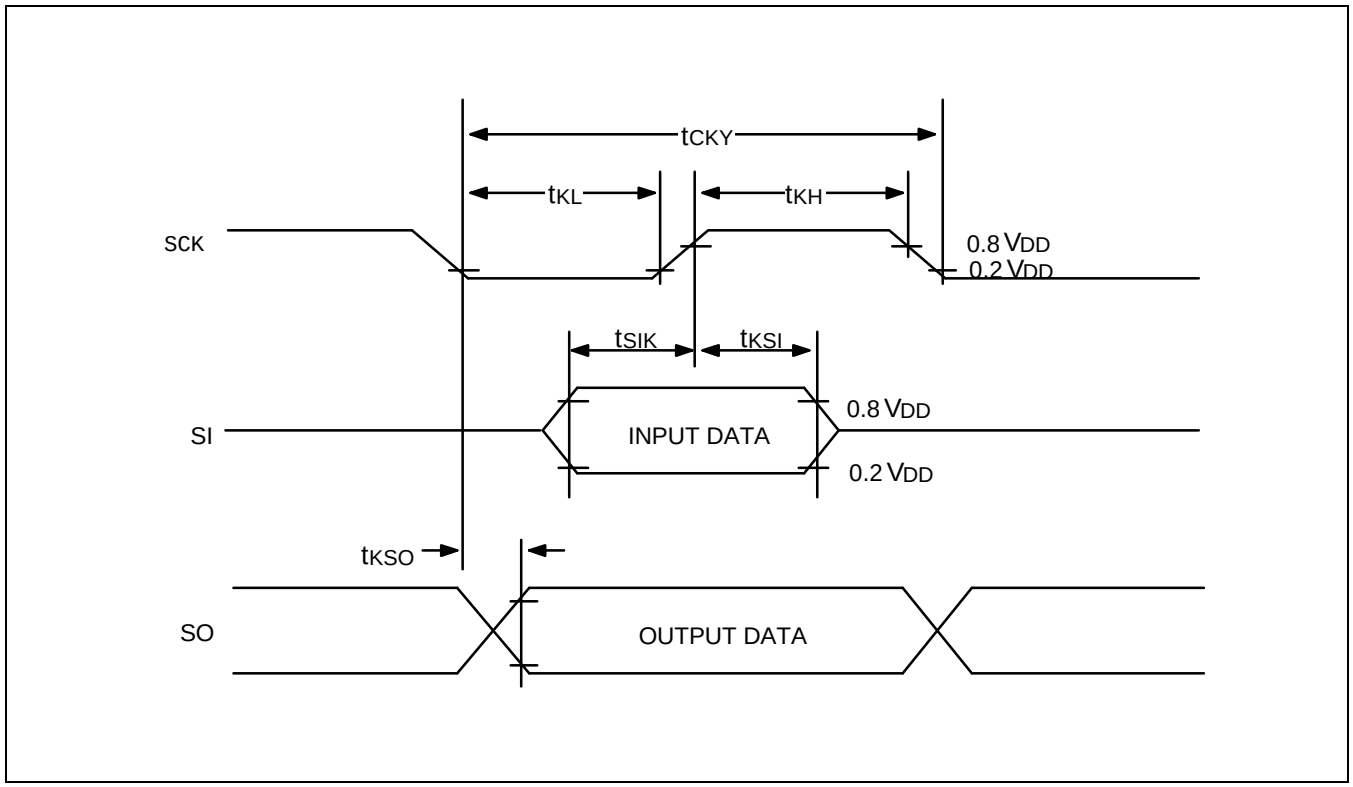
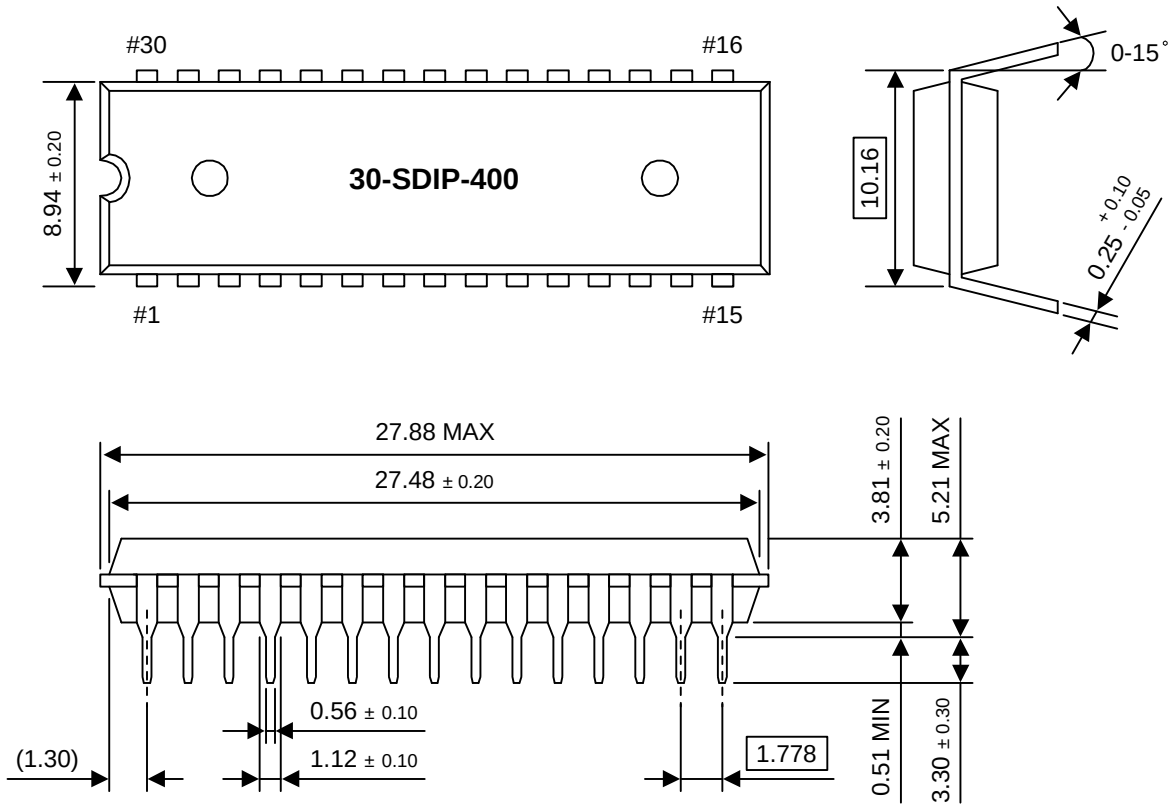


Figure 14-9. Serial Data Transfer Timing

15 MECHANICAL DATA

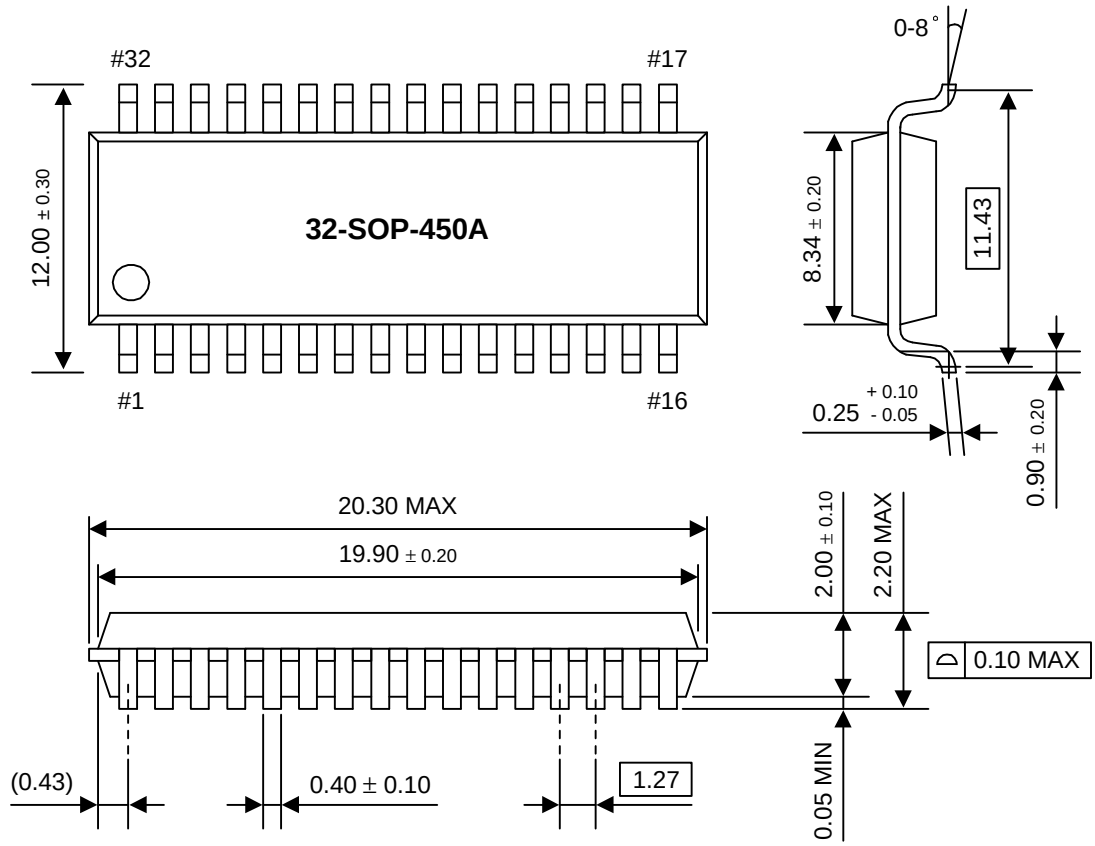
OVERVIEW

The KS57C01502/C01504/P01504 microcontroller is available in a 30-pin SDIP package (Samsung part number 30-SDIP-400) and a 32-SOP package (Samsung part number 30-SOP-450A).



NOTE: Dimensions are in millimeters.

Figure 15-1. 30-SDIP-400 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 15-2. 30-SOP-450A Package Dimensions

16 KS57P01504 OTP

OVERVIEW

The KS57P01504 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C01502/C01504 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS57P01504 is fully compatible with the KS57C01502/C0504, both in function and in pin configuration. Because of its simple programming requirements, the KS57P01504 is ideal for use as an evaluation chip for the KS57C01502/C01504.

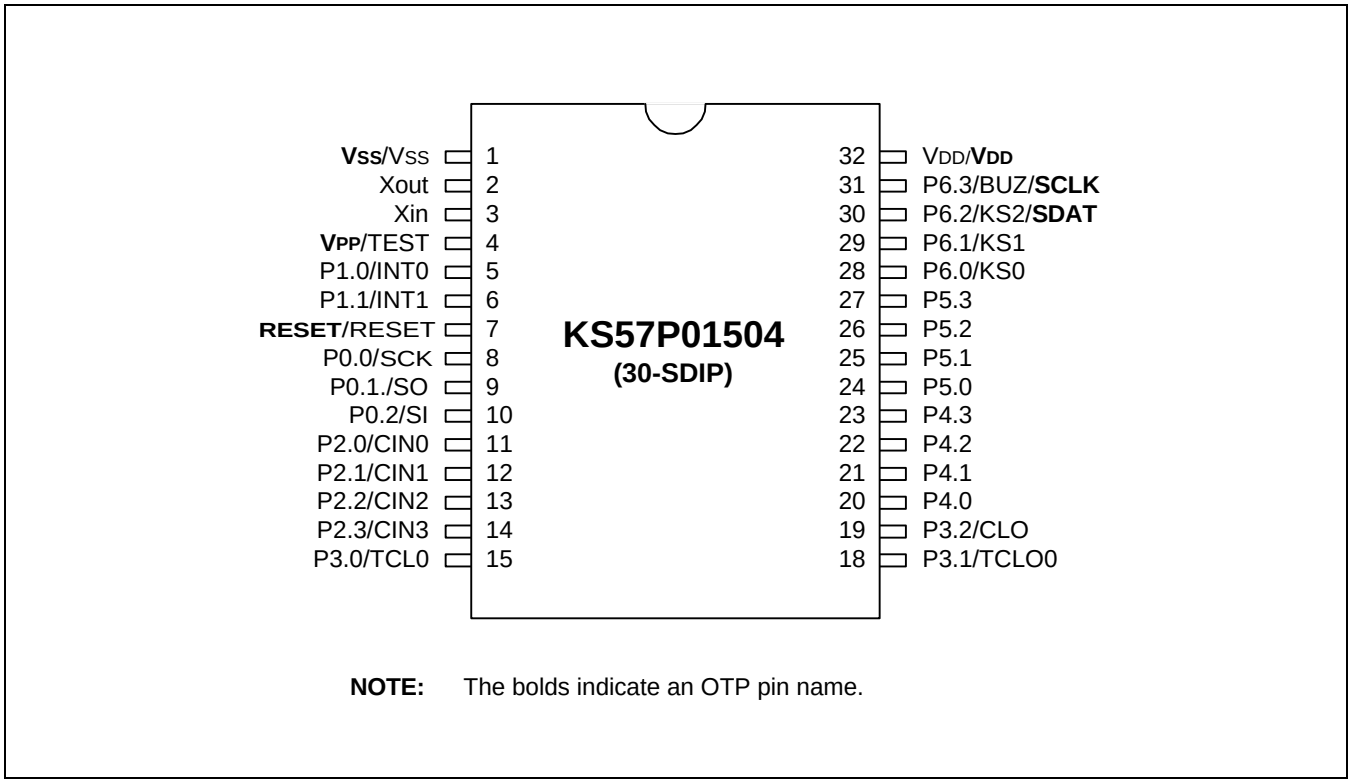
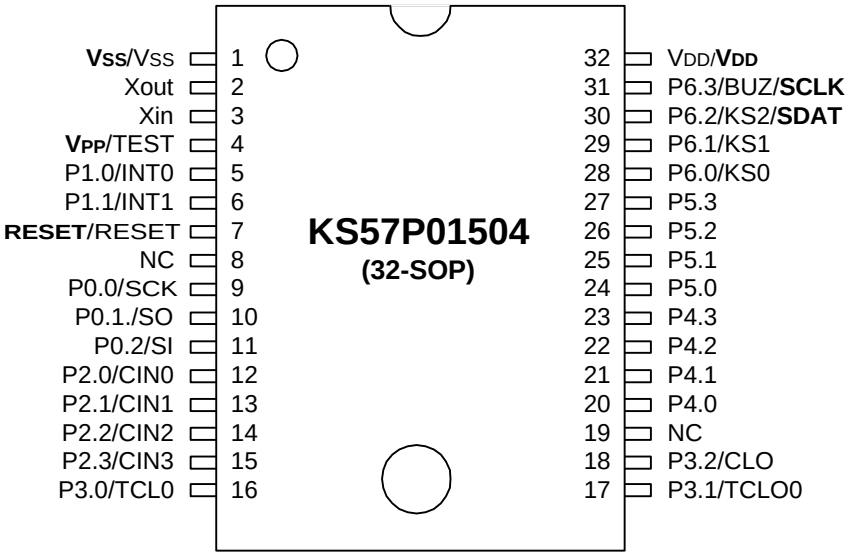


Figure 16-1. KS57P01504 Pin Assignments (30-SDIP Package)



NOTE: The bolds indicate an OTP pin name.

Figure 16-2. KS57P01504 Pin Assignments (32-SOP Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P6.2	SDAT	28 (30)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P6.3	SCLK	29 (31)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	4 (4)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	7 (7)	I	Chip initialization
V_{DD} / V_{SS}	V_{DD} / V_{SS}	30/1 (32/1)	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: ( ) means the 32-SOP OTP pin number.

Table 16-2. Comparison of KS57P01504 and KS57C01502/C01504 Features

Characteristic	KS57P01504	KS57C01502/C01504
Program Memory	4 K-byte EPROM	2 K-byte mask ROM: KS57C01502 4 K-byte mask ROM: KS57C01504
Operating Voltage (V_{DD})	2.0 V to 5.5 V	1.8 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	–
Pin Configuration	30 SDIP, 32 SOP	30 SDIP, 32 SOP
EPROM Programmability	User Program one time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the KS57P0504, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16–3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	VPP (TEST)	REG/ MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

OTP ELECTRICAL DATA

Table 16-4. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 5	mA
		All I/O ports active	– 15	
Output Current Low	I_{OL}	Ports 0, 3, and 6	5	mA
		Ports 4 and 5	30	
		All ports, total	+ 100	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

Table 16-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 4 and 5	0.7V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 3, 6, and RESET	0.8V_{DD}	–	V_{DD}	
	V_{IH3}	X_{in} and X_{out}	V_{DD} – 0.1	–	V_{DD}	
Input Low Voltage	V_{IL1}	Ports 4 and 5	–	–	0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 2, 3, 6, and RESET			0.2V_{DD}	
	V_{IL3}	X_{in} and X_{out}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 3, 4, 5, 6	V_{DD} - 1.0	–	–	V

Table 16-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4, 5	–	–	2	V
		V_{DD} = 4.5 V to 5.5 V I_{OL} = 4.0mA All output pins except Ports 4, 5		–	2	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{in} and X_{out}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{in} and X_{out}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{in}, X_{out} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{in} and X_{out}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V	–	–	– 3	µA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V Port 0, 1, 3, 4, 5, 6	25	50	100	kΩ
		V_{DD} = 3 V	50	100	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	250	400	
		V_{DD} = 3 V	200	500	800	

Table 16-5. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.0	8.0	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		2.0	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.3	4.0	
			4.19MHz		1.0	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	0.8	2.5	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		0.6	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.6	1.5	
			4.19MHz		0.4	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.5	3.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.3	2.0	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers, output port drive currents and comparator.
2. The supply current assumes a CPU clock of fx/4.

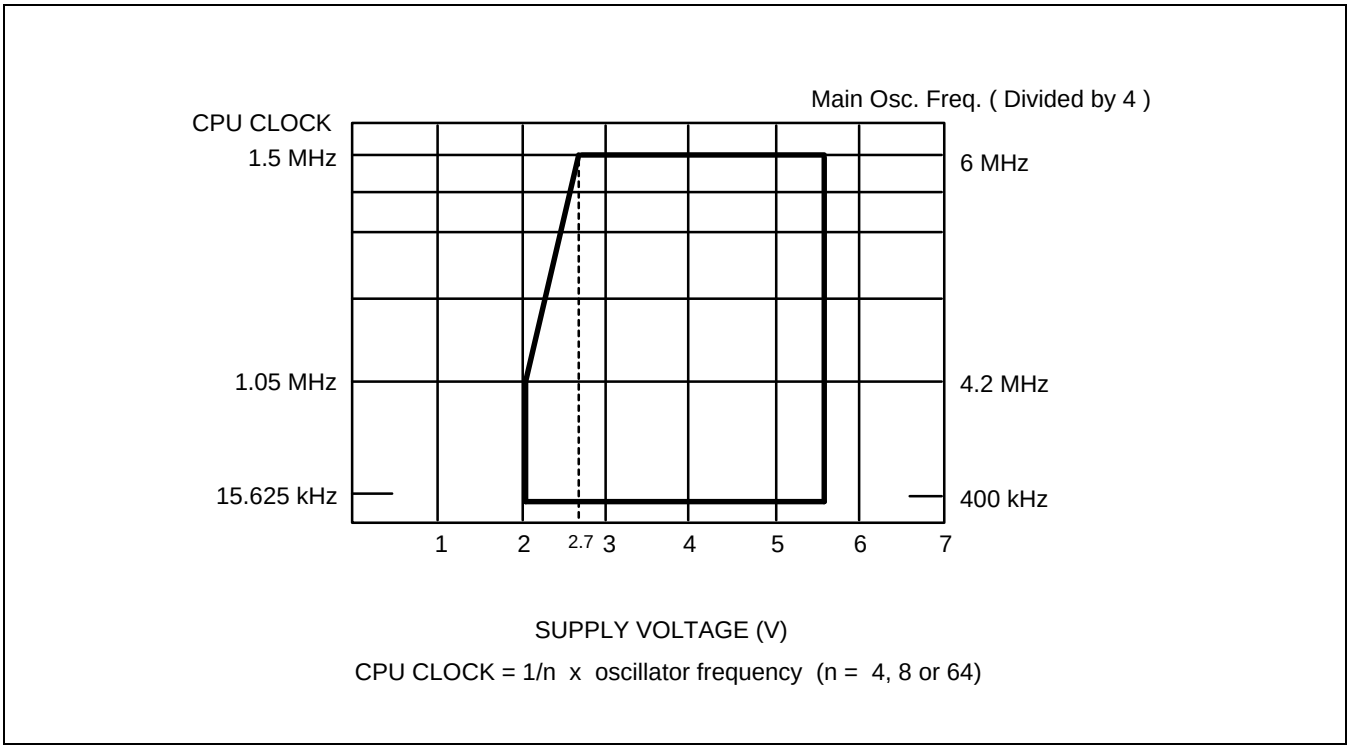
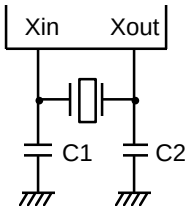
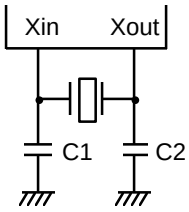
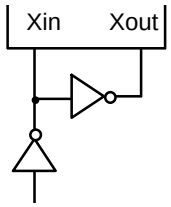


Figure 16-3. Standard Operating Voltage Range

Table 16-6. Oscillators Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{in} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-7. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}				15	pF
I/O Capacitance	C_{IO}				15	pF

Table 16-8. Comparator Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.5V, V_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	–	–	0	–	V_{DD}	V
Reference Voltage Range	V_{REF}	–	0	–	V_{DD}	V
Input Voltage Accuracy	V_{CIN}	–	–	–	±150	mV
Input Leakage Current	I_{CIN}, I_{REF}	–	– 3	–	3	µA

Table 16-9. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 2.0 V to 5.5 V	0.95			
TCL0 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 2.0 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 2.0 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	670			
		V_{DD} = 2.0 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			

Table 16-9. A.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	ns
		Internal SCK source	t_{KCY}/2 - 50			
		V_{DD} = 2.0 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}/2 - 150			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 2.0 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 2.0 V to 5.5 V External SCK source	600			
		Internal SCK source	500			
Output Delay for SCK to SO	t_{KSO} (1)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 2.0 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, KS0–KS2	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES:

1. R(1Kohm) and C (100pF) are the load resistance and load capacitance of the SO output line.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

Table 16-10. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

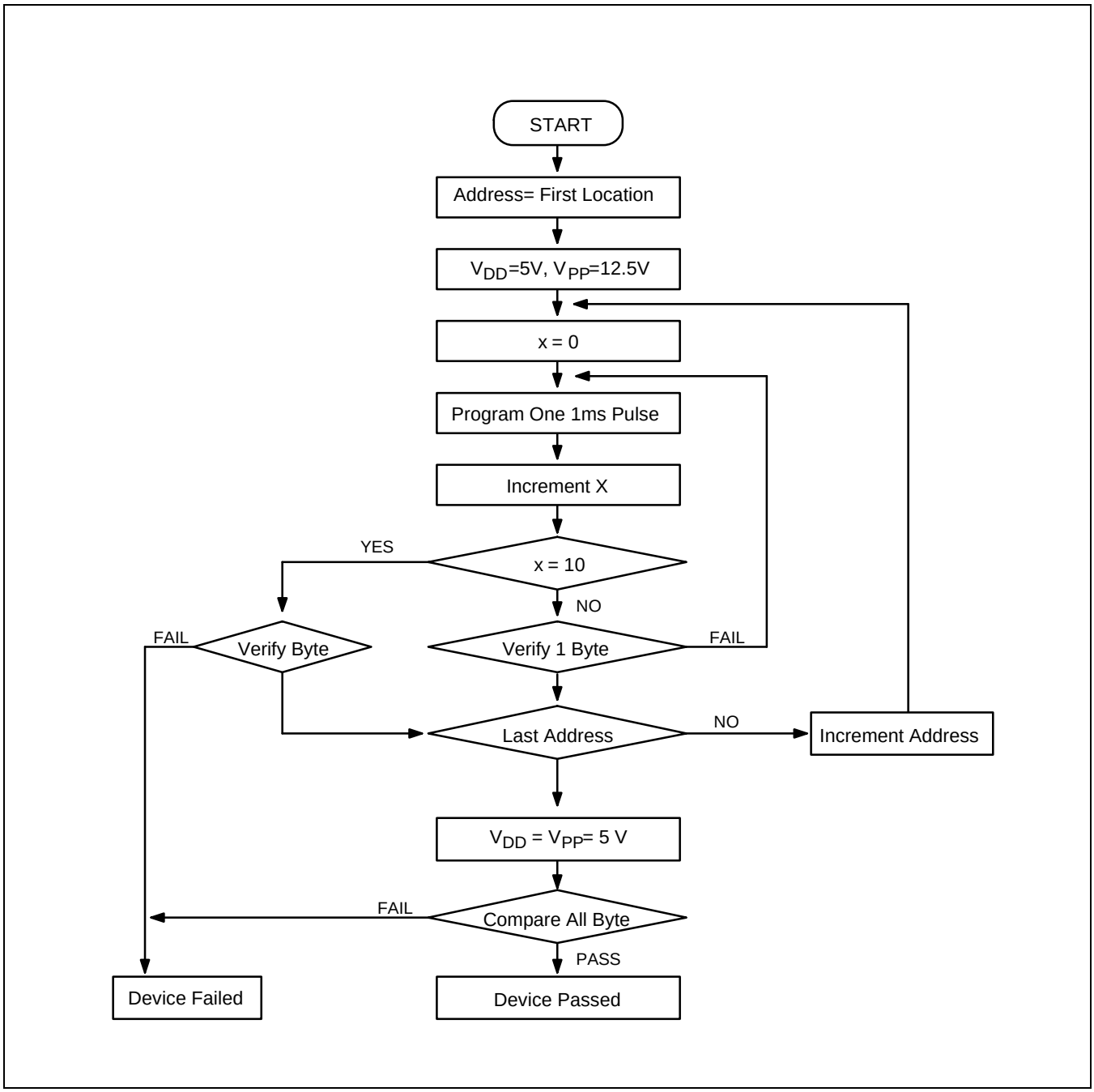


Figure 16-4. OTP Programming Algorithm