

2N5518

DIFFERENTIAL PAIRS N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise noted)

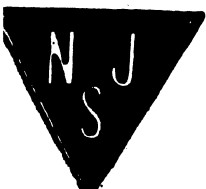
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (each side), $T_A = 85^\circ\text{C}$, (derate 2.0 mW/°C)	250 mW
Total Device Dissipation, $T_A = 85^\circ\text{C}$, (derate 3.0 mW/°C)	375 mW
Storage Temperature Range	-65 to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Test Conditions		Min	Max	Unit
I _{GSS}	Gate Reverse Current	V _{GS} = -30 V, V _{DS} = 0	25 ° C		-250	pA
			150 ° C		-250	nA
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1 μA, V _{DS} = 0		-40		V
V _P	Gate-Source Pinch-Off Voltage	V _{DS} = 20 V, I _D = 1 nA		-0.7	-4	V
I _{DSS}	Drain Current at Zero Gate Voltage †	V _{DS} = 20 V, V _{GS} = 0		0.5	7.5	mA
g _{fs}	Common-Source Forward Transconductance †		f = 1 kHz	1000	4000	μmho
g _{oss}	Common-Source Output Conductance				10	μmho
C _{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		5	pF
C _{iss}	Common-Source Input Capacitance				25	pF
ē _n	Equivalent Input Noise Voltage	V _{DG} = 20 V, I _D = 200 μA	f = 10 Hz	30		nV √Hz
			f = 1 kHz		10	
I _G	Gate Current		25 ° C		-100	pA
			125 ° C		-100	nA
V _{GS}	Gate Source Voltage			-0.2	-3.8	V
g _{fs}	Common-Source Forward Transconductance †		f = 1 kHz	500	1000	μmho
g _{oss}	Common-Source Output Conductance				1	μmho

*JEDEC Registered Data

† Pulse test required, pulsewidth 300 μs , duty cycle $\leq 3\%$



*MATCHING CHARACTERISTICS

Characteristic		Test Conditions			Unit	
			Min	Max		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage †	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ $V_{DG} = 20 \text{ V},$ $I_D = 200 \mu\text{A}$	0.95	1	--	
$ I_{G1} - I_{G2} $	Differential Gate Current		125 °C	10	nA	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio †		f = 1 kHz	0.95	1	--
$ g_{oss1} - g_{oss2} $	Differential Output Conductance		f = 1 kHz	0.1	μmho	
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage			15	mV	
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift †		T _A = 25 °C T _B = 125 °C	40	μV/°C	
			T _A = -55 °C T _B = 25 °C	40	μV/°C	
CMRR	Common Mode Rejection Ratio **	$V_{DD} = 10 \text{ to } 20 \text{ V},$ $I_D = 200 \mu\text{A}$			dB	

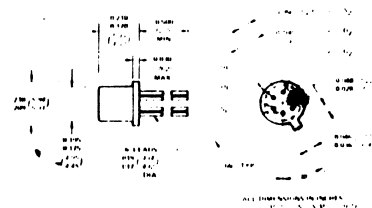
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† Pulse test required, pulsewidth 300 μs , duty cycle = 3%

‡ Measured at end points, T_A and T_B .

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**CMRR = $20 \log_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$, ($\Delta V_{DD} = 10\text{V}$)



All leads isolated from case