

## 4-Mbit (256K words × 16 bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)

### Features

- High speed
  - Access time ( $t_{AA}$ ) = 10 ns / 15 ns
- Ultra-low power Deep-Sleep (DS) current
  - $I_{DS}$  = 15  $\mu$ A
- Low active and standby currents
  - Active Current  $I_{CC}$  = 38-mA typical
  - Standby Current  $I_{SB2}$  = 6-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- 1.0-V data retention
- TTL- compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 44-pin TSOP II and 48-ball VFBGA

### Functional Description

The CY7S1041G is a high-performance PowerSnooze™ static RAM organized as 256K words × 16 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep-Sleep mode. With Deep-Sleep mode currents as low as 15  $\mu$ A, the CY7S1041G/ CY7S1041GE devices combine the best features of fast and low- power SRAMs in industry-standard package options. The device also features embedded ECC. logic which can detect and correct single-bit errors in the accessed location.

Deep-Sleep input ( $\overline{DS}$ ) must be deasserted HIGH for normal operating mode.

To perform data writes, assert the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, and provide the data and address on device data pins ( $I/O_0$  through  $I/O_{15}$ ) and address pins ( $A_0$  through  $A_{17}$ ) respectively. The Byte High Enable ( $\overline{BHE}$ ) and Byte Low Enable ( $\overline{BLE}$ ) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified.  $\overline{BHE}$  controls  $I/O_8$  through  $I/O_{15}$  and  $\overline{BLE}$  controls  $I/O_0$  through  $I/O_7$ .

To perform data reads, assert the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and provide the required address on the address lines. Read data is accessible on the I/O lines ( $I/O_0$  through  $I/O_{15}$ ). You can perform byte accesses by asserting the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location

The device is placed in a low-power Deep-Sleep mode when the Deep-Sleep input ( $\overline{DS}$ ) is asserted LOW. In this state, the device is disabled for normal operation and is placed in a low power data retention mode. The device can be activated by deasserting the Deep-Sleep input ( $\overline{DS}$ ) to HIGH.

The CY7S1041G is available in 44-pin TSOP II, 48-ball VFBGA and 44-pin (400-mil) Molded SOJ.

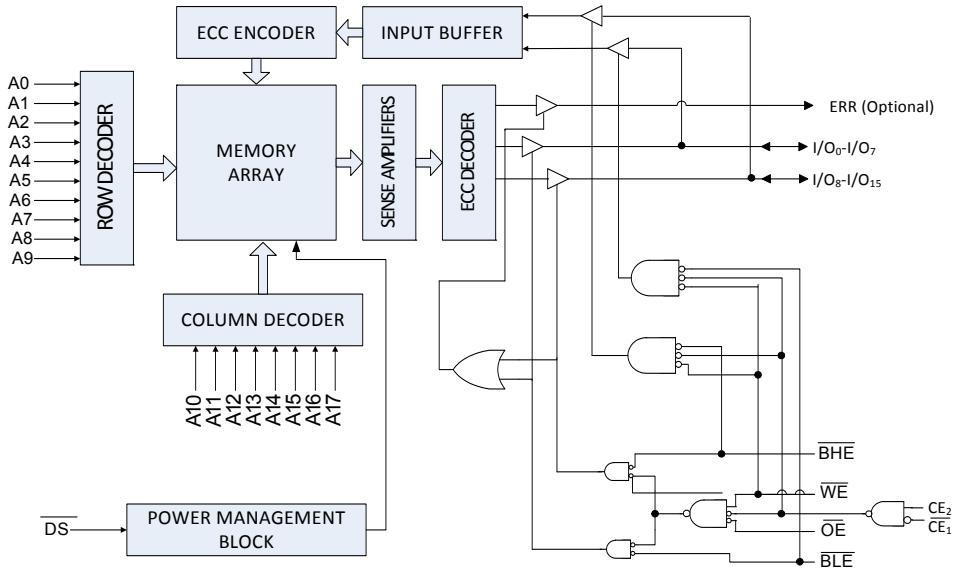
### Product Portfolio

Product <sup>[2]</sup>	Range	$V_{CC}$ Range (V)	Speed (ns)	Power Dissipation							
				Operating $I_{CC}$ , (mA)		Standby, $I_{SB2}$ (mA)		Deep-Sleep current ( $\mu$ A)			
				$f = f_{max}$		Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
				Typ <sup>[3]</sup>	Max						
CY7S1041G(E)18	Industrial	1.65 V–2.2 V	15	–	40	6	8	–	15		
CY7S1041G(E)30		2.2 V–3.6 V	10	38	45						
CY7S1041G(E)		4.5–5.5 V	10	38	45						

#### Notes

1. This device does not support automatic write back on error detection.
2. ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer [Ordering Information](#) for details.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for  $V_{CC}$  range of 1.65 V – 2.2 V),  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V – 3.6 V), and  $V_{CC} = 5$  V (for  $V_{CC}$  range of 4.5 V – 5.5 V),  $T_A = 25^\circ\text{C}$ .

**Logic Block Diagram – CY7S1041G / CY7S1041GE**

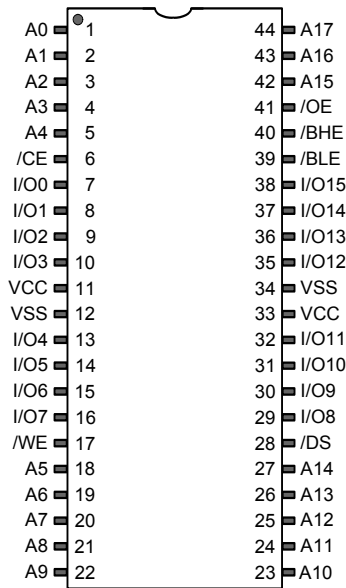


## Contents

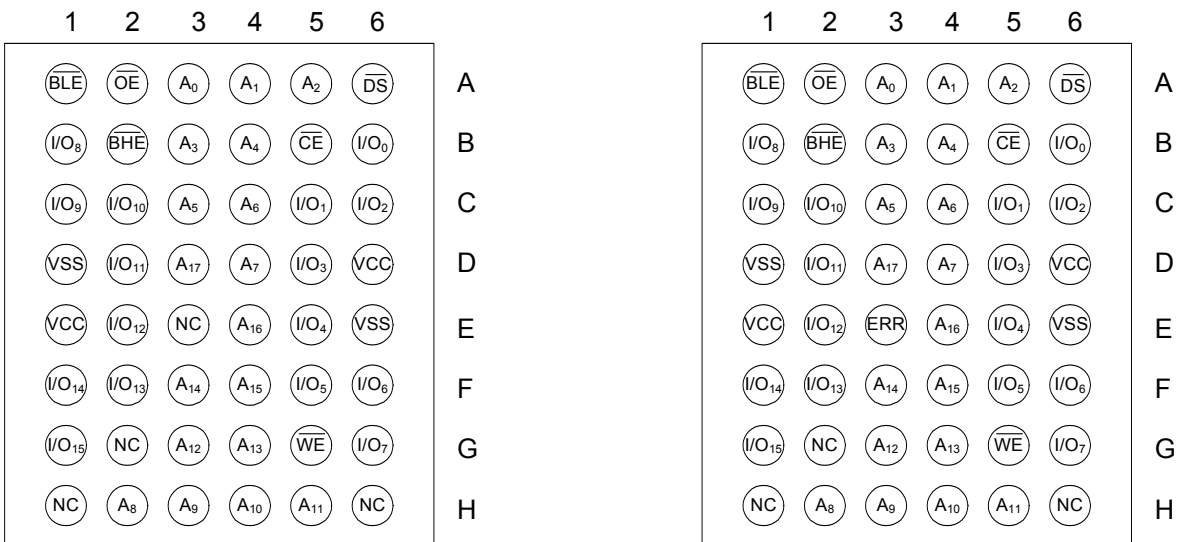
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## Pin Configurations

**Figure 1. 44-pin TSOP II pinout, CY7S1041G**



**Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7S1041G [4], Package/Grade ID: BVJXI [6]**      **Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7S1041GE [4, 5], Package/Grade ID: BVJXI [6]**

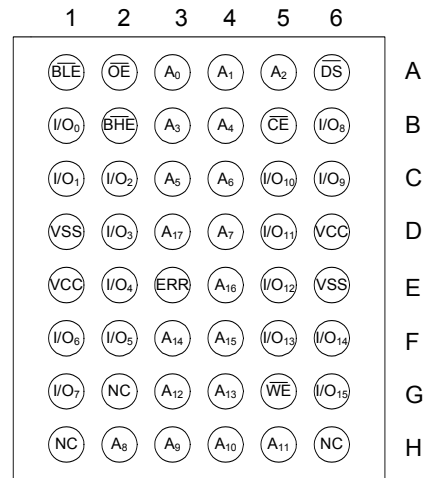
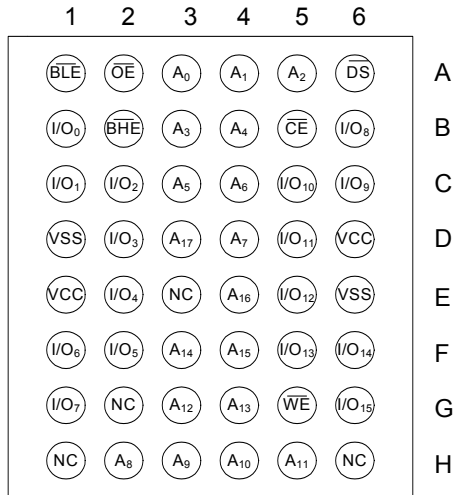


**Notes**

- 4. NC pins are not connected internally to the die.
- 5. ERR is an output pin.
- 6. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O<sub>[7:0]</sub> and I/O<sub>[15:8]</sub> balls are swapped.

**Pin Configurations** (continued)

**Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7S1041G [7], Package/Grade ID: BVXI [9]**      **Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7S1041GE [7, 8], Package/Grade ID: BVXI [9]**



**Notes**

7. NC pins are not connected internally to the die.
8. ERR is an output pin.
9. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O<sub>[7:0]</sub> and I/O<sub>[15:8]</sub> balls are swapped).

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature  
 with power applied ..... -55 °C to +125 °C  
 Supply voltage  
 on V<sub>CC</sub> relative to GND <sup>[10]</sup> ..... -0.5 V to + 6.0 V  
 DC voltage applied to outputs  
 in HI-Z State <sup>[10]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage <sup>[10]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage  
 (MIL-STD-883, Method 3015) ..... > 2001 V  
 Latch-up current ..... > 140 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the Operating Range of -40 °C to +85 °C

Parameter	Description	Test Conditions	10 ns/ 15 ns			Unit	
			Min	Typ <sup>[11]</sup>	Max		
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2	-	-	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.2	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> -0.5 <sup>[13]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA	-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
		3.6 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
V <sub>IH</sub> <sup>[10, 12]</sup>	Input HIGH voltage	1.65 V to 2.2 V		1.4	-	V <sub>CC</sub> + 0.2	V
		2.2 V to 2.7 V		2	-	V <sub>CC</sub> + 0.3	
		2.7 V to 3.6 V		2	-	V <sub>CC</sub> + 0.3	
		3.6 V to 5.5 V		2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub> <sup>[10, 12]</sup>	Input LOW voltage	1.65 V to 2.2 V		-0.2	-	0.4	V
		2.2 V to 2.7 V		-0.3	-	0.6	
		2.7 V to 3.6 V		-0.3	-	0.8	
		3.6 V to 5.5 V		-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz	-	38	45	mA
			f = 66.7 MHz	-	40	40	
I <sub>SB1</sub>	Standby current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	-	15	mA	
I <sub>SB2</sub>	Standby current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	6	8	mA	
I <sub>DS</sub>	Deep-Sleep current	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \leq 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	-	15	μA	

### Notes

- V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V for pulse durations of less than 2 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V – 2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2V – 3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V – 5.5 V), T<sub>A</sub> = 25 °C.
- For the  $\overline{DS}$  pin, V<sub>IH</sub> (min) is V<sub>CC</sub> - 0.2 V and V<sub>IL</sub> (max) is 0.2 V.
- This parameter is guaranteed by design and not tested.

## Capacitance

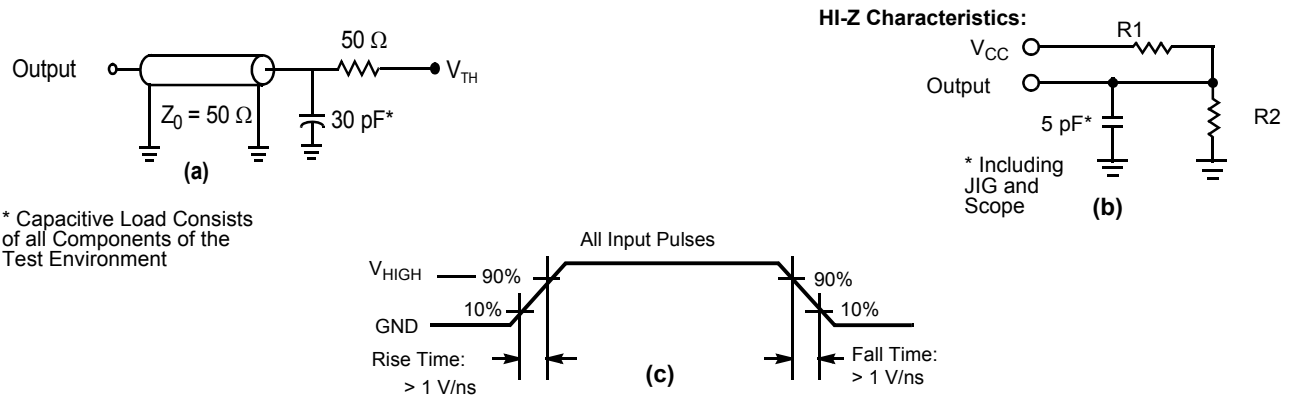
Parameter <sup>[14]</sup>	Description	Test Conditions	All packages	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> (typ)	10	pF
C <sub>OUT</sub>	I/O capacitance		10	pF

## Thermal Resistance

Parameter <sup>[14]</sup>	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	31.35	68.85	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		14.74	15.97	°C/W

## AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms <sup>[15]</sup>



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	V <sub>CC</sub> /2	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3.0	3.0	V

### Notes

14. Tested initially and after any design or process changes that may affect these parameters.
15. Full-device AC operation assumes a 100-μs ramp time from 0 to V<sub>CC</sub>(min) or 100-μs wait time after V<sub>CC</sub> stabilization.

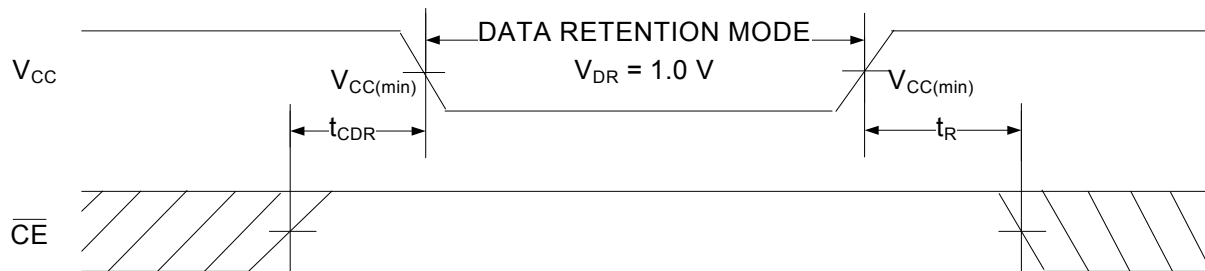
## Data Retention Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions <sup>[16]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{DS} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}^{[17]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[17, 18]}$	Operation recovery time	$2.2\text{ V} < V_{CC} \leq 5.5\text{ V}$	10	–	ns
		$V_{CC} \leq 2.2\text{ V}$	15	–	ns

## Data Retention Waveform

Figure 7. Data Retention Waveform <sup>[18]</sup>



### Notes

16.  $\overline{DS}$  signal must be HIGH during Data Retention Mode.

17. These parameters are guaranteed by design

18. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .

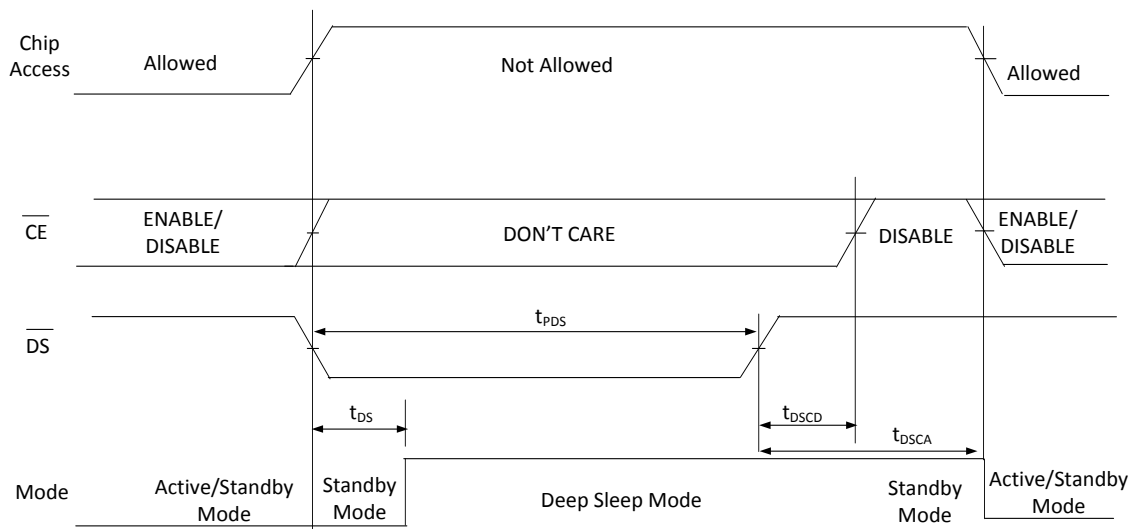


## Deep-Sleep Mode Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$I_{DS}$	Deep-Sleep mode current	$V_{CC} = V_{CC}(\text{max}), \overline{DS} \leq 0.2\text{ V},$ $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	15	$\mu\text{A}$
$t_{PDS}^{[19]}$	Minimum time for $\overline{DS}$ to be LOW for part to successfully exit Deep-Sleep mode		100	–	ns
$t_{DS}^{[20]}$	$\overline{DS}$ assertion to Deep-Sleep mode transition time		–	1	ms
$t_{DSCD}^{[19]}$	$\overline{DS}$ deassertion to chip disable	If $t_{PDS} \geq t_{PDS(\text{min})}$	–	100	$\mu\text{s}$
		If $t_{PDS} < t_{PDS(\text{min})}$	–	0	$\mu\text{s}$
$t_{DSCA}$	$\overline{DS}$ deassertion to chip access (Active/Standby)	If $t_{PDS} \geq t_{PDS(\text{min})}$	300	–	$\mu\text{s}$
		If $t_{PDS} < t_{PDS(\text{min})}$			

**Figure 8. Active, Standby, and Deep-Sleep Operation Modes**



**Note**

19.  $\overline{CE}$  must be pulled HIGH within  $t_{DSCD}$  time of  $\overline{DS}$  deassertion to avoid SRAM data loss.

20. After assertion of  $\overline{DS}$  signal, device will take a maximum of  $t_{DS}$  time to stabilize to Deep-Sleep current  $I_{DS}$ . During this period,  $\overline{DS}$  signal must continue to be asserted to logic level LOW to keep the device in Deep-Sleep mode.

## AC Switching Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

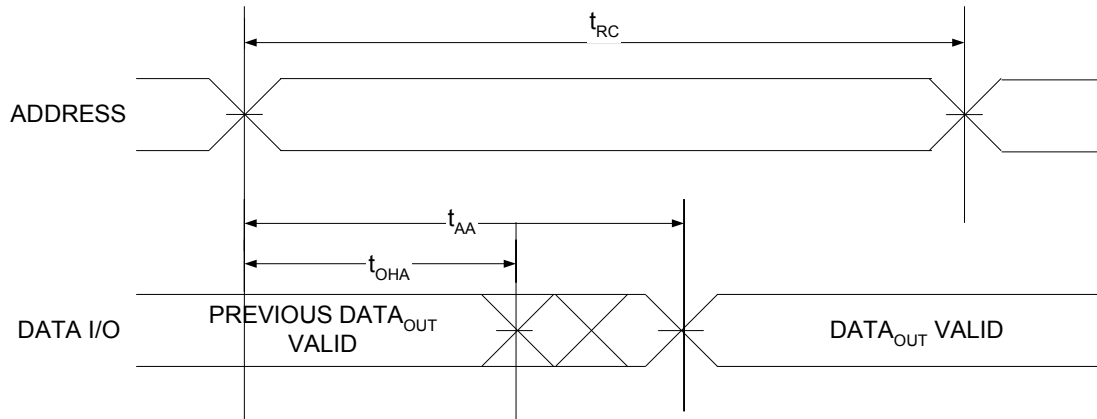
Parameter <sup>[21]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	10	–	15	–	ns
$t_{AA}$	Address to data valid	–	10	–	15	ns
$t_{OHA}$	Data hold from address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	–	15	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	4.5	–	8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low impedance <sup>[22, 23, 24]</sup>	0	–	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low impedance <sup>[22, 23, 24]</sup>	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[24]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[24]</sup>	–	10	–	15	ns
$t_{DBE}$	Byte enable to data valid	–	4.5	–	8	ns
$t_{LZBE}$	Byte enable to low impedance <sup>[22, 23, 24]</sup>	0	–	0	–	ns
$t_{HZBE}$	Byte disable to HI-Z <sup>[22, 23, 24]</sup>	–	6	–	8	ns
<b>Write Cycle <sup>[25, 26]</sup></b>						
$t_{WC}$	Write cycle time	10	–	15	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7	–	12	–	ns
$t_{AW}$	Address setup to write end	7	–	12	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	12	–	ns
$t_{SD}$	Data setup to write end	5	–	8	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low impedance <sup>[22, 23, 24]</sup>	3	–	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns
$t_{BW}$	Byte Enable to End of Write	7	–	12	–	ns

### Notes

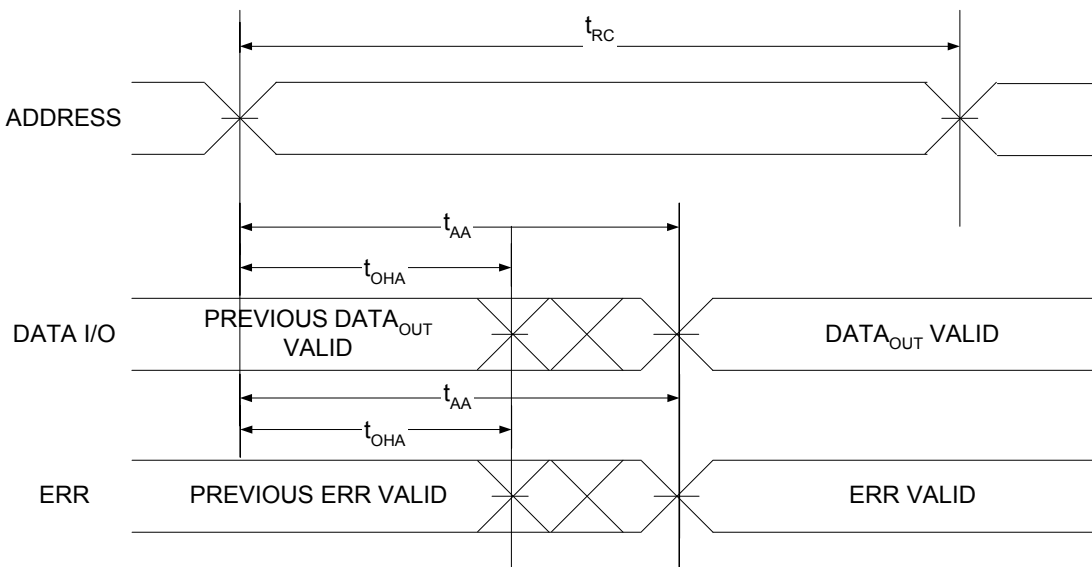
- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3\text{ V}$ ) and  $V_{CC}/2$  (for  $V_{CC} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3\text{ V}$ ) and 0 to  $V_{CC}$  (for  $V_{CC} < 3\text{ V}$ ). Test conditions for the read cycle use output loading shown in part (a) of Figure 6 on page 7, unless specified otherwise.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of Figure 6 on page 7. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- These parameters are guaranteed by design
- The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{DS} = V_{IH}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ .  $\overline{WE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and  $\overline{BLE}$  signals must be LOW and  $\overline{DS}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{WE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and  $\overline{BLE}$  signals or LOW transition on  $\overline{DS}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 9. Read Cycle No. 1 of CY7S1041G (Address Transition Controlled)** [27, 28, 29]



**Figure 10. Read Cycle No. 2 of CY7S1041GE (Address Transition Controlled)** [27, 28, 29]

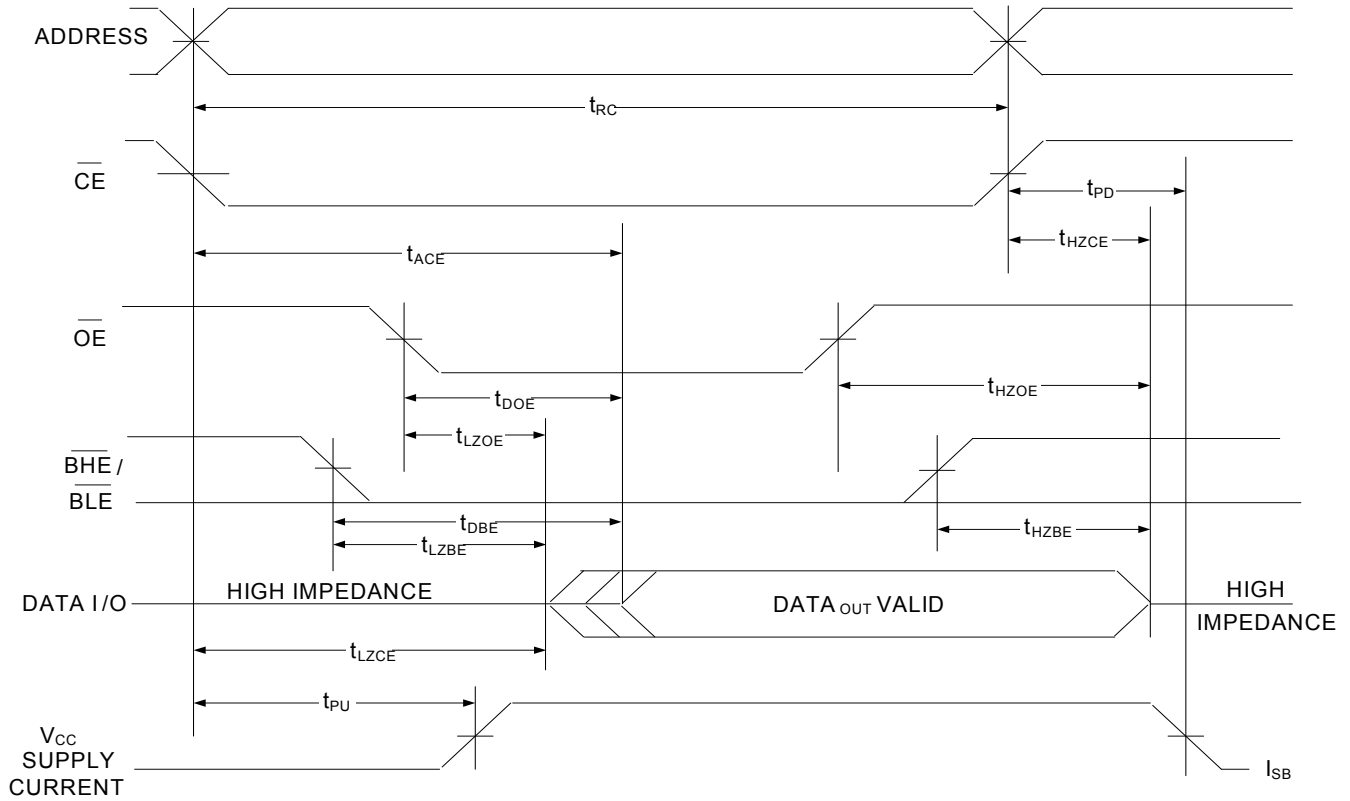


### Notes

- 27. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .
- 28.  $\overline{WE}$  is HIGH for read cycle.
- 29.  $\overline{DS}$  is HIGH for chip access.

**Switching Waveforms** (continued)

**Figure 11. Read Cycle No. 3 ( $\overline{\text{OE}}$  Controlled)** [30, 31, 32]

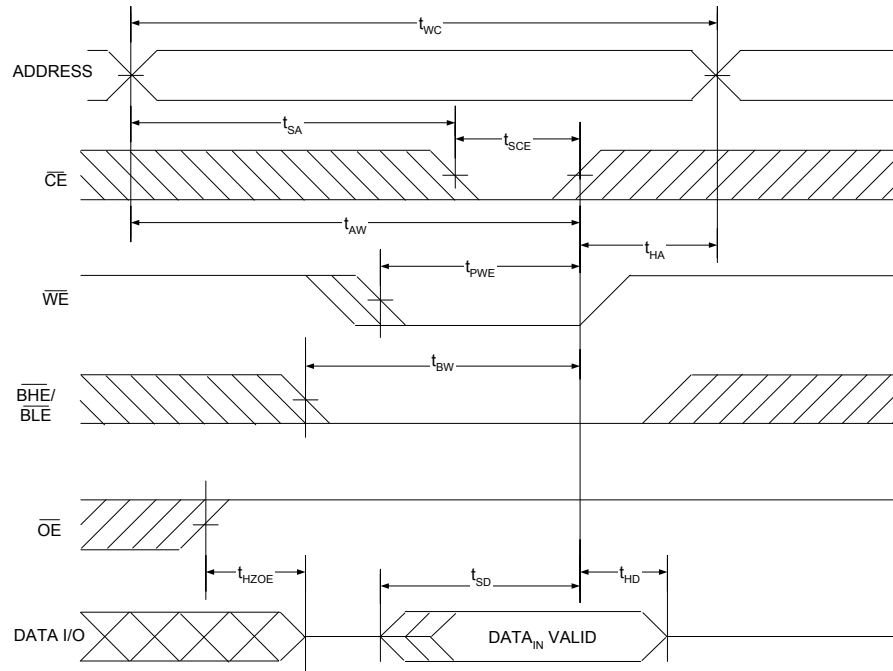


**Notes**

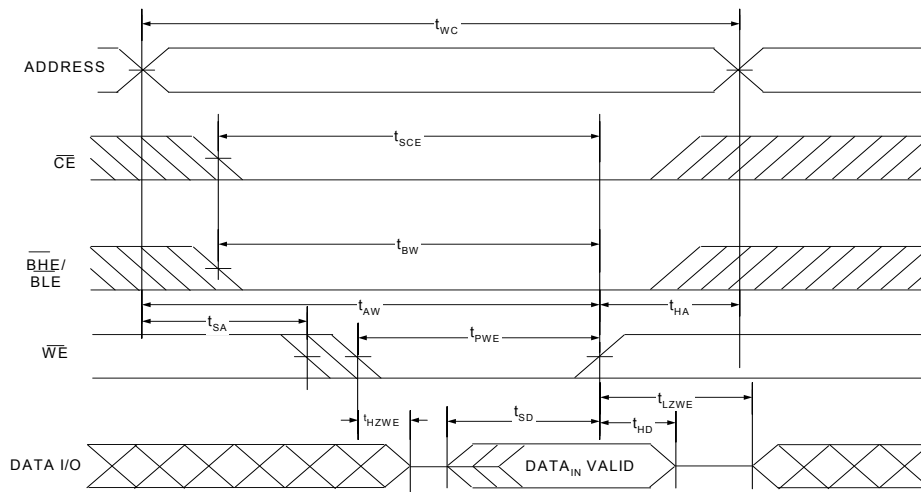
- 30.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 31. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.
- 32.  $\overline{\text{DS}}$  must be HIGH for chip access

**Switching Waveforms** (continued)

**Figure 12. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [33, 34, 35]



**Figure 13. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [33, 34, 35, 36]



**Notes**

33. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{DS}} = V_{IH}$  and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ .  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  signals must be LOW and  $\overline{\text{DS}}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  signals or LOW transition on  $\overline{\text{DS}}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

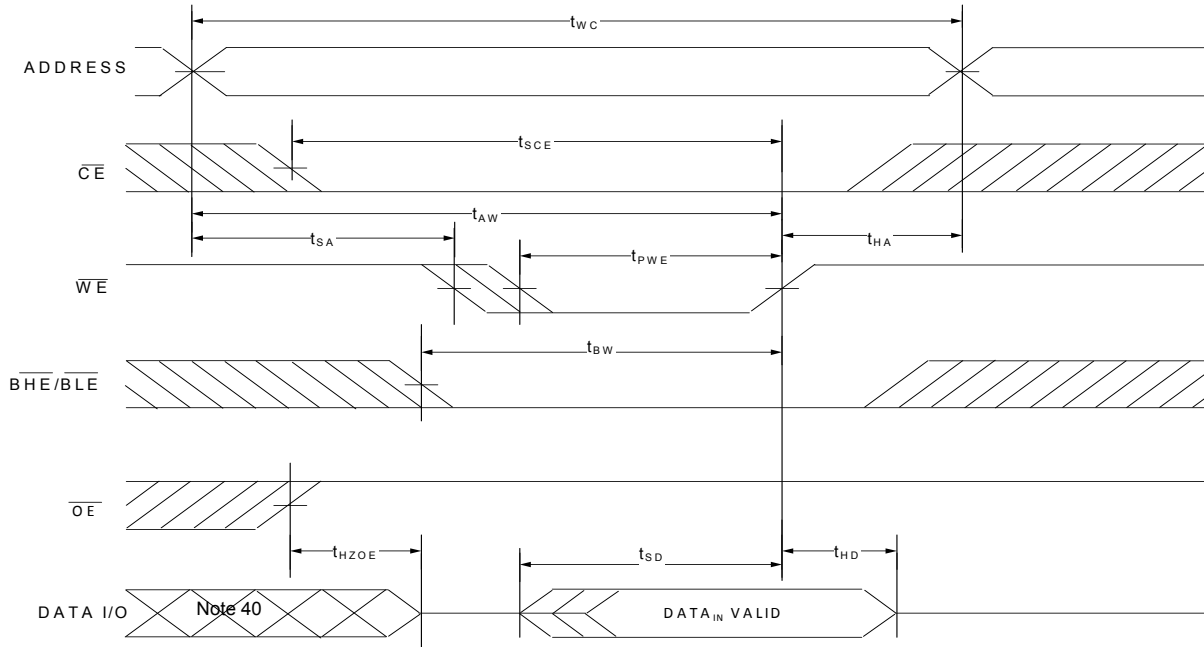
34. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

35.  $\overline{\text{DS}}$  must be HIGH for chip access.

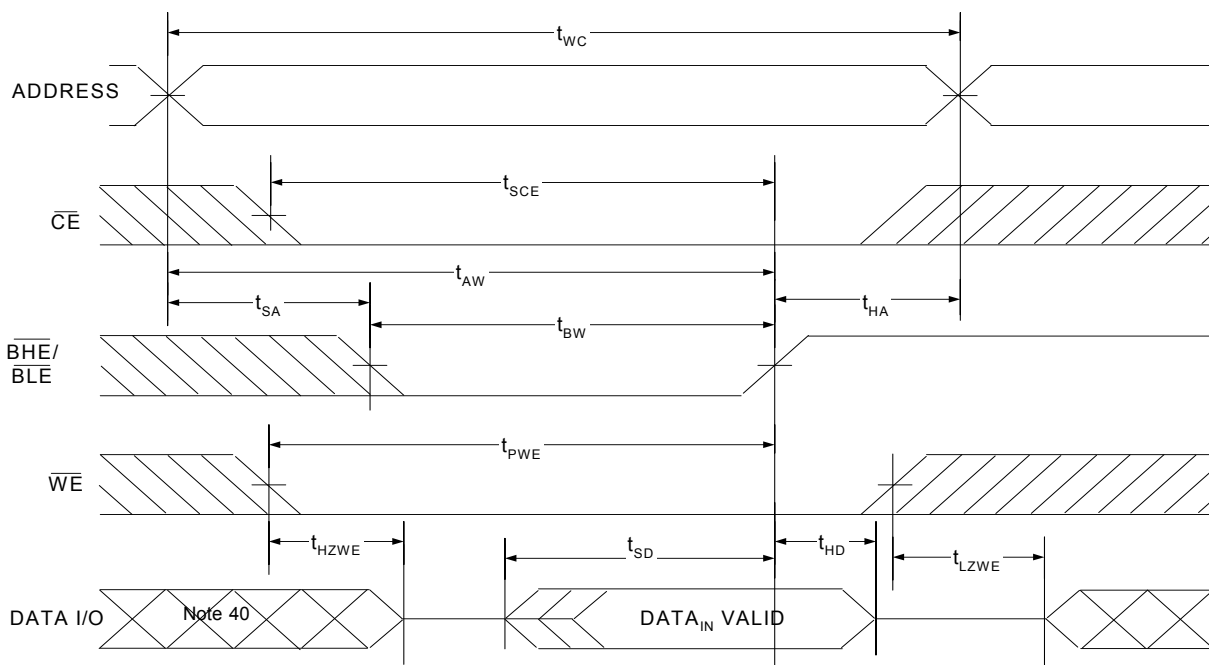
36. The minimum write pulse width for Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms** (continued)

**Figure 14. Write Cycle No. 3 ( $\overline{WE}$  Controlled)** [37, 38, 39]



**Figure 15. Write Cycle No. 4 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)** [37, 38, 39]



**Notes**

37. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{DS} = V_{IH}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ .  $\overline{WE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and  $\overline{BLE}$  signals must be LOW and  $\overline{DS}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{WE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and  $\overline{BLE}$  signals or LOW transition on  $\overline{DS}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

38. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{DS} = V_{IL}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .

39.  $\overline{DS}$  must be HIGH for chip access.

40. During this period, the I/Os are in output state. Do not apply input signals.

### Truth Table

$\overline{DS}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	H	X <sup>[41]</sup>	X <sup>[41]</sup>	X <sup>[41]</sup>	X <sup>[41]</sup>	HIGH-Z	HIGH-Z	Standby	Standby (I <sub>SB</sub> )
H	L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
H	L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I <sub>CC</sub> )
H	L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
H	L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
H	L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I <sub>CC</sub> )
H	L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
H	L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L <sup>[42]</sup>	X	X	X	X	X	HI-Z	HI-Z	Deep-Sleep	Deep-Sleep Ultra Low Power (I <sub>DS</sub> )

### ERR Output – CY7S1041GE

Output <sup>[43]</sup>	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected or outputs disabled or Write operation

#### Notes

41. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

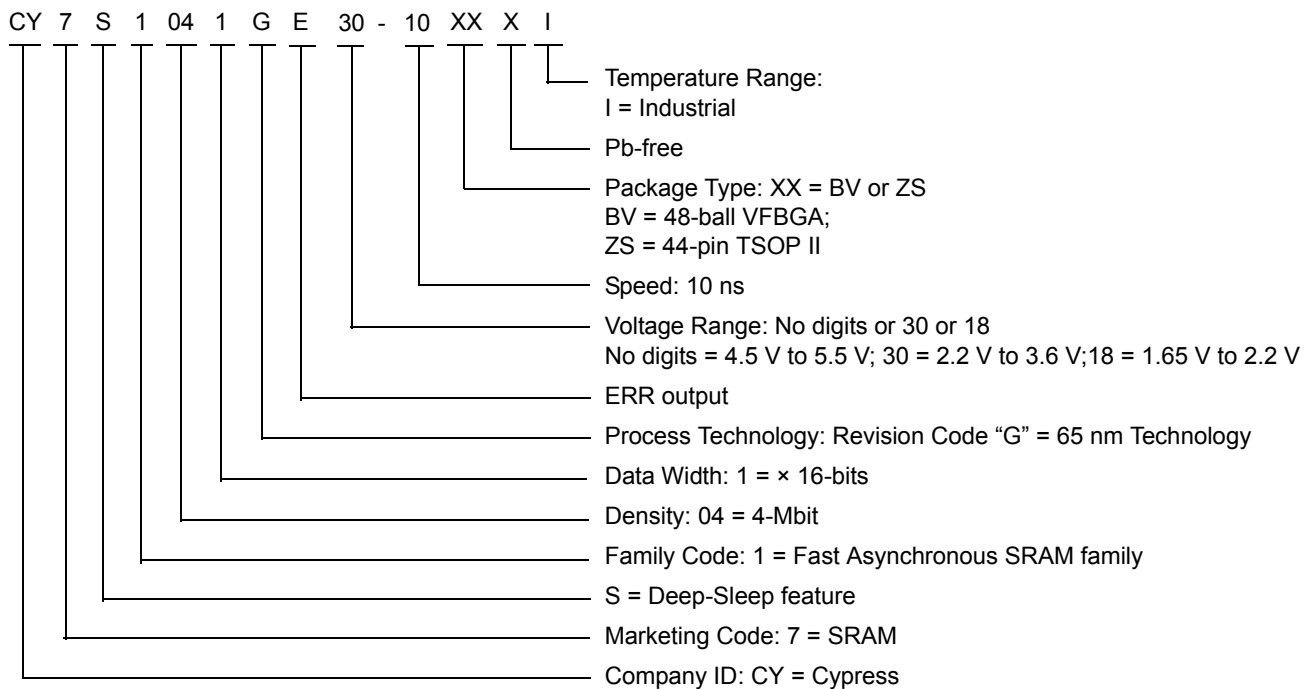
42. V<sub>IL</sub> on  $\overline{DS}$  must be  $\leq 0.2$  V.

43. ERR is an Output pin. If not used, this pin should be left floating.

### Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7S1041GE30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output	Industrial
		CY7S1041G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7S1041G30-10ZSXI	51-85087	44-pin TSOP II	
	4.5 V–5.5 V	CY7S1041G-10ZSXI	51-85087	44-pin TSOP II	

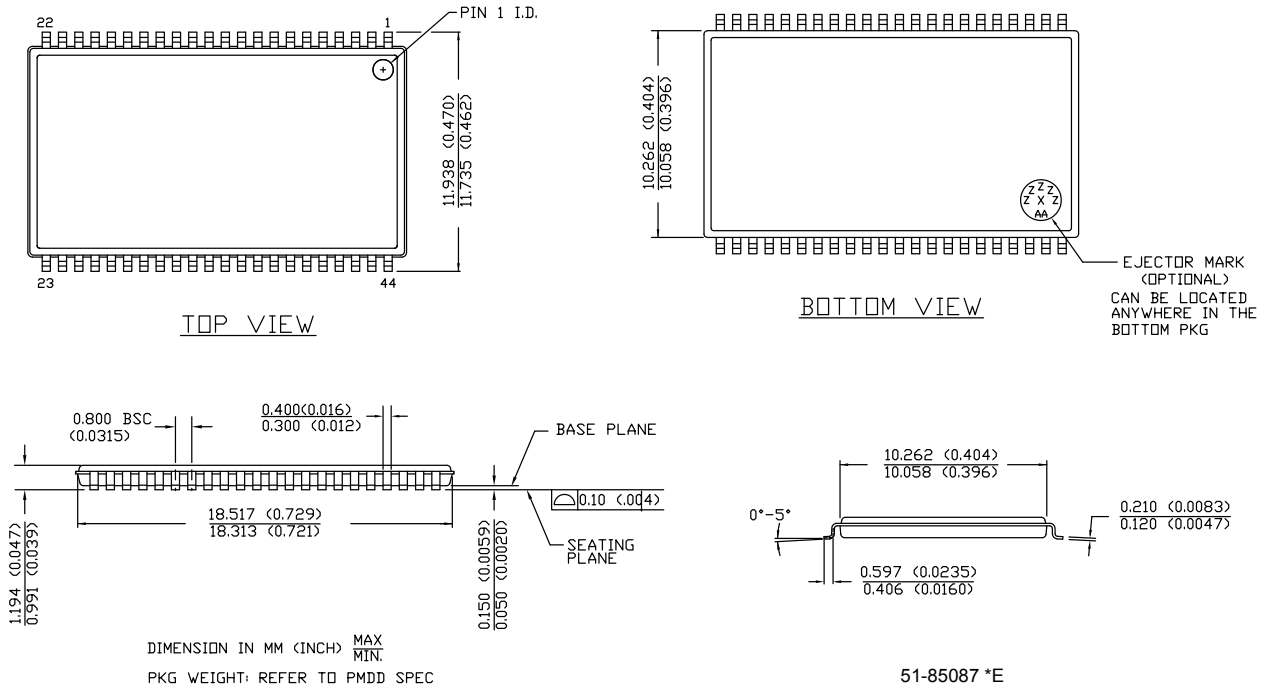
### Ordering Code Definitions





**Package Diagrams**

**Figure 16. 44-pin TSOP II Package Outline, 51-85087**





## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
ECC	Error Correcting Code
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degrees Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7S1041G/CY7S1041GE, 4-Mbit (256K words × 16 bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)				
Document Number: 001-92576				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	4867081	NILE	07/31/2015	Changed status from Preliminary to Final.
*E	5020880	VINI	11/19/2015	Updated <a href="#">Pin Configurations</a> : Removed 44-pin SOJ package related information. Updated <a href="#">Thermal Resistance</a> : Removed 44-pin SOJ package related information. Added 48-ball VFBGA package related information. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> : Removed spec 51-85082 *E.

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