

## FEATURES

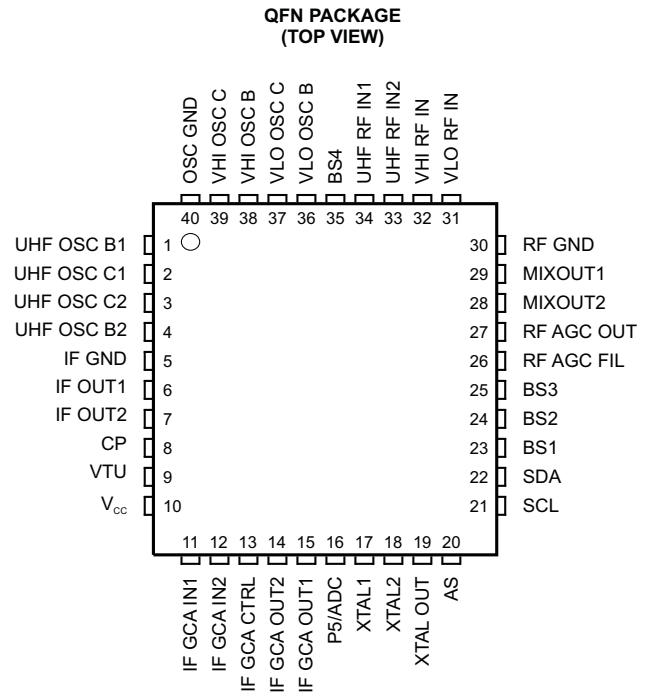
- Integrated Mixer/Oscillator/PLL and IF GCA
- VHF-L, VHF-H, UHF Three-Band Local Oscillator
- RF AGC Detector Circuit
- I<sup>2</sup>C Bus Protocol Bidirectional Data Transmission
- High-Voltage Tuning Voltage Output
- Four NPN-Type Band-Switch Drivers
- One Auxiliary Port/5-Level ADC
- Crystal Oscillator Output
- Programmable Reference Divider Ratio (24/28/50/64/80/128)
- Low Distortion IF Gain Controlled Amplifier
- Standby Mode
- 5-V Power Supply
- 40-Pin Quad Flatpack No-Lead (QFN) Package

## APPLICATIONS

- Digital TV
- Digital CATV
- Set-Top Box

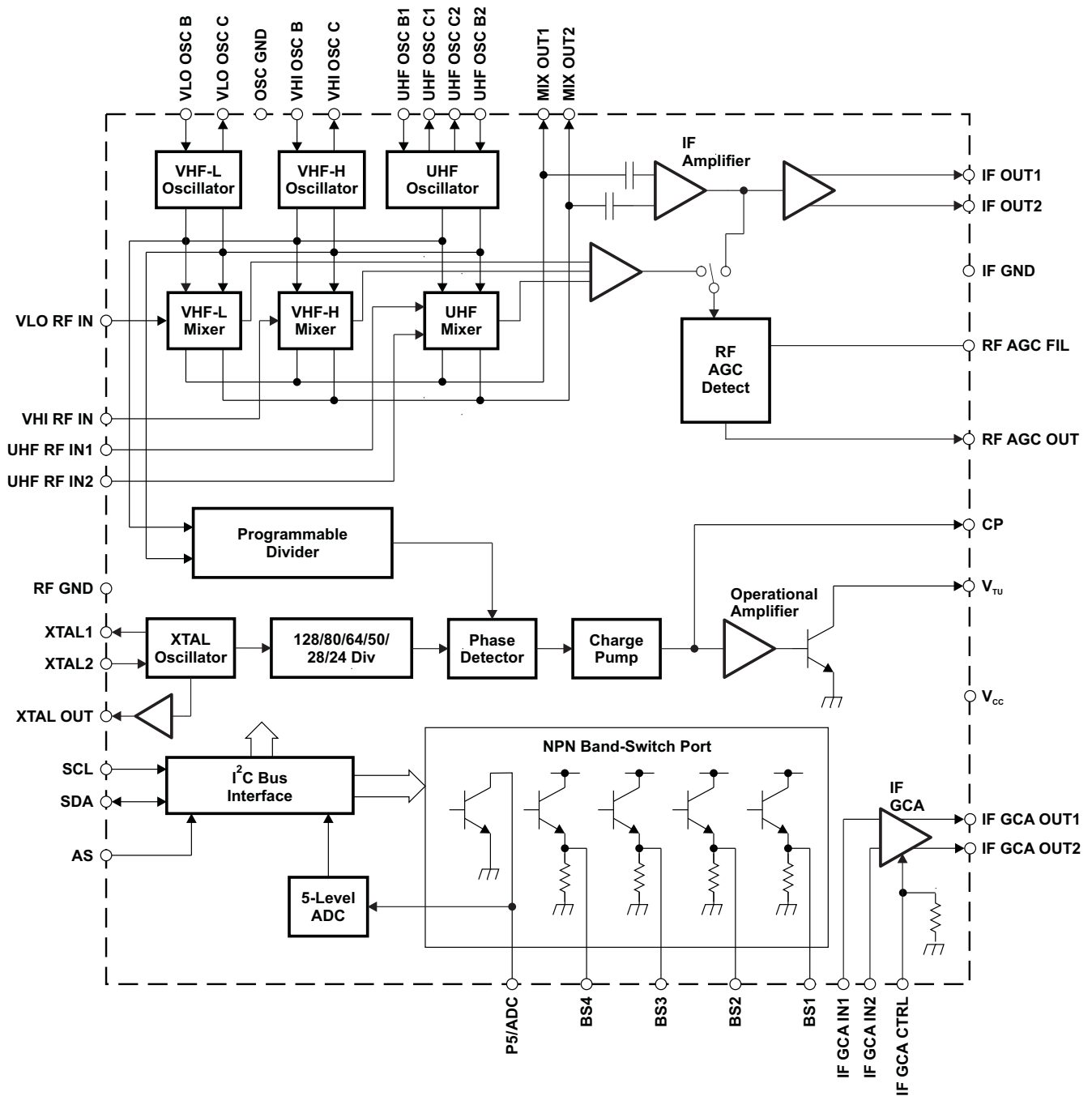
## DESCRIPTION

The SN761667 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, RF AGC detector circuit, and IF gain-controlled amplifier. The SN761667 is available in a small QFN package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

TERMINAL NAME		NO.	DESCRIPTION	SCHEMATIC
AS		20	Address selection input	<a href="#">Figure 1</a>
BS1		23	Band-switch 1 output	<a href="#">Figure 2</a>
BS2		24	Band-switch 2 output	<a href="#">Figure 2</a>
BS3		25	Band-switch 3 output	<a href="#">Figure 2</a>
BS4		35	Band-switch 4 output	<a href="#">Figure 2</a>
CP		8	Charge-pump output	<a href="#">Figure 3</a>
IF GCA CTRL		13	IF GCA CTRL voltage input	<a href="#">Figure 4</a>
IF GCA IN1		11	IF GCA input 1	<a href="#">Figure 5</a>
IF GCA IN2		12	IF GCA input 2	<a href="#">Figure 5</a>
IF GCA OUT1		15	IF GCA output 1	<a href="#">Figure 6</a>
IF GCA OUT2		14	IF GCA output 2	<a href="#">Figure 6</a>
IF GND		5	IF ground	
IF OUT1		6	IF amplifier output 1	<a href="#">Figure 7</a>
IF OUT2		7	IF amplifier output 2	<a href="#">Figure 7</a>
MIX OUT1		29	Mixer output 1	<a href="#">Figure 8</a>
MIX OUT2		28	Mixer output 2	<a href="#">Figure 8</a>
OSC GND		40	Oscillator ground	
P5/ADC		16	Port-5 output/ADC input	<a href="#">Figure 9</a>
RF AGC FIL		26	RF AGC additional capacitor pin	<a href="#">Figure 10</a>
RF AGC OUT		27	RF AGC output	<a href="#">Figure 11</a>
RF GND		30	RF ground	
SCL		21	Serial clock input	<a href="#">Figure 12</a>
SDA		22	Serial data input/output	<a href="#">Figure 13</a>
UHF OSC B1		1	UHF oscillator base 1	<a href="#">Figure 14</a>
UHF OSC B2		4	UHF oscillator base 2	<a href="#">Figure 14</a>
UHF OSC C1		2	UHF oscillator collector 1	<a href="#">Figure 14</a>
UHF OSC C2		3	UHF oscillator collector 2	<a href="#">Figure 14</a>
UHF RF IN1		34	UHF RF input 1	<a href="#">Figure 15</a>
UHF RF IN2		33	UHF RF input 2	<a href="#">Figure 15</a>
V <sub>CC</sub>		10	Supply voltage: 5 V	
VHI OSC B		38	VHF HIGH oscillator base	<a href="#">Figure 16</a>
VHI OSC C		39	VHF HIGH oscillator collector	<a href="#">Figure 16</a>
VHI RF IN		32	VHF-H RF input	<a href="#">Figure 17</a>
VLO OSC B		36	VHF LOW oscillator base	<a href="#">Figure 18</a>
VLO OSC C		37	VHF LOW oscillator collector	<a href="#">Figure 18</a>
VLO RF IN		31	VHF-L RF input	<a href="#">Figure 19</a>
VTU		9	Tuning voltage amplifier output	<a href="#">Figure 3</a>
XTAL1		17	4-MHz crystal oscillator output	<a href="#">Figure 20</a>
XTAL2		18	4-MHz crystal oscillator input	<a href="#">Figure 20</a>
XTAL OUT		19	4-MHz crystal oscillator output	<a href="#">Figure 21</a>

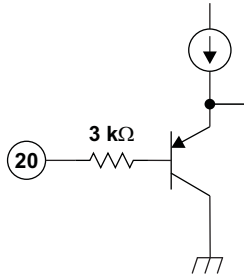


Figure 1. AS

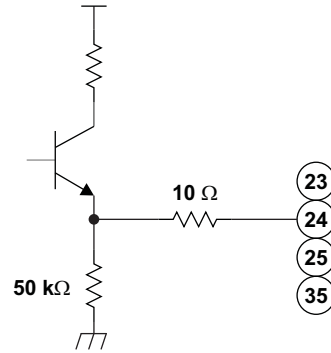


Figure 2. BS1, BS2, BS3, and BS4

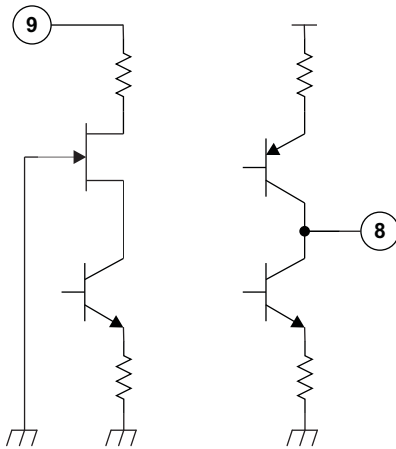


Figure 3. CP and VTU

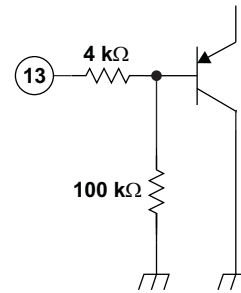


Figure 4. IF GCA CTRL

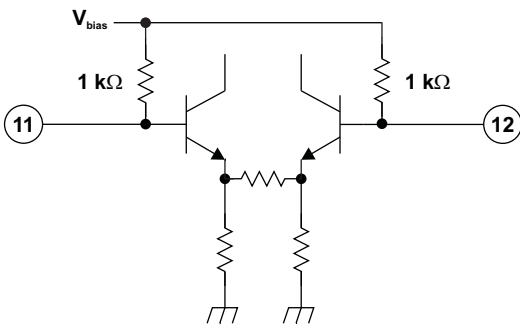


Figure 5. IF GCA IN1 and IF GCA IN2

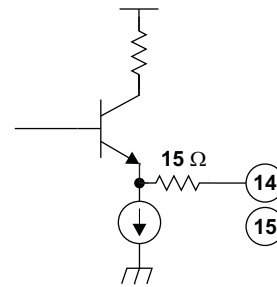


Figure 6. IF GCA OUT1 and IF GCA OUT2

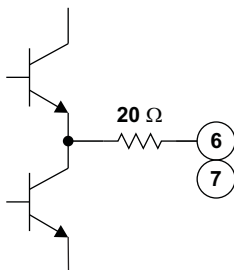


Figure 7. IF OUT1 and IF OUT2

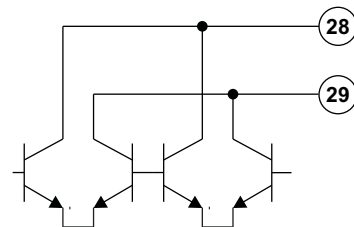


Figure 8. MIX OUT1 and MIX OUT2

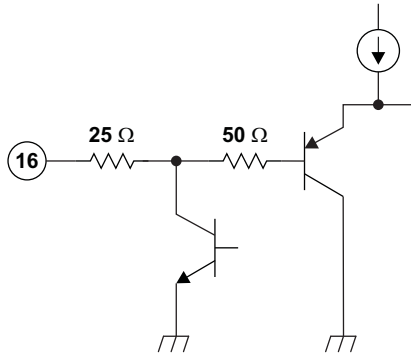


Figure 9. P5/ADC

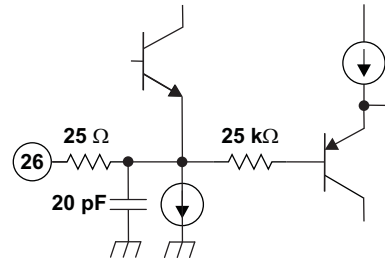


Figure 10. RF AGC FIL

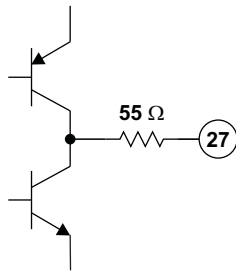


Figure 11. RF AGC OUT

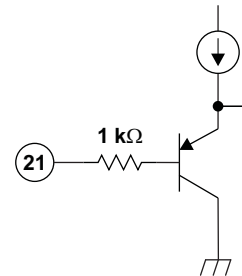


Figure 12. SCL

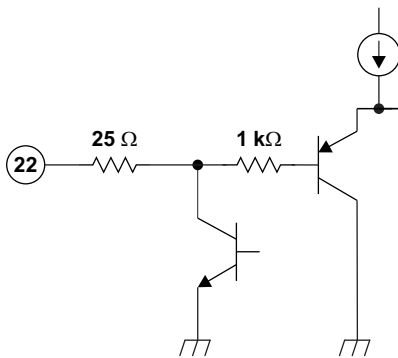


Figure 13. SDA

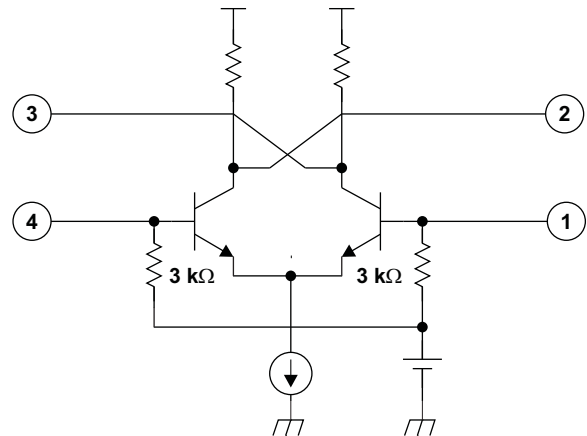


Figure 14. UHF OSC B1, UHF OSC B2, UHF OSC C1, and UHF OSC C2

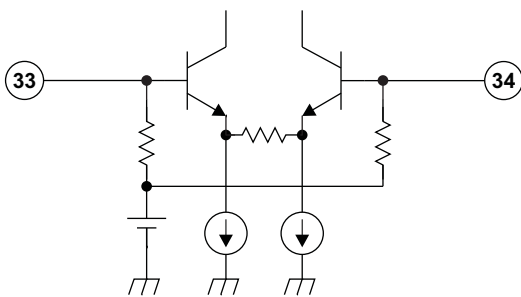


Figure 15. UHF RF IN1 and UHF RFIN2

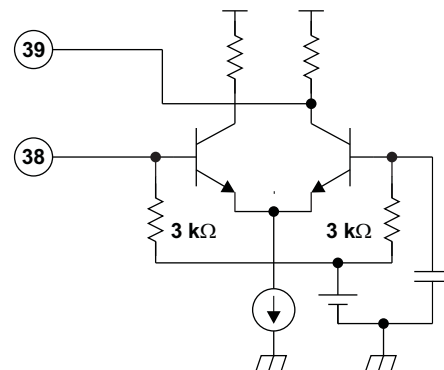


Figure 16. VHI OSC B and VHI OSC C

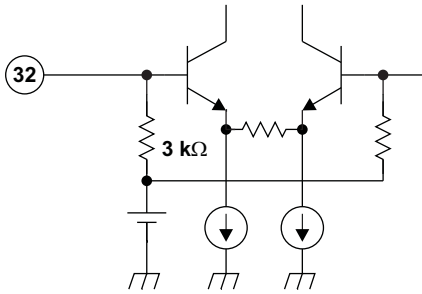


Figure 17. VHI RF IN

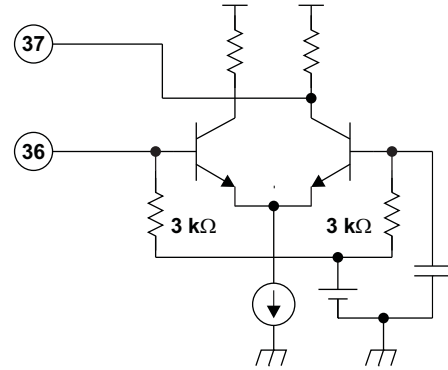


Figure 18. VLO OSC B and VLO OSC C

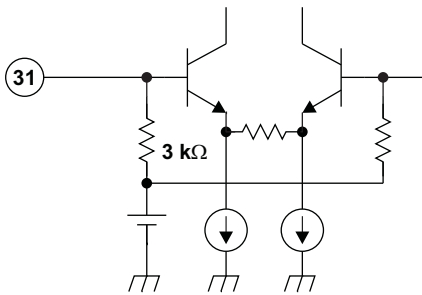


Figure 19. VLO RF IN

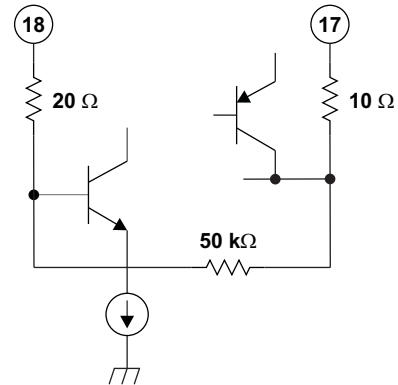


Figure 20. XTAL1 and XTAL2

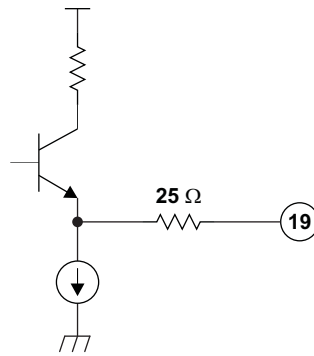


Figure 21. XTAL OUT

## Absolute Maximum Ratings<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	V <sub>CC</sub>	-0.4	6.5	V
V <sub>GND</sub>	Input voltage 1 <sup>(2)</sup>	RF GND, OSC GND	-0.4	0.4	V
VTU	Input voltage 2 <sup>(2)</sup>	VTU	-0.4	35	V
V <sub>IN</sub>	Input voltage 3 <sup>(2)</sup>	Other pins	-0.4	6.5	V
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>			32.5	°C/W
T <sub>A</sub>	Operating free-air temperature range		-20	85	°C
T <sub>stg</sub>	Storage temperature range		-65	150	°C
T <sub>JC</sub>	Maximum junction temperature			150	°C
t <sub>SC(max)</sub>	Maximum short-circuit time	Each pin to V <sub>CC</sub> or to GND		10	s

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage values are with respect to the IF GND of the circuit.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
VTU	Tuning supply voltage			30	33	V
I <sub>BS</sub>	Output current of band-switch	BS1–BS4, one band switch on			10	mA
I <sub>P5</sub>	Output current of port 5	P5/ADC			-5	mA
T <sub>A</sub>	Operating free-air temperature		-20		85	°C



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

MIXOUT1 and MIXOUT2 (pins 28 and 29) withstand 1.5 kV and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

**Electrical Characteristics – Total Device and Serial Interface**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$	Supply current 1			115	140	mA
$I_{CC2}$	Supply current 2	One band switch on ( $I_{BS} = 10\text{ mA}$ )		125	150	mA
$I_{CC-STBY}$	Standby supply current	STBY = 1		9		mA
$V_{IH}$	High-level input voltage (SCL, SDA)		2.5			V
$V_{IL}$	Low-level input voltage (SCL, SDA)				1.35	V
$I_{IH}$	High-level input current (SCL, SDA)				10	$\mu\text{A}$
$I_{IL}$	Low-level input current (SCL, SDA)		-10			$\mu\text{A}$
$V_{POR}$	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
<b>I<sup>2</sup>C Interface</b>						
$V_{ASH}$	Address-select high-input voltage (AS)	$V_{CC} = 5\text{ V}$	4.5		5	V
$V_{ASM1}$	Address-select mid-input 1 voltage (AS)	$V_{CC} = 5\text{ V}$	2		3	V
$V_{ASM2}$	Address-select mid-input 2 voltage (AS)	$V_{CC} = 5\text{ V}$	1		1.5	V
$V_{ASL}$	Address-select low-input voltage (AS)	$V_{CC} = 5\text{ V}$			0.5	V
$I_{ASH}$	Address-select high-input current (AS)				10	$\mu\text{A}$
$I_{ASL}$	Address-select low-input current (AS)		-10			$\mu\text{A}$
$V_{ADC}$	ADC input voltage	See <a href="#">Table 10</a>	0		$V_{CC}$	V
$I_{ADH}$	ADC high-level input current	$V_{ADC} = V_{CC}$			10	$\mu\text{A}$
$I_{ADL}$	ADC low-level input current	$V_{ADC} = 0\text{ V}$	-10			$\mu\text{A}$
$V_{OL}$	Low-level output voltage (SDA)	$V_{CC} = 5\text{ V}$ , $I_{OL} = 3\text{ mA}$			0.4	V
$I_{SDAH}$	High-level output leakage current (SDA)	$V_{SDA} = 5.5\text{ V}$			10	$\mu\text{A}$
$f_{SCL}$	Clock frequency (SCL)			100	400	kHz
$t_{HD-DAT}$	Data hold time	See <a href="#">Figure 22</a>	0			$\mu\text{s}$
$t_{BUF}$	Bus free time		1.3			$\mu\text{s}$
$t_{HD-STA}$	Start hold time		0.6			$\mu\text{s}$
$t_{LOW}$	SCL-low hold time		0.6			$\mu\text{s}$
$t_{HIGH}$	SCL-high hold time		0.6			$\mu\text{s}$
$t_{SU-STA}$	Start setup time		0.6			$\mu\text{s}$
$t_{SU-DAT}$	Data setup time		0.1			$\mu\text{s}$
$t_r$	Rise time (SCL, SDA)				0.3	$\mu\text{s}$
$t_f$	Fall time (SCL, SDA)				0.3	$\mu\text{s}$
$t_{SU-STO}$	Stop setup time		0.6			$\mu\text{s}$

### Electrical Characteristics – PLL and Band Switch

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
$f_{XTAL}$	Crystal oscillator frequency	$R_{XTAL} = 25\ \Omega$ to $300\ \Omega$		4		MHz
$Z_{XTAL}$	Crystal oscillator input impedance			1.6		k $\Omega$
$V_{XLO}$	XTAL OUT output voltage	Load = 10 pF/5.1 k $\Omega$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		0.4		V <sub>p-p</sub>
$V_{VTUL}$	Tuning amplifier low-level output voltage	$R_L = 22\text{ k}\Omega$ , $VTU = 33\text{ V}$	0.2	0.3	0.46	V
$I_{VTUOFF}$	Tuning amplifier leakage current	Tuning amplifier = off, $VTU = 33\text{ V}$			10	$\mu\text{A}$
$I_{CP11}$	Charge-pump current	CP[1:0] = 11		600		$\mu\text{A}$
$I_{CP10}$		CP[1:0] = 10		350		
$I_{CP01}$		CP[1:0] = 01		140		
$I_{CP00}$		CP[1:0] = 00		70		
$V_{CP}$	Charge-pump output voltage	PLL locked		1.95		V
$I_{CPOFF}$	Charge-pump leakage current	$V_{CP} = 2\text{ V}$ , $T_A = 25^\circ\text{C}$	-15		15	nA
$I_{BS}$	Band-switch driver output current (BS1–BS4)				10	mA
$V_{BS1}$	Band-switch driver output voltage (BS1–BS4)	$I_{BS} = 10\text{ mA}$		3		V
$V_{BS2}$		$I_{BS} = 10\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		3.5	3.9	
$I_{BSOFF}$	Band-switch driver leakage current (BS1–BS4)	$V_{BS} = 0\text{ V}$			8	$\mu\text{A}$
$I_{P5}$	Band-switch port sink current (P5/ADC)				-5	mA
$V_{P5ON}$	Band-switch port output voltage (P5/ADC)	$I_{P5} = -2\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			0.6	V

### Electrical Characteristics – RF AGC

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 23](#) reference measurement circuit at 50- $\Omega$  system, IF = 44 MHz, IF filter characteristics:  $f_{peak} = 44\text{ MHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$I_{OAGC0}$	RF AGC output source current	ATC = 0	300	nA
$I_{OAGC1}$		ATC = 1	15	$\mu\text{A}$
$I_{OAGCSINK}$	RF AGC peak sink current	ATC = 0	100	$\mu\text{A}$
$V_{AGCSP00}$	Start-point IF output level <sup>(1)</sup>	T1/ATSS = 0, ATP[2:0] = 000	117	dB $\mu\text{V}$
$V_{AGCSP01}$		T1/ATSS = 0, ATP[2:0] = 001	114	
$V_{AGCSP02}$		T1/ATSS = 0, ATP[2:0] = 010	111	
$V_{AGCSP03}$		T1/ATSS = 0, ATP[2:0] = 011	108	
$V_{AGCSP04}$		T1/ATSS = 0, ATP[2:0] = 100	105	
$V_{AGCSP05}$		T1/ATSS = 0, ATP[2:0] = 101	102	
$V_{AGCSP06}$		T1/ATSS = 0, ATP[2:0] = 110	99	
$V_{AGCSP10}$		T1/ATSS = 1, ATP[2:0] = 000	112	
$V_{AGCSP11}$		T1/ATSS = 1, ATP[2:0] = 001	109	
$V_{AGCSP12}$		T1/ATSS = 1, ATP[2:0] = 010	106	
$V_{AGCSP13}$		T1/ATSS = 1, ATP[2:0] = 011	103	
$V_{AGCSP14}$		T1/ATSS = 1, ATP[2:0] = 100	100	
$V_{AGCSP15}$		T1/ATSS = 1, ATP[2:0] = 101	97	
$V_{AGCSP16}$		T1/ATSS = 1, ATP[2:0] = 110	94	

(1) When AISL = 1, RF AGC function is not available at VHF-L band.

**Electrical Characteristics – Mixer, Oscillator, IF Amplifier**

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 23](#) reference measurement circuit at 50- $\Omega$  system, IF = 44 MHz, IF filter characteristics:  $f_{peak} = 44\text{ MHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$G_{c1}$	Conversion gain (mixer-IF amplifier), VHF-LOW	$f_{in} = 57\text{ MHz}^{(1)}$	35	dB
$G_{c3}$		$f_{in} = 171\text{ MHz}^{(1)}$	35	
$G_{c4}$	Conversion gain (mixer-IF amplifier), VHF-HIGH	$f_{in} = 177\text{ MHz}^{(1)}$	35	dB
$G_{c6}$		$f_{in} = 467\text{ MHz}^{(1)}$	35	
$G_{c7}$	Conversion gain (mixer-IF amplifier), UHF	$f_{in} = 473\text{ MHz}^{(1)}$	35	dB
$G_{c9}$		$f_{in} = 864\text{ MHz}^{(1)}$	35	
$NF_1$	Noise figure, VHF-LOW	$f_{in} = 57\text{ MHz}$	9	dB
$NF_3$		$f_{in} = 171\text{ MHz}$	9	
$NF_4$	Noise figure, VHF-HIGH	$f_{in} = 177\text{ MHz}$	9	dB
$NF_6$		$f_{in} = 467\text{ MHz}$	9	
$NF_7$	Noise figure, UHF	$f_{in} = 473\text{ MHz}$	12	dB
$NF_9$		$f_{in} = 864\text{ MHz}$	12	
$CM_1$	Input voltage causing 1% cross-modulation distortion, VHF-LOW	$f_{in} = 57\text{ MHz}^{(2)}$	79	dB $\mu$ V
$CM_3$		$f_{in} = 171\text{ MHz}^{(2)}$	79	
$CM_4$	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	$f_{in} = 177\text{ MHz}^{(2)}$	79	dB $\mu$ V
$CM_6$		$f_{in} = 467\text{ MHz}^{(2)}$	79	
$CM_7$	Input voltage causing 1% cross-modulation distortion, UHF	$f_{in} = 473\text{ MHz}^{(2)}$	77	dB $\mu$ V
$CM_9$		$f_{in} = 864\text{ MHz}^{(2)}$	77	
$V_{IF01}$	IF output voltage, VHF-LOW	$f_{in} = 57\text{ MHz}$	117	dB $\mu$ V
$V_{IF03}$		$f_{in} = 171\text{ MHz}$	117	
$V_{IF04}$	IF output voltage, VHF-HIGH	$f_{in} = 177\text{ MHz}$	117	dB $\mu$ V
$V_{IF06}$		$f_{in} = 467\text{ MHz}$	117	
$V_{IF07}$	IF output voltage, UHF	$f_{in} = 473\text{ MHz}$	117	dB $\mu$ V
$V_{IF09}$		$f_{in} = 864\text{ MHz}$	117	
$\Phi_{PLVL11}$	Phase noise, VHF-LOW	$f_{in} = 57\text{ MHz}$ , Offset = 1 kHz <sup>(3)</sup>	-90	dBc/Hz
$\Phi_{PLVL12}$		$f_{in} = 57\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-95	
$\Phi_{PLVL31}$		$f_{in} = 171\text{ MHz}$ , Offset = 1 kHz <sup>(5)</sup>	-85	
$\Phi_{PLVL32}$		$f_{in} = 171\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-95	
$\Phi_{PLVL41}$	Phase noise, VHF-HIGH	$f_{in} = 177\text{ MHz}$ , Offset = 1 kHz <sup>(3)</sup>	-85	dBc/Hz
$\Phi_{PLVL42}$		$f_{in} = 177\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-90	
$\Phi_{PLVL61}$		$f_{in} = 467\text{ MHz}$ , Offset = 1 kHz <sup>(5)</sup>	-77	
$\Phi_{PLVL62}$		$f_{in} = 467\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-90	
$\Phi_{PLVL71}$	Phase noise, UHF	$f_{in} = 473\text{ MHz}$ , Offset = 1 kHz <sup>(3)</sup>	-80	dBc/Hz
$\Phi_{PLVL72}$		$f_{in} = 473\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-85	
$\Phi_{PLVL91}$		$f_{in} = 864\text{ MHz}$ , Offset = 1 kHz <sup>(5)</sup>	-77	
$\Phi_{PLVL92}$		$f_{in} = 864\text{ MHz}$ , Offset = 10 kHz <sup>(4)</sup>	-90	

- (1) IF = 44 MHz, RF input level = 70 dB $\mu$ V, differential output
- (2)  $f_{undes} = f_{des} \pm 6\text{ MHz}$ ,  $P_{in} = 70\text{ dB}\mu\text{V}$ , AM 1 kHz, 30%, DES/CM = S/I = 46 dB
- (3) CP[1:0] = 10 (CP current 350  $\mu$ A), RS[2:0] = 011 (reference divider 64)
- (4) CP[1:0] = 00 (CP current 70  $\mu$ A), RS[2:0] = 100 (reference divider 128)
- (5) CP[1:0] = 11 (CP current 600  $\mu$ A), RS[2:0] = 011 (reference divider 64)

### Electrical Characteristics – IF Gain Controlled Amplifier

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 23](#) reference measurement circuit at 50- $\Omega$  system,  $IF = 44\text{ MHz}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IFGCA}$	Input current (IF GCA CTRL)	$V_{IFGCA} = 3\text{ V}$		30	60	$\mu\text{A}$
$V_{IFGCAMAX}$	Maximum gain control voltage	Gain maximum	2.5		$V_{CC}$	V
$V_{IFGCAMIN}$	Minimum gain control voltage	Gain minimum	0		0.4	V
$G_{IFGCAMAX}$	Maximum gain	$V_{IFGCA} = 3\text{ V}$	49	53	57	dB
$G_{IFGCAMIN}$	Minimum gain	$V_{IFGCA} = 0\text{ V}$	-4	-1	2	dB
$GCR_{IFGCA}$	Gain control range	$V_{IFGCA} = 0\text{--}3\text{ V}$		54		dB
$V_{IFGCAOUT}$	Output voltage	Single-ended output		2.1		Vp-p
$NF_{IFGCA}$	Noise figure	$V_{IFGCA} = 3\text{ V}$		8.5		dB
$IM3_{IFGCA}$	Third order intermodulation distortion	$f_{IFGCAIN1} = 43\text{ MHz}$ , $f_{IFGCAIN2} = 44\text{ MHz}$ , $V_{IFGCAOUT} = -2\text{ dBm}$ , $V_{IFGCA} = 3\text{ V}$		-50		dBc
$IIP3_{IFGCA}$	Input intercept point	$V_{IFGCA} = 0\text{ V}$		11		dBm
$R_{IFGCAIN}$	Input resistance (IF GCA IN1, IF GCA IN2)			1		k $\Omega$

## FUNCTIONAL DESCRIPTION

### I<sup>2</sup>C Bus Mode

#### I<sup>2</sup>C Write Mode ( $R/\bar{W} = 0$ )

Table 1. Write Data Format

	MSB							LSB	(1)
Address byte (ADB)	1	1	0	0	0	MA1	MA0	$R/\bar{W} = 0$	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A
Band-switch byte (BB)	CP1	CP0	AISL	P5	BS4	BS3	BS2	BS1	A
Control byte 2 (CB2)	1	1	ATC	STBY	T3	T2	T1/ATSS	T0/XLO	A

(1) A: Acknowledge

**Table 2. Write Data Symbol Description**

SYMBOL	DESCRIPTION	DEFAULT													
MA[1:0]	Address-set bits (see <a href="#">Table 3</a> )														
N[14:0]	Programmable counter set bits $N = N_{14} \times 2^{14} + N_{13} \times 2^{13} + \dots + N_1 \times 2 + N_0$	$N_{14} = N_{13} = N_{12} = \dots = N_0 = 0$													
ATP[2:0]	RF AGC start-point control bits (see <a href="#">Table 4</a> )	ATP[2:0] = 011													
RS[2:0]	Reference divider ratio-selection bits (see <a href="#">Table 5</a> )	RS[2:0] = 111													
CP[1:0]	Charge-pump current-set bit (see <a href="#">Table 6</a> )	CP[1:0] = 11													
AISL	RF AGC detector input selection bit AISL = 0: IF amplifier AISL = 1: Mixer output	AISL = 0													
P5	Port output/ADC input control bit P5 = 0: ADC INPUT P5 = 1: Tr = ON	P5 = 0													
BS[4:1]	Band-switch control bits BSn = 0: Tr = OFF BSn = 1: Tr = ON	BSn = 0													
	Band selection by BS[1:2] <table border="1"> <thead> <tr> <th>BS1</th> <th>BS2</th> <th></th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>VHF-LO</td> </tr> <tr> <td>0</td> <td>1</td> <td>VHF-HI</td> </tr> <tr> <td>0</td> <td>0</td> <td>UHF</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>		BS1	BS2		1	0	VHF-LO	0	1	VHF-HI	0	0	UHF	1
BS1	BS2														
1	0	VHF-LO													
0	1	VHF-HI													
0	0	UHF													
1	1	Reserved													
ATC	RF AGC current-set bit ATC = 0: Current = 300 nA ATC = 1: Current = 15 $\mu$ A	ATC = 0													
STBY	Power standby mode-control bit STBY = 0: Normal operation STBY = 1: Standby mode/stop MOP function (XTALOUT is available even in standby mode)	STBY = 0													
T3, T2, T1/ATSS, T0/XLO	TEST bits, RFAGC shift bit, XTAL OUT control bit (see <a href="#">Table 7</a> )	T[3:0] = 0010													
X	Don't care														

**Table 3. Address Selection**

MA1	MA0	VOLTAGE APPLIED ON AS INPUT
0	0	0 V to 0.1 V <sub>CC</sub> (Low)
0	1	OPEN, or 0.2 V <sub>CC</sub> to 0.3 V <sub>CC</sub> (Mid2)
1	0	0.4 V <sub>CC</sub> to 0.6 V <sub>CC</sub> (Mid1)
1	1	0.9 V <sub>CC</sub> to V <sub>CC</sub> (High)

**Table 4. RF AGC Start Point<sup>(1)</sup>**

T1/ATSS	ATP2	ATP1	ATP0	IF OUT LEVEL (dB $\mu$ V)
0	0	0	0	117
0	0	0	1	114
0	0	1	0	111
0	0	1	1	108
0	1	0	0	105
0	1	0	1	102
0	1	1	0	99
0	1	1	1	Disabled
1	0	0	0	112
1	0	0	1	109
1	0	1	0	106
1	0	1	1	103
1	1	0	0	100
1	1	0	1	97
1	1	1	0	94
1	1	1	1	Disabled

(1) When AISL = 1, RF AGC function is not available at VHF-L band (output level is undefined).

**Table 5. Reference Divider Ratio**

RS2	RS1	RS0	REFERENCE DIVIDER RATIO
0	0	0	24
0	0	1	28
0	1	0	50
0	1	1	64
1	0	0	128
1	X	1	80

**Table 6. Charge-Pump Current**

CP1	CP0	CHARGE PUMP CURRENT ( $\mu$ A)
0	0	70
0	1	140
1	0	350
1	1	600

**Table 7. Test Bits/XTAL OUT Control <sup>(1)</sup>**

T3	T2	T1/ATSS	T0/XLO	DEVICE OPERATION	XTAL OUT 4-MHz OUTPUT
0	0	X	0	Normal operation	Enabled
0	0	X	1	Normal operation	Disabled
X	1	X	X	Test mode	Not available
1	X	X	X	Test mode	Not available

(1) RF AGC and XTAL OUT are not available in test mode.

**Example I<sup>2</sup>C Data Write Sequences**

Telegram examples:

Start-ADB-DB1-DB2-CB1-BB-CB2-Stop  
Start-ADB-DB1-DB2-Stop  
Start-ADB-CB1-BB-CB2-Stop  
Start-ADB-CB1-BB-Stop  
Start-ADB-CB2-Stop

Abbreviations:

ADB: Address byte  
BB: Band-switch byte  
CB1: Control byte 1  
CB2: Control byte 2  
DB1: Divider byte 1  
DB2: Divider byte 2  
Start: Start condition  
Stop: Stop condition

**I<sup>2</sup>C Read Mode ( $R/\overline{W} = 1$ )**

**Table 8. Read Data Format (A: Acknowledge)**

	MSB							LSB		
Address byte (ADB)	1	1	0	0	0	0	MA1	MA0	$R/\overline{W} = 1$	A
Status byte (SB)	POR	FL	1	1	X		A2	A1	A0	–

**Table 9. Read Data Symbol Description**

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address set bits (see <a href="#">Table 3</a> )	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag PLL locked (FL = 1), unlocked (FL = 0)	
A[2:0]	Digital data of ADC (see <a href="#">Table 10</a> ) Bit P5 must be set to 0.	

Table 10. ADC Level<sup>(1)</sup>

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	0.6 V <sub>CC</sub> to V <sub>CC</sub>
0	1	1	0.45 V <sub>CC</sub> to 0.6 V <sub>CC</sub>
0	1	0	0.3 V <sub>CC</sub> to 0.45 V <sub>CC</sub>
0	0	1	0.15 V <sub>CC</sub> to 0.3 V <sub>CC</sub>
0	0	0	0 V to 0.15 V <sub>CC</sub>

(1) Accuracy is  $0.03 \times V_{CC}$ .

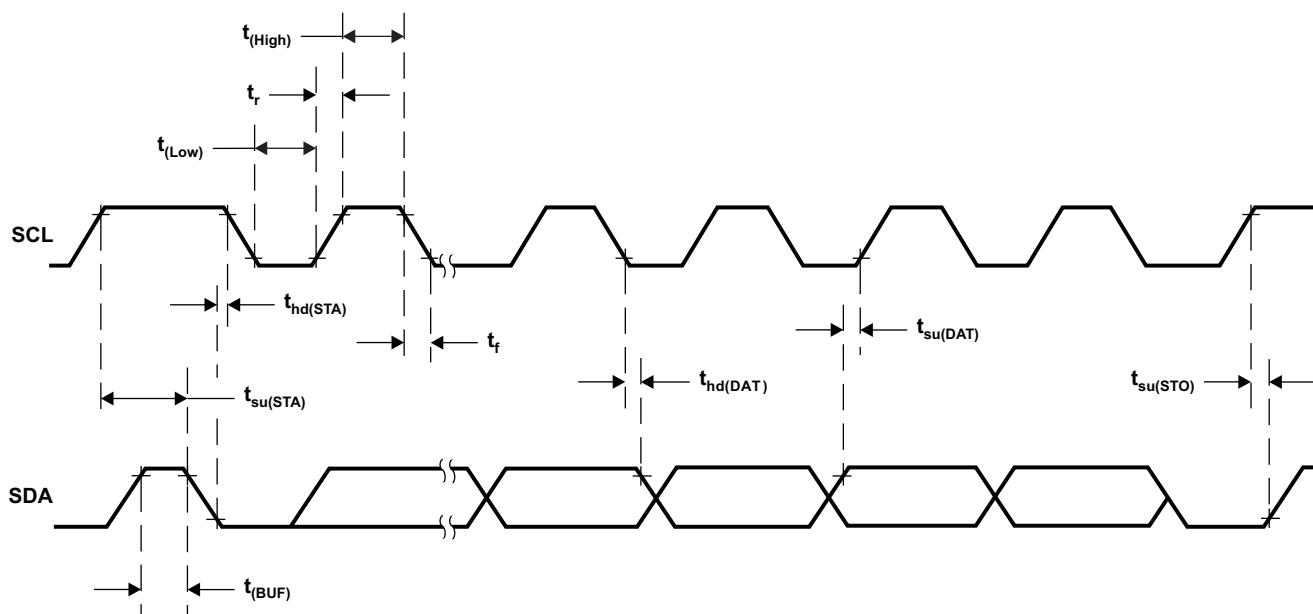
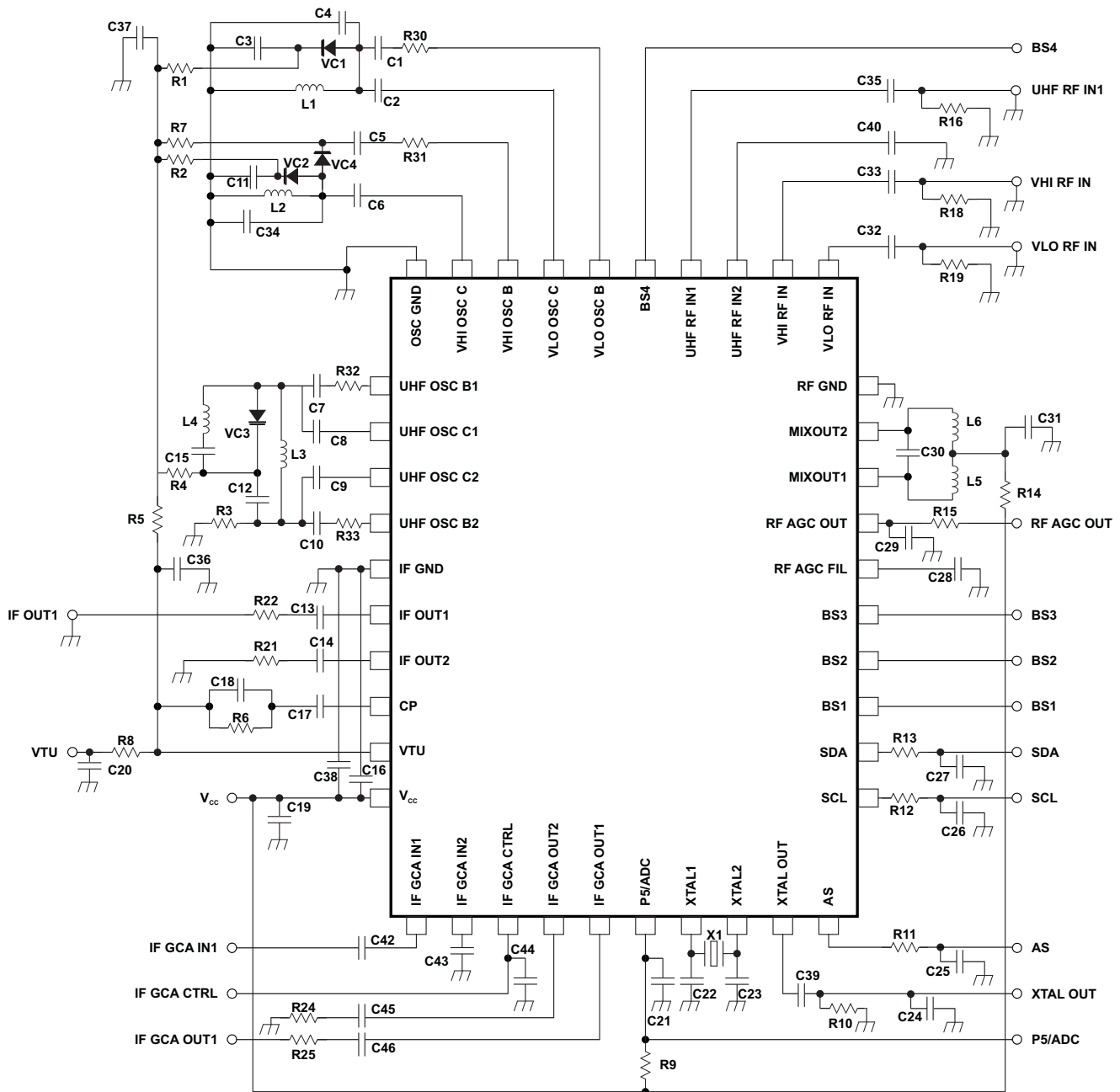


Figure 22. I²C Timing Chart

APPLICATION INFORMATION



NOTE: This application information is advisory, and a performance check is required for actual application circuits. TI assumes no responsibility for the consequences of the use of this circuit, nor for any infringement of patent or patent rights of third parties that may result from its use.

Figure 23. Reference Measurement Circuit

**APPLICATION INFORMATION (continued)**
**Component Values for Measurement Circuit**

PART NAME	VALUE	PART NAME	VALUE
C1 (VLO OSC B)	1 pF	C43 (IF GCA IN2)	2.2 nF
C2 (VLO OSC C)	2 pF	C44 (IF GCA CTRL)	2.2 nF
C3 (VLO OSC)	47 pF	C45 (IF GCA OUT1)	2.2 nF
C4 (VLO OSC)	Open	C46 (IF GCA OUT2)	2.2 nF
C5 (VHI OSC)	7 pF	L1 (VLO OSC)	φ3.0 mm, 7T, wire 0.32 mm
C6 (VHI OSC C)	5 pF	L2 (VHI OSC)	φ2.0 mm, 3T, wire 0.4 mm
C7 (UHF OSC B1)	1.5 pF	L3 (UHF OSC)	φ1.8 mm, 3T, wire 0.4 mm
C8 (UHF OSC C1)	1 pF	L4 (UHF OSC)	φ1.8 mm, 3T, wire 0.4 mm
C9 (UHF OSC C2)	1 pF	L5 (MIX OUT)	680 nH (LK1608R68K-T)
C10 (UHF OSC B2)	1.5 pF	L6 (MIX OUT)	680 nH (LK1608R68K-T)
C11 (VHI OSC)	51 pF	R1 (VLO OSC)	3.3 kΩ
C12 (UHF OSC)	10 pF	R2 (VHI OSC)	3.3 kΩ
C13 (IF OUT)	2.2 nF	R3 (UHF OSC)	2.2 kΩ
C14 (IF OUT)	2.2 nF	R4 (UHF OSC)	1 kΩ
C15 (UHF OSC)	100 pF	R5 (VTU)	3 kΩ
C16 (V <sub>CC</sub> )	4.7 nF	R6 (CP)	47 kΩ
C17 (CP)	0.01 μF/50 V	R7 (VHI OSC)	3.3 kΩ
C18 (CP)	22 pF/50 V	R8 (VTU)	22 kΩ
C19 (V <sub>CC</sub> )	2.2 nF	R9 (P5/ADC)	Open
C20 (VTU)	2.2 nF/50 V	R10 (XTALOUT)	5.1 kΩ
C21 (P5/ADC)	Open	R11 (AS)	330 Ω
C22 (XTAL)	27 pF	R12 (SCL)	330 Ω
C23 (XTAL)	27 pF	R13 (SDA)	330 Ω
C24 (XTALOUT)	10 pF	R14 (V <sub>CC</sub> )	0
C25 (AS)	Open	R15 (RF AGC OUT)	0
C26 (SCL)	Open	R16 (UHF RF IN1)	(50 Ω)
C27 (SDA)	Open	R18 (VHI RF IN)	(50 Ω)
C28 (AGC FIL)	Open	R19 (VLO RF IN)	(50 Ω)
C29 (RF AGC OUT)	0.15 μF	R21 (IF OUT2)	1 kΩ
C30 (MIX OUT)	5.6 pF	R22 (IF OUT1)	1 kΩ
C31 (MIX OUT)	2.2 nF	R24 (IF GCA OUT1)	250 Ω
C32 (VLO RF IN)	2.2 nF	R25 (IF GCA OUT2)	200 Ω
C33 (VHI RF IN)	2.2 nF	R30 (VLO OSC B)	0
C34 (VHI OSC)	0.5 pF	R31 (VHI OSC B)	4.7 Ω
C35 (UHF RF IN1)	2.2 nF	R32 (UHF OSC B1)	0
C36 (VTU)	22 pF	R33 (UHF OSC B2)	0
C37 (VTU)	2.2 nF/50 V	VC1 (VLO OSC)	MA2S374
C38 (V <sub>CC</sub> )	0.1 μF	VC2 (VHI OSC)	MA2S374
C39 (XTAL OUT)	2.2 nF	VC3 (UHF OSC)	MA2S372
C40 (UHF RF IN2)	2.2 nF	VC4 (VHI OSC)	MA2S372
C42 (IF GCA IN1)	2.2 nF	X1	4-MHz crystal

APPLICATION INFORMATION (CONTINUED)

Test Circuits

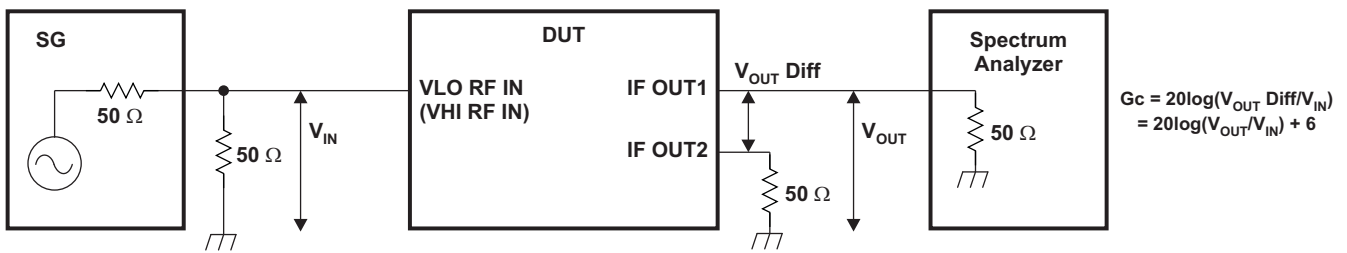


Figure 24. VHF-Conversion Gain-Measurement Circuit

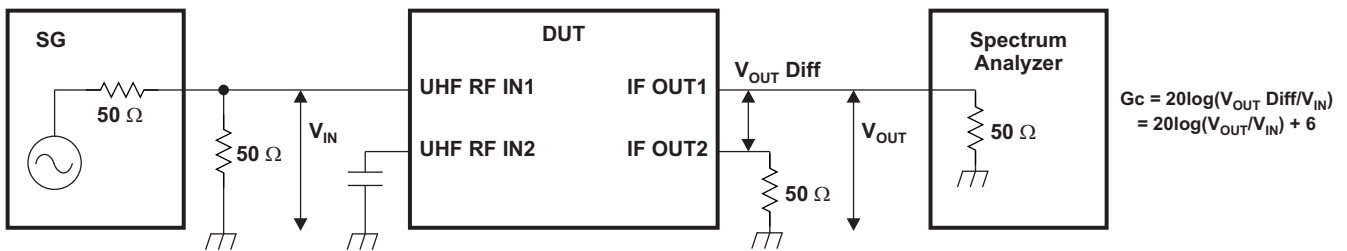


Figure 25. UHF-Conversion Gain-Measurement Circuit

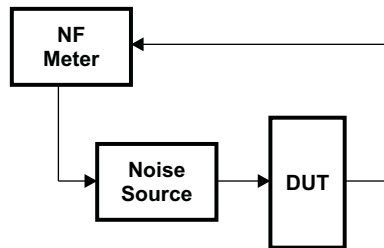


Figure 26. Noise-Figure Measurement Circuit

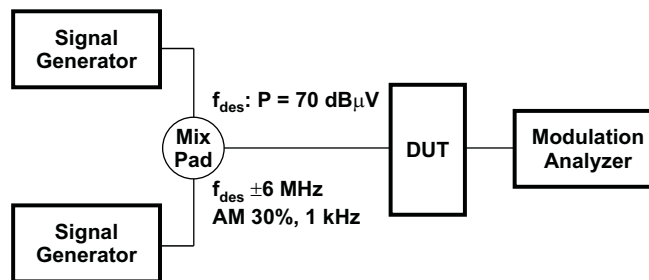


Figure 27. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band-Switch Driver Output Voltage (BS1–BS4)

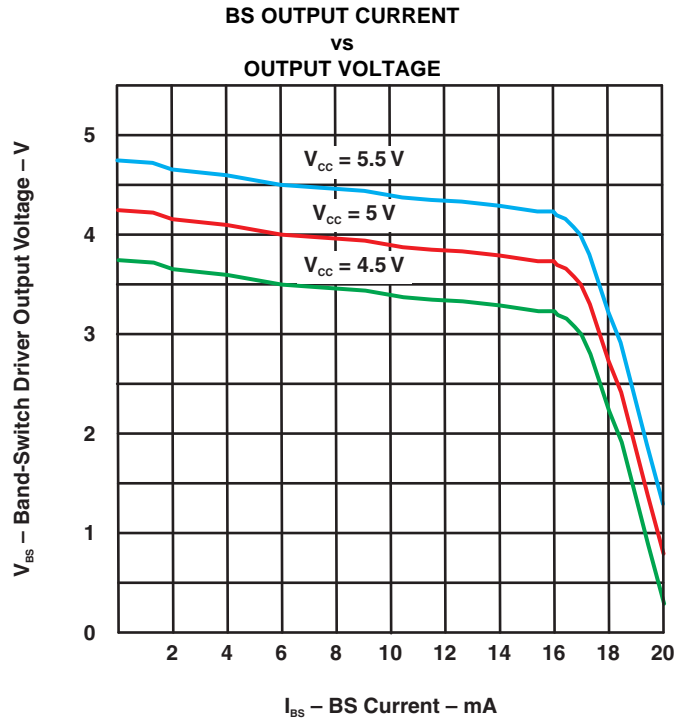


Figure 28. Band-Switch Driver Output Voltage

S-Parameter

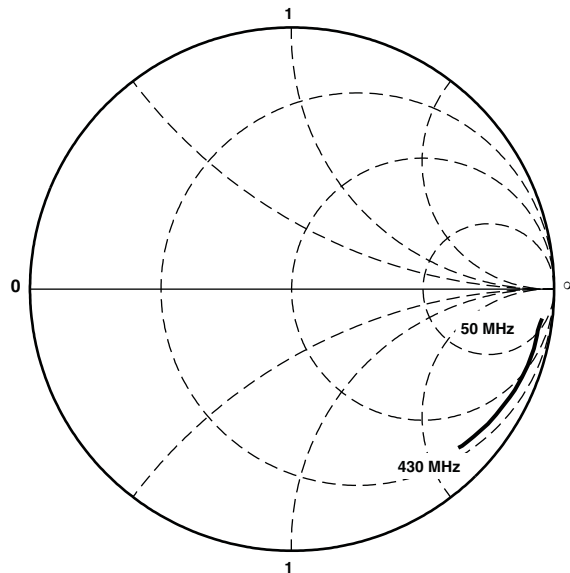


Figure 29. VLO RFIN, VHI RFIN

TYPICAL CHARACTERISTICS (continued)

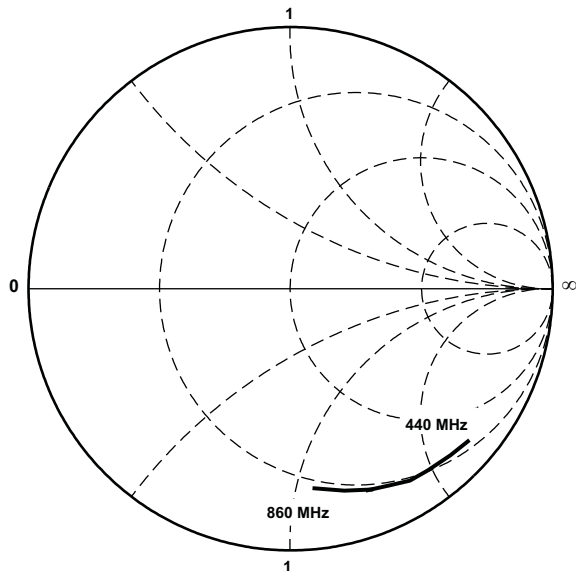


Figure 30. UHF RFIN

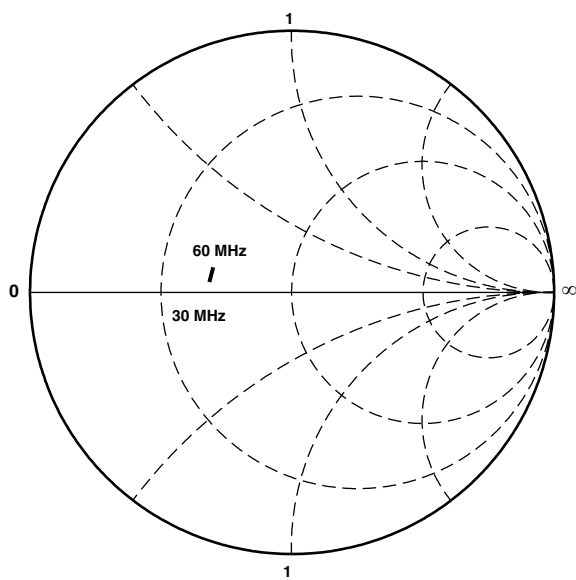


Figure 31. IF OUT

TYPICAL CHARACTERISTICS (continued)

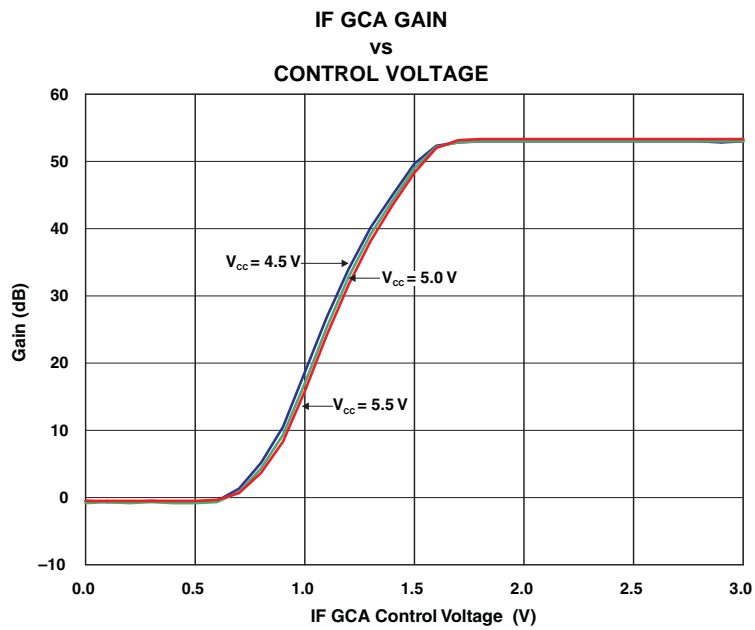


Figure 32.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN761667RHAR	PREVIEW	QFN	RHA	40		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

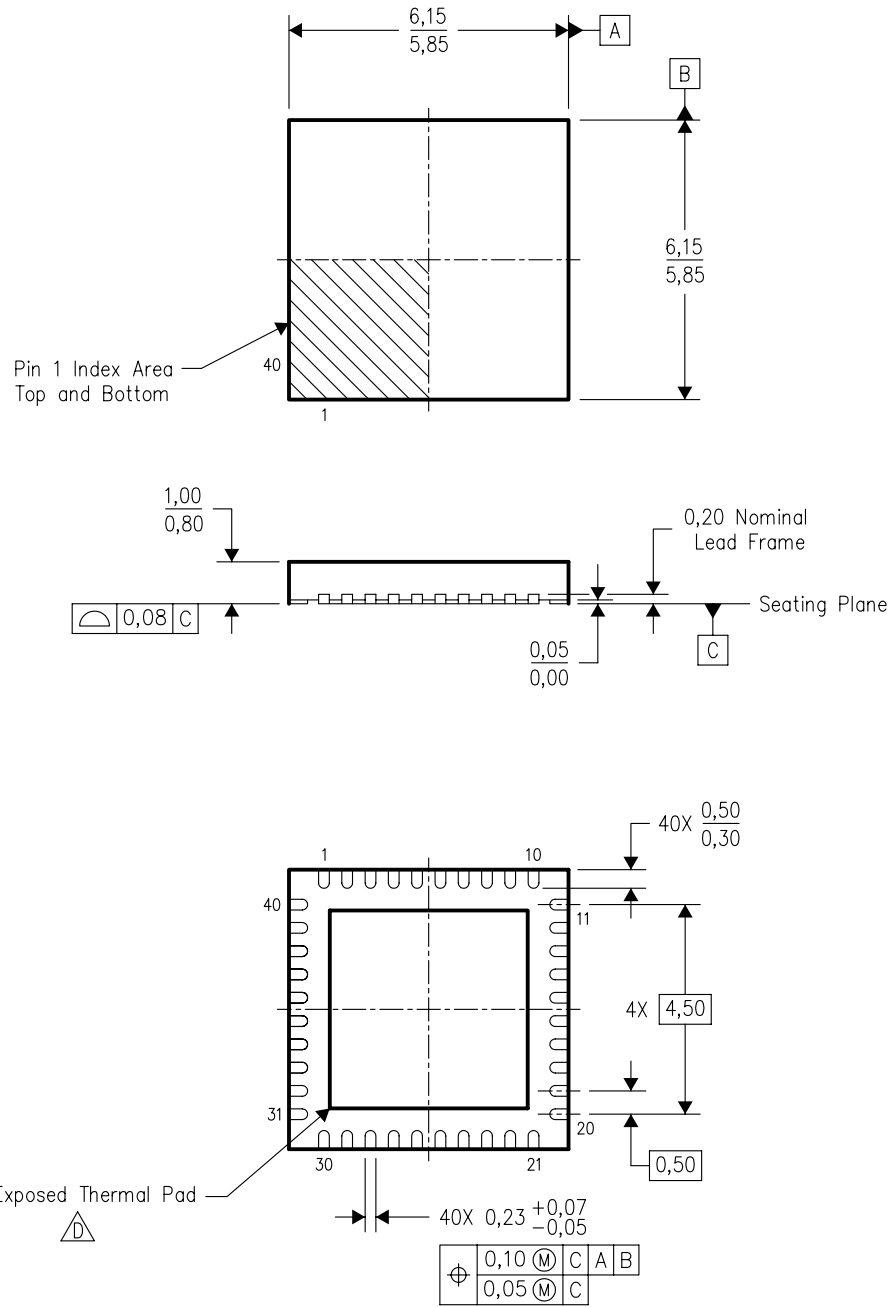
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHA (S-PQFP-N40)

PLASTIC QUAD FLATPACK



Bottom View

4204276/C 12/2004

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-220 variation VJJD-2.

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