Ordering number: EN 3510A

CMOS LSI

SANYO No. 3510A

LC7886,7886M

18-Bit A/D Converter for Digital Audio Applications

Overview

The LC7886/7886M are 16/18-bit CMOS A/D converters that can be used in digital audio applications. The conversion is performed based on the electric charge redistribution type sequential comparison method with an internal calibration function.

Features:

- On-chip independent 2-channel A/D converter. In-phase sampling is supported.
- Maximum conversion frequency = 96kHz and Two-times oversampling
- On-chip Sample and Hold circuit
- On-chip calibration function. No external adjustment is required.
- Single +5V power supply
- Low power dissipation thanks to CMOS process

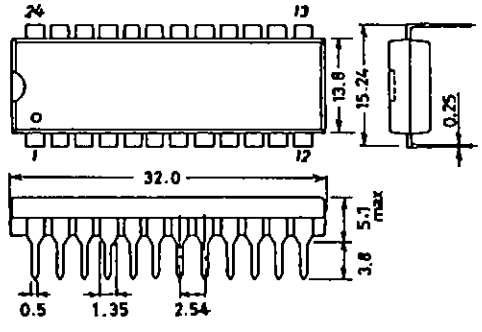
Absolute Maximum Ratings

Parameter	Symbol	Rated values	Unit
Maximum Supply Voltage	V_{DD} max	−0.3to+7.0	V
Input Voltage	V_{IN}	−0.3toV_{DD}+0.3	V
Output Voltage	V_{OUT}	−0.3toV_{DD}+0.3	V
Operating Temperature	Topr	−30to+75	℃
Storage Temperature	Tstg	−40to+125	℃

Allowable Operating Range at Ta = -30 ℃ to +75 ℃

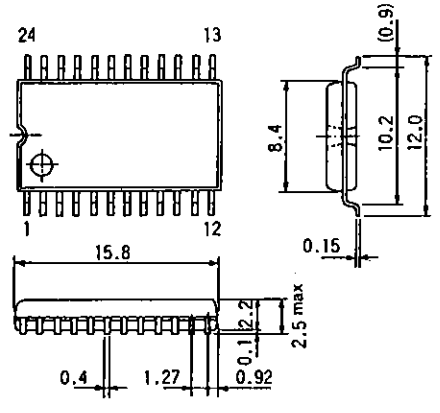
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
'H' Level Reference Voltage	V_H	V_{DD}−0.5		V_{DD}	V
'L' Level Reference Voltage	V_L	0		0.5	V
Analog input voltage	V_{AIN}	V_L		V_H	V

Package Dimensions 3072D24NS (LC7886)
(unit: mm)



SANYO : DIP-24

Package Dimensions 3155M24VL (LC7886M)
(unit: mm)



SANYO : MFP-24

DC Characteristics at Ta = -30 °C to +75 °C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

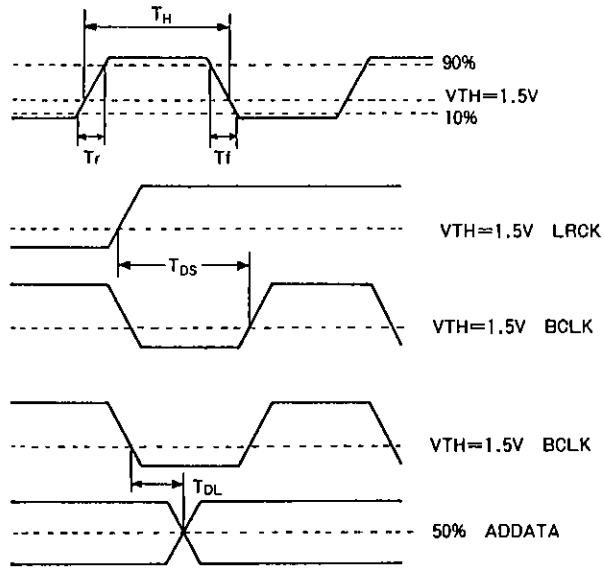
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input 'H' Level Voltage	V_{IH}		2.2			V
Input 'L' Level Voltage	V_{IL}				0.8	V
Output 'H' Level Voltage	V_{OH}	I_{OH} = −1 μA	V_{DD}−0.05			V
Output 'L' Level Voltage	V_{OL}	I_{OL} = 1 μA			V_{SS}+0.05	V

Switching Characteristics at Ta = -30 °C to +75 °C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rise Time	Tr	※1			30	ns
Fall Time	Tf	※1			30	ns
High-level Time	T_H	BCLK	50			ns
Set-up Time	T_{DS}	LRCK	40			ns
Data Delay Time	T_{DL}	ADDATA			50	ns

※1 : BCLK, LRCK

Timing Diagram

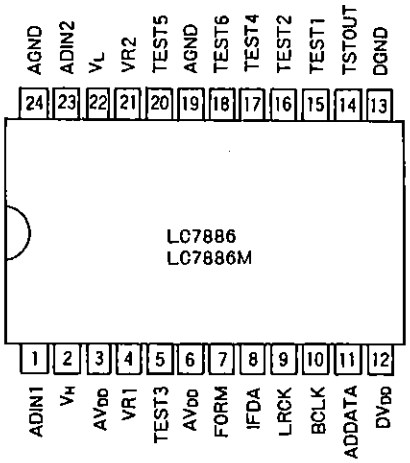


Analog Characteristics at Ta = 25 °C, AV_{DD} = DV_{DD} = 5.0V, VH = 5.0V, VL = 0V

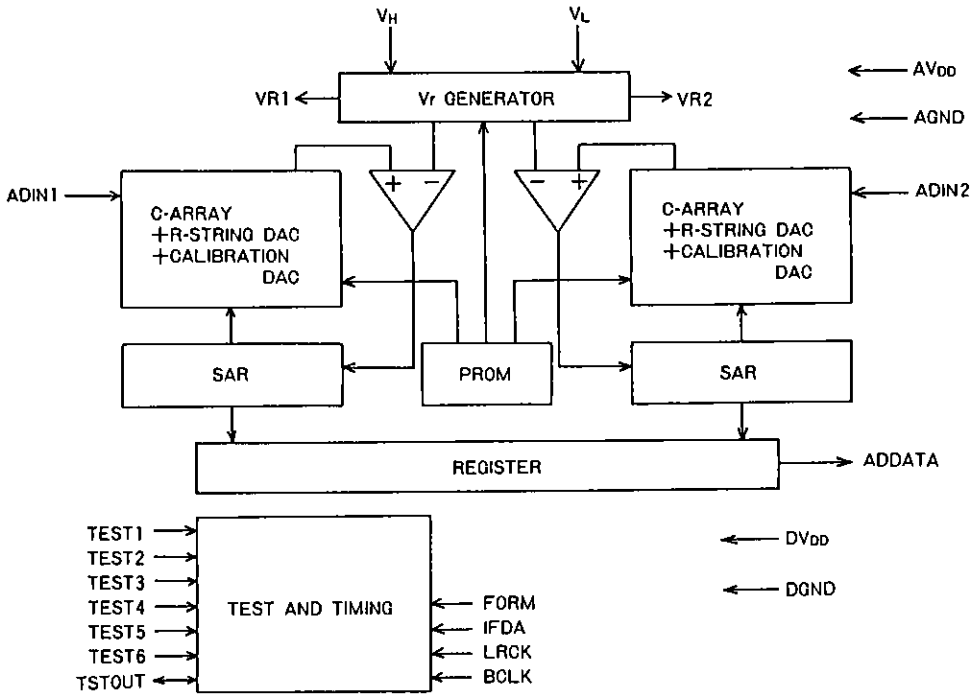
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Conversion Cycle	fs				96	kHz
All-harmonics Distortion	THD	1kHz, at 0dB ※1			0.02	%
Signal-noise Ratio	S/N	※1		86		dB
Maximum Power Dissipation	Pd max	※1		175	250	mW

※1: The measurement circuit is equivalent to the example application circuit. The LRCK is 96kHz.

Pin Assignment



Block Diagram



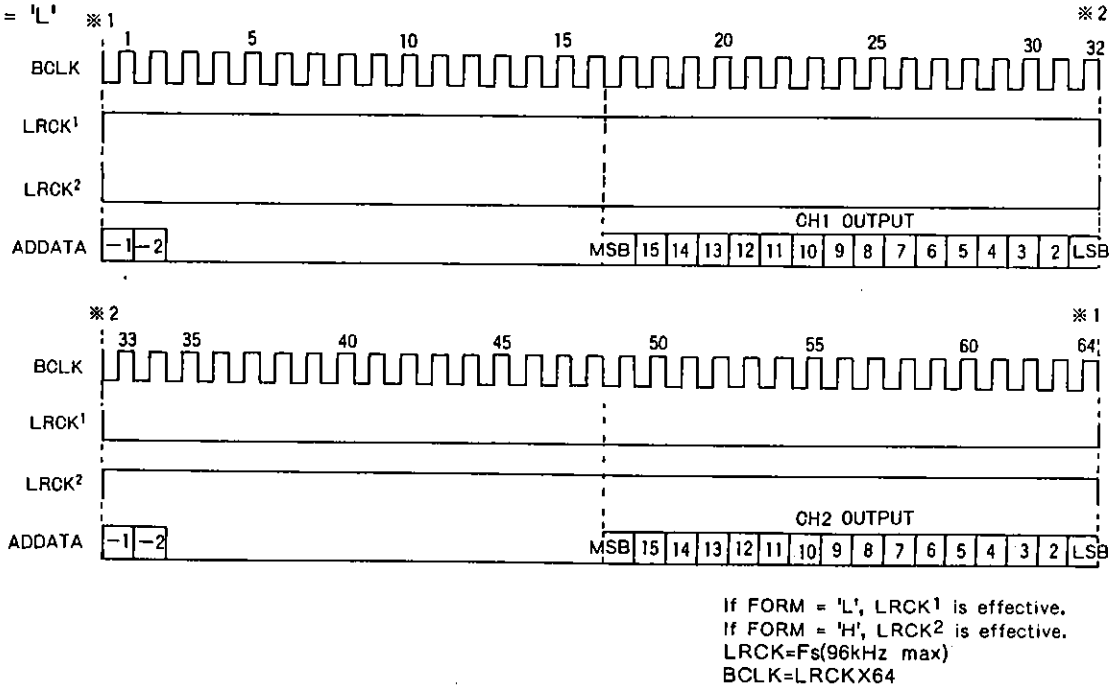
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Pin Description

Pin Number	Pin Name	Functional Description
1	ADIN1	CH1 analog input pin
2	V_H	'H' level reference voltage input pin
3	AV_{DD}	Analog supply voltage pin
4	VR1	CH1 reference voltage output pin ((VH + VL)/2)
5	TEST3	Test pin. Normally, this pin is connected to the analog GND pin.
6	AV_{DD}	Analog supply voltage pin
7	FORM	Input pin 1) FORM = 'H' level. CH1 will be selected if LRCK = 'L'. CH2 will be selected if LRCK = 'H'. 2) FORM = 'L' level. CH1 will be selected if LRCK = 'H'. CH2 will be selected if LRCK = 'L'.
8	IFDA	Input pin 18-bit digital data operation will be selected if IFDA = 'H'. 16-bit digital data operation will be selected if IFDA = 'L'.
9	LRCK	Input pin CH1 or CH2 will be selected for the output digital data (ADDATA). Refer to pin 7, 'FORM'.
10	BCLK	Input pin Bit clock pin This is the clock that enables digital data bit serial output.
11	ADDATA	Data output pin Bit serial output is started on an MSB-first basis. Output data has 2's complement form.
12	DV_{DD}	Digital supply voltage pin
13	DGND	Digital GND pin
14	TSTOUT	Test input/output pin Normally, this pin is connected to the digital GND pin.
15	TEST1	Test input pin Normally, this pin is connected to the digital GND pin.
16	TEST2	Test input pin Normally, this pin is connected to the digital GND pin.
17	TEST4	Test pin Normally, this pin is connected to the digital GND pin.
18	TEST6	Test input pin Normally, this pin is connected to the digital GND pin.
19	AGND	Analog GND pin
20	TEST5	Test output pin Normally, this pin is connected to the analog GND pin.
21	VR2	CH2 reference voltage output pin ((VH + VL)/2)
22	V_L	'L' level reference voltage input pin
23	ADIN2	CH2 analog input pin
24	AGND	Analog GND pin

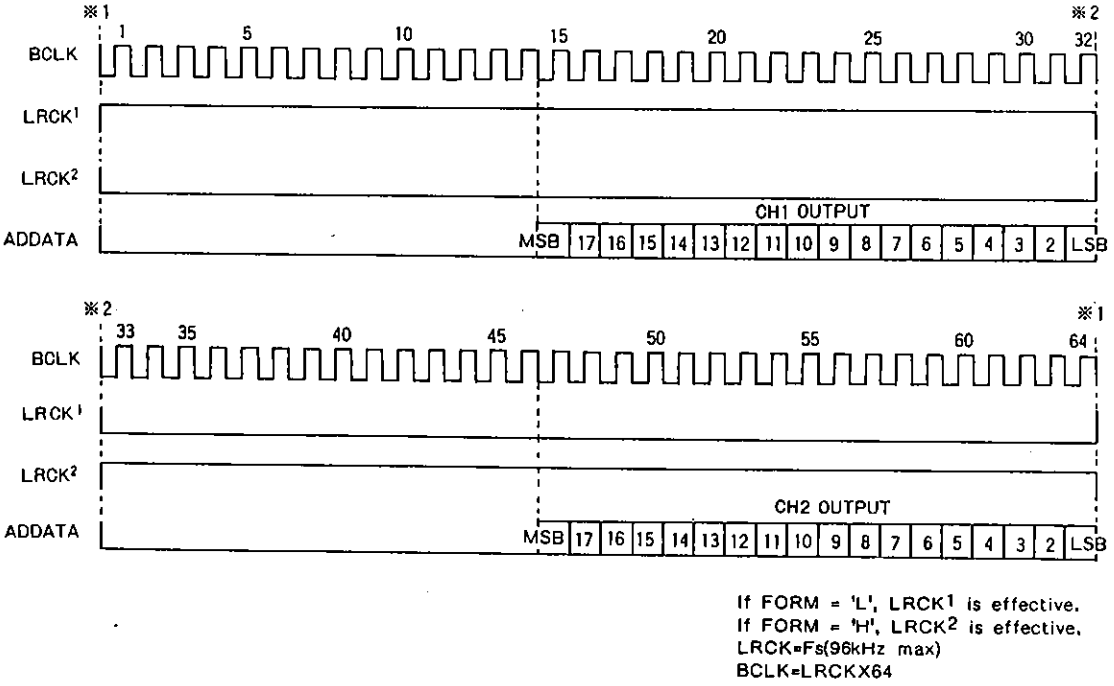
Timing Diagram

1. IFDA = 'L'



If FORM = 'L', $LRCK^1$ is effective.
If FORM = 'H', $LRCK^2$ is effective.
LRCK=Fs(96kHz max)
BCLK=LRCKX64

2. IFDA = 'H'



If FORM = 'L', $LRCK^1$ is effective.
If FORM = 'H', $LRCK^2$ is effective.
LRCK=Fs(96kHz max)
BCLK=LRCKX64

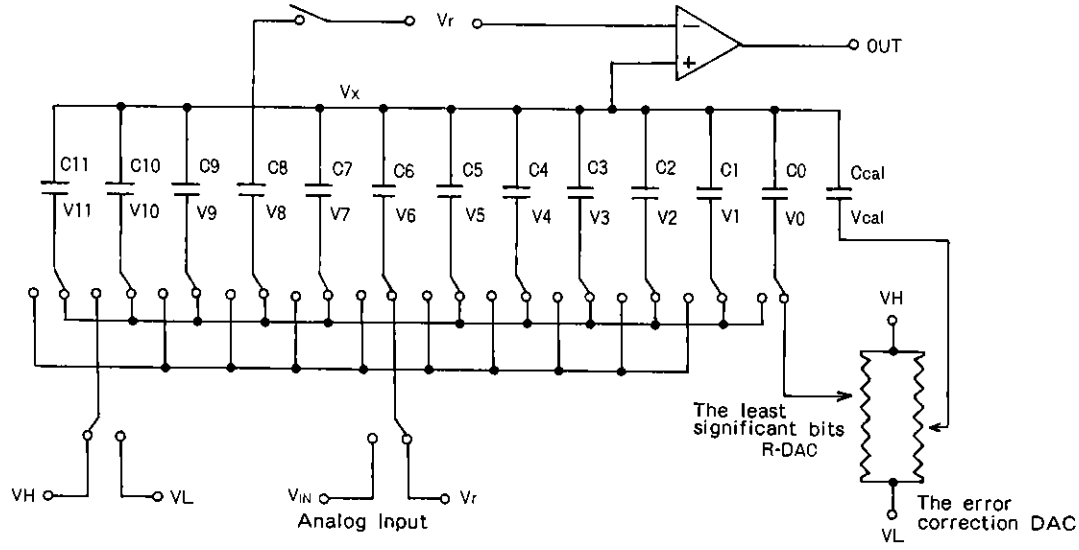
Functional Description

The LC7886 uses two, independent capacitive-array successive approximation A/D converters. When converting each sample, the most significant twelve bits are converted using a binary-ratioed capacitor array as shown in the following figure, and the least significant six bits converted using a resistor-string D/A converter. Each A/D converter also incorporates a resistor-string D/A converter for error correction.

Each of the binary-ratioed capacitors stores a charge proportional to its binary weight. The capacitive-array converter encodes the sample starting from the most-significant bit by successively comparing its approximation with the voltage of the capacitive array. The capacitors also function as sample-and-hold capacitors.

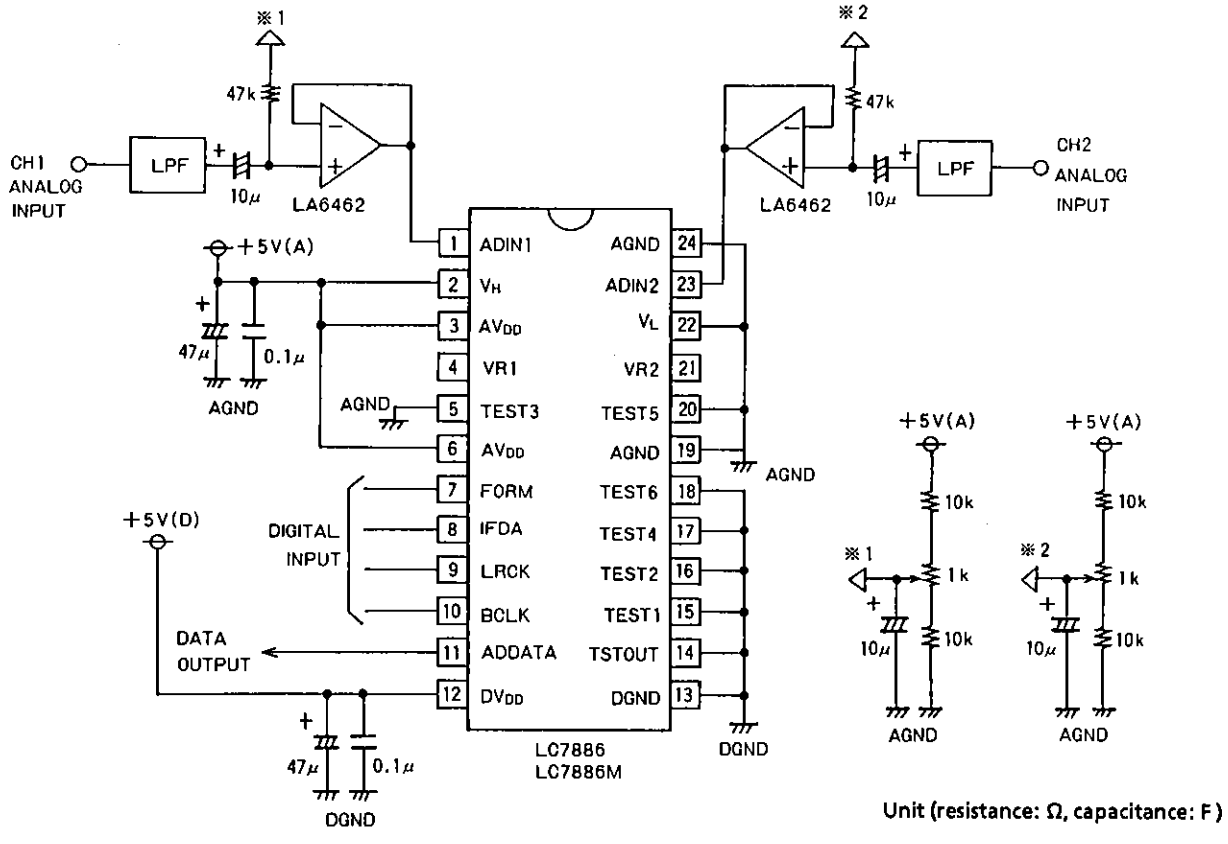
The LC7886 operates from a single supply. So that the A/D converters produce signed output, the internal reference voltage, V_R, is set at $(V_H+V_L)/2$, Where V_H and V_L are the input reference voltages.

The conversion accuracy depends upon the accuracy of the reference voltage, V_R, and the tolerances of the capacitors in the array. The accuracy of each LC7886 is tested before shipping, and then error correction data is stored in the built-in PROM. The PROM data is used during the encoding operation to correct the output of the A/D converter.



The electric charge redistribution converter

Example Application Circuit



Unit (resistance: Ω, capacitance: F)

AV_{DD}, AGND, +5V(A) --- Analog processing
DV_{DD}, DGND, +5V(D) --- Digital processing

※1 and ※2 --- Some extra works should be done so that the center voltage between V_H and V_L can be produced.
The supply voltage of input buffer LA6462 should be greater than 6V.