bq2201

SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3-volt battery-backup applications
- Write-protect control
- 3-volt primary cell inputs
- Less than 10ns chip-enable propagation delay
- 5% or 10% supply operation

General Description

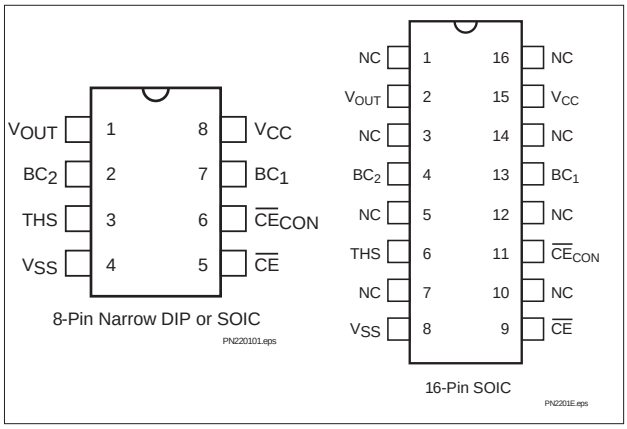
The CMOS bq2201 SRAM Nonvolatile Controller Unit provides all necessary functions for converting a standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, a conditioned chip-enable output is forced inactive to write-protect any standard CMOS SRAM.

During a power failure, the external SRAM is switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAM is write-protected until a power-valid condition exists.

The bq2201 is footprint- and timing-compatible with industry standards with the added benefit of a chip-enable propagation delay of less than 10ns.

Pin Connections



Pin Names

V_{OUT}	Supply output
BC_1—BC_2	3-volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	chip-enable active low input
$\overline{CE}_{CON}$	Conditioned chip-enable output
V_{CC}	+5-volt supply input
V_{SS}	Ground
NC	No Connect

Functional Description

An external CMOS static RAM can be battery-backed using the V_{OUT} and the conditioned chip-enable output pin from the bq2201. As V_{CC} slews down during a power failure, the conditioned chip-enable output $\overline{CE}_{CON}$ is forced inactive independent of the chip-enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS.

If THS is tied to V_{SS}, power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the $\overline{CE}_{CON}$ output is unconditionally driven high, write-protecting the memory.

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As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the V_{CC} supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ms maximum) after the supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is fed through to the $\overline{CE}_{CON}$ output with a propagation delay of less than 10ns. Nonvolatility is achieved by hardware hookup, as shown in Figure 1.

Energy Cell Inputs—BC_1, BC_2

Two primary backup energy source inputs are provided on the bq2201. The BC_1 and BC_2 inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to V_{SS}.

If both inputs are used, during power failure the V_{OUT} output is fed only by BC_1 as long as it is greater than 2.5V. If the voltage at BC_1 falls below 2.5V, an internal isolation switch automatically switches V_{OUT} from BC_1 to BC_2.

To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{CON}$ are internally isolated from BC_1 and BC_2 by either of the following:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. See Figure 2. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)*V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}.

The appropriate battery is connected to V_{OUT} and $\overline{CE}_{CON}$ immediately on subsequent application and removal of V_{CC}.

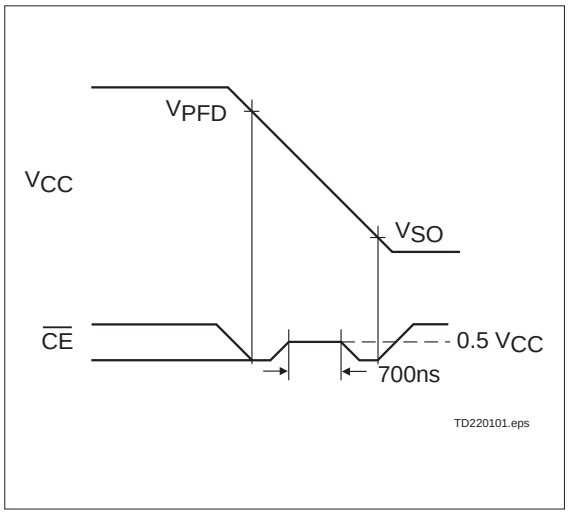


Figure 2. Battery Isolation Signal

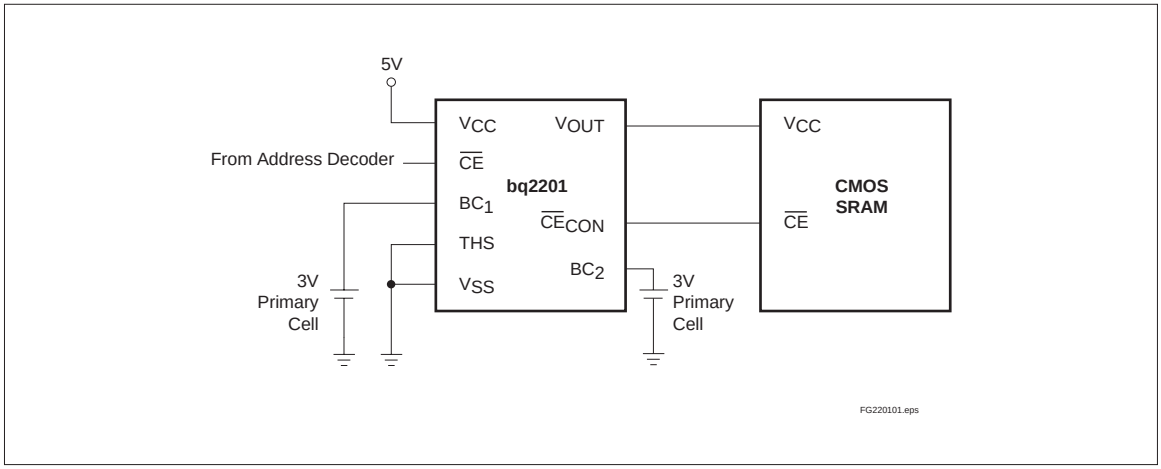


Figure 1. Hardware Hookup (5% Supply Operation)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0	-	4.0	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0mA
I_{CC}	Operating supply current	-	3	5	mA	No load on V_{OUT} and $\overline{CE}_{CON}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BC2}	-	V	V_{BC1} < 2.5V
		-	V_{BC1}	-	V	V_{BC1} > 2.5V
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

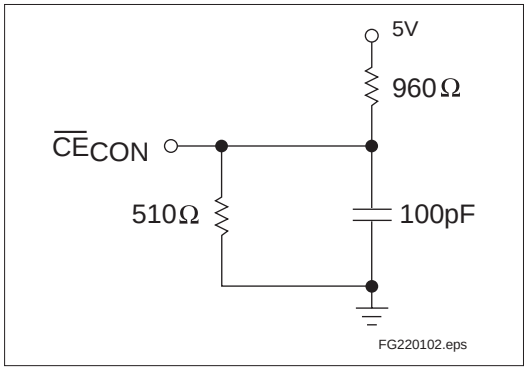


Figure 3. Output Load

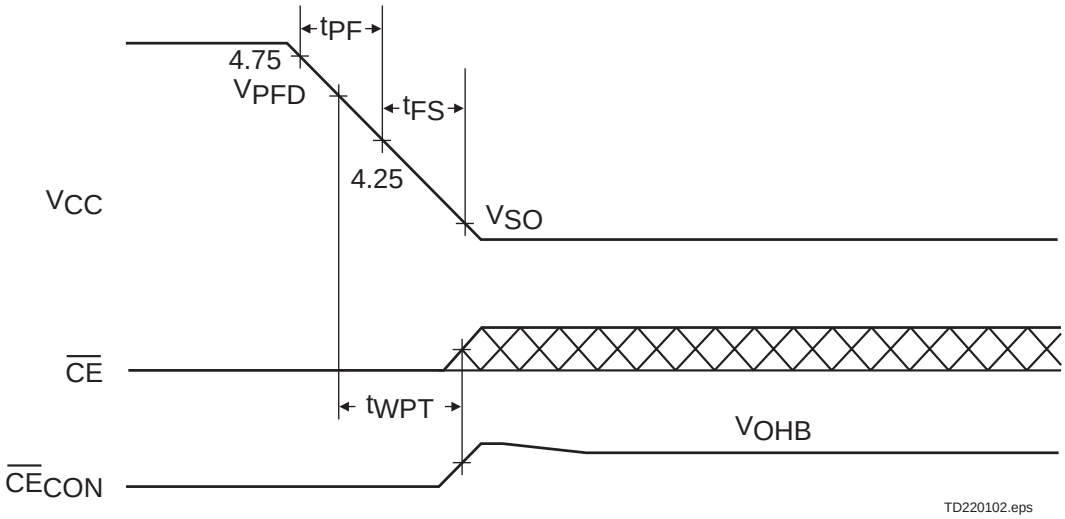
Power-Fail Control (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
t_{CER}	Chip-enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

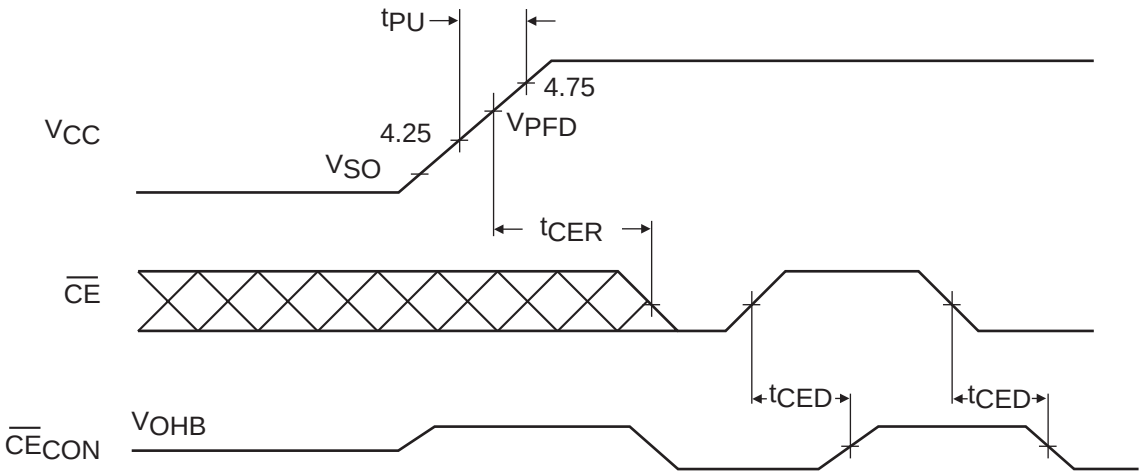
Note: Typical values indicate operation at T_A = 25°C.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down Timing

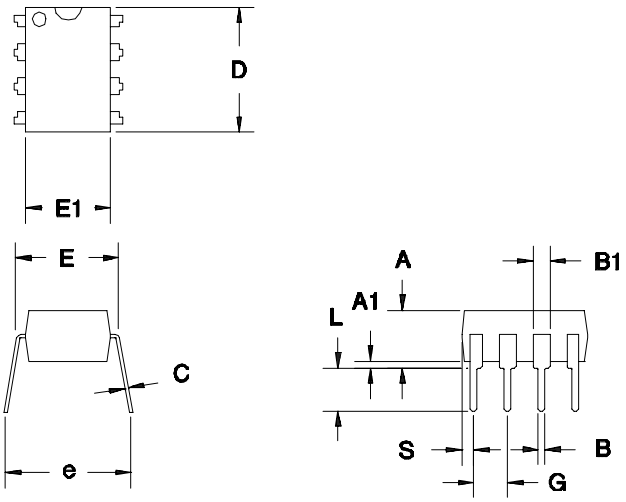


Power-Up Timing



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8-Pin DIP Narrow (PN)

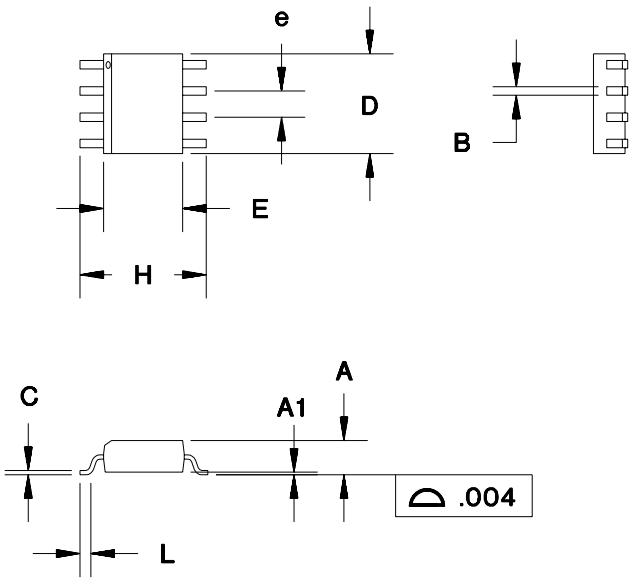


8-Pin DIP Narrow (PN)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.350	0.380
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

All dimensions are in inches.

8-Pin SOIC Narrow (SN)

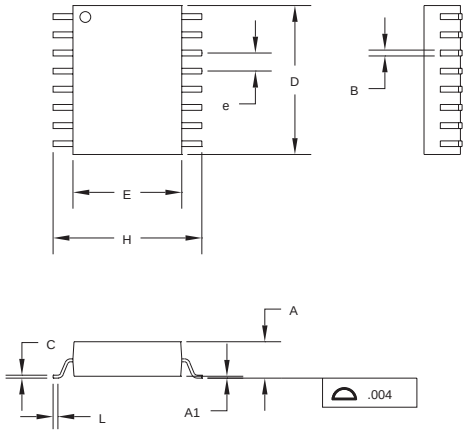


8-Pin SOIC Narrow (SN)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.185	0.200
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

S: 16-Pin SOIC



16-Pin S (SOIC)

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.400	0.415
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

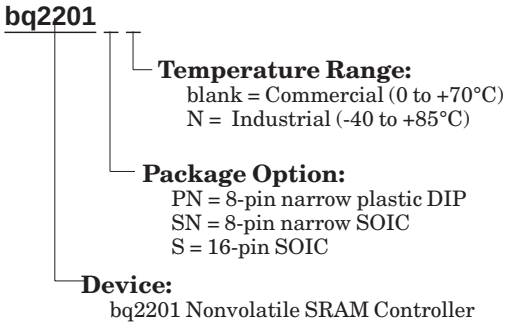
All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1		Added industrial temperature range	
2	1, 3, 4	10% supply operation	Was: THS tied to V_{OUT} Is: THS tied to V_{CC}
3	1, 9, 11	Added 16-pin package option	

Note: Change 1 = Sept. 1991 B changes from Sept. 1990 A.
Change 2 = Aug. 1997 C changes from Sept. 1991 B.
Change 3 = Oct. 1998 D changes from Aug. 1997 C.

Ordering Information



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