

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 15/20/25/35 ns (Commercial/Industrial)
 - 15/20/25/35/45 ns (Military)
- Low Power Operation
- Single 5V±10% Power Supply
- Output Enable (\overline{OE}) & Chip Enable (\overline{CE}_1 and \overline{CE}_2) Control Functions
- Data Retention with 2.0V Supply (P4C1299L)
- Three-State Outputs
- TTL/CMOS Compatible Outputs
- Fully TTL Compatible Inputs
- Standard Pinout (JEDEC Approved)
 - 28-Pin 300 mil DIP, SOJ
 - 28-Pin 350x550 mil LCC



DESCRIPTION

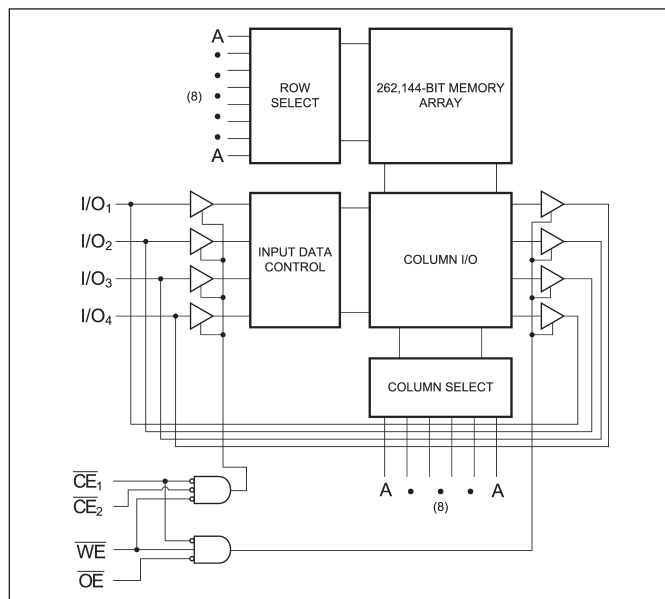
The P4C1299 and P4C1299L are a 262,144-bit ultra high-speed static RAM organized as 64Kx4. The CMOS memory requires no clock or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply. With battery backup (P4C1299L Only), data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10 μ A from a 2.0V supply.

Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system speeds. CMOS is utilized to reduce power consumption.

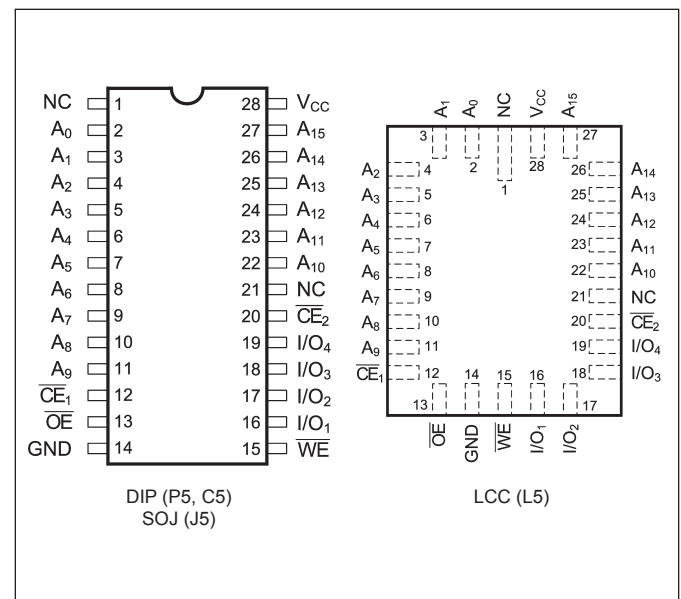
The P4C1299 and P4C1299L are available in a 28-pin 300 mil DIP or SOJ, as well as a 28-pin 350x550 mil LCC package, providing excellent board level densities.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



**MAXIMUM RATINGS⁽¹⁾**

| Sym | Parameter | Value | Unit |
|-------------------|---|-------------------------------|------|
| V _{CC} | Power Supply Pin with Respect to GND | -0.5 to +7 | V |
| V _{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to V _{CC} + 0.5 | V |
| T _A | Operating Temperature | -55 to +125 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

RECOMMENDED OPERATING CONDITIONS

| Grade ⁽²⁾ | Ambient Temp | GND | V _{CC} |
|----------------------|-----------------|-----|-----------------|
| Commercial | 0°C to 70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |

CAPACITANCES⁽⁴⁾(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

| Sym | Parameter | Conditions | Typ | Unit |
|------------------|--------------------|-----------------------|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | pF |

DC ELECTRICAL CHARACTERISTICS(Over Recommended Operating Temperature & Supply Voltage)⁽²⁾

| Sym | Parameter | Test Conditions | P4C1299 | | P4C1299L | | Unit | |
|------------------|--|--|-----------------------|-----------------------|-----------------------|-----------------------|------|----|
| | | | Min | Max | Min | Max | | |
| V _{IH} | Input High Voltage | | 2.2 | V _{CC} + 0.5 | 2.2 | V _{CC} + 0.5 | V | |
| V _{IL} | Input Low Voltage | | -0.5 ⁽³⁾ | 0.8 | -0.5 ⁽³⁾ | 0.8 | V | |
| V _{HC} | CMOS Input High Voltage | | V _{CC} - 0.2 | V _{CC} + 0.5 | V _{CC} - 0.2 | V _{CC} + 0.5 | V | |
| V _{LC} | CMOS Input Low Voltage | | -0.5 ⁽³⁾ | 0.2 | -0.5 ⁽³⁾ | 0.2 | V | |
| V _{CD} | Input Clamp Diode Voltage | V _{CC} = Min, I _{IN} = 18 mA | | -1.2 | | -1.2 | V | |
| V _{OL} | Output Low Voltage (TTL Load) | I _{OL} = +8 mA, V _{CC} = Min | | 0.4 | | 0.4 | V | |
| V _{OH} | Output High Voltage (TTL Load) | I _{OH} = -4 mA, V _{CC} = Min | 2.4 | | 2.4 | | V | |
| I _{LI} | Input Leakage Current | V _{CC} = Max, V _{IN} = GND to V _{CC} | MIL | -10 | +10 | -10 | +10 | µA |
| | | | IND/COM | -5 | +5 | -5 | +5 | |
| I _{LO} | Output Leakage Current | V _{CC} = Max, V _{OUT} = GND to V _{CC} | MIL | -10 | +10 | -10 | +10 | µA |
| | | | IND/COM | -5 | +5 | -5 | +5 | |
| I _{SB} | Standby Power Supply Current (TTL Input Levels) | $\overline{CE}_{1,2} \geq V_{IN}$, V _{CC} = Max, f = Max, Outputs Open | MIL | — | 40 | — | 35 | mA |
| | | | IND/COM | — | 30 | — | 30 | |
| I _{SB1} | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}_{1,2} \geq V_{HC}$, V _{CC} = Max, f = 0, Outputs Open V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} | MIL | — | 15 | — | 10 | mA |
| | | | IND/COM | — | 10 | — | 8 | |

N/A = Not applicable



POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Sym | Parameter | Temperature Range | -15 | -20 | -25 | -35 | -45 | Unit |
|-----------------|----------------------------|-------------------|-----|-----|-----|-----|-----|------|
| I _{CC} | Dynamic Operating Current* | Commercial | 160 | 125 | 115 | 110 | 110 | mA |
| | | Industrial | 160 | 135 | 120 | 115 | 115 | mA |
| | | Military | 160 | 150 | 120 | 120 | 120 | mA |

* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}_{1,2} = V_{IL}$

DATA RETENTION CHARACTERISTICS (P4C1299L Only)

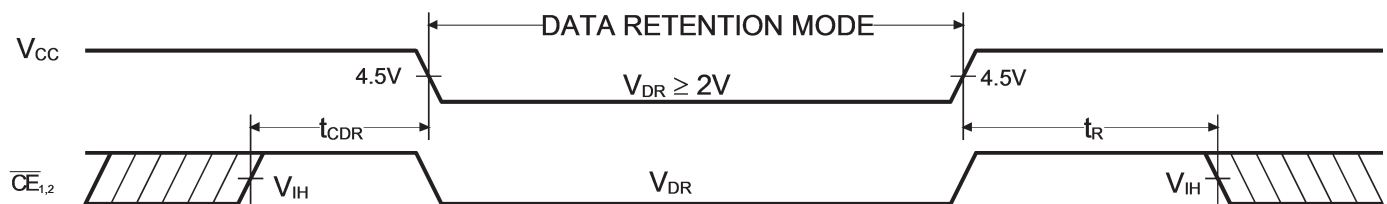
| Sym | Parameter | Test Conditions | Min | Typ* V _{CC} = | | Max V _{CC} = | | Unit |
|-----------------------------|--------------------------------------|--|------------------------------|------------------------|------|-----------------------|------|------|
| | | | | 2.0V | 3.0V | 2.0V | 3.0V | |
| V _{DR} | V _{CC} for Data Retention | | 2.0 | | | | | V |
| I _{CCDR} | Data Retention Current | $\overline{CE}_{1,2} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 10 | 15 | 1000 | 2000 | μA |
| t _{CDR} | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| t _R [†] | Operation Recovery Time | | t _{RC} [§] | | | | | ns |

* T_A = +25°C

§ t_{RC} = Read Cycle Time

† This Parameter is guaranteed but not tested

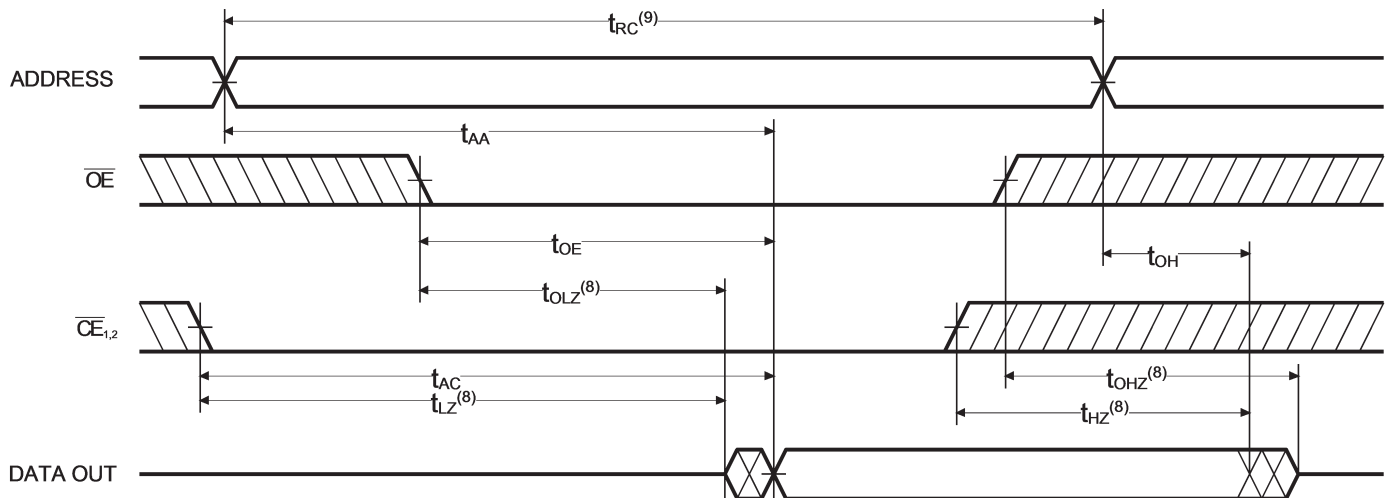
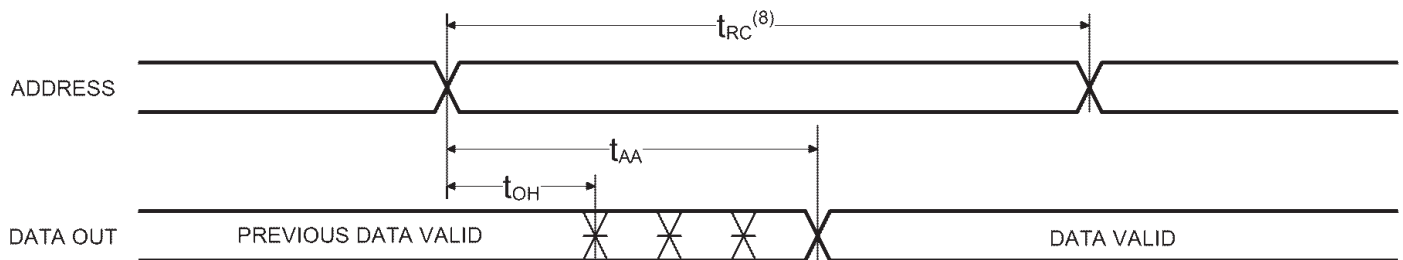
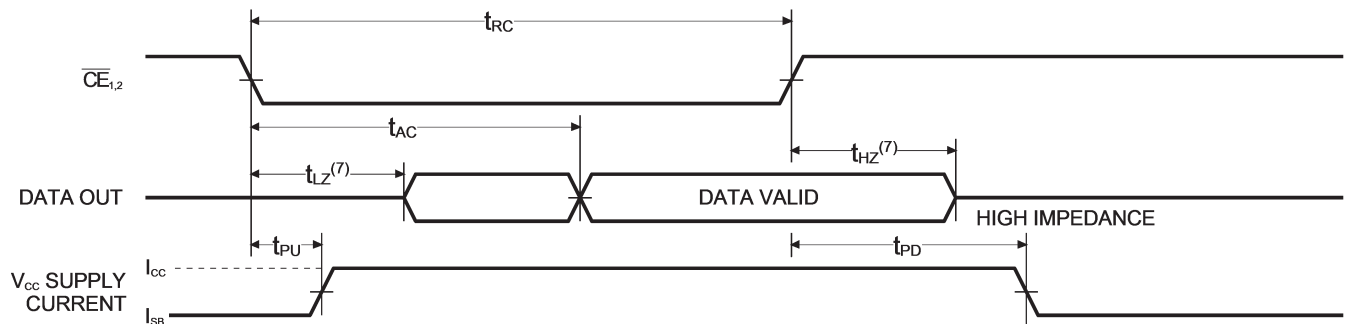
DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)⁽²⁾

| Sym | Parameter | -15 | | -20 | | -25 | | -35 | | -45 | | Unit |
|------------------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{RC} | Read Cycle Time | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| t _{AA} | Address Access Time | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| t _{AC} | Chip Enable Access Time | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| t _{OH} | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t _{LZ} | Chip Enable to Output in Low Z | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZ} | Chip Disable to Output in High Z | | 8 | | 10 | | 15 | | 15 | | 20 | ns |
| t _{OE} | Output Enable Low to Data Valid | | 8 | | 10 | | 15 | | 25 | | 30 | ns |
| t _{OLZ} | Output Enable Low to Low Z | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{OHZ} | Output Enable High to High Z | | 9 | | 9 | | 15 | | 20 | | 20 | ns |
| t _{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PD} | Chip Disable to Power Down | | 15 | | 20 | | 25 | | 35 | | 45 | ns |

**TIMING WAVEFORM OF READ CYCLE NO. 1 (\overline{OE} CONTROLLED)⁽⁵⁾****TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)^(5,6)****TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}_{1,2}$ CONTROLLED)^(5,6)****Notes:**

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_L and I_L not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.
- \overline{CE}_1 and \overline{CE}_2 are LOW and \overline{WE} is HIGH for READ cycle.
- \overline{WE} is HIGH and ADDRESS must be valid prior to, or coincident with \overline{CE}_1 and \overline{CE}_2 transitions LOW.
- Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
- Read Cycle Time is measured from the last valid address to the first transitioning address.

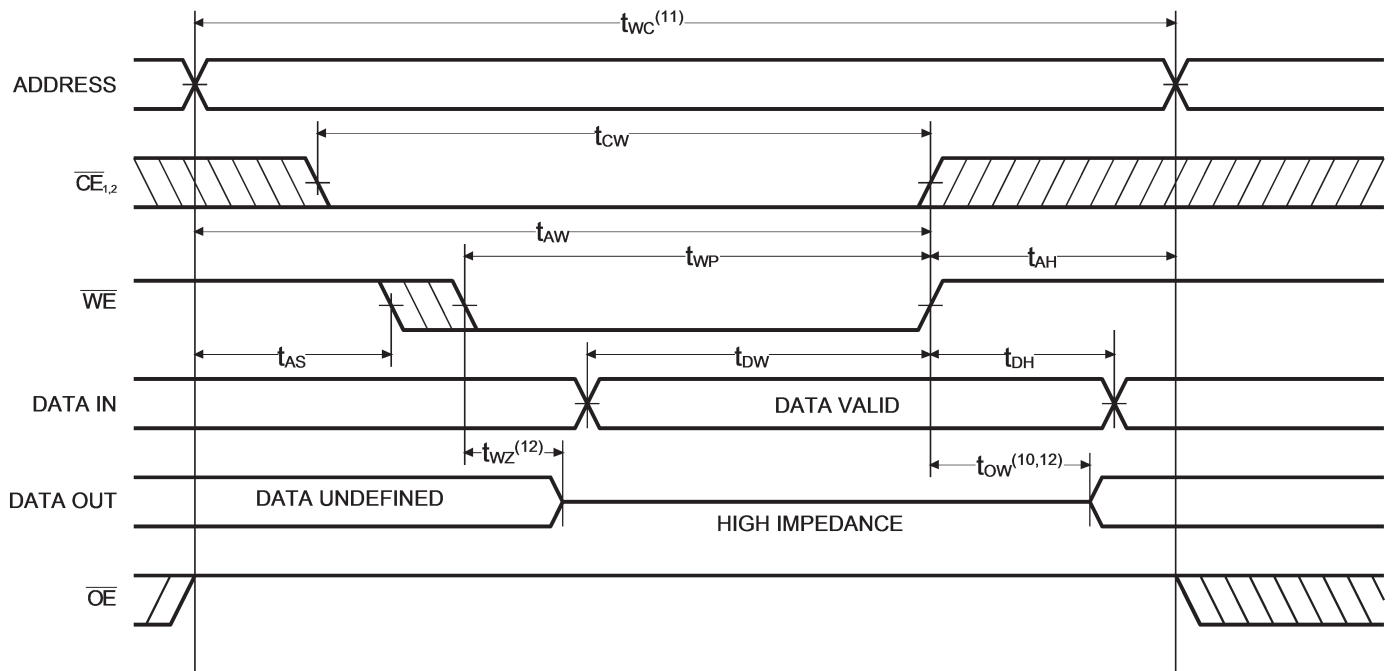


AC CHARACTERISTICS—WRITE CYCLE

($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Sym | Parameter | -15 | | -20 | | -25 | | -35 | | -45 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 8 | | 10 | | 12 | | 15 | | 18 | | ns |
| t_{AW} | Address Valid to End of Write | 8 | | 10 | | 12 | | 15 | | 18 | | ns |
| t_{AS} | Address Setup Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 8 | | 10 | | 12 | | 15 | | 18 | | ns |
| t_{AH} | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 7 | | 8 | | 10 | | 12 | | 15 | | ns |
| t_{DH} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 6 | | 7 | | 8 | | 10 | | 15 | ns |
| t_{OW} | Output Active from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽⁹⁾



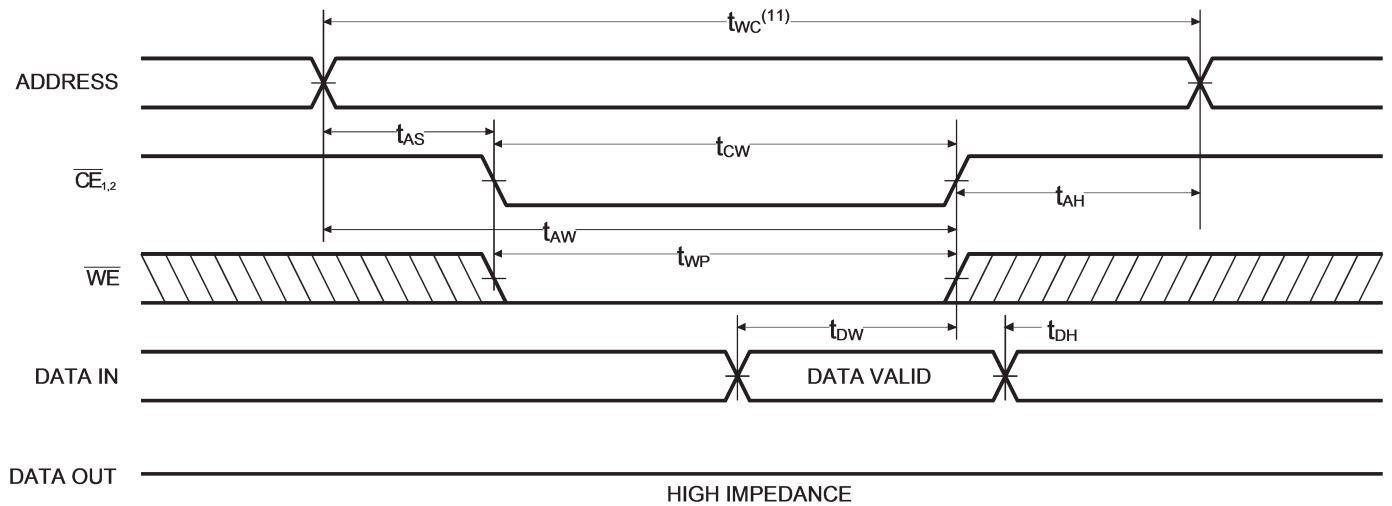
Notes:

10. $\overline{CE}_{1,2}$ and \overline{WE} must be LOW for WRITE cycle.
11. \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
12. If $\overline{CE}_{1,2}$ goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.

13. Write Cycle Time is measured from the last valid address to the first transitioning address.



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽¹⁰⁾



AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

TRUTH TABLE

| Mode | \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | I/O | Power |
|---------------------|-------------------|--------|-----------------|-----------------|----------|---------|
| Deselect/Power-Down | H | X | X | X | High Z | Standby |
| | X | H | X | X | | |
| Read | L | L | H | L | Data Out | Active |
| Write | L | L | L | X | Data In | Active |
| Deselect | L | L | H | H | High Z | Active |

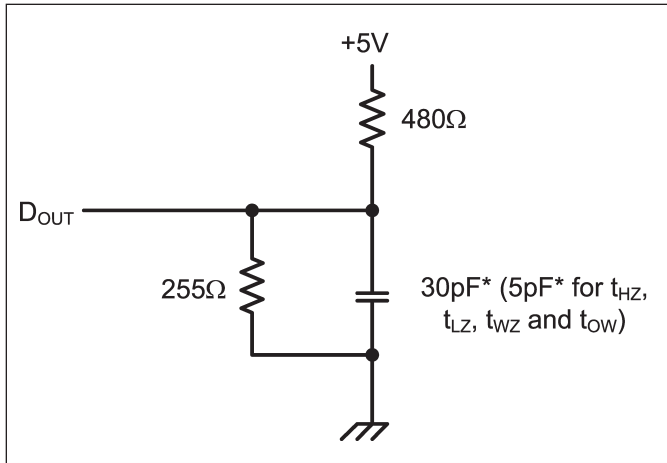


Figure 1. Output Load

* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C1299, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor

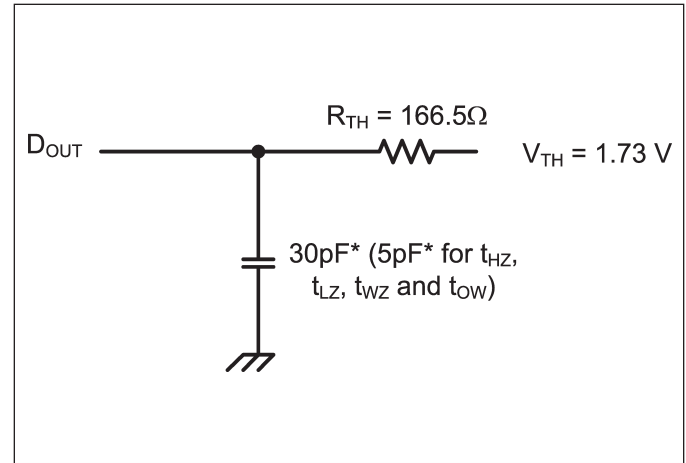


Figure 2. Thevenin Equivalent

is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).



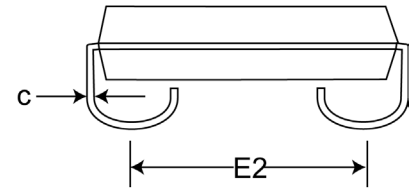
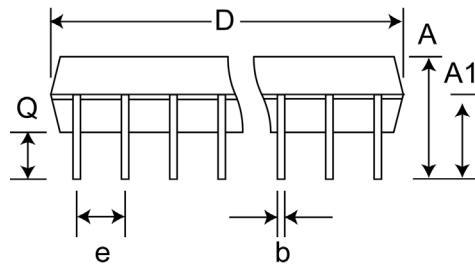
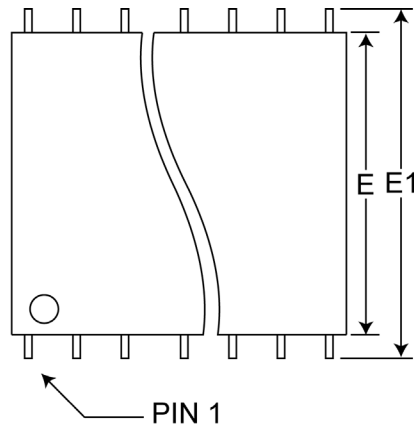
ORDERING INFORMATION

| <u>P4C1299</u> Device Type | <u>xx</u> Speed | <u>x</u> Package | <u>x</u> Processing | |
|-------------------------------|--------------------|---------------------|------------------------|--|
| | | | C | 0°C to +70°C |
| | | | I | -40°C to +85°C |
| | | | M | -55°C to +125°C |
| | | | MB | Mil Temp with MIL-STD-883 Class B Compliance |
| | | | C | Ceramic side brazed DIP, 300 mil |
| | | | J | Plastic SOJ, 300 mil |
| | | | P | Plastic DIP, 300 mil |
| | | | L | Rectangular LCC (350x550 mil) |
| | | | | 15, 20, 25, 35, 45 ns |
| | | | | 64K x 4 SRAM |



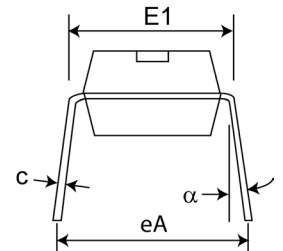
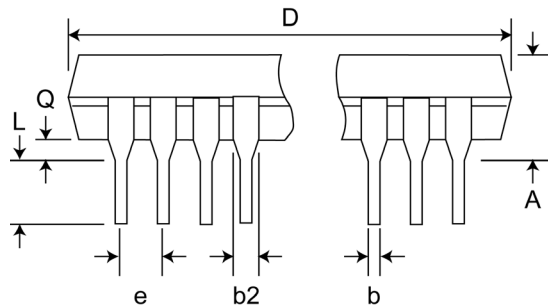
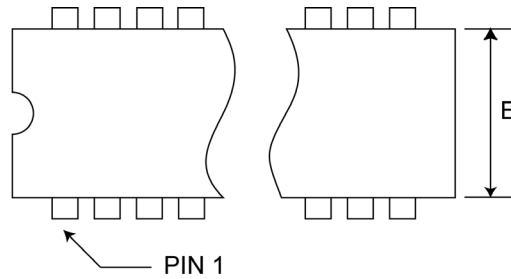
| Pkg # | J5 | |
|--------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | 0.120 | 0.148 |
| A1 | 0.078 | - |
| b | 0.014 | 0.020 |
| C | 0.007 | 0.011 |
| D | 0.700 | 0.730 |
| e | 0.050 BSC | |
| E | 0.292 | 0.300 |
| E1 | 0.335 | 0.347 |
| E2 | 0.262 | 0.272 |
| Q | 0.025 | - |

SOJ SMALL OUTLINE IC PACKAGE



| Pkg # | P5 | |
|----------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.210 |
| A1 | - | - |
| b | 0.014 | 0.023 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 1.345 | 1.400 |
| E1 | 0.270 | 0.300 |
| E | 0.300 | 0.380 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| α | 0° | 15° |

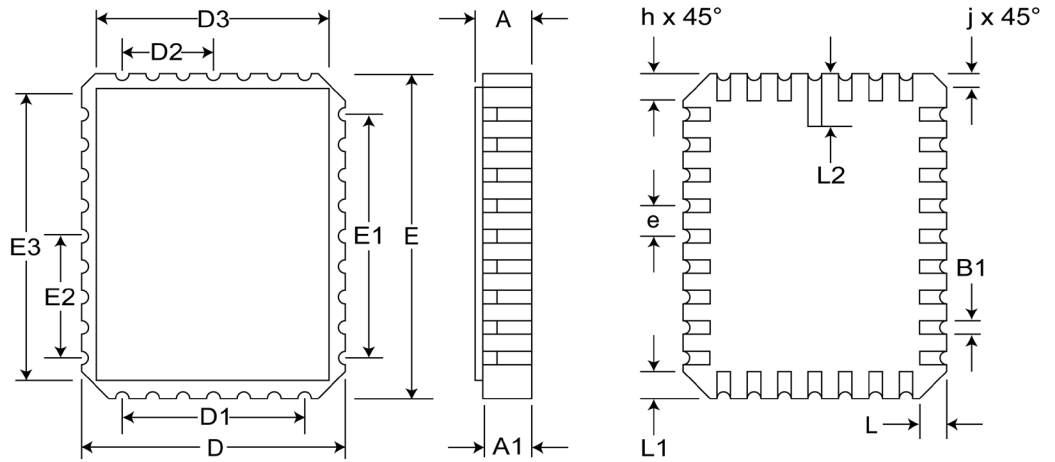
PLASTIC DUAL IN-LINE PACKAGE





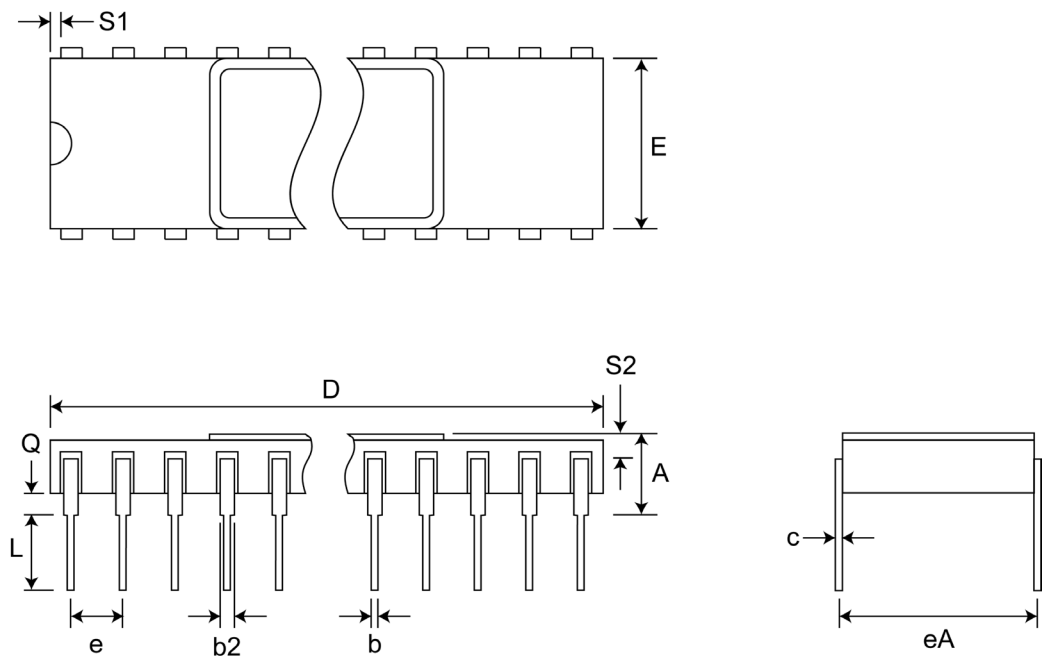
RECTANGULAR LEADLESS CHIP CARRIER

| | | |
|--------|-----------|-------|
| Pkg # | L5 | |
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.342 | 0.358 |
| D1 | 0.200 BSC | |
| D2 | 0.100 BSC | |
| D3 | - | 0.358 |
| E | 0.540 | 0.560 |
| E1 | 0.400 BSC | |
| E2 | 0.200 BSC | |
| E3 | - | 0.558 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.095 |
| ND | 5 | |
| NE | 9 | |



| | | |
|--------|--------------|-------|
| Pkg # | C5 | |
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDEBRAZED DUAL IN-LINE PACKAGE





REVISIONS

| | |
|------------------------|---|
| DOCUMENT NUMBER | SRAM 144 |
| DOCUMENT TITLE | P4C1299/P4C1299L - ULTRA HIGH SPEED 64K x 4 STATIC CMOS RAM |

| REV | ISSUE DATE | ORIGINATOR | DESCRIPTION OF CHANGE |
|------------|-------------------|-------------------|------------------------------|
| OR | Nov-2012 | JDB | New Data Sheet |