+5V TO ±10V VOLTAGE CONVERTER

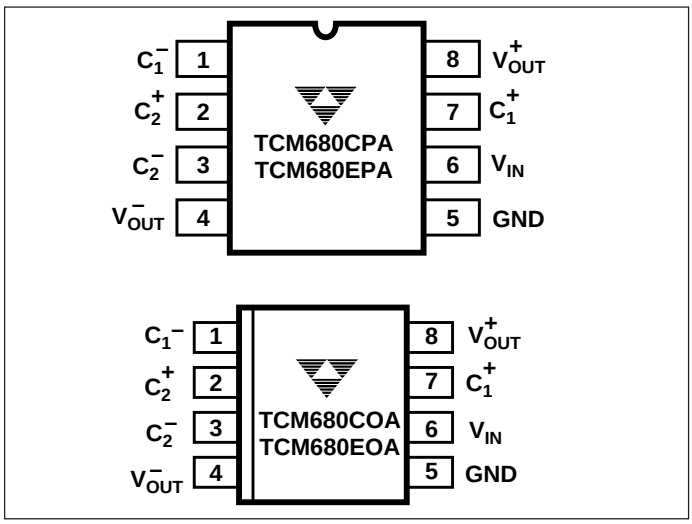
FEATURES

- **99% Voltage Conversion Efficiency**
- **85% Power Conversion Efficiency**
- **Wide Voltage Range .....+2.0V to +5.5V**
- **Only 4 External Capacitors Required**
- **Space Saving 8-Pin SOIC Design**

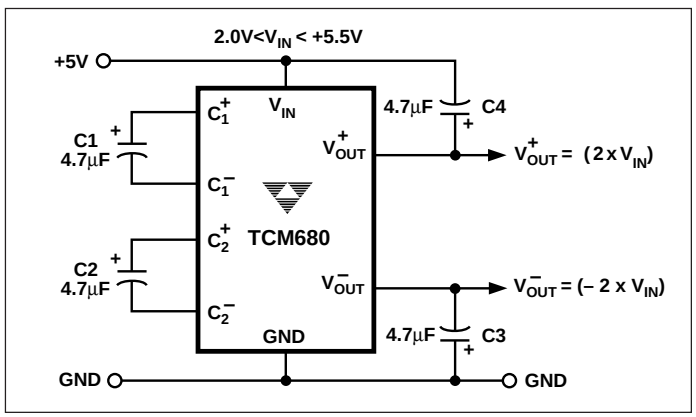
APPLICATIONS

- **±10V From +5V Logic Supply**
- **±6V From a 3V Lithium Cell**
- **Handheld Instruments**
- **Portable Cellular Phones**
- **LCD Display Bias Generator**
- **Panel Meters**
- **Operational Amplifier Power Supplies**

PIN CONFIGURATIONS (DIP AND SOIC)



TYPICAL OPERATING CIRCUIT



GENERAL DESCRIPTION

The TCM680 is a dual charge pump voltage converter that develops output voltages of $+2V_{IN}$ and $-2V_{IN}$ from a single input voltage of +2.0V to +5.5V. Common applications include ±10V from a single +5V logic supply, and ±6V from a +3V lithium battery.

The TCM680 is packaged in a space-saving 8-pin SOIC package and requires only four inexpensive external capacitors. The charge pumps are clocked by an on-board 8kHz oscillator. Low output source impedances (typically 150Ω) provides maximum output currents of 10mA for each output. Typical power conversion efficiency is 85%.

High efficiency, small installed size and low cost make the TCM680 suitable for a wide variety of applications that need both positive and negative power supplies derived from a single input voltage.

4

ORDERING INFORMATION

Part No.	Package	Temperature
TCM680COA	8-Pin SOIC	0°C to +70°C
TCM680CPA	8-Pin Plastic DIP	0°C to +70°C
TCM680EOA	8-Pin SOIC	– 40°C to +85°C
TCM680EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660EV	***Charge Pump Family Evaluation Kit***	

TCM680

ABSOLUTE MAXIMUM RATINGS*

V_{IN} ..... +6.0V
V^+_{OUT} ..... +12.0V
V^-_{OUT} ..... – 12.0V
V^-_{OUT} Short-Circuit Duration ..... Continuous
V^+_{OUT} Current 75mA
V_{IN} dV/dT 1V/µsec

Power Dissipation ($T_A \le 70°C$)
Plastic DIP 730mW
Small Outline 470mW
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or other conditions above those indicated in the operation section of the specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{IN} = +5V, T_A = +25°C, test circuit Figure 1, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Supply Voltage Range	MIN. ≤ T_A ≤ MAX., R_L = 2kΩ	2.0	1.5 to 5.5	5.5	V
	Supply Current	V_{IN} = 3V, R_L = ∞	—	0.5	1	mA
		V_{IN} = 5V, R_L = ∞	—	1	2	
		V_{IN} = 5V, 0°C ≤ T_A ≤ +70°C, R_L = ∞	—	—	2.5	
		V_{IN} = 5V, – 40°C ≤ T_A ≤ +85°C, R_L = ∞	—	—	3	
	Negative Charge Pump Output Source Resistance	I^-_L = 10mA, I^+_L = 0mA, V_{IN} = 5V	—	140	180	Ω
		I^-_L = 5mA, I^+_L = 0mA, V_{IN} = 2.8V	—	180	250	
		I^-_L = 10mA, I^+_L = 0mA, V_{IN} = 5V:				
		0°C ≤ T_A ≤ +70°C	—	—	220	
		– 40°C ≤ T_A ≤ +85°C	—	—	250	
	Positive Charge Pump Output Source Resistance	I^+_L = 10mA, I^-_L = 0mA, V_{IN} = 5V	—	140	180	Ω
		I^+_L = 5mA, I^-_L = 0mA, V_{IN} = 2.8V	—	180	250	
		I^+_L = 10mA, I^-_L = 0mA, V_{IN} = 5V:				
		0°C ≤ T_A ≤ +70°C	—	—	220	
		– 40°C ≤ T_A ≤ +85°C	—	—	250	
F_{OSC}	Oscillator Frequency		—	21	—	kHz
P_{EFF}	Power Efficiency	R_L = 2kΩ	—	85	—	%
$V_{OUT}E_{FF}$	Voltage Conversion Efficiency	V^+_{OUT}, R_L = ∞	97	99	—	%
		V^-_{OUT}, R_L = ∞	97	99	—	

TelCom Semiconductor reserves the right to make changes in the circuitry or specifications detailed in this manual at any time without notice. Minimums and maximums are guaranteed. All other specifications are intended as guidelines only. TelCom Semiconductor assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

PIN DESCRIPTION

8-Pin DIP/SOIC	Symbol	Description
1	C^-_1	Input. Capacitor C1 negative terminal.
2	C^+_2	Input. Capacitor C2 positive terminal.
3	C^-_2	Input. Capacitor C2 negative terminal.
4	V^-_{OUT}	Output. Negative output voltage (–2V_{IN}).
5	GND	Input. Device ground.
6	V_{IN}	Input. Power supply voltage.
7	C^+_1	Input. Capacitor C1 positive terminal.
8	V^+_{OUT}	Output. Positive output voltage (+2V_{IN})

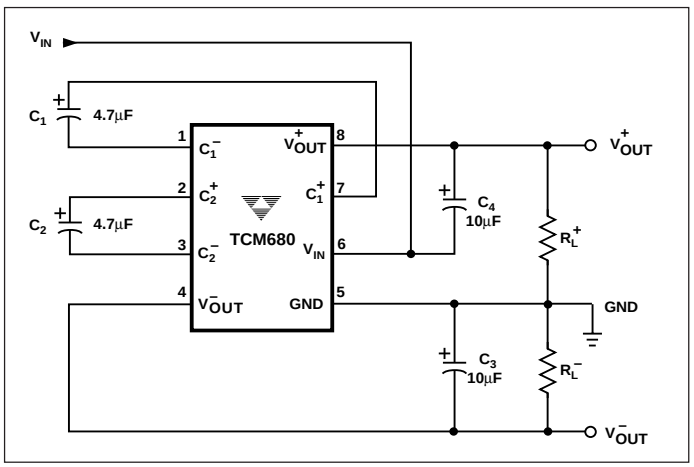


Figure 1. Test Circuit

DETAILED DESCRIPTION

Phase 1

V_{SS} charge storage – The positive side of capacitors C_1 and C_2 are connected to +5V at the start of this phase. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

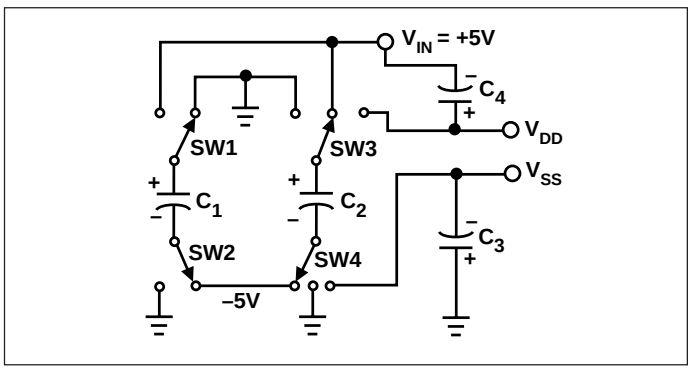


Figure 2. Charge Pump – Phase 1

Phase 2

V_{SS} transfer – Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor C_3 and the positive terminal of C_2 to ground, transferring the generated –10V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

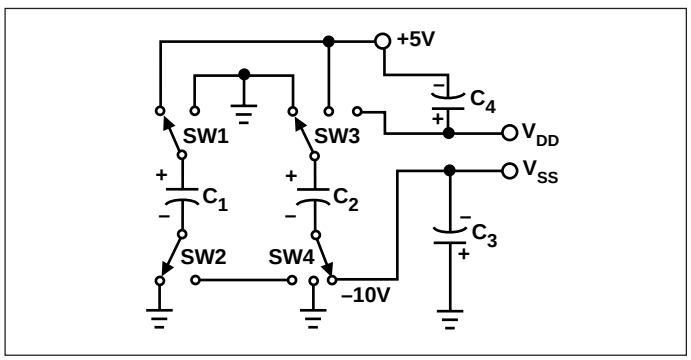


Figure 3. Charge Pump – Phase 2

Phase 3

V_{DD} charge storage – The third phase of the clock is identical to the first phase – the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

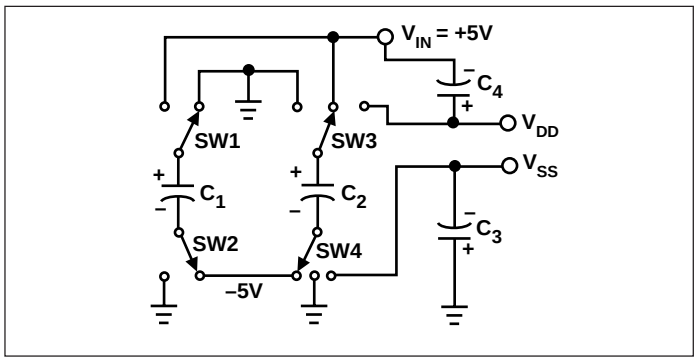


Figure 4. Charge Pump – Phase 3

Phase 4

V_{DD} transfer – The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

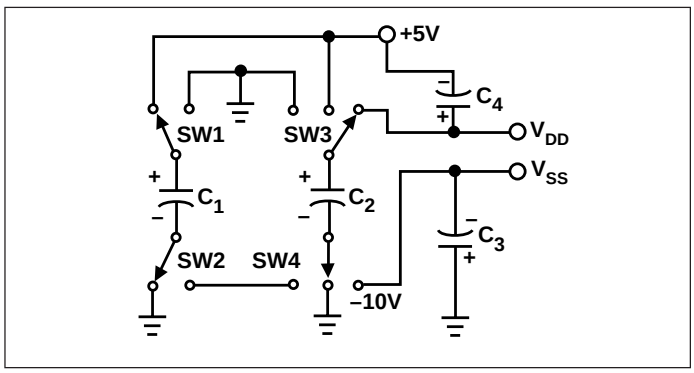


Figure 5. Charge Pump – Phase 4

MAXIMUM OPERATING LIMITS

The TCM680 has on-chip zener diodes that clamp V_{IN} to 5.8V, V_{OUT}^+ to 11.6V, and $V_{\overline{OUT}}$ to –11.6V. Never exceed the maximum supply voltage or excessive current will be shunted by these diodes, potentially damaging the chip. The TCM680 will operate over the entire operating temperature range with an input voltage of 2V to 5.5V.

EFFICIENCY CONSIDERATIONS

Theoretically a charge pump can approach 100% efficiency under the following conditions:

- The charge Pump switches have virtually no offset and extremely low on resistance
- Minimal power is consumed by the drive circuitry
- The impedances of the reservoir and pump capacitors are negligible

For the TCM680, efficiency is as shown below:

$$\text{Efficiency } V^+ = V_{DD}/(2V_{IN})$$
$$V_{DD} = 2V_{IN} - V^+_{DROP}$$
$$V^+_{DROP} = (I^+_{OUT})(R^+_{OUT})$$

$$\text{Efficiency } V^- = V_{SS}/(-2V_{IN})$$
$$V_{SS} = 2V_{IN} - V^-_{DROP}$$
$$V^-_{DROP} = (I^-_{OUT})(R^-_{OUT})$$

$$\text{Power Loss} = (V^+_{DROP})(I^+_{OUT}) + (V^-_{DROP})(I^-_{OUT})$$

There will be a substantial voltage difference between ($V^+_{OUT} - V_{IN}$) and V_{IN} for the positive pump and between V^+_{OUT} and V_{OUT} if the impedances of the pump capacitors C_1 and C_2 are high with respect to the output loads.

Larger values of reservoir capacitors C_3 and C_4 will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency. See "Capacitor Selection" in Applications Section.

APPLICATIONS

Positive and negative Converter

The most common application of the TCM680 is as a dual charge pump voltage converter which provides positive and negative outputs of two times a positive input voltage. The simple circuit of Figure 6 performs this same function using the TCM680 and external capacitors, C_1, C_2, C_3 and C_4.

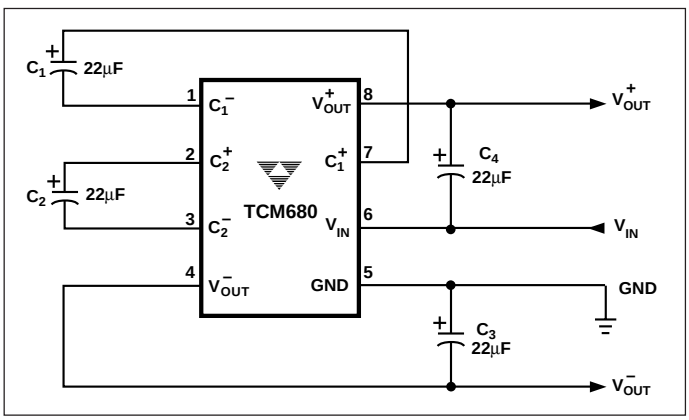


Figure 6. Positive and Negative Converter

Capacitor Selection

The TCM680 requires only 4 external capacitors for operation. These can be inexpensive polarized aluminum electrolytic types. For the circuit in Figure 6 the output characteristics are largely determined by the external capacitors. An expression for R_{OUT} can be derived as shown below:

$$R^+_{OUT} = 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C4}$$

$$R^-_{OUT} = 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C3}$$

Assuming all switch resistances are approximately equal...

$$R^+_{OUT} = 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C4} + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2)$$

$$R^-_{OUT} = 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C3} + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2)$$

R_{OUT} is typically 140Ω at +25°C with V_{IN} = +5V and C1 and C2 as 4.7µF low ESR capacitors. The fixed term ($32R_{SW}$) is about 130Ω. It can be seen easily that increasing or decreasing values of C1 and C2 will affect efficiency by changing R_{OUT}. However, be careful about ESR. This term can quickly become dominant with large electrolytic capacitors. Table 1 shows R_{OUT} for various values of C1 and C2 (assume 0.5Ω ESR). C1 and C4 must be rated at 6VDC or greater while C2 and C3 must be rated at 12VDC or greater.

Output voltage ripple is affected by C3 and C4. Typically the larger the value of C3 and C4 the less the ripple for a given load current. The formula for $V_{RIPPLE(p-p)}$ is given below:

$$V_{RIPPLE(p-p)} = \{1/[2(f_{PUMP}/3) \times C4] + 2(ESR_{C4})\}(I^+_{OUT})$$
$$V_{RIPPLE(p-p)} = \{1/[2(f_{PUMP}/3) \times C3] + 2(ESR_{C3})\}(I^-_{OUT})$$

For a 10µF (0.5Ω ESR) capacitor for C3, C4, f_{PUMP} = 21kHz and I_{OUT} = 10mA the peak-to-peak ripple voltage at the output will be less than 100mV. In most applications (I_{OUT} <= 10mA) 10-20µF output capacitors and 1-5µF pump capacitors will suffice. Table 2 shows V_{RIPPLE} for different values of C3 and C4 (assume 1Ω ESR).

Table 1. R_{OUT} vs. C1 ,C2

C1, C2 (μF)	R_{OUT} (Ω)
0.1	1089
0.47	339
1	232
3.3	165
4.7	157
10	146
22	141
100	137

Table 2. $V_{RIPPLE\ (p-p)}$ vs. C3, C4 (I_{OUT} = 10mA)

C3, C4 (μF)	V_{RIPPLE} (mV)
0.47	1540
1	734
3.3	236
4.7	172
10	91
22	52
100	27

Paralleling Devices

Paralleling multiple TCM680s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure 7, each requires separate pump capacitors C_1 and C_2, but all can share a single set of reservoir capacitors.

±5V Regulated Supplies From A Single 3V Battery

Figure 8 shows a complete ±5V power supply using one 3V battery. The TCM680 provides +6V at V^+_{OUT}, which is regulated to +5V by the TC55, and –5V by the negative LDO. The input to the TCM680 can vary from 3V to 6V without affecting regulation appreciably. With higher input voltage, more current can be drawn from the outputs of the TCM680. With 5V at V_{IN}, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150Ω source resistance for both converters, with $(I^+_L + I_L)$ = 20mA, the positive charge pump will droop 3V, providing +7V for the negative charge pump.

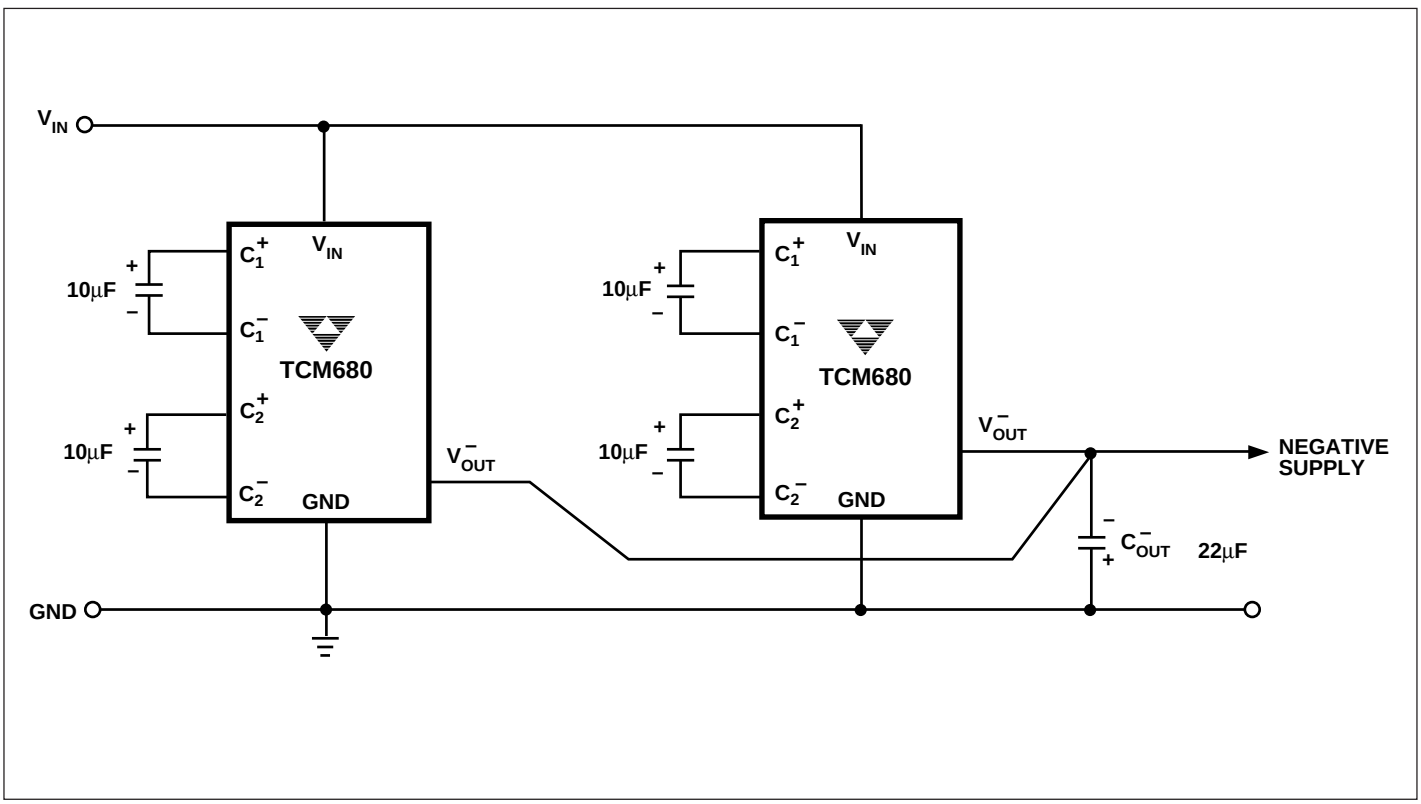


Figure 7. Paralleling TCM680 for Lower Output Source Resistance

TCM680

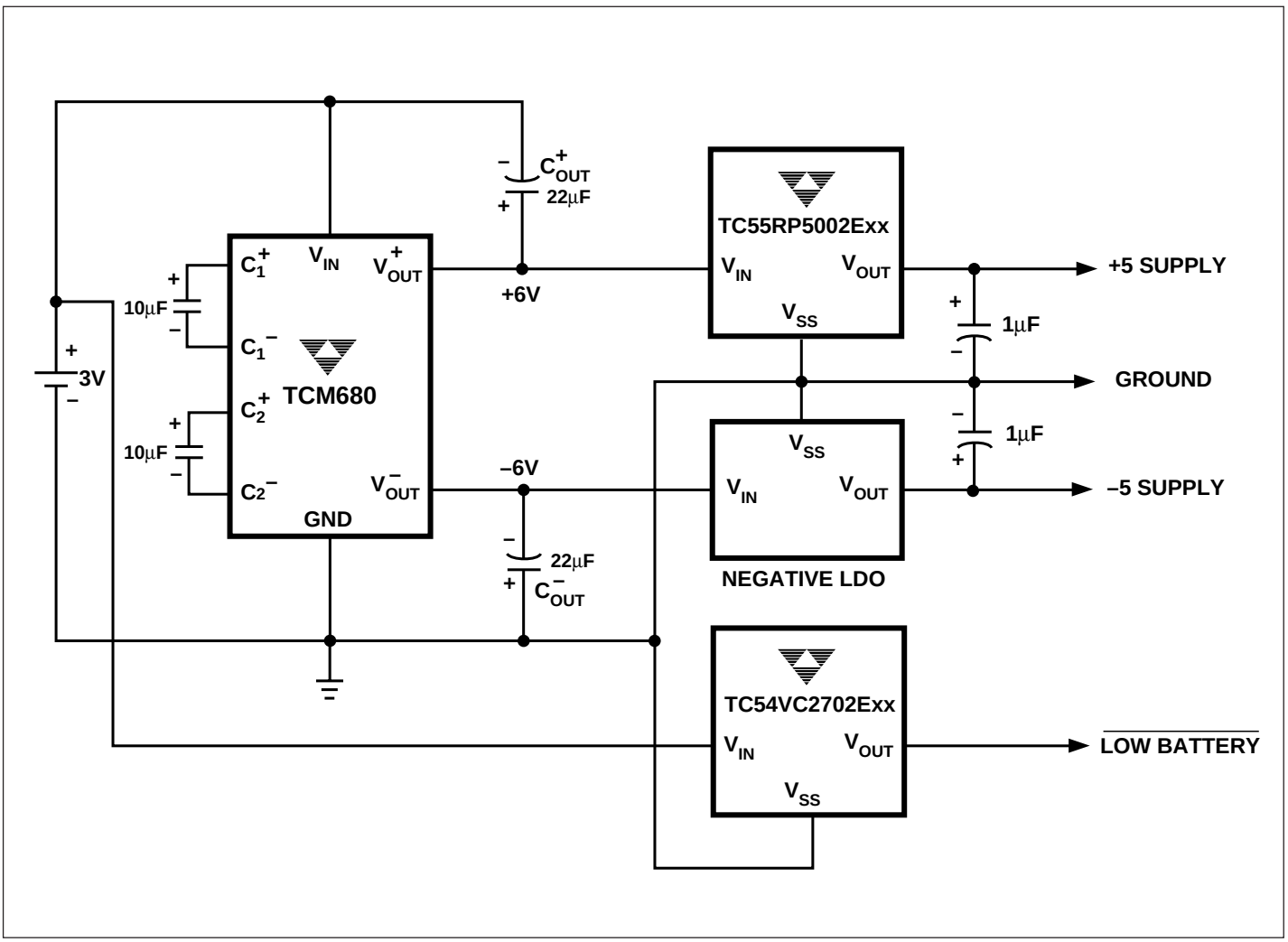
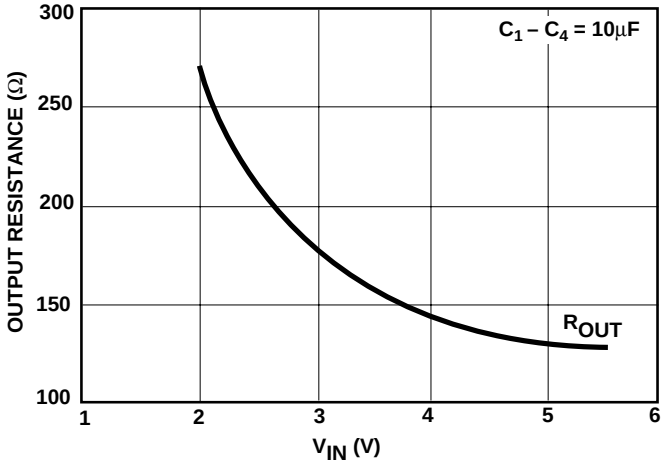


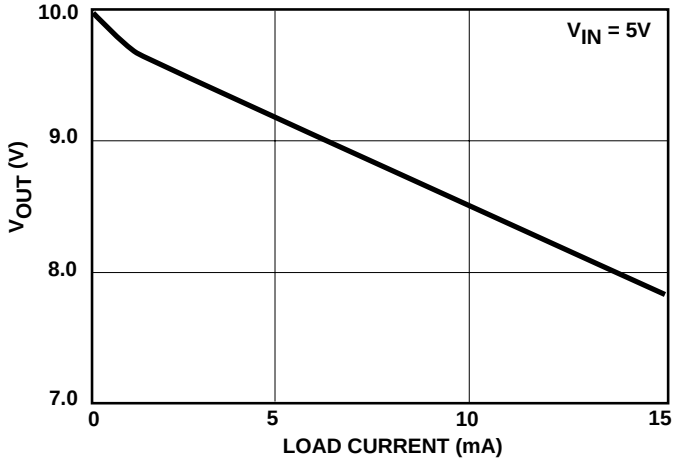
Figure 8. Split Supply Derived from 3V Battery

TYPICAL CHARACTERISTICS

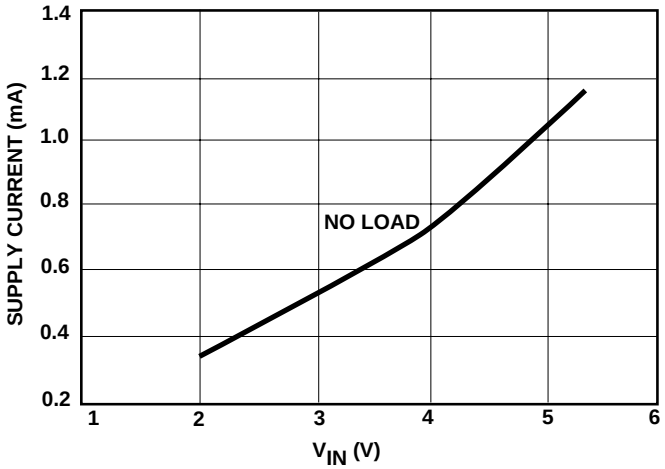
V^+_{OUT} or V^-_{OUT}
Output Resistance vs. V_{IN}



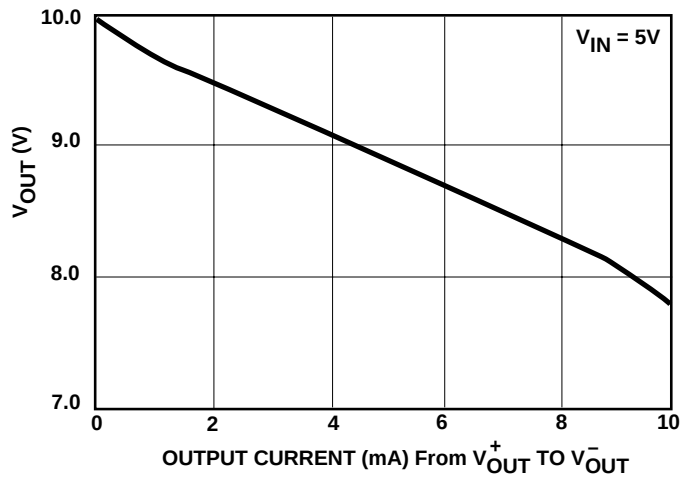
V^+_{OUT} or V^-_{OUT} vs. Load Current



Supply Current vs. V_{IN}



Output Voltage vs. Output Current From V^+_{OUT} to V^-_{OUT}



Output Source Resistance vs. Temperature

