TF Semiconductor Solutions

TF2117/TF2118

Single Channel Driver

Features

- **Floating channel in bootstrap operation to 600V**
- **Drives one N-channel MOSFET or IGBT**
- **Outputs tolerant to negative transients**
- **Wide logic supply: 10V to 20V**
- **Schmitt triggered logic input with internal pull down**
- **Undervoltage lockout for V_{CC} and V_{BS}**
- **Extended temperature range: -40°C to +125°C**

Applications

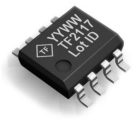
- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Description

The TF2117 and TF2118 are high voltage, high speed gate drivers capable of driving one N-channel MOSFETs and IGBTs in a bootstrap operation. TF Semiconductor's high voltage process enables the TF2117 and TF2118 to switch at 600V. The TF2117 and TF2118 logic input is compatible with standard CMOS outputs (to 3.3V). The driver output features high pulse current buffers designed for minimum driver cross conduction. The single floating channel can be used in high side or low side configuration.

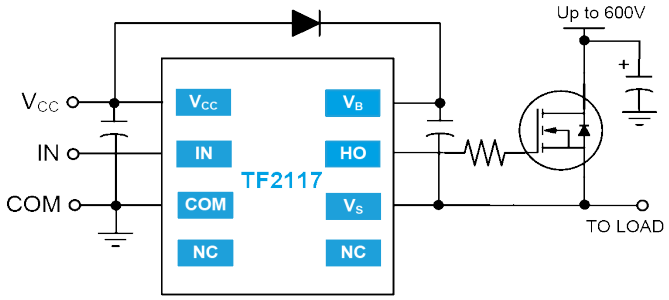
The TF2117 and TF2118 are offered in a space saving 8-pin SOIC and 8-pin PDIP package. They operate over an extended -40 °C to +125 °C temperature range.

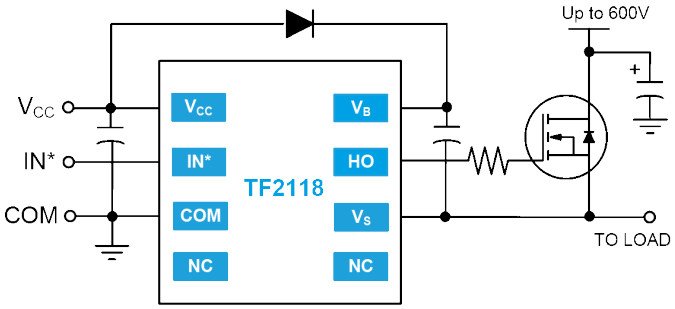
SOIC-8(N)



PDIP-8

Typical Application



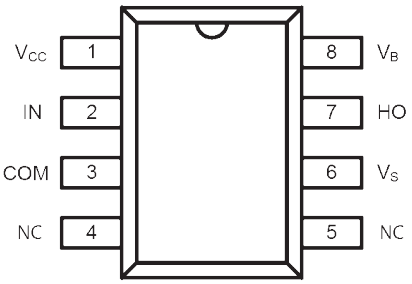


Ordering Information

Year Year Week Week

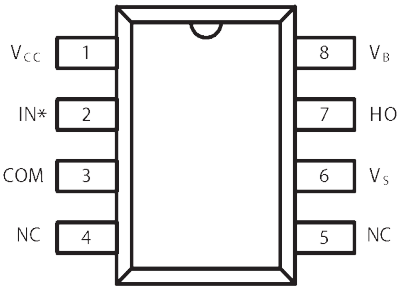
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2117-TAU	SOIC-8	Tube / 100	YYWW TF2117 Lot ID
TF2117-TAH		T&R / 2500	
TF2117-3AS	PDIP-8	Tube / 50	YYWW TF2117 Lot ID
TF2118-TAU	SOIC-8	Tube / 100	YYWW TF2118 Lot ID
TF2118-TAH		T&R / 2500	
TF2118-3AS	PDIP-8	Tube / 50	YYWW TF2118 Lot ID

Pin Diagrams



Top View: PDIP-8, SOIC-8

TF2117



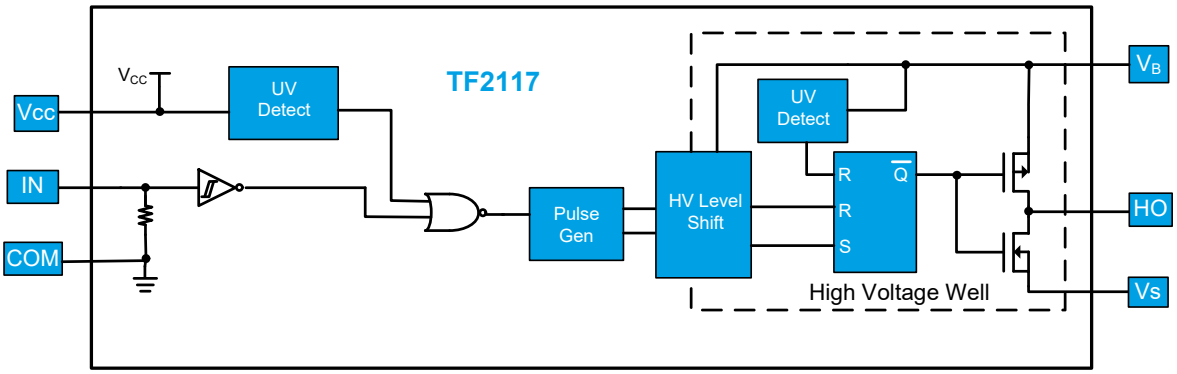
Top View: PDIP-8, SOIC-8

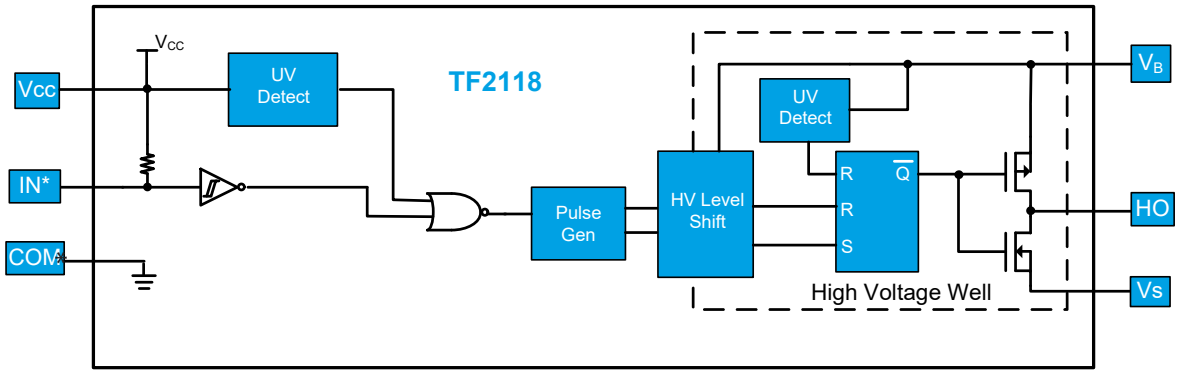
TF2118

Pin Descriptions

PIN NAME	PIN DESCRIPTION
VCC	Logic and gate drive supply
IN	TF2117 Logic input for gate driver output (HO), in phase with HO
IN*	TF2118 Logic input for gate driver output (HO), out of phase with HO
COM	Logic ground
NC	No Connect
V_S	High-side floating supply return
HO	High-side gate drive output
V_B	High-side floating supply

Functional Block Diagram





Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
V_{CC} - Logic supply voltage.....-0.3V to +24V
V_{IN} - Logic input voltage.....-0.3V to V_{CC} +0.3V
dV_S / dt - Allowable offset supply voltage transient.....50 V/ns

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
PDIP-8.....1.0W
$R_{\theta JA}$ - Thermal Resistance, junction to Ambient
SOIC-8.....200° C/W
PDIP-8.....200° C/W

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

T_J - Junction temperature.....+150 °C
T_S - Storage temerature .....-55 to 150 °C
T_L - Lead Temperature (soldering, 10 seconds.....300 °C

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

PDIP-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....35 °C/W
θ_{JA}.....125 °C/W

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10		V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***		600	
V_{HO}	High side floating output voltage	V_S		V_B	
V_{CC}	Low side and logic fixed supply voltage	10		20	
V_{IN}	Logic input voltage (IN/IN*)	0		V_{CC}	
T_A	Ambient temperature	-40		125	°C

NOTE3 *Logic operational for VS of -5V to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	*NOTE 5*	9.5			V
V_{IL}	Logic "0" input voltage				6.0	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or V_{CC}		50	240	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or V_{CC}		70	340	
I_{IN+}	Logic "1" input bias current	V_{IN} = V_{CC}		20	40	
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			5.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.6	8.6	9.6	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.2	8.2	9.2	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.6	8.6	9.6	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.2	8.2	9.2	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10 µs	200	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10 µs	420	600		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM and are applicable to logic input pins: IN and IN*. The V_0 and I_0 parameters are referenced to COM and are applicable to the output pins HO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to IN and IN*) should have an amplitude of 9.5V minimum with a pulse width of 250ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		125	200	ns
t_{OFF}	Turn-off propagation delay	V_S = 600V		105	180	
t_r	Turn-on rise time			75	130	
t_f	Turn-off fall time			35	65	

Timing Waveforms

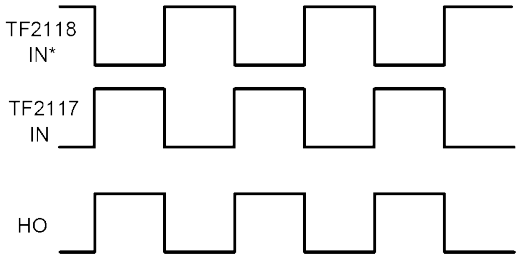


Figure 1. Input / Output Timing Diagram

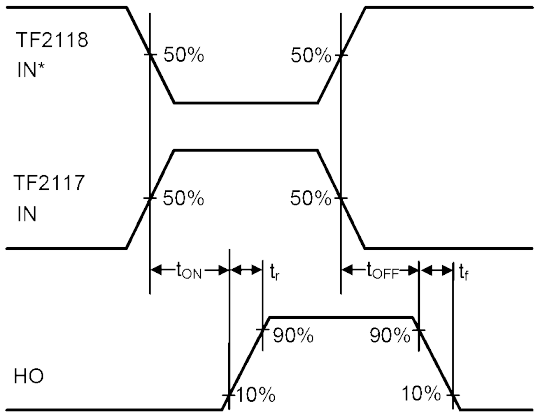


Figure 2. Switching Time Waveform Definitions

Application Information

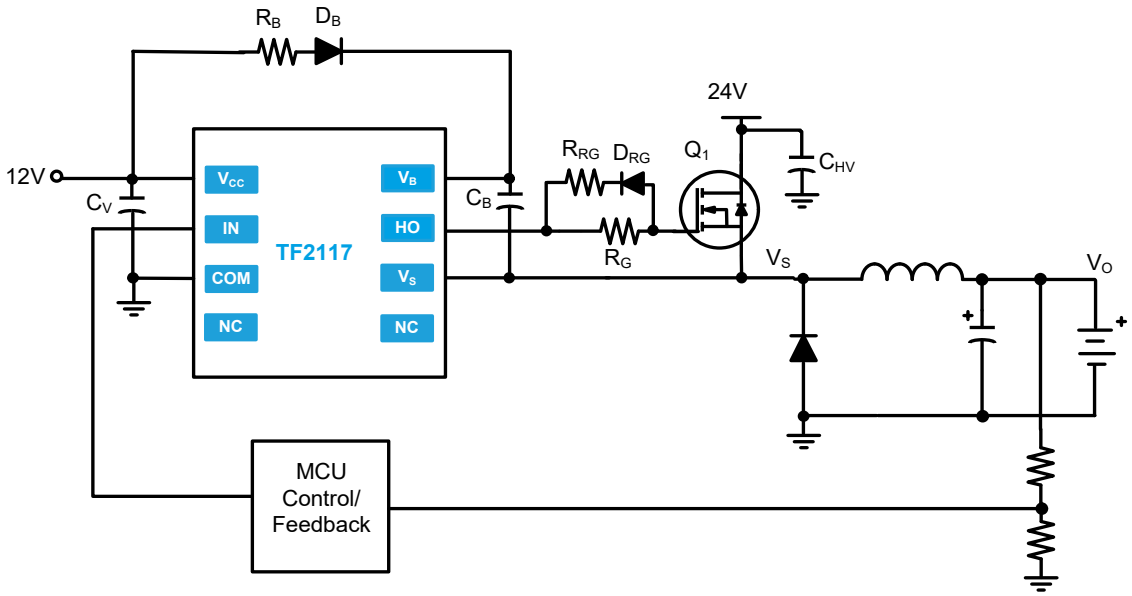


Figure 3. Buck converter using TF2117 in basic battery charger application

- RRG value is typically between 5Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

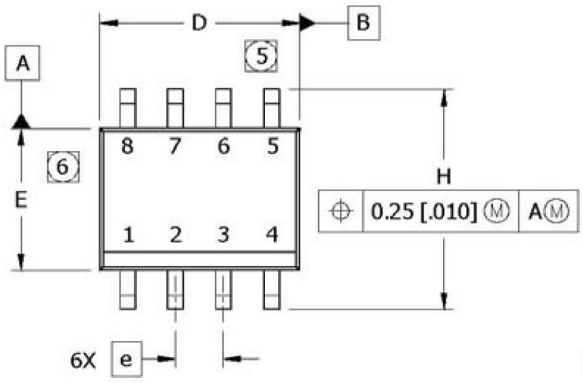
- RG value is typically between 10Ω and 50Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 20Ω is used in this example.

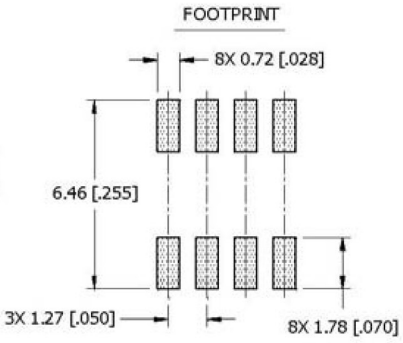
- RB value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

- It is recommended that the input pulse (to IN) should have an amplitude of 9.5V minimum (for VDD=15V) with a minimum pulse width of 250ns.

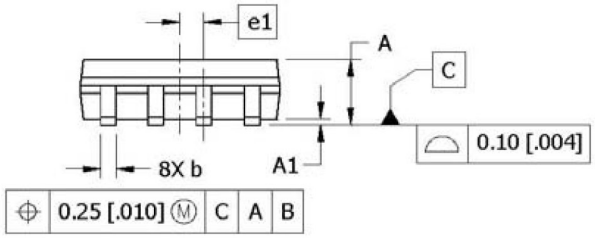
Package Dimensions (SOIC-8 N)

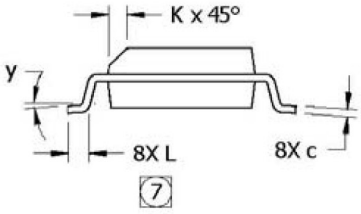
Please contact support@tfsemi.com for package availability.





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°





NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

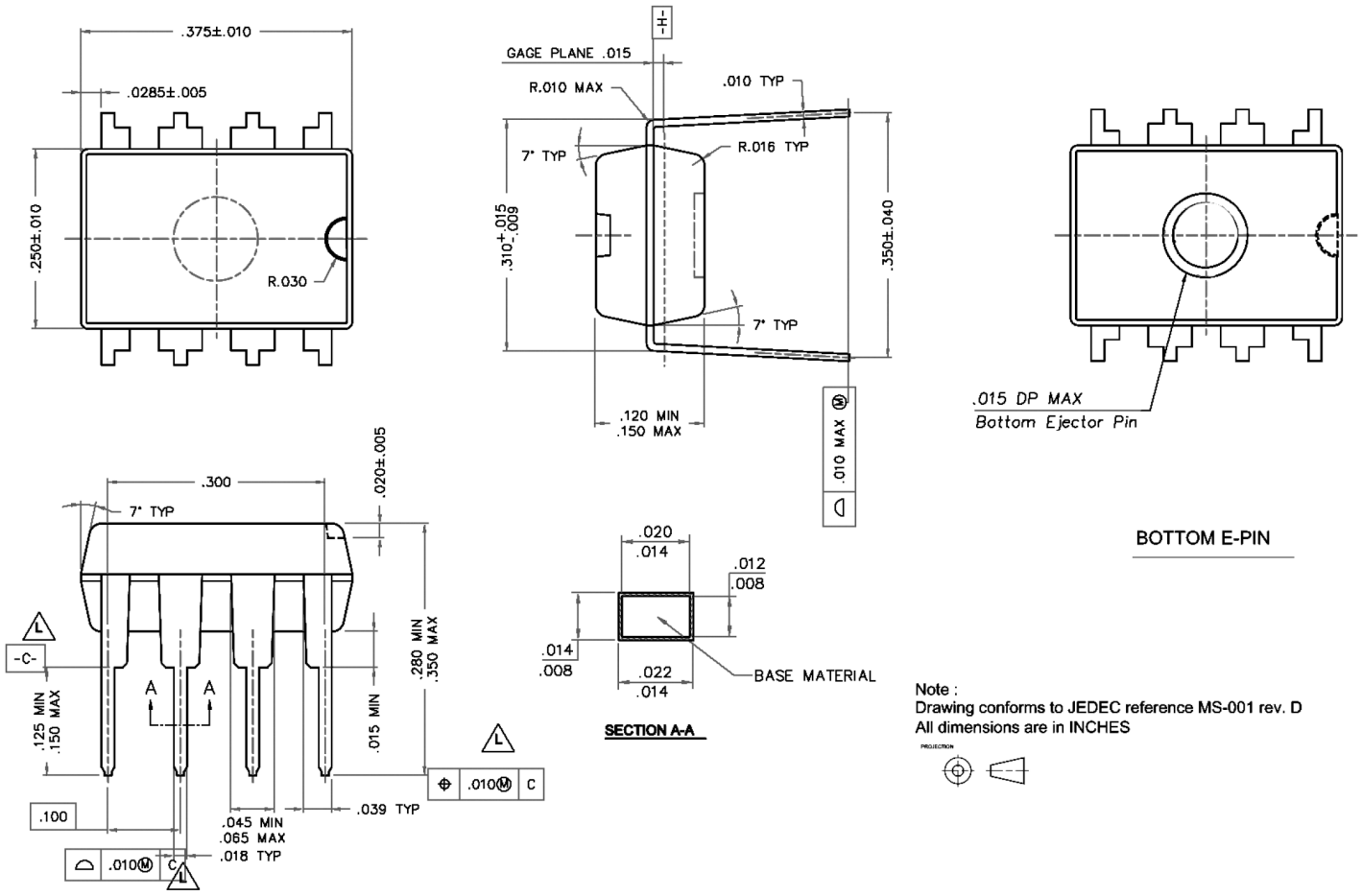
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027

Package Dimensions (PDIP-8)

Please contact support@tfsemi.com for package availability.



Revision History

Rev.	Change	Owner	Date
2.0	First release, Advance info datasheet	Keith Spaulding	12/5/2015
2.1	Add note 5	Keith Spaulding	10/31/2019
2.2	Add Application Information, pg. 7	Keith Spaulding	5/18/2020

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