Precision Single and Dual Low Noise Operational Amplifiers

ISL28127, ISL28227

ISL28127, ISL28227

The ISL28127 and ISL28227 are very high precision amplifiers featuring very low noise, low offset voltage, low input bias current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28127 single and ISL28227 dual are available in an 8 Ld SOIC, TDFN and MSOP packages. All devices are offered in standard pin configurations and operate over the extended temperature range to -40°C to +125°C.

Features

- Very Low Voltage Noise 2.5nV/Hz
- Low Input Offset . . . . 70µV, Max.
- Superb Offset Drift . . . . 0.5µV/°C, Max.
- Input Bias Current . . . . 10nA, Max.
- Wide Supply Range. . . . . 4.5V to 40V
- Gain-bandwidth Product . 10MHz Unity Gain Stable
- No Phase Reversal

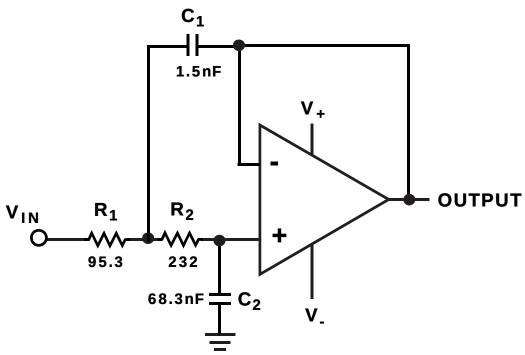
Applications* (see page 20)

- Precision Instruments
- Medical Instrumentation
- Industrial Controls
- Active Filter Blocks
- Data Acquisition
- Power Supply Control

Related Literature* (see page 20)

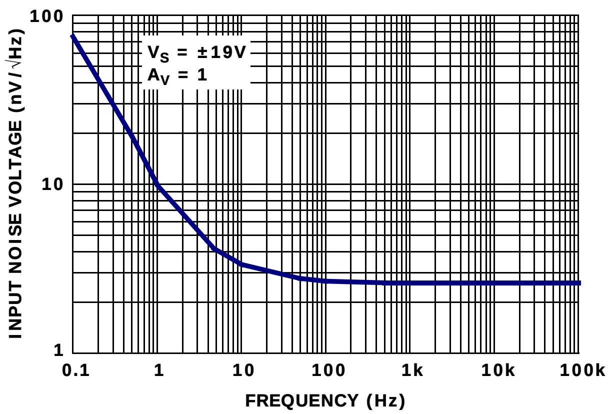
- AN1508: ISL281X7SOICEVAL1Z Evaluation Board User's Guide

Typical Application



Sallen-Key Low Pass Filter (1MHz)

Input Noise Voltage Spectral Density



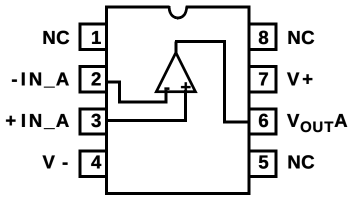
Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	V_{OS} (MAX) (µV)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28127FBZ (Note 1)	28127 FBZ	70	8 Ld SOIC	M8.15E
Coming Soon ISL28127FRTBZ (Note 2)	127Z	TBD (B Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28127FRTZ (Note 2)	-C 127Z	150 (C Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28127FUBZ (Note 2)	8127Z	TBD (B Grade)	8 Ld MSOP	M8.118
ISL28127FUZ (Note 2)	8127Z -C	150 (C Grade)	8 Ld MSOP	M8.118
ISL28227FBZ (Note 2)	28227 FBZ	75	8 Ld SOIC	M8.15E
Coming Soon ISL28227FRTBZ (Note 2)	227Z	TBD (B Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28227FRTZ (Note 2)	-C 227Z	150 (C Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28227FUBZ (Note 2)	8227Z	TBD (B Grade)	8 Ld MSOP	M8.118
Coming Soon ISL28227FUZ (Note 2)	8227Z -C	150 (C Grade)	8 Ld MSOP	M8.118
ISL28127SOICEVAL1Z	Evaluation Board			

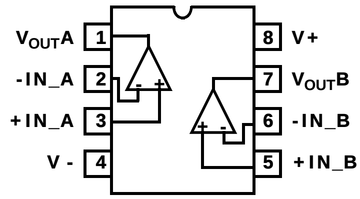
1. Add "-T7" or "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Add "-T13" suffix for tape and reel.Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL28127, ISL28227. For more information on MSL please see techbrief TB363.

Pin Configurations

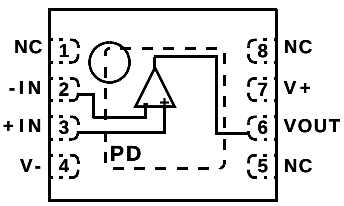
ISL28127
(8 LD SOIC, MSOP)
TOP VIEW



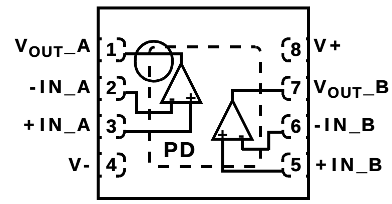
ISL28227
(8 LD SOIC, MSOP)
TOP VIEW



ISL28127
(8 LD TDFN)
TOP VIEW

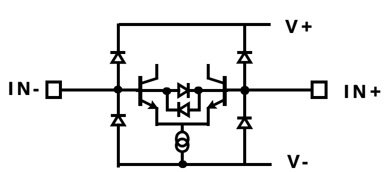


ISL28227
(8 LD TDFN)
TOP VIEW

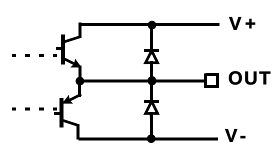


Pin Descriptions

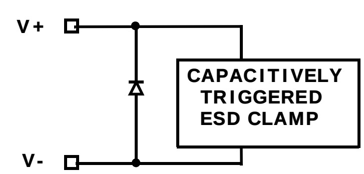
ISL28127 (8 LD SOIC, 8 LD MSOP)	ISL28127 (8 LD TDFN)	ISL28227 (8 LD SOIC, 8 LD MSOP)	ISL28227 (8 LD TDFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
	3			+IN	Circuit 1	Amplifier non-inverting input
3		3	3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	4	4	4	V-	Circuit 3	Negative power supply
		5	5	+IN_B	Circuit 1	Amplifier B non-inverting input
	2			-IN	Circuit 1	Amplifier inverting input
		6	6	-IN_B	Circuit 1	Amplifier B inverting input
	6			V_{OUT}	Circuit 2	Amplifier output
		7	7	$V_{OUT}B$	Circuit 2	Amplifier B output
7	7	8	8	V+	Circuit 3	Positive power supply
6		1	1	$V_{OUT}A$	Circuit 2	Amplifier A output
2		2	2	-IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8	1, 5, 8			NC	-	Not Connected – This pin is not electrically connected internally.
	PD			PD	-	Thermal Pad. Pad should be connecte to lowest potential source in the circuit.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 0.5V
Min/Max Input Voltage . . . . .V- - 0.5V to V+ + 0.5V
Max/Min Input Current for
  Input Voltage >V+ or <V- . . . .±20mA
Output Short-Circuit Duration
  (1 Output at a Time) . . . . Indefinite
ESD Tolerance
  Human Body Model (Tested per JESD22-A114F)
    ISL28127. . . . . .4.0kV
    ISL28227. . . . . .6.0kV
  Machine Model (Tested per EIA/JESD22-A115-A) 500V
  Charged Device Model (Tested per JESD22-C101D) . . 1.5kV
Di-electrically Isolated PR40 process. . . . . Latch-up free

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (Note 5, 7)		
ISL28127	120	60
ISL28227	110	55
8 Ld TDFN (Notes 5, 6)		
ISL28127	48	7
ISL28227	47	6
8 Ld MSOP (Note 5, 7)		
ISL28127	155	50
ISL28227	150	45

Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Offset Voltage; SOIC Package	ISL28127	-70	10	70	µV
			-120	-	**120**	µV
		ISL28227	-75	10	75	µV
			-150	-	**150**	µV
	Offset Voltage; MSOP, TDFN Grade C Package	ISL28127 ISL28227	-150	10	150	µV
			-250	-	**250**	µV
TCV_{OS}	Offset Voltage Drift; SOIC Pacakge	ISL28127	**-0.5**	0.1	**0.5**	µV/°C
		ISL28227	**-0.75**	0.1	**0.75**	µV/°C
	Offset Voltage Drift; MSOP, TDFN, Grade C	ISL28127 ISL28227	**-1**	0.1	**1**	µV/°C
I_{OS}	Input Offset Current		-10	1	10	nA
			-12	**-**	**12**	nA
I_B	Input Bias Current		-10	1	10	nA
			-12	-	**12**	nA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	-13	-	13	V
			-12	**-**	**12**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	115	120	-	dB
		V_{CM} = -12V to +12V	**115**	-	-	dB

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
PSRR	Power Supply Rejection Ratio ISL28127	V_S = ±2.25V to ±20V	115	125	-	dB
		V_S = ±3V to ± 20V	**115**	-	-	dB
	Power Supply Rejection Ratio ISL28227	V_S = ±2.25V to ±20V	110	117	-	dB
		V_S = ±3V to ± 20V	**110**	-	-	dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V R_L = 10kΩ to ground	1000	1500	-	V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.65	-	V
			13.2	-	-	V
		R_L = 2kΩ to ground	13.4	13.5	-	V
			13.1	-	-	V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground	-	-13.65	-13.5	V
			-	**-**	**-13.2**	V
		R_L = 2kΩ to ground	-	-13.5	-13.4	V
			-	-	**-13.1**	V
I_S	Supply Current/Amplifier		-	2.2	2.8	mA
			-	-	**3.7**	mA
I_{SC}	Short-Circuit	R_L = 0Ω to ground	-	±45	-	mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	±2.25	-	±20	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			10		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		85		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		3		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		2.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		2.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		2.5		nV/√Hz
in	Current Noise Density	f = 10kHz		0.4		pA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 2kΩ		0.00022		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ, V_O = 4V_{P-P}		±3.6		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		36		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		38		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1 V_{OUT} = 10V_{P-P}, R_g = R_f =10k, R_L = 2kΩ to V_{CM}		3.4		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 2kΩ to V_{CM}		3.8		µs
t_{OL}	Output Overload Recovery Time	A_V = 100, V_{IN} = 0.2V R_L = 2kΩ to V_{CM}		1.7		µs

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Offset Voltage		-70	10	70	µV
			-120	-	**120**	µV
V_{OS}/T	Offset Voltage Drift		**-0.5**	0.1	**0.5**	µV/°C
I_{OS}	Input Offset Current		-10	1	10	nA
			-12	-	**12**	nA
I_B	Input Bias Current		10	1	10	nA
			-12	-	**12**	nA
V_{CM}	Common Mode Input Voltage Range	Guaranteed by CMRR	-3	-	3	V
			-2	**-**	**2**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	115	120	**-**	dB
		V_{CM} = -2V to +2V	**115**	-	-	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	115	125	-	dB
		V_S = ±3V to ±5V	**115**	-	-	dB
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V R_L = 10kΩ to ground	1000	1500	-	V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.65	-	V
			3.2	-	-	V
		R_L = 2kΩ to ground	3.4	3.5	-	
			3.1	-	-	V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground	-	-3.65	-3.5	V
			-	**-**	**-3.2**	V
		R_L = 2kΩ to ground	-	-3.5	-3.4	
			-	-	**-3.1**	V
I_S	Supply Current/Amplifier		-	2.2	2.8	mA
			-	-	**3.7**	mA
I_{SC}	Short-Circuit		**-**	± 45	**-**	mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			10		MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, Vo = 2.5V_{RMS}, R_L = 2kΩ		0.0034		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ		±3.6		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		36		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		38		ns
t_s	Settling Time to 0.1%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		1.6		µs
	Settling Time to 0.01%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		4.2		µs

NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

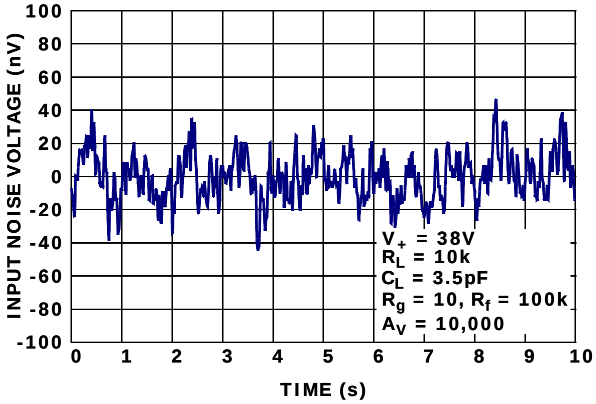


FIGURE 1. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

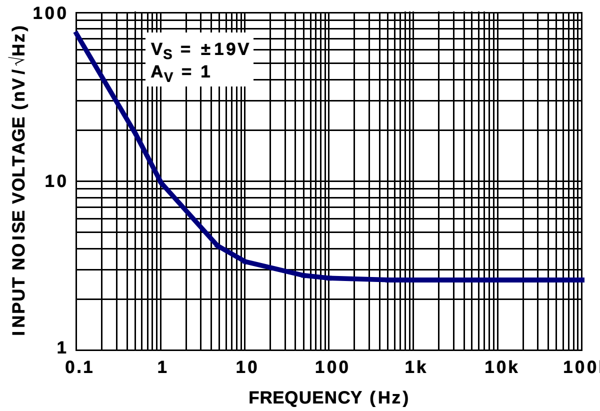


FIGURE 2. INPUT NOISE VOLTAGE SPECTRAL DENSITY

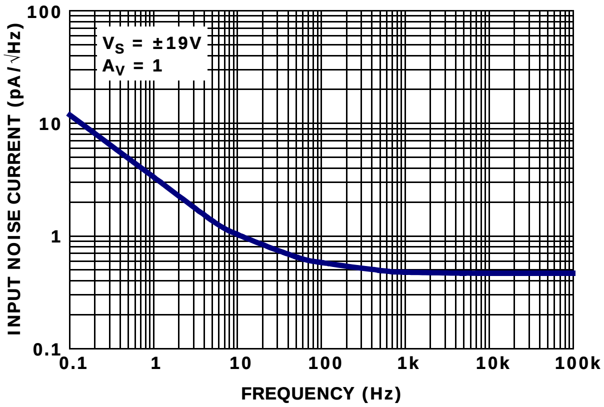


FIGURE 3. INPUT NOISE CURRENT SPECTRAL DENSITY

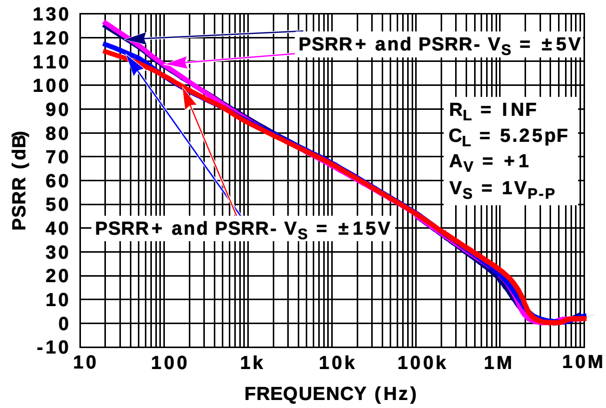


FIGURE 4. PSRR vs FREQUENCY, V_S = ±5V, ±15V

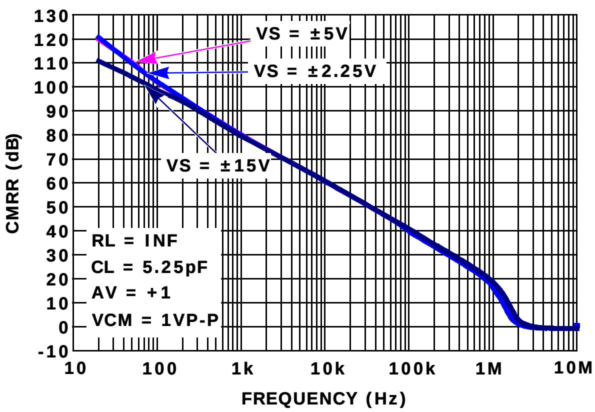


FIGURE 5. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

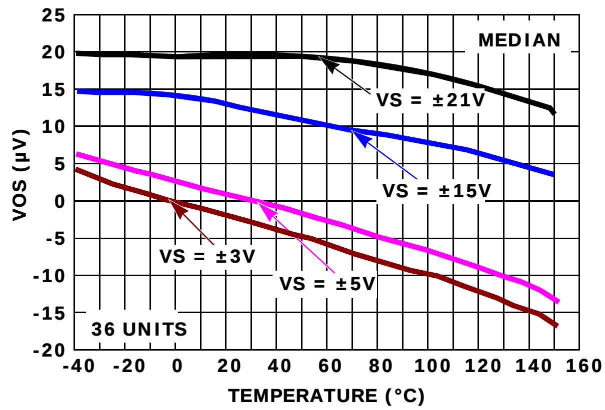


FIGURE 6. V_{OS} vs TEMPERATURE vs V_{SUPPLY}

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

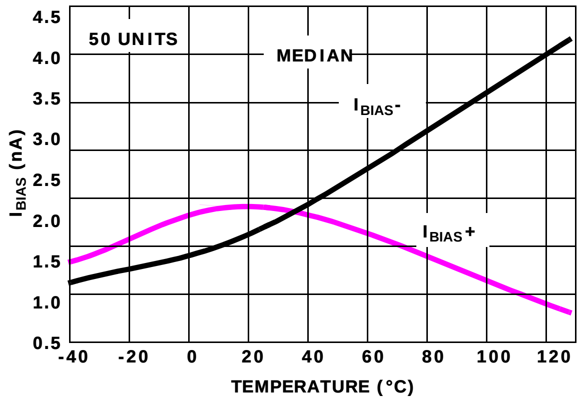


FIGURE 7. I_{IB} vs TEMPERATURE, $V_S = \pm15V$

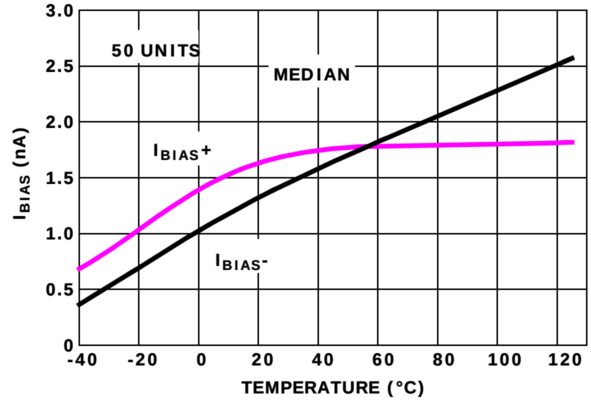


FIGURE 8. I_{IB} vs TEMPERATURE, $V_S = \pm5V$

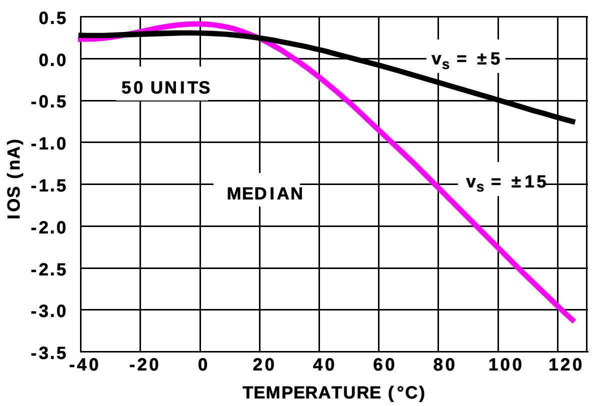


FIGURE 9. I_{OS} vs TEMPERATURE vs SUPPLY

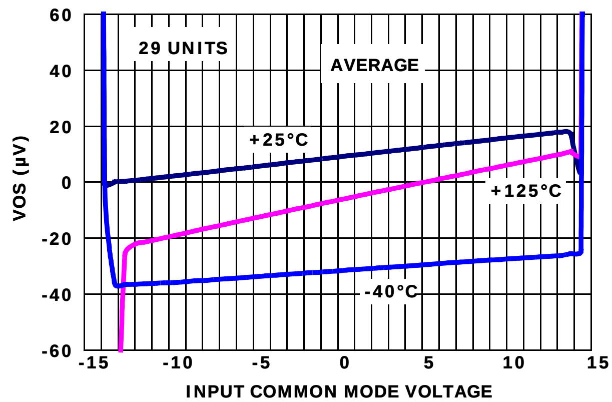


FIGURE 10. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, $V_S = \pm15V$

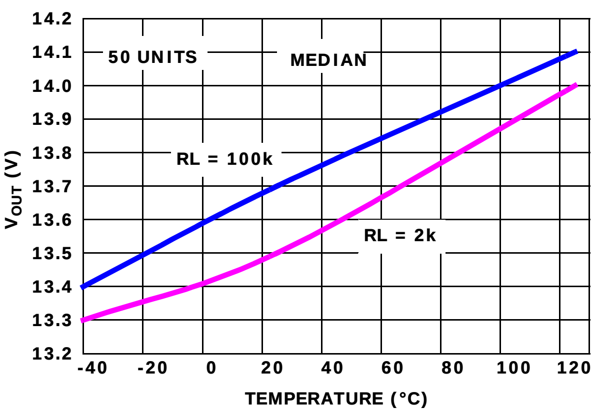


FIGURE 11. V_{OH} vs TEMPERATURE, $V_S = \pm15V$

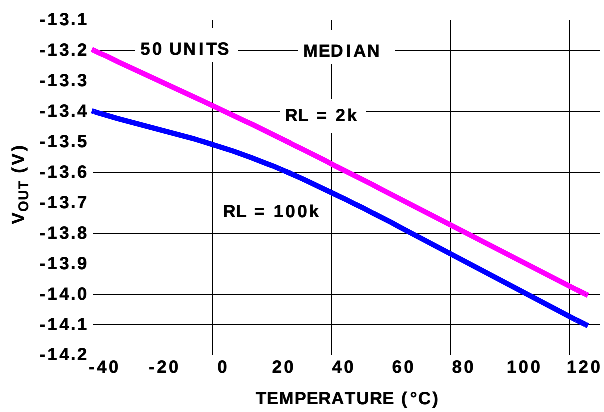


FIGURE 12. V_{OL} vs TEMPERATURE, $V_S = \pm15V$

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

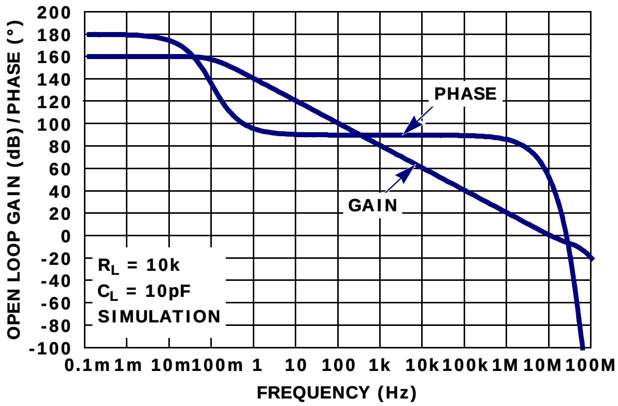


FIGURE 13. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

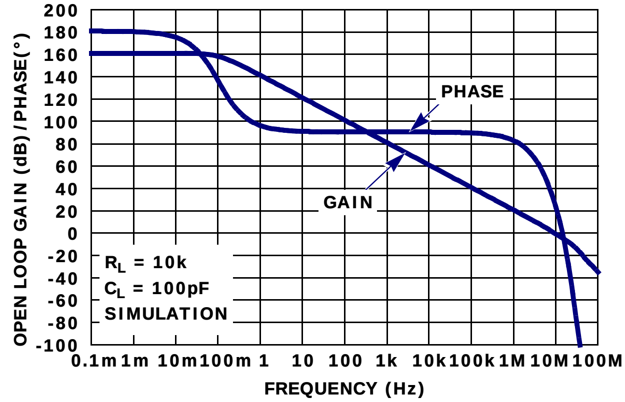


FIGURE 14. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

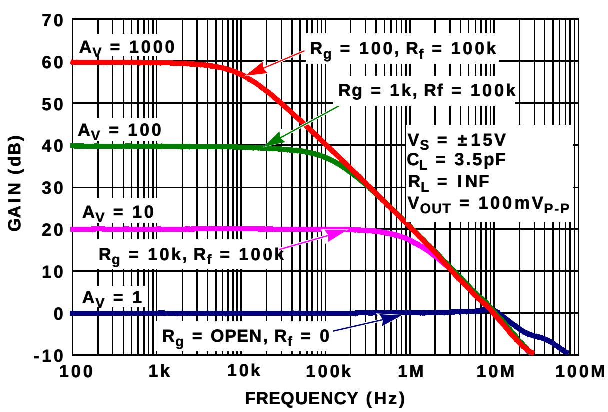


FIGURE 15. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

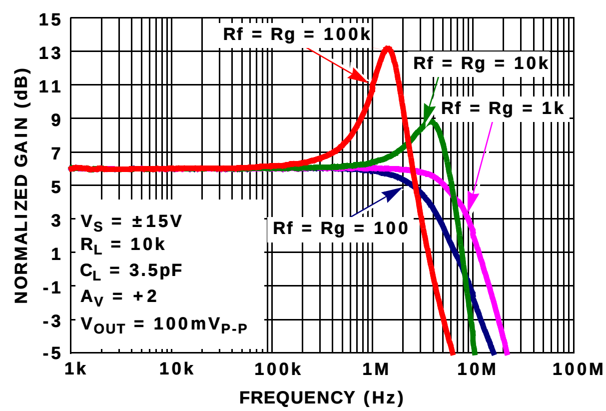


FIGURE 16. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f / R_g

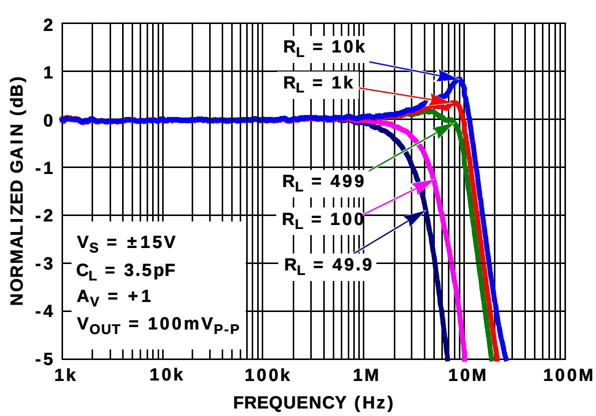


FIGURE 17. GAIN vs FREQUENCY vs R_L

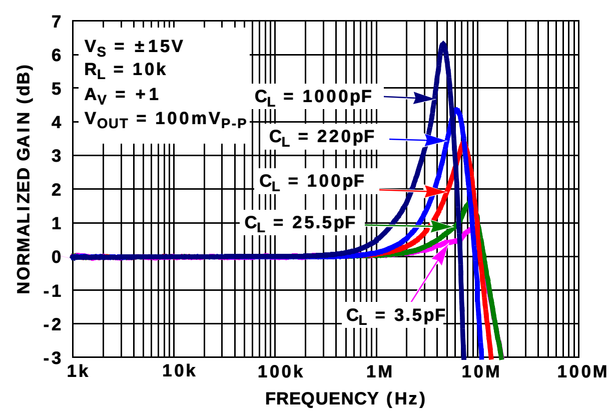


FIGURE 18. GAIN vs FREQUENCY vs C_L

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

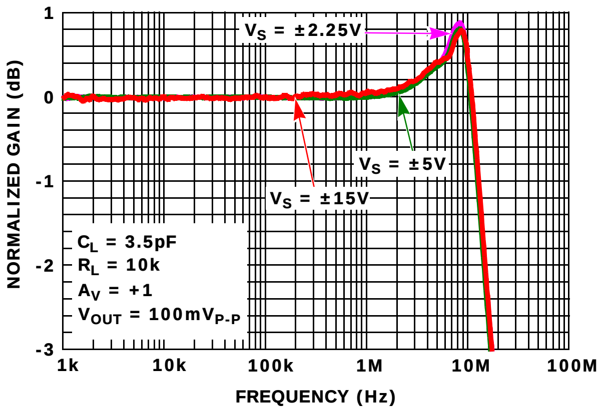


FIGURE 19. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

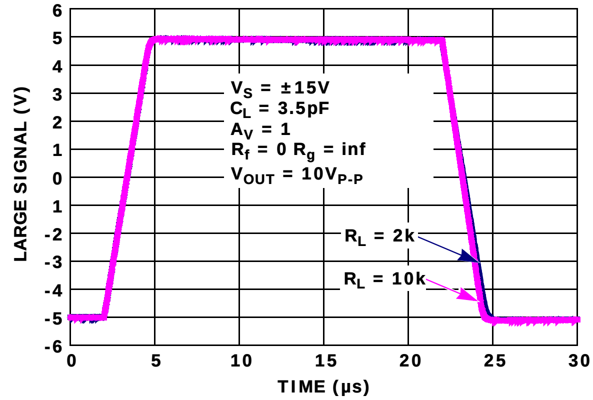


FIGURE 20. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

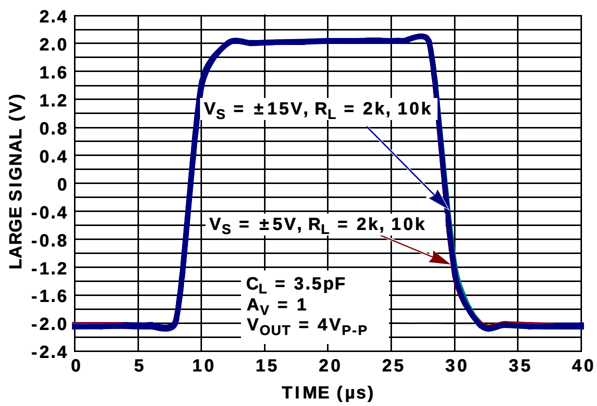


FIGURE 21. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

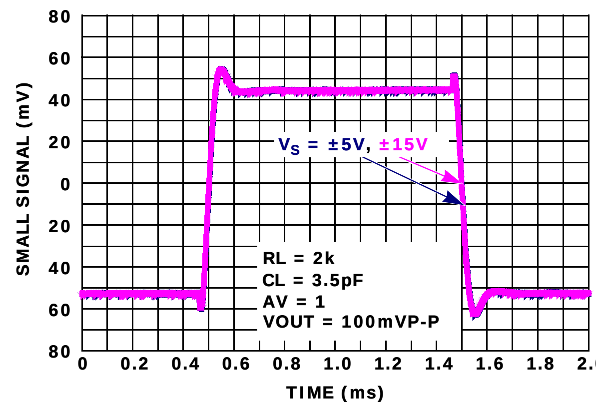


FIGURE 22. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

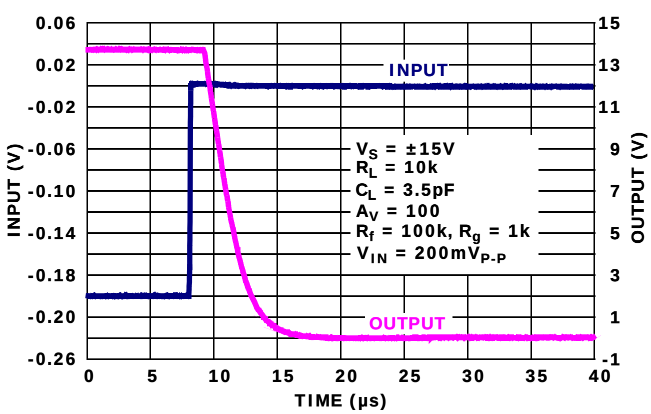


FIGURE 23. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

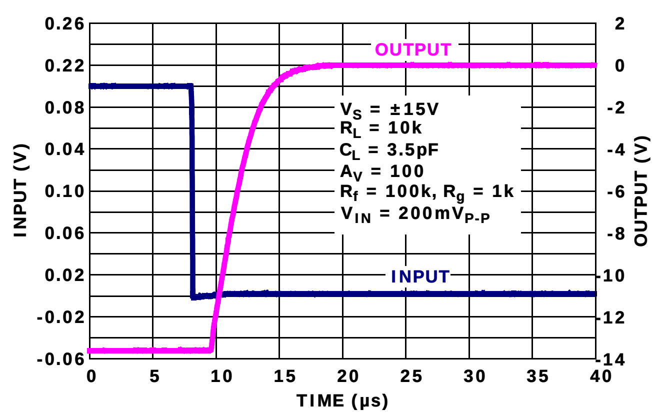


FIGURE 24. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

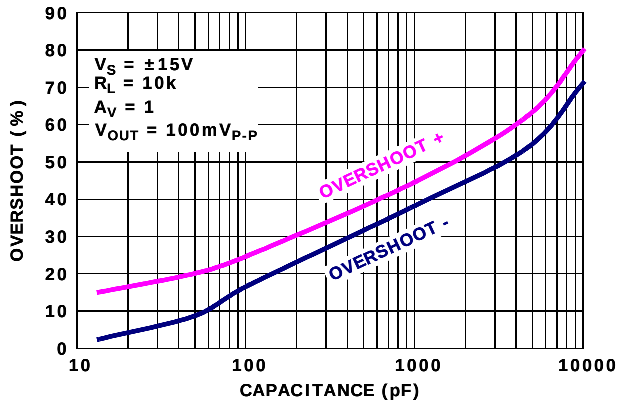


FIGURE 25. % OVERSHOOT vs LOAD CAPACITANCE, $V_S = \pm 15V$

Applications Information

Functional Description

The ISL28127 and ISL28227 are single and dual, low noise 10MHz BW precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (1nA typical), low input offset voltage (10µV typ), low input noise voltage (3nV/√Hz), and low 1/f noise corner frequency (5Hz). These amplifiers also feature high open loop gain (1500V/mV) for excellent CMRR (120dB) and THD+N performance (0.0002% @ 3.5V_{RMS}, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 7.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, and an additional anti-parallel diode pair across the inputs (see Figures 26 and 27).

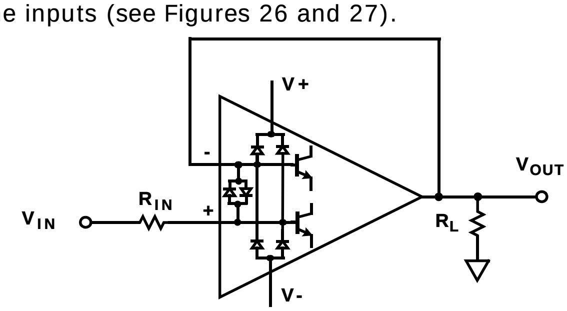


FIGURE 26. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

For unity gain applications (see Figure 26) where the output is connected directly to the non-inverting input a current limiting resistor (R_{IN}) will be needed under the following conditions to protect the anti-parallel differential input protection diodes.

- The amplifier input is supplied from a low impedance source.
- The input voltage rate-of-rise (dV/dt) exceeds the maximum slew rate of the amplifier (±3.6V/µs).

If the output lags far enough behind the input, the anti-parallel input diodes can conduct. For example, if an input pulse ramps from 0V to +10V in 1µs, then the output of the ISL28x27 will reach only +3.6V (slew rate = 3.6V/µs) while the input is at 10V, The input differential voltage of 6.4V will force input ESD diodes to conduct, dumping the input current directly into the output stage and the load. The resulting current flow can cause permanent damage to the ESD diodes. The ESD diodes are rated to 20mA, and in the previous example, setting R_{IN} to 1k resistor (see Figure 26) would limit the current to < 6.4mA, and provide additional protection up to ±20V at the input.

In applications where one or both amplifier input terminals are at risk of exposure to high voltage, current limiting resistors may be needed at each input terminal (see Figure 27 R_{IN}+, R_{IN}-) to limit current through the power supply ESD diodes to 20mA.

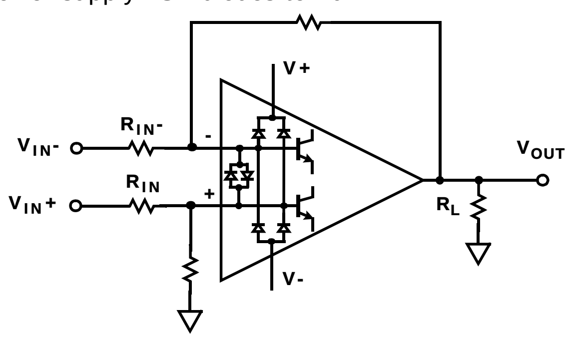


FIGURE 27. INPUT ESD DIODE CURRENT LIMITING - DIFFERENTIAL INPUT

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand an short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28127 and ISL28227 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ.2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

R_L = Load resistance

ISL28127 and ISL28227 SPICE Model

Figure 28 shows the SPICE model schematic and Figure 29 shows the net list for the ISL28127 and ISL28227 SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model does not model input bias current. The model uses typical parameters given in the “Electrical Specifications” Table beginning on page 4. The AVOL is adjusted for 128dB with the dominate pole at 5Hz. The CMRR is set higher than the “Electrical Specifications” Table to better match design simulations (150dB, f = 50Hz). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 30 through 45 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs Rf/Rg, Closed Loop Gain vs RL, Closed Loop Gain vs CL, Large Signal 10V Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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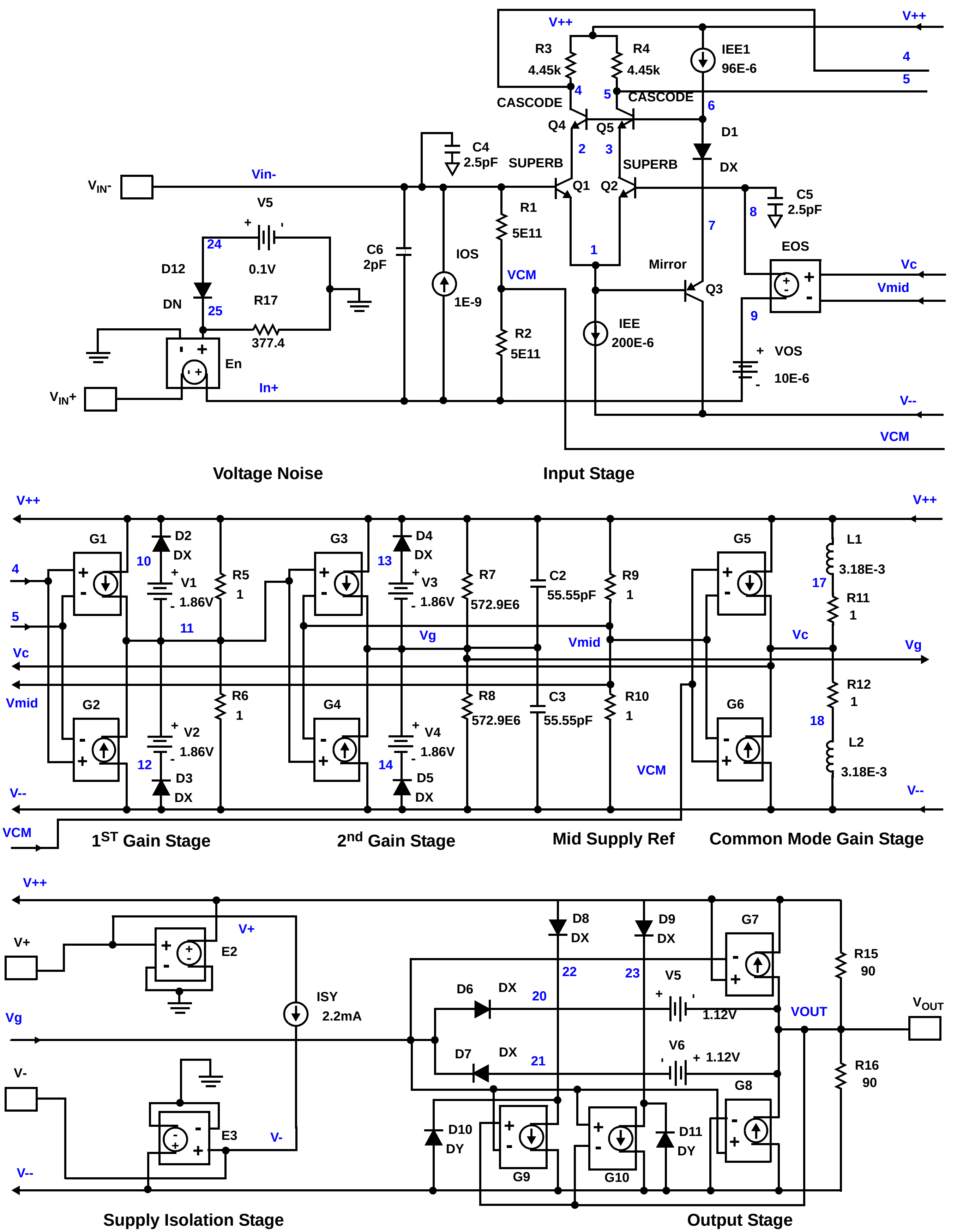

FIGURE 28. SPICE SCHEMATIC

```
* source ISL28127_SPICEmodel
* Revision C, August 8th 2009 LaFontaine
* Model for Noise, supply currents, 150dB f=50Hz
CMRR, *128dB f=5Hz AOL
*Copyright 2009 by Intersil Corporation
*Refer to data sheet “LICENSE STATEMENT” Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections: +input
*              |    -input
*              |    |    +Vsupply
*              |    |    |    -Vsupply
*              |    |    |    |    output
*              |    |    |    |    |
.subckt ISL28127subckt Vin+ Vin-V+ V- VOUT
* source ISL28127_SPICEMODEL_0_0
*
*Voltage Noise
E_En         IN+ VIN+ 25 0 1
R_R17         25 0  377.4 TC=0,0
D_D12         24 25 DN
V_V7         24 0 0.1
*
*Input Stage
I_IOS         IN+ VIN- DC 1e-9
C_C6         IN+ VIN- 2E-12
R_R1         VCM VIN-  5e11 TC=0,0
R_R2         IN+ VCM  5e11 TC=0,0
Q_Q1         2 VIN- 1 SuperB
Q_Q2         3 8 1 SuperB
Q_Q3         V-- 1 7 Mirror
Q_Q4         4 6 2 Cascode
Q_Q5         5 6 3 Cascode
R_R3         4 V++ 4.45e3 TC=0,0
R_R4         5 V++ 4.45e3 TC=0,0
C_C4 VIN- 0  2.5e-12
C_C5 8 0  2.5e-12
D_D1         6 7 DX
I_IEE         1 V-- DC 200e-6
I_IEE1         V++ 6 DC 96e-6
V_VOS         9 IN+ 10e-6
E_EOS         8 9 VC VMID 1
*
*1st Gain Stage
G_G1         V++ 11 4 5 0.0487707
G_G2         V-- 11 4 5 0.0487707
R_R5         11 V++ 1 TC=0,0
R_R6         V-- 11  1 TC=0,0
D_D2         10 V++ DX
D_D3         V-- 12 DX
V_V1         10 11 1.86
V_V2         11 12 1.86
*
*2nd Gain Stage
G_G3         V++ VG 11 VMID 4.60767E-3
G_G4         V-- VG 11 VMID 4.60767E-3
R_R7         VG V++ 572.958E6 TC=0,0
R_R8         V-- VG  572.958E6 TC=0,0
C_C2         VG V++ 55.55e-12  TC=0,0
C_C3         V-- VG  55.55e-12  TC=0,0
D_D4         13 V++ DX
D_D5         V-- 14 DX
V_V3         13 VG 1.86
V_V4         VG 14 1.86
*
*Mid supply Ref
R_R9         VMID V++ 1 TC=0,0
R_R10         V-- VMID  1 TC=0,0
I_ISY     V+ V- DC 2.2E-3
E_E2         V++ 0 V+ 0 1
E_E3         V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5         V++ VC VCM VMID 31.6228e-9
G_G6         V-- VC VCM VMID 31.6228e-9
R_R11         VC 17  1 TC=0,0
R_R12         18 VC  1 TC=0,0
L_L1         17 V++ 3.183e-3
L_L2         18 V-- 3.183e-3
*
*Output Stage with Correction Current Sources
G_G7         VOUT V++ V++ VG 1.11e-2
G_G8         V-- VOUT VG V-- 1.11e-2
G_G9         22 V-- VOUT VG 1.11e-2
G_G10         23 V-- VG VOUT 1.11e-2
D_D6         VG 20 DX
D_D7         21 VG DX
D_D8         V++ 22 DX
D_D9         V++ 23 DX
D_D10         V-- 22 DY
D_D11         V-- 23 DY
V_V5         20 VOUT 1.12
V_V6         VOUT 21 1.12
R_R15         VOUT V++ 9E1 TC=0,0
R_R16         V-- VOUT  9E1 TC=0,0
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3 rb=140
+ re=0.011 rc=900 cje=0.2E-12 cjc=0.16E-12f
+ kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12 cjc=0.44E-12
+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28127subckt
```

FIGURE 29. SPICE NET LIST

Characterization vs Simulation Results

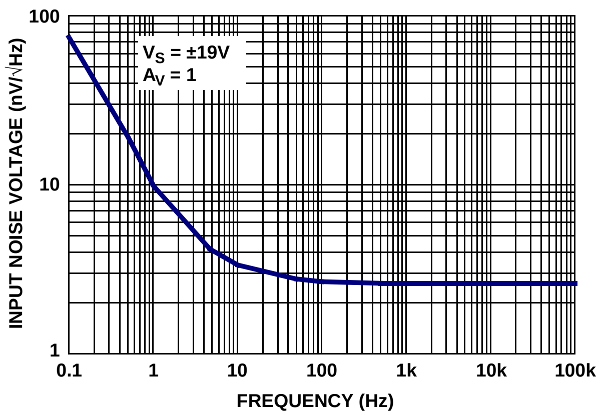

FIGURE 30. CHARACTERIZED INPUT NOISE VOLTAGE

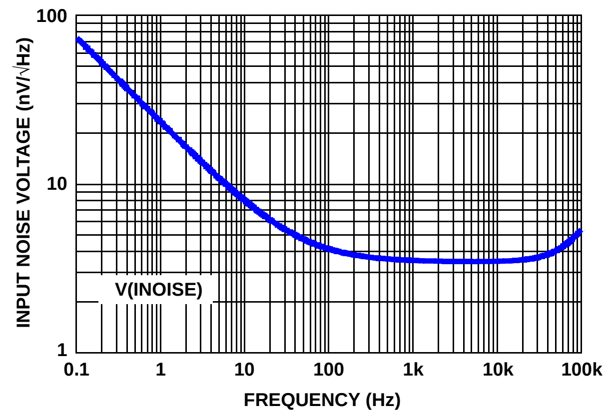

FIGURE 31. SIMULATED INPUT NOISE VOLTAGE

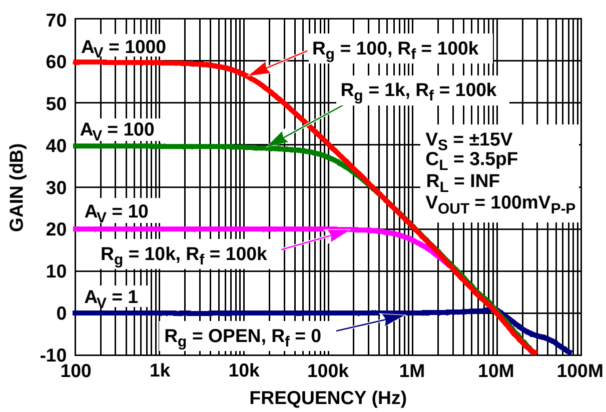

FIGURE 32. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

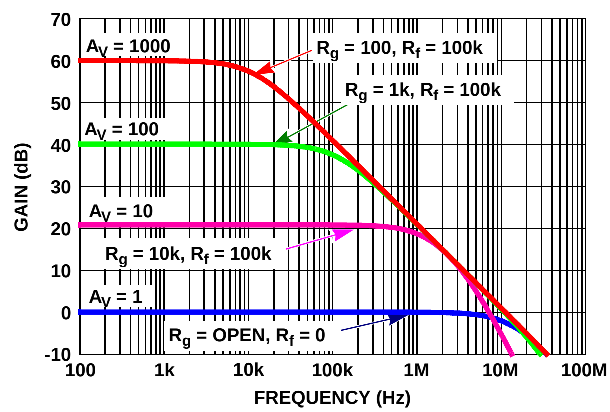

FIGURE 33. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

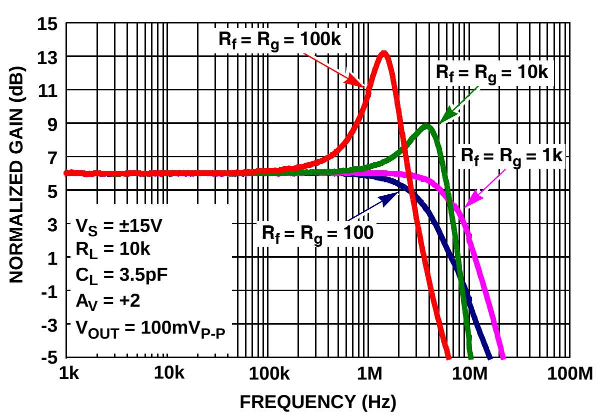

FIGURE 34. CHARACTERIZED CLOSED LOOP GAIN vs R_f / R_g

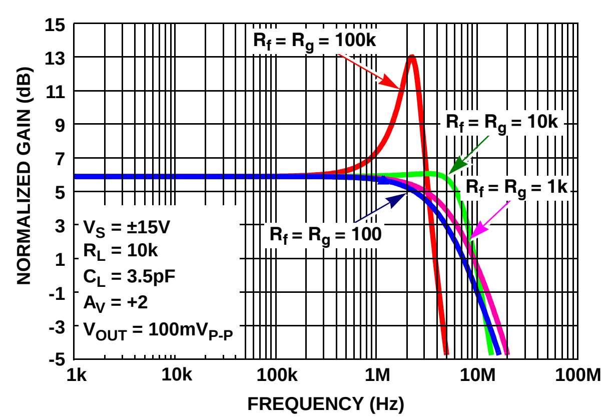

FIGURE 35. SIMULATED CLOSED LOOP GAIN vs R_f / R_g

Characterization vs Simulation Results (Continued)

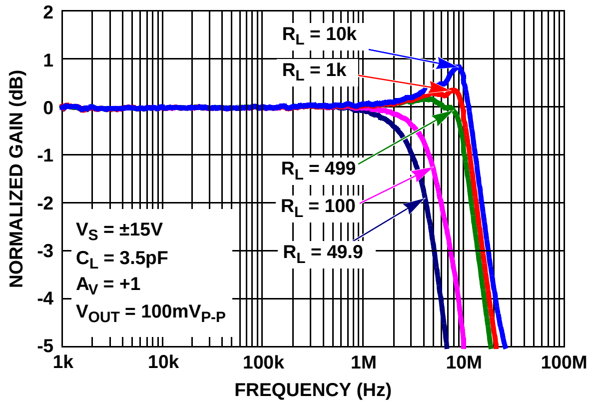

FIGURE 36. CHARACTERIZED CLOSED LOOP GAIN vs R_L

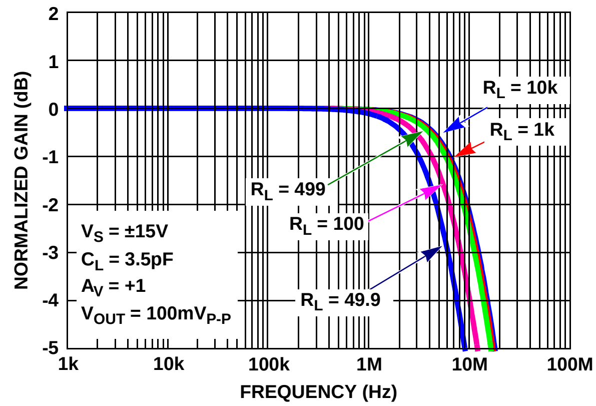

FIGURE 37. SIMULATED CLOSED LOOP GAIN vs R_L

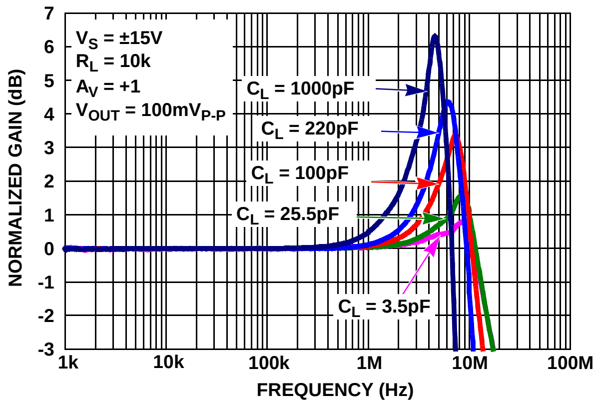

FIGURE 38. CHARACTERIZED CLOSED LOOP GAIN vs C_L

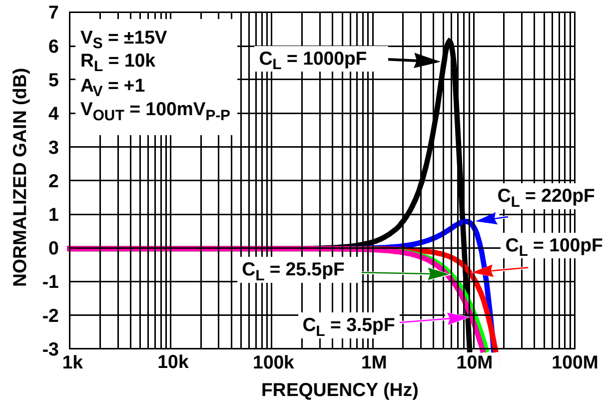

FIGURE 39. SIMULATED CLOSED LOOP GAIN vs C_L

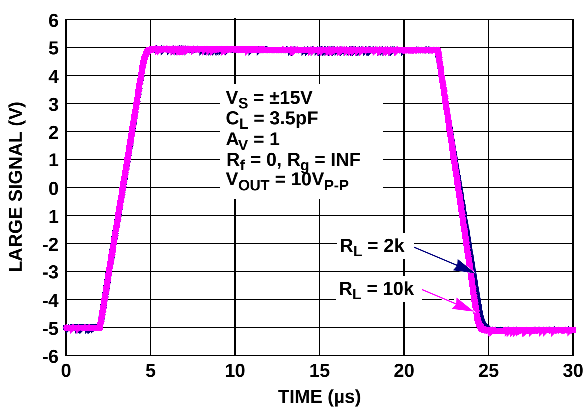

FIGURE 40. CHARACTERIZED LARGE SIGNAL 10V STEP RESPONSE

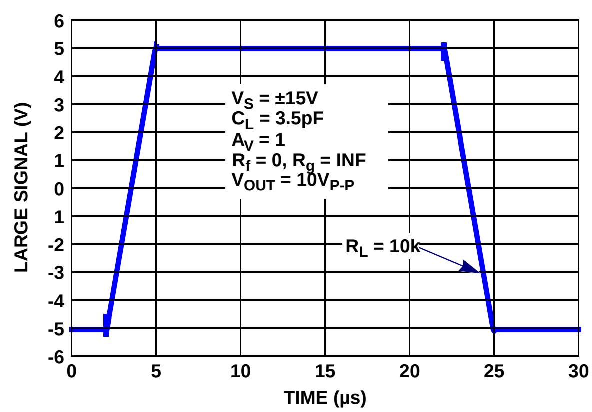

FIGURE 41. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

Characterization vs Simulation Results (Continued)

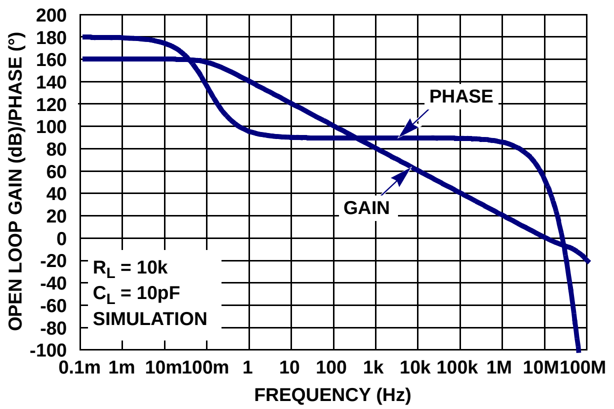

FIGURE 42. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

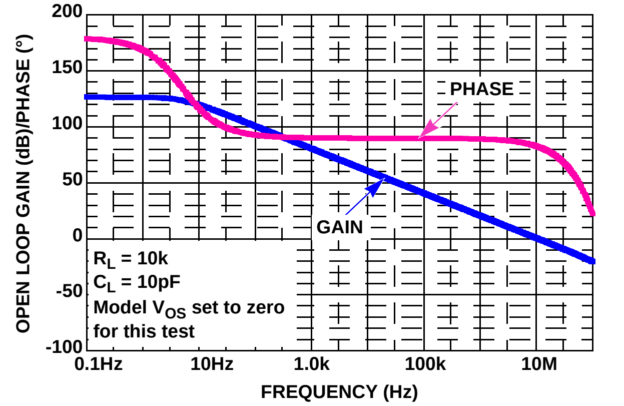

FIGURE 43. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

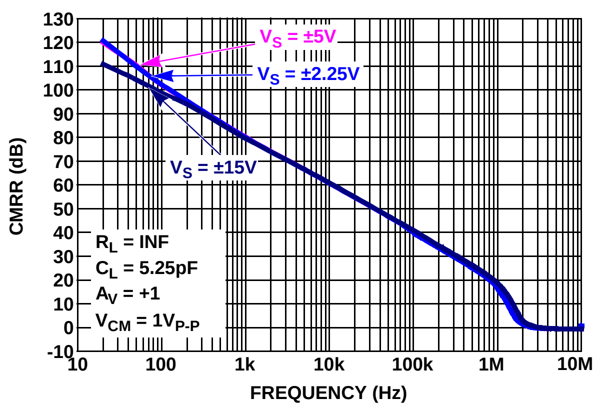

FIGURE 44. CHARACTERIZED CMRR vs FREQUENCY

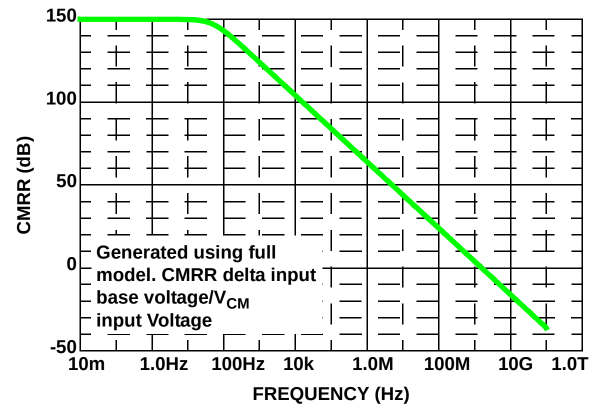

FIGURE 45. SIMULATED CMRR vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

REVISION	DATE	CHANGE
FN6633.3	3/11/10	PODs M8.118 and L8.3x3A - Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing.
	3/3/10	Page 2: Under "Ordering Information" ISL28227FBZ: Changed Vos max from 80µV to 75µV Page 4: Changed: 1. ISL28227 SOIC Room Temp limit for Vos from 80µV (MAX) and -80µV (MIN) to 75µV (MAX) and -75µV (MIN). 2. ISL28227 SOIC Full Temp limit for Vos from 160µV (MAX) and -160µV (MIN) to 150µV (MAX) and -150µV (MIN) 3. ISL28227 SOIC limit for TCVos from 0.8µV (MAX) and -0.8µV (MIN) to 0.75µV (MAX) and -0.75µV (MIN)
	3/2/10	HBM for ISL28227 changed from “4kV” to “6kV” Tjc values for ISL28227 changed: For MSOP from “50” to “45” For SOIC from “60” to “55”
	2/25/10	On the ordering info (page 2): Part Number Part Marking Vos (Max) (uV) ISL28127FRTBZ TBD instead of 70 ISL28127FRTZ -C 127Z instead of 127Z C ISL28127FUBZ TBD instead of 70 ISL28127FUZ 8127Z -C instead of 8127Z 150 instead of 70 Removed "Coming Soon) for ISL28127FUZ package ISL28227FBZ 80 instead of 70 Removed "Coming Soon) for ISL28227FBZ package ISL28227FRTBZ TBD instead of 70 ISL28227FRTZ -C 227Z instead of 227Z C ISL28227FUZ 8227Z -C instead of 8227Z 150 instead of 70 Added the following row of data ISL28227FUBZ 8227Z TBD On the Electrical specifications on page 4 and page 6 the following changes were made. The change applies to the same spec found on page 4 and page 6. VOS Offset Voltage; SOIC Package, ISL28127: Added -70 to MIN across room temp and -120 MIN across full temp VOS Offset Voltage; SOIC Package, ISL28227: Added -80 to MIN across room temp and -160 MIN across full temp VOS Offset Voltage; MSOP and TDFN Package Grade C, ISL28127/ISL28227: Added -150 to MIN across room temp and -250 MIN across full temp TCVOS Offset Voltage Drift; SOIC Package, ISL28127: Added -0.5 to MIN across full temp TCVOS Offset Voltage Drift; SOIC Package, ISL28227: Added -0.8 to MIN across full temp TCVOS Offset Voltage Drift; MSOP and TDFN Package Grade C, ISL28127/ISL28227: Added -1 to MIN across full temp IOS Input Offset Current: Added -10 to MIN across room temp and -12 to MIN across full temp IB Input Bias Current :Added -10 to MIN across room temp and -12 to MIN across full temp
	2/19/10	Added differentiated part numbers for B-grade and C-grade for TDFN and MSOP. Added ESD and latch-up information. Broke out Theta JA to list the single and dual and added Theta JC.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

REVISION	DATE	CHANGE
FN6633.2	1/29/10	Added license statement for P-Spice Model. Updated Spice Schematic by adding capacitors C4, C5 and C6 Updated Spice Net List as follows: From: Revision B, July 23 2009 To: Revision C, August 8th 2009 LaFontaine From: source ISL28127_SPICEMODEL_7_9 To: source ISL28127_SPICEMODEL_0_0 Added after I_IOS: C_C6 IN+ VIN- 2E-12 Added after R_R4: C_C4 VIN- 0 2.5e-12 C_C5 8 0 2.5e-12 From: .ends ISL28127 To: .ends ISL28127subckt Replaced POD MDP0027 with M8.15E to match ASYD in Intrepid (no dimension changes; the PODs are the same. The change was to update to the Intersil format, moving dimensions from table onto drawing and adding land pattern)
FN6633.1	9/14/09	"Functional Description" on page 11. Corrected low 1/f noise corner frequency from 3Hz to 5Hz to match "Input Noise Voltage Spectral Density" on page 1. Corrected high open loop gain from 1400V/mV to 1500V/mV to match "Open-Loop Gain" on page 5 spec table. "Operating Voltage Range" on page 11. Removed following 2 sentences since there are no graphs illustrating common mode voltage sensitivity vs temperature or VOS as a function of supply voltage and temperature: "The input common mode voltage sensitivity to temperature is shown in Figure 3 (±15V). Figure 20 shows VOS as a function of supply voltage and temperature with the common mode voltage at 0V for split supply operation."
	9/2/09	Added Theta JC in Thermal Information for TDFN package
	7/21/09	Updated Features to show only key features and updated applications section. Added Typical Application Circuit and performance graph, Updated Ordering Information to match Intrepid and added POD's L8.3x3A and M8.118, also added MSL level as part of new format. Added TDFN pinouts, updated pin descriptions to include TDFN pinouts, Added Theta Ja in Thermal information for TDFN and MSOP packages. Added Revision History and Products Text with device info links. Added SPICE Model with referencing text and Net List.
FN6633.0	5/28/09	Techdocs Issued File Number FN6633. Initial release of Datasheet with file number FN6633 making this a Rev 0.

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28127, ISL28227

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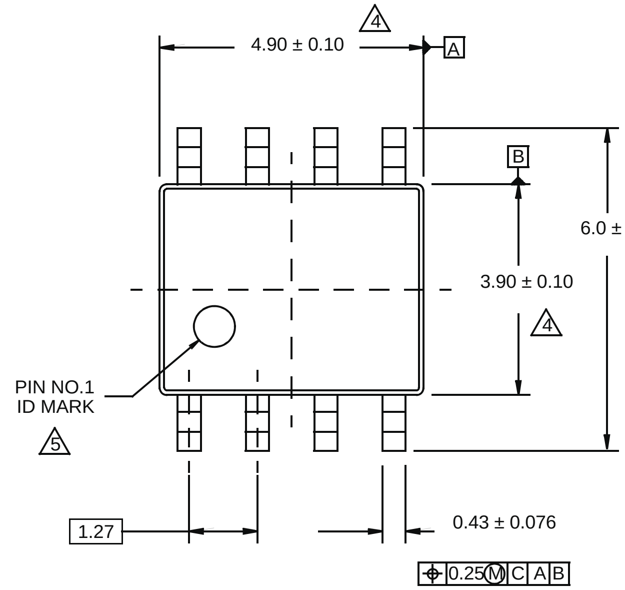
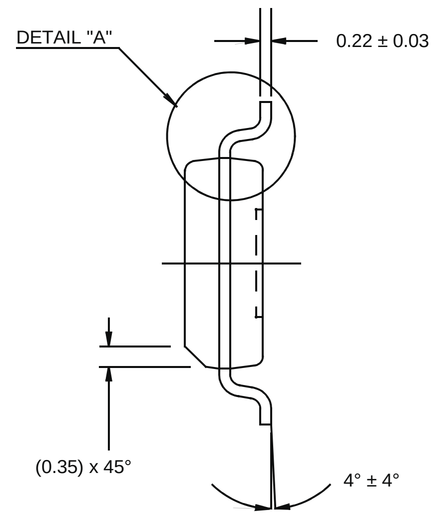
Package Outline Drawing

M8.15E

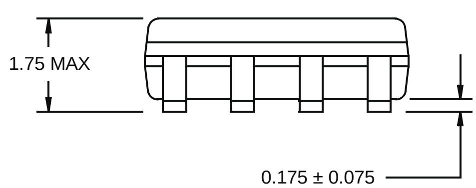
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



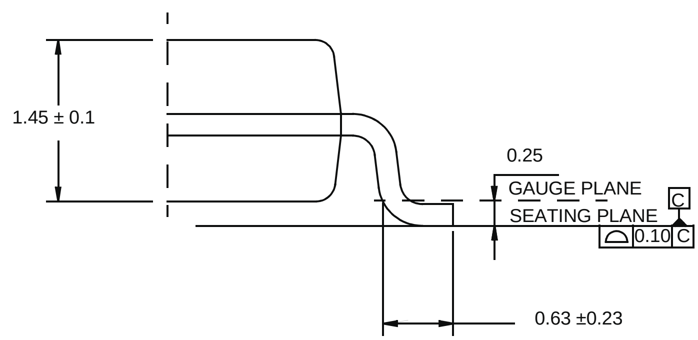
TOP VIEW



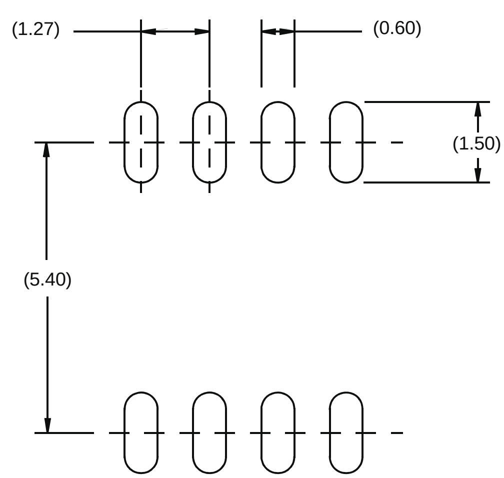
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

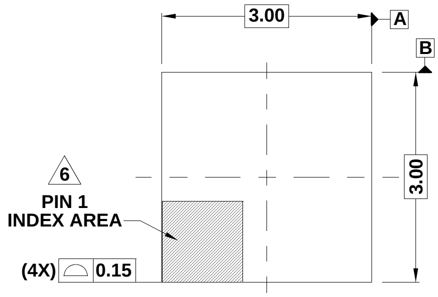
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

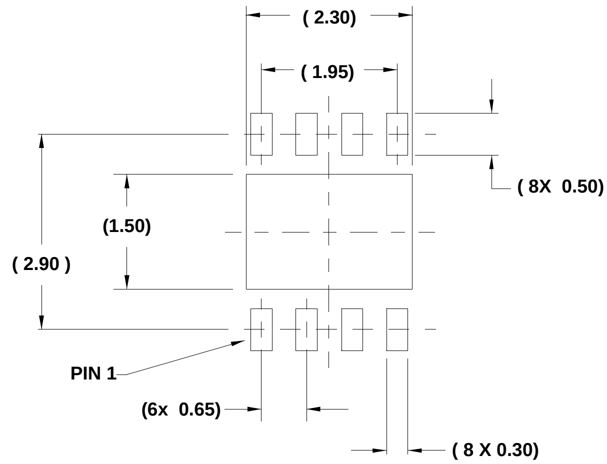
Package Outline Drawing

L8.3x3A

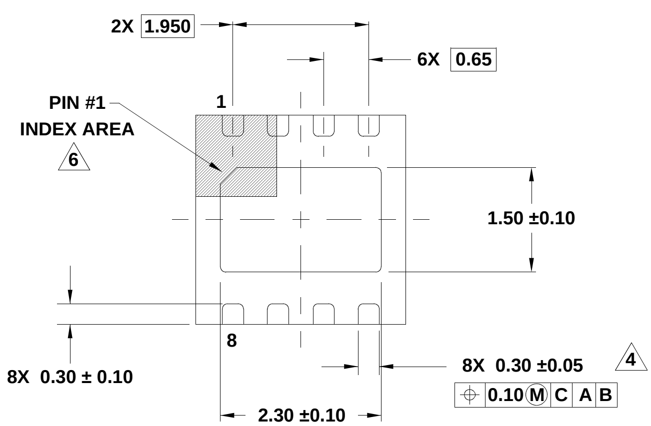
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



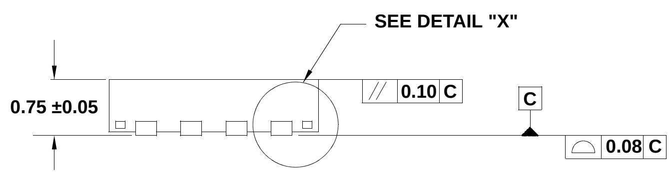
TOP VIEW



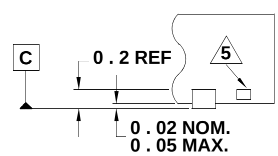
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

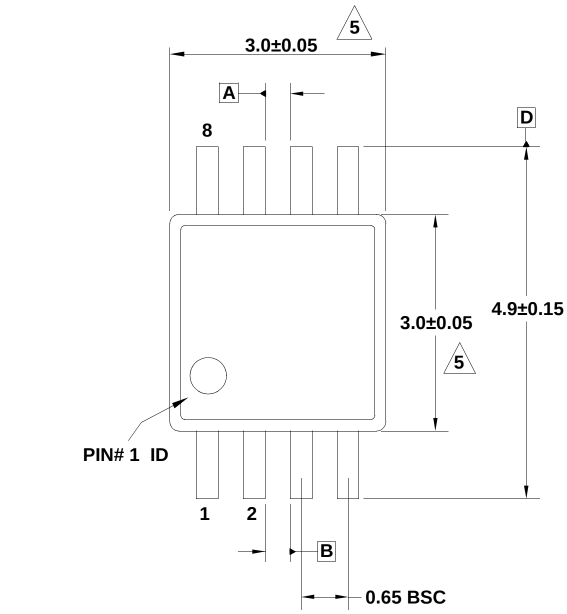
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

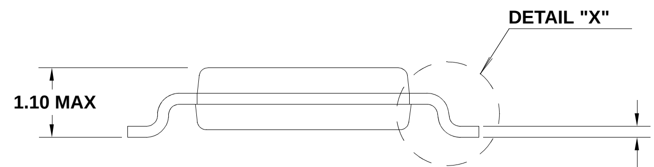
Package Outline Drawing

M8.118

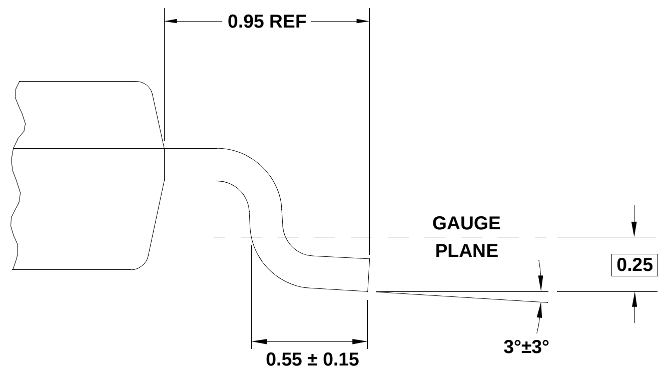
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



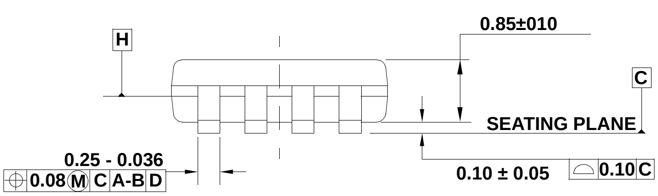
TOP VIEW



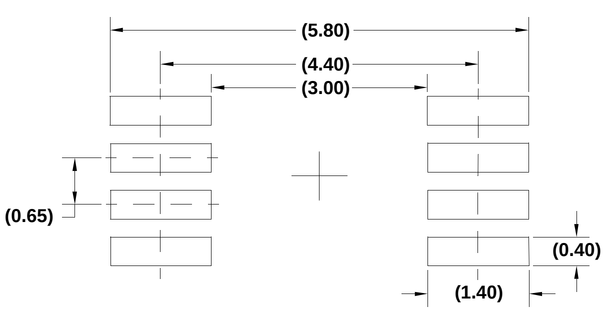
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.