2-CHANNEL HIGH DEFINITION AUDIO CODEC STAC9200/9200D

Description

The STAC9200/9200D is a high quality, 2-channel audio CODEC compatible with the Intel High Definition (HD) Audio Interface. The STAC9200/9200D provides Stereo 24-Bit resolution with sample rates up to 192 KHz. SPDIF I/O provides connectivity to consumer electronic equipment. The STAC9200/9200D incorporates IDT's proprietary SD technology to achieve an estimated DAC SNR in excess of 100dB.

The STAC9200/9200D provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

Features

- **High performance** SD **technology**
- **100dB DAC SNR**
- **Intel HD Audio Interface**
- **Two Channel DACs and ADCs with 24-bit resolution**
- **Sample rates up to 192 KHz**
- **Mixer-less design**
  - Low-latency Karaoke Mode Supported
- **Integrated Headphone Amplifiers**
- **Stereo Microphone**
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- **Direct CDROM Recording Mixerless Design**
- **S/PDIF In and Out**
- **Universal Jacks™ Functionality for jack retasking**
- **Adjustable VREF Out**
- **Digital PC Beep to all outputs**
- **+3.3 V, +4 V and +5 V analog power supply options** (The +4 V Analog voltage is supported by the +5 V version of the STAC9200 or STAC9200D. Request +4 V configuration of the driver.)
- **32-pad QFN (5mm x 5mm) and 48-pin LQFP package options**
- **Dolby Sound Room Compliant (STAC9200D only)** (System manufacturers must obtain system license from Dolby.)
- **Dolby Home Theater Compliant (STAC9200D only)** (System manufacturers must obtain system license from Dolby.)

Table of Contents

1. DESCRIPTION 9
2. PERFORMANCE 10
2.1. Audio Fidelity 10
2.2. Electrical Specifications 10
2.2.1. Absolute Maximum Ratings 10
2.2.2. Recommended Operation Conditions 10
2.3. Power Consumption 11
2.3.1. Digital 11
2.3.2. Analog 11
2.4. STAC9200/9200D 5V Analog Performance Characteristics 12
2.5. STAC9200/9200D 4V Analog Performance Characteristics 14
2.6. STAC9200/9200D 3.3V Analog Performance Characteristics 16
3. EXTENDED FEATURE EXPLANATION 18
3.1. SPDIF Input 18
3.2. SPDIF Output 18
3.3. Universal JacksTM 18
3.4. Audio Jack Presence Detect 18
4. BLOCK DIAGRAMS AND TYPICAL HOOKUPS 19
4.1. Functional Block Diagram 19
4.2. STAC9200/9200D Typical Connection Diagram for 48-pin LQFP 20
4.3. STAC9200/9200D Split Independent Power Supply for 48-pin LQFP 20
4.4. STAC9200/9200D Typical Connection Diagram for 32-pad QFN 20
4.5. STAC9200/9200D Split Independent Power Supply for 32-pad QFN 20
5. WIDGET INFORMATION 21
5.1. Widget Diagram 21
5.2. STAC9200/9200D Widget List 22
5.3. Root Node (NID = 0x00) 23
5.3.1. Root PnpID 23
5.3.2. Root RevID 23
5.3.3. Root NodeInfo 24
5.4. AFG Node (NID = 0x01) 24
5.4.1. AFG Reset 24
5.4.2. AFG NodeInfo 25
5.4.3. AFG Type 25
5.4.4. AFG GrpCap 25
5.4.5. AFG FrmtCap 26
5.4.6. AFG StreamCap 27
5.4.7. AFG PwrCap 28
5.4.8. AFG GPIOCap 28
5.4.9. AFG OutAmpCap 29
5.4.10. AFG PwrState 30
5.4.11. AFG UnsolResp 30
5.4.12. AFG GPIO 31
5.4.13. AFG GPIOEn 32
5.4.14. AFG GPIODir 33
5.4.15. AFG GPIOWake 33
5.4.16. AFG GPIOUnsolEn 34
5.4.17. AFG GPIOSticky 35
5.4.18. AFG SysID 36
5.5. DAC0Cnvtr Node (NID = 0x02) 37
5.5.1. DAC0Cnvtr Frmt 37
5.5.2. DAC0Cnvtr WCap 38
5.5.3. DAC0Cnvtr PwrState 39

5.5.4. DAC0Cnvtr Stream 40
5.6. ADC0Cnvtr Node (NID = 0x03) 40
5.6.1. ADC0Cnvtr Frmt 40
5.6.2. ADC0Cnvtr WCap 41
5.6.3. ADC0Cnvtr ConnLen 42
5.6.4. ADC0Cnvtr ConnLst 43
5.6.5. ADC0Cnvtr ProcState 43
5.6.6. ADC0Cnvtr PwrState 44
5.6.7. ADC0Cnvtr Stream 45
5.7. SPDIFinCnvtr Node (NID = 0x04) 45
5.7.1. SPDIFinCnvtr Frmt 45
5.7.2. SPDIFinCnvtr WCap 46
5.7.3. SPDIFinCnvtr FrmtCap 47
5.7.4. SPDIFinCnvtr StreamCap 48
5.7.5. SPDIFinCnvtr ConnLen 49
5.7.6. SPDIFinCnvtr ConnLst 49
5.7.7. SPDIFinCnvtr Stream 50
5.7.8. SPDIFinCnvtr DigCtl 50
5.8. SPDIFoutCnvtr Node (NID = 0x05) 51
5.8.1. SPDIFoutCnvtr Frmt 51
5.8.2. SPDIFoutCnvtr WCap 52
5.8.3. SPDIFoutCnvtr FrmtCap 53
5.8.4. SPDIFoutCnvtr StreamCap 54
5.8.5. SPDIFoutCnvtr Stream 55
5.8.6. SPDIFoutCnvtr DigCtl 55
5.9. DAC0Mux Node (NID = 0x07) 56
5.9.1. DAC0Mux WCap 56
5.9.2. DAC0Mux ConnLen 57
5.9.3. DAC0Mux ConnSel 58
5.9.4. DAC0Mux ConnLst 58
5.9.5. DAC0Mux LR 58
5.10. DigInPin Node (NID = 0x08) 59
5.10.1. DigInPin WCap 59
5.10.2. DigInPin Cap 60
5.10.3. DigInPin PwrState 61
5.10.4. DigInPin Ctl 61
5.10.5. DigInPin UnsolResp 62
5.10.6. DigInPin Sense 62
5.10.7. DigInPin EAPD 63
5.10.8. DigInPin Config 63
5.11. DigOutPin Node (NID = 0x09) 64
5.11.1. DigOutPin WCap 64
5.11.2. DigOutPin Cap 65
5.11.3. DigOutPin ConnLen 66
5.11.4. DigOutPin ConnSel 67
5.11.5. DigOutPin ConnLst 67
5.11.6. DigOutPin Ctl 67
5.11.7. DigOutPin Config 68
5.12. ADC0Mux Node (NID = 0x0A) 69
5.12.1. ADC0Mux VolRight 69
5.12.2. ADC0Mux VolLeft 69
5.12.3. ADC0Mux WCap 70
5.12.4. ADC0Mux OutAmpCap 71
5.12.5. ADC0Mux ConnLen 71
5.12.6. ADC0Mux ConnLst 72

5.12.7. ADC0Mux LR 72
5.13. MasterVol Node (NID = 0x0B) 73
5.13.1. MasterVol Right 73
5.13.2. MasterVol Left 73
5.13.3. MasterVol WCap 74
5.13.4. MasterVol ConnLen 75
5.13.5. MasterVol ConnLst 75
5.14. InPortMux Node (NID = 0x0C) 76
5.14.1. InPortMux VolRight 76
5.14.2. InPortMux VolLeft 76
5.14.3. InPortMux WCap 77
5.14.4. InPortMux ConnLen 78
5.14.5. InPortMux AmpCap 78
5.14.6. InPortMux ConnSel 79
5.14.7. InPortMux ConnLst0 79
5.14.8. InPortMux ConnLst4 79
5.15. PortAPin Node (NID = 0x0D) 80
5.15.1. PortAPin WCap 80
5.15.2. PortAPin Cap 81
5.15.3. PortAPin ConnLen 82
5.15.4. PortAPin ConnLst 82
5.15.5. PortAPin Ctl 82
5.15.6. PortAPin UnsolResp 83
5.15.7. PortAPin Sense 84
5.15.8. PortAPin Config 84
5.16. PortDPin Node (NID = 0x0E) 85
5.16.1. PortDPin WCap 85
5.16.2. PortDPin Cap 86
5.16.3. PortDPin ConnLen 87
5.16.4. PortDPin ConnLst 87
5.16.5. PortDPin Ctl 88
5.16.6. PortDPin UnsolResp 88
5.16.7. PortDPin Sense 89
5.16.8. PortDPin Config 90
5.17. PortCPin Node (NID = 0x0F) 90
5.17.1. PortCPin WCap 90
5.17.2. PortCPin Cap 91
5.17.3. PortCPin ConnLen 92
5.17.4. PortCPin ConnLst 93
5.17.5. PortCPin Ctl 93
5.17.6. PortCPin UnsolResp 94
5.17.7. PortCPin Sense 94
5.17.8. PortCPin Config 95
5.18. PortBPin Node (NID = 0x10) 96
5.18.1. PortBPin WCap 96
5.18.2. PortBPin Cap 97
5.18.3. PortBPin ConnLen 98
5.18.4. PortBPin ConnLst 98
5.18.5. PortBPin Ctl 98
5.18.6. PortBPin UnsolResp 99
5.18.7. PortBPin Sense 100
5.18.8. PortBPin Config 100
5.19. MonoOutPin Node (NID = 0x11) 101
5.19.1. MonoOutPin Vol 101
5.19.2. MonoOutPin WCap 102

5.19.3. MonoOutPin Cap 103
5.19.4. MonoOutPin ConnLen 103
5.19.5. MonoOutPin ConnLst 104
5.19.6. MonoOutPin Ctl 104
5.19.7. MonoOutPin Config 105
5.20. CDPin Node (NID = 0x12) 106
5.20.1. CDPin WCap 106
5.20.2. CDPin Cap 107
5.20.3. CDPin Ctl 108
5.20.4. CDPin Config 108
5.21. MonoOutMix Node (NID = 0x13) 109
5.21.1. MonoOutMix WCap 109
5.21.2. MonoOutMix ConnLen 110
5.21.3. MonoOutMix ConnLst 110
5.22. PCBeep Node (NID = 0x14) 111
5.22.1. PCBeep Vol 111
5.22.2. PCBeep WCap 111
5.22.3. PCBeep OutAmpCap 112
5.22.4. PCBeep Gen 113
6. ORDERING INFORMATION 114
6.1. STAC9200 Family Options and Part Order Numbers 114
7. PIN INFORMATION 115
7.1. Pin Out 115
7.2. Pin Table for 48-pin LQFP and 32-pad QFN Packages 116
8. PACKAGE DRAWINGS 118
8.1. 32-pin QFN 118
8.2. 48-Pin LQFP 119
9. SOLDER REFLOW PROFILE 120
9.1. Standard Reflow Profile Data 120
9.2. Pb Free Process - Package Classification Reflow Temperatures 121
10. REVISION HISTORY 122

List of Figures

Figure 1. Functional Block Diagram 21
Figure 2. Widget Diagram 23
Figure 3. 32-Pad QFN Package Outline and Package Dimensions 120
Figure 4. 48-Pin LQFP Package Outline and Package Dimensions 121
Figure 5. Solder Reflow Profile 122

List of Tables

Table 1. Digital Power Consumption 13
Table 2. Analog Power Consumption 13
Table 3. High Definition Audio Widget 24
Table 4. Root PnpID Command Verb Format 25
Table 5. Root PnpID Command Response Format 25
Table 6. Root RevID Command Verb Format 25
Table 7. Root RevID Command Response Format 25

Table 8. Root NodeInfo Command Verb Format 26
Table 9. Root NodeInfo Command Response Format 26
Table 10. AFG Reset Command Verb Format 26
Table 11. AFG Reset Command Response Format 26
Table 12. AFG NodeInfo Command Verb Format 27
Table 13. AFG NodeInfo Command Response Format 27
Table 14. AFG Type Command Verb Format 27
Table 15. AFG Type Command Response Format 27
Table 16. AFG GrpCap Command Verb Format 27
Table 17. AFG GrpCap Command Response Format 28
Table 18. AFG FrmtCap Command Verb Format 28
Table 19. AFG FrmtCap Command Response Format 28
Table 20. AFG StreamCap Command Verb Format 29
Table 21. AFG StreamCap Command Response Format 29
Table 22. AFG PwrCap Command Verb Format 30
Table 23. AFG PwrCap Command Response Format 30
Table 24. AFG GPIOCap Command Verb Format 30
Table 25. AFG GPIOCap Command Response Format 31
Table 26. AFG OutAmpCap Command Verb Format 31
Table 27. AFG OutAmpCap Command Response Format 31
Table 28. AFG PwrState Command Verb Format 32
Table 29. AFG PwrState Command Response Format 32
Table 30. AFG UnsolResp Command Verb Format 32
Table 31. AFG UnsolResp Command Response Format 33
Table 32. AFG GPIO Command Verb Format 33
Table 33. AFG GPIO Command Response Format 33
Table 34. AFG GPIOEn Command Verb Format 34
Table 35. AFG GPIOEn Command Response Format 34
Table 36. AFG GPIODir Command Verb Format 35
Table 37. AFG GPIODir Command Response Format 35
Table 38. AFG GPIOWake Command Verb Format 35
Table 39. AFG GPIOWake Command Response Format 36
Table 40. AFG GPIOUnsolEn Command Verb Format 36
Table 41. AFG GPIOUnsolEn Command Response Format 36
Table 42. AFG GPIOSticky Command Verb Format 37
Table 43. AFG GPIOSticky Command Response Format 37
Table 44. AFG SysID Command Verb Format 38
Table 45. AFG SysID Command Response Format 38
Table 46. DAC0Cnvtr Frmt Command Verb Format 39
Table 47. DAC0Cnvtr Frmt Command Response Format 39
Table 48. DAC0Cnvtr WCap Command Verb Format 40
Table 49. DAC0Cnvtr WCap Command Response Format 40
Table 50. DAC0Cnvtr PwrState Command Verb Format 41
Table 51. DAC0Cnvtr PwrState Command Response Format 41
Table 52. DAC0Cnvtr Stream Command Verb Format 42
Table 53. DAC0Cnvtr Stream Command Response Format 42
Table 54. ADC0Cnvtr Frmt Command Verb Format 42
Table 55. ADC0Cnvtr Frmt Command Response Format 42
Table 56. ADC0Cnvtr WCap Command Verb Format 43
Table 57. ADC0Cnvtr WCap Command Response Format 44
Table 58. ADC0Cnvtr ConnLen Command Verb Format 44
Table 59. ADC0Cnvtr ConnLen Command Response Format 45
Table 60. ADC0Cnvtr ConnLst Command Verb Format 45
Table 61. ADC0Cnvtr ConnLst Command Response Format 45
Table 62. ADC0Cnvtr ProcState Command Verb Format 45

Table 63. ADC0Cnvtr ProcState Command Response Format 46
Table 64. ADC0Cnvtr PwrState Command Verb Format 46
Table 65. ADC0Cnvtr PwrState Command Response Format 46
Table 66. ADC0Cnvtr Stream Command Verb Format 47
Table 67. ADC0Cnvtr Stream Command Response Format 47
Table 68. SPDIFinCnvtr Frmt Command Verb Format 47
Table 69. SPDIFinCnvtr Frmt Command Response Format 47
Table 70. SPDIFinCnvtr WCap Command Verb Format 48
Table 71. SPDIFinCnvtr WCap Command Response Format 48
Table 72. SPDIFinCnvtr FrmtCap Command Verb Format 49
Table 73. SPDIFinCnvtr FrmtCap Command Response Format 49
Table 74. SPDIFinCnvtr StreamCap Command Verb Format 50
Table 75. SPDIFinCnvtr StreamCap Command Response Format 51
Table 76. SPDIFinCnvtr ConnLen Command Verb Format 51
Table 77. SPDIFinCnvtr ConnLen Command Response Format 51
Table 78. SPDIFinCnvtr ConnLst Command Verb Format 51
Table 79. SPDIFinCnvtr ConnLst Command Response Format 51
Table 80. SPDIFinCnvtr Stream Command Verb Format 52
Table 81. SPDIFinCnvtr Stream Command Response Format 52
Table 82. SPDIFinCnvtr DigCtl Command Verb Format 52
Table 83. SPDIFinCnvtr DigCtl Command Response Format 52
Table 84. SPDIFoutCnvtr Frmt Command Verb Format 53
Table 85. SPDIFoutCnvtr Frmt Command Response Format 53
Table 86. SPDIFoutCnvtr WCap Command Verb Format 54
Table 87. SPDIFoutCnvtr WCap Command Response Format 55
Table 88. SPDIFoutCnvtr FrmtCap Command Verb Format 55
Table 89. SPDIFoutCnvtr FrmtCap Command Response Format 56
Table 90. SPDIFoutCnvtr StreamCap Command Verb Format 56
Table 91. SPDIFoutCnvtr StreamCap Command Response Format 57
Table 92. SPDIFoutCnvtr Stream Command Verb Format 57
Table 93. SPDIFoutCnvtr Stream Command Response Format 57
Table 94. SPDIFoutCnvtr DigCtl Command Verb Format 57
Table 95. SPDIFoutCnvtr DigCtl Command Response Format 58
Table 96. DAC0Mux WCap Command Verb Format 58
Table 97. DAC0Mux WCap Command Response Format 58
Table 98. DAC0Mux ConnLen Command Verb Format 59
Table 99. DAC0Mux ConnLen Command Response Format 59
Table 100. DAC0Mux ConnSel Command Verb Format 60
Table 101. DAC0Mux ConnSel Command Response Format 60
Table 102. DAC0Mux ConnLst Command Verb Format 60
Table 103. DAC0Mux ConnLst Command Response Format 60
Table 104. DAC0Mux LR Command Verb Format 60
Table 105. DAC0Mux LR Command Response Format 61
Table 106. DigInPin WCap Command Verb Format 61
Table 107. DigInPin WCap Command Response Format 61
Table 108. DigInPin Cap Command Verb Format 62
Table 109. DigInPin Cap Command Response Format 62
Table 110. DigInPin PwrState Command Verb Format 63
Table 111. DigInPin PwrState Command Response Format 63
Table 112. DigInPin Ctl Command Verb Format 63
Table 113. DigInPin Ctl Command Response Format 63
Table 114. DigInPin UnsolResp Command Verb Format 64
Table 115. DigInPin UnsolResp Command Response Format 64
Table 116. DigInPin Sense Command Verb Format 64
Table 117. DigInPin Sense Command Response Format 65

Table 118. DigInPin EAPD Command Verb Format 65
Table 119. DigInPin EAPD Command Response Format 65
Table 120. DigInPin Config Command Verb Format 65
Table 121. DigInPin Config Command Response Format 66
Table 122. DigOutPin WCap Command Verb Format 66
Table 123. DigOutPin WCap Command Response Format 67
Table 124. DigOutPin Cap Command Verb Format 67
Table 125. DigOutPin Cap Command Response Format 68
Table 126. DigOutPin ConnLen Command Verb Format 68
Table 127. DigOutPin ConnLen Command Response Format 68
Table 128. DigOutPin ConnSel Command Verb Format 69
Table 129. DigOutPin ConnSel Command Response Format 69
Table 130. DigOutPin ConnLst Command Verb Format 69
Table 131. DigOutPin ConnLst Command Response Format 69
Table 132. DigOutPin Ctl Command Verb Format 69
Table 133. DigOutPin Ctl Command Response Format 70
Table 134. DigOutPin Config Command Verb Format 70
Table 135. DigOutPin Config Command Response Format 70
Table 136. ADC0Mux VolRight Command Verb Format 71
Table 137. ADC0Mux VolRight Command Response Format 71
Table 138. ADC0Mux VolLeft Command Verb Format 71
Table 139. ADC0Mux VolLeft Command Response Format 72
Table 140. ADC0Mux WCap Command Verb Format 72
Table 141. ADC0Mux WCap Command Response Format 72
Table 142. ADC0Mux OutAmpCap Command Verb Format 73
Table 143. ADC0Mux OutAmpCap Command Response Format 73
Table 144. ADC0Mux ConnLen Command Verb Format 73
Table 145. ADC0Mux ConnLen Command Response Format 74
Table 146. ADC0Mux ConnLst Command Verb Format 74
Table 147. ADC0Mux ConnLst Command Response Format 74
Table 148. ADC0Mux LR Command Verb Format 74
Table 149. ADC0Mux LR Command Response Format 74
Table 150. MasterVol Right Command Verb Format 75
Table 151. MasterVol Right Command Response Format 75
Table 152. MasterVol Left Command Verb Format 75
Table 153. MasterVol Left Command Response Format 76
Table 154. MasterVol WCap Command Verb Format 76
Table 155. MasterVol WCap Command Response Format 76
Table 156. MasterVol ConnLen Command Verb Format 77
Table 157. MasterVol ConnLen Command Response Format 77
Table 158. MasterVol ConnLst Command Verb Format 77
Table 159. MasterVol ConnLst Command Response Format 77
Table 160. InPortMux VolRight Command Verb Format 78
Table 161. InPortMux VolRight Command Response Format 78
Table 162. InPortMux VolLeft Command Verb Format 78
Table 163. InPortMux VolLeft Command Response Format 78
Table 164. InPortMux WCap Command Verb Format 79
Table 165. InPortMux WCap Command Response Format 79
Table 166. InPortMux ConnLen Command Verb Format 80
Table 167. InPortMux ConnLen Command Response Format 80
Table 168. InPortMux AmpCap Command Verb Format 80
Table 169. InPortMux AmpCap Command Response Format 80
Table 170. InPortMux ConnSel Command Verb Format 81
Table 171. InPortMux ConnSel Command Response Format 81
Table 172. InPortMux ConnLst0 Command Verb Format 81

Table 173. InPortMux ConnLst0 Command Response Format 81
Table 174. InPortMux ConnLst4 Command Verb Format 81
Table 175. InPortMux ConnLst4 Command Response Format 82
Table 176. PortAPin WCap Command Verb Format 82
Table 177. PortAPin WCap Command Response Format 82
Table 178. PortAPin Cap Command Verb Format 83
Table 179. PortAPin Cap Command Response Format 83
Table 180. PortAPin ConnLen Command Verb Format 84
Table 181. PortAPin ConnLen Command Response Format 84
Table 182. PortAPin ConnLst Command Verb Format 84
Table 183. PortAPin ConnLst Command Response Format 84
Table 184. PortAPin Ctl Command Verb Format 84
Table 185. PortAPin Ctl Command Response Format 85
Table 186. PortAPin UnsolResp Command Verb Format 85
Table 187. PortAPin UnsolResp Command Response Format 85
Table 188. PortAPin Sense Command Verb Format 86
Table 189. PortAPin Sense Command Response Format 86
Table 190. PortAPin Config Command Verb Format 86
Table 191. PortAPin Config Command Response Format 87
Table 192. PortDPin WCap Command Verb Format 87
Table 193. PortDPin WCap Command Response Format 87
Table 194. PortDPin Cap Command Verb Format 88
Table 195. PortDPin Cap Command Response Format 88
Table 196. PortDPin ConnLen Command Verb Format 89
Table 197. PortDPin ConnLen Command Response Format 89
Table 198. PortDPin ConnLst Command Verb Format 89
Table 199. PortDPin ConnLst Command Response Format 90
Table 200. PortDPin Ctl Command Verb Format 90
Table 201. PortDPin Ctl Command Response Format 90
Table 202. PortDPin UnsolResp Command Verb Format 90
Table 203. PortDPin UnsolResp Command Response Format 91
Table 204. PortDPin Sense Command Verb Format 91
Table 205. PortDPin Sense Command Response Format 91
Table 206. PortDPin Config Command Verb Format 92
Table 207. PortDPin Config Command Response Format 92
Table 208. PortCPin WCap Command Verb Format 92
Table 209. PortCPin WCap Command Response Format 93
Table 210. PortCPin Cap Command Verb Format 93
Table 211. PortCPin Cap Command Response Format 94
Table 212. PortCPin ConnLen Command Verb Format 94
Table 213. PortCPin ConnLen Command Response Format 94
Table 214. PortCPin ConnLst Command Verb Format 95
Table 215. PortCPin ConnLst Command Response Format 95
Table 216. PortCPin Ctl Command Verb Format 95
Table 217. PortCPin Ctl Command Response Format 95
Table 218. PortCPin UnsolResp Command Verb Format 96
Table 219. PortCPin UnsolResp Command Response Format 96
Table 220. PortCPin Sense Command Verb Format 96
Table 221. PortCPin Sense Command Response Format 96
Table 222. PortCPin Config Command Verb Format 97
Table 223. PortCPin Config Command Response Format 97
Table 224. PortBPin WCap Command Verb Format 98
Table 225. PortBPin WCap Command Response Format 98
Table 226. PortBPin Cap Command Verb Format 99
Table 227. PortBPin Cap Command Response Format 99

Table 228. PortBPin ConnLen Command Verb Format 100
Table 229. PortBPin ConnLen Command Response Format 100
Table 230. PortBPin ConnLst Command Verb Format 100
Table 231. PortBPin ConnLst Command Response Format 100
Table 232. PortBPin Ctl Command Verb Format 100
Table 233. PortBPin Ctl Command Response Format 101
Table 234. PortBPin UnsolResp Command Verb Format 101
Table 235. PortBPin UnsolResp Command Response Format 101
Table 236. PortBPin Sense Command Verb Format 102
Table 237. PortBPin Sense Command Response Format 102
Table 238. PortBPin Config Command Verb Format 102
Table 239. PortBPin Config Command Response Format 103
Table 240. MonoOutPin Vol Command Verb Format 103
Table 241. MonoOutPin Vol Command Response Format 103
Table 242. MonoOutPin WCap Command Verb Format 104
Table 243. MonoOutPin WCap Command Response Format 104
Table 244. MonoOutPin Cap Command Verb Format 105
Table 245. MonoOutPin Cap Command Response Format 105
Table 246. MonoOutPin ConnLen Command Verb Format 105
Table 247. MonoOutPin ConnLen Command Response Format 106
Table 248. MonoOutPin ConnLst Command Verb Format 106
Table 249. MonoOutPin ConnLst Command Response Format 106
Table 250. MonoOutPin Ctl Command Verb Format 106
Table 251. MonoOutPin Ctl Command Response Format 107
Table 252. MonoOutPin Config Command Verb Format 107
Table 253. MonoOutPin Config Command Response Format 107
Table 254. CDPin WCap Command Verb Format 108
Table 255. CDPin WCap Command Response Format 108
Table 256. CDPin Cap Command Verb Format 109
Table 257. CDPin Cap Command Response Format 109
Table 258. CDPin Ctl Command Verb Format 110
Table 259. CDPin Ctl Command Response Format 110
Table 260. CDPin Config Command Verb Format 110
Table 261. CDPin Config Command Response Format 110
Table 262. MonoOutMix WCap Command Verb Format 111
Table 263. MonoOutMix WCap Command Response Format 111
Table 264. MonoOutMix ConnLen Command Verb Format 112
Table 265. MonoOutMix ConnLen Command Response Format 112
Table 266. MonoOutMix ConnLst Command Verb Format 112
Table 267. MonoOutMix ConnLst Command Response Format 113
Table 268. PCBeep Vol Command Verb Format 113
Table 269. PCBeep Vol Command Response Format 113
Table 270. PCBeep WCap Command Verb Format 113
Table 271. PCBeep WCap Command Response Format 114
Table 272. PCBeep OutAmpCap Command Verb Format 114
Table 273. PCBeep OutAmpCap Command Response Format 114
Table 274. PCBeep Gen Command Verb Format 115
Table 275. PCBeep Gen Command Response Format 115

1. DESCRIPTION

The STAC9200/9200D is a high quality, 2-channel audio CODEC compatible with the Intel High Definition (HD) Audio Interface (formerly known as “Azalia”). The STAC9200/9200D provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications. The STAC9200/9200D has been designed as a drop-in replacement for the STAC9772/73 Dual Mode (HD Audio and AC97) 2-channel CODEC once the need to support AC97 is eliminated.

The STAC9200/9200D incorporates IDT's proprietary SD technology to achieve a DAC SNR in excess of 100dB. The higher performance and quality of IDT’s audio solutions brings consumer device level performance to the notebook, desktop and media center PCs.

The STAC9200/9200D provides Stereo 24-Bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9200/9200D DAC, ADC and SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz. Additionally, the SPDIF Out supports 32 KHz. The CODEC’s driver supports additional sample rate options.

The STAC9200/9200D supports all desired two channel configurations, including switchable Headphone Out, and Universal Jacks™ functionality for automatic jack detection sensing and retasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9200/9200D has four General Purpose I/O (GPIO) pins. The STAC9200/9200D also provides a single ended CD input to avoid DRM incompatibility and to support legacy OS issues.

The STAC9200/9200D integrates a headphone amplifier which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODEC to detect when audio devices are connected to the CODEC, sense the type of device (LINE_IN, LINE_OUT, MIC, Headphone) that is inserted, and to allow the CODEC to be reconfigured to support these devices wherever they are plugged into the system. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The STAC9200/9200D operates with a 3.3V digital supply and is available in either 5V, 4V or 3.3V analog supply. The +4V Analog voltage is supported by the +5V version of the STAC9200 or STAC9200D appropriate configuration settings of the driver.

The STAC9200/9200D is available in 48-pin LQFP and 32-pad QFN package options. The 32-pad QFN package can be co-located inside the standard 48-pin footprint allowing systems to be designed to accept either version of the STAC9200/9200D or be compatible with existing 48-pin CODECs. Both the 48-pin LQFP and the 32-pad QFN are available in the ROHS compliant Lead (Pb) free package.

The STAC9200/9200D is supported with IDT’s high quality software solutions which include drivers for all major Windows operating systems from Microsoft Parametric SoftEQ, and Digital Rights Management. Third party plugin capability is easily achieved with the IDT Kernel Processing Interface, to support high valued third party technologies like SRS WOW®, Knowles® Microphone Beam forming, Waves MaxxBASS®, Dolby Headphone®, Dolby ProLogic II® and Dolby Virtual Speaker® and more.

The STAC9200D is designed to support Dolby Sound Room and Dolby Home Theater levels of Dolby’s PC Entertainments Experience logo program.

2. PERFORMANCE

2.1. Audio Fidelity

DAC SNR: 100dB
ADC SNR: 90dB

2.2. Electrical Specifications

2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9200/9200D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0^{o}C to +70^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		260 ^{o}C for 10 seconds * Soldering temperature information for all available packages begins on page 122.

2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4V Analog voltage is supported by the +5V version of the STAC9200 or STAC9200D.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9200/9200D is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9200/9200D implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.3. Power Consumption

2.3.1. Digital

Table 1. Digital Power Consumption

Power State	Typical	Max	Units
D0	25	29	mA
D1	12	16	mA
D2	12	16	mA
D3	12	16	mA

2.3.2. Analog

Table 2. Analog Power Consumption

Power State	Typical	Max	Units
D0	36	48	mA
D1	26	35	mA
D2	26	35	mA
D3	26	35	mA

2.4. STAC9200/9200D 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 KW/50pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0 dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1VRMS Input Referenced)	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-85	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-88	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to DAC (1 KHz Signal Frequency) Crosstalk		-100		dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	W
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. Sample Frequency = 48 KHz.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.5. STAC9200/9200D 4V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 4.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 KW/50 pF load, Testbench Characterization BW: 20 Hz – 20 Hz, 0 dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1VRMS Input Referenced)	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-85	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-88	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 Hz)	-	-70	-	dB
Power Supply Rejection Ratio (20 Hz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift		100	-	ppm/ºC
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	W
HEADPHONE_OUT Load Capacitance		-100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. Sample Frequency = 48 KHz.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.6. STAC9200/9200D 3.3V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 3.3V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 KW/50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0 dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	0.7	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1VRMS Input Referenced)	-	80	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-75	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-88	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-75	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift		100	-	ppm/ºC
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	W
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. Sample Frequency = 48 KHz.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

3. EXTENDED FEATURE EXPLANATION

3.1. SPDIF Input

SPDIF IN can run at 44.1 KHz, 48 KHz and 96 KHz, and has internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF_IN routing to the DAC allows for simultaneous record and play.

3.2. SPDIF Output

SPDIF Output can run at 44.1 KHz, 48 KHz, and 96 KHz at bit rates up to 24 bits, as defined in the Intel High Definition Audio Specification. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and multi-media centers.

3.3. Universal Jacks™

IDT's Universal Jacks™ technology allows for the greatest flexibility in board design and implementation.

For the STAC9200/9200D the Universal Jacks™ capabilities are as follows

- All of the STAC9200/9200D ports support:
  - Line Out
  - Line In
  - Mic with 0/10/20/30/40 dB Mic Boost
- Ports A and D also support
  - Headphone Out[1]

[1]Headphone capabilities are available on pins 39/41 and 35/36, but one should not put headphone loads on both sets of pins at the same time.

Note: On the STAC9200/9200D only one function can be selected at a time, you cannot have an input and output at the same time on the same set of pins. This function can be changed at any time.

3.4. Audio Jack Presence Detect

Sense_A pin is used to detect the presence of plugs in ports A, B, C, and D. Refer to the reference design for port detect circuitry. Select the precision of the resistors used as follows:

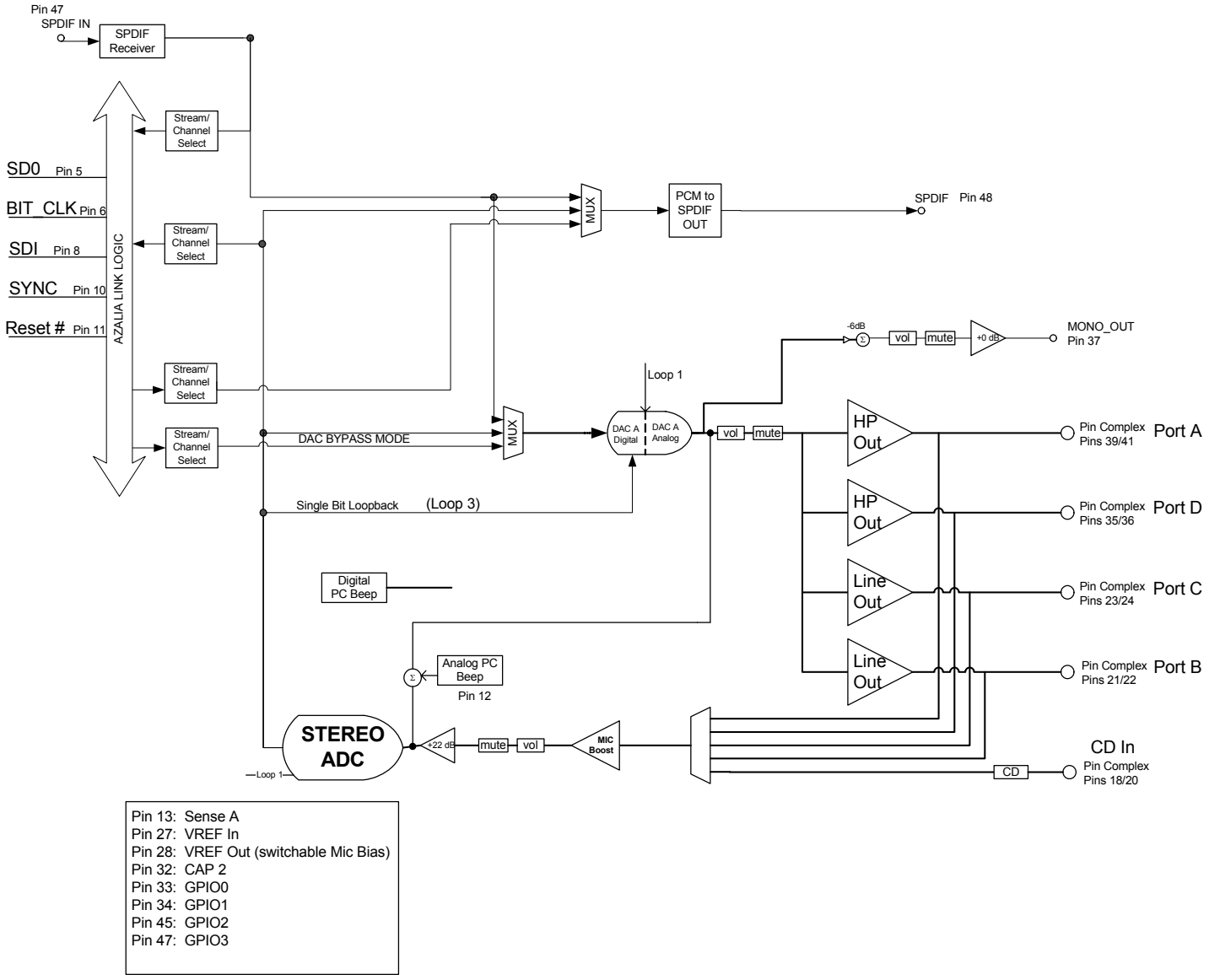
AVDD Nominal Voltage (+- 5%)	Resistor Tolerance (If Port D is used)	Resistor Tolerance (If Port D is not used)
5V	1%	1%
4.5V	1%	1%
4V	0.50%	1%
3.3V	0.10%	1%

Includes pull-up resistors on Sense A and series resistors between jack switch and Sense A.

4. BLOCK DIAGRAMS AND TYPICAL HOOKUPS

4.1. Functional Block Diagram

Figure 1. Functional Block Diagram



4.2. STAC9200/9200D Typical Connection Diagram for 48-pin LQFP

Please see the reference design for this information.

4.3. STAC9200/9200D Split Independent Power Supply for 48-pin LQFP

Please see the reference design for this information.

4.4. STAC9200/9200D Typical Connection Diagram for 32-pad QFN

Please see the reference design for this information.

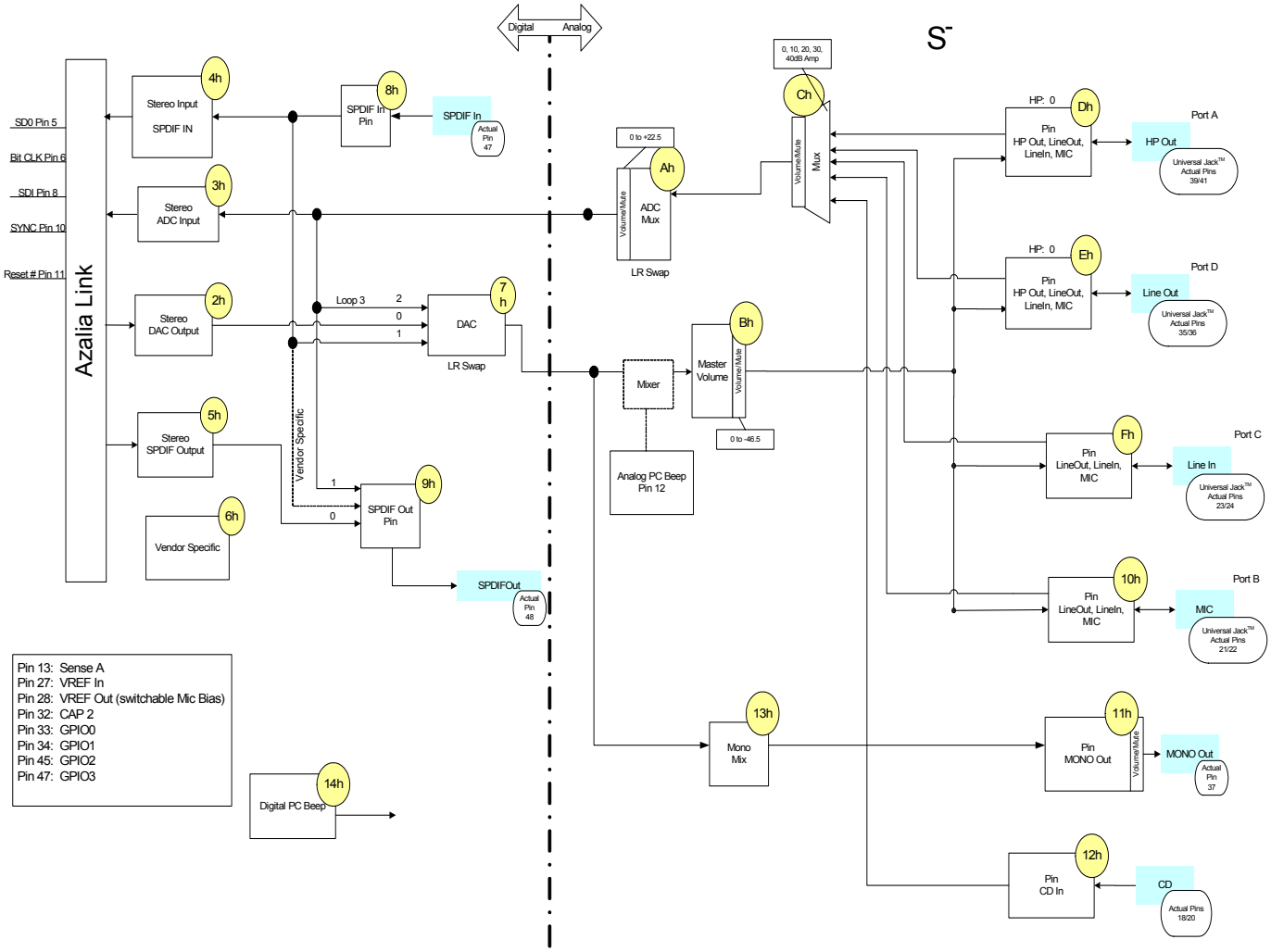
4.5. STAC9200/9200D Split Independent Power Supply for 32-pad QFN

Please see the reference design for this information.

5. WIDGET INFORMATION

5.1. Widget Diagram

Figure 2. Widget Diagram



5.2. STAC9200/9200D Widget List

Table 3. High Definition Audio Widget

ID	Widget Name	Description
1h	Audio Function Group	Audio Function Group
2h	DAC0	Stereo Output to DAC
3h	ADC0	Stereo Input Mux from ADC
4h	SPDIF_IN	Stereo Input for SPDIF_In
5h	SPDIF_OUT	Stereo Output for SPDIF_Out
6h	Reserved	Reserved: Unused
7h	DAC0Mux	Digital Mux for DAC
8h	SPDIF-In Pin	Pin Widget for SPDIF_In Pin 47
9h	SPDIF-Out Pin	Pin Widget for SPDIF_Out Pin 48
10h	Mic	Mic Pin Widget pins 21/22 (can also act as Line Out and Line In)
11h	Mono Out	Mono Out Volume Controls and Capabilities for pin 37
12h	CD	CD Pin Widget pins 18/20
13h	Mono Mix	Combines the Two Stereo Channels into one Mono Signal
14h	Digital PC Beep	Digital PC Beep
15h-19h	Reserved	Reserved: Unused
Ah	ADC0Mux	ADC Mux and Volume Control for inputs to ADC
Bh	Master Volume	Master Volume Controls
Ch	Input Mux	Input Mux to ADC for Widgets Dh, Eh, Fh, 10h, and 12h
Dh	Headphone	Headphone Pin Widget pins 39/41 (can also act as Line In, Line Out ,or Mic)
Eh	Line Out	Line Out Pin Widget pins 35/36 (can also act as HP, Line In, or Mic)
Fh	Line In	Line In Pin Widget pins 23/24 (can also act as Mic or Line Out)

Note: All widgets in this document are applicable to theSTAC9200/9200D B1 Revision. For widgets pertaining to the STAC9200/9200D A1 Revision, see STAC9200/9200D Datasheet Revision 0.8.

5.3. Root Node (NID = 0x00)

5.3.1. Root PnpID

Table 4. Root PnpID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 5. Root PnpID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Vendor	R	0x8384	Vendor ID STAC9200/9200D = 8384h
[15.:0]	Device	R	0x7690	Device ID: STAC9200 = 7690h Device ID: STAC9200D = 7691h

5.3.2. Root RevID

Table 6. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 7. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd	R	0x00	Reserved
[23.:20]	Major	R	0x1	Major rev number of compliant Azalia spec.
[19.:16]	Minor	R	0x0	Minor rev number of compliant Azalia spec.
[15.:8]	Vendor	R	0x22	Vendor rev number for this device ID: STAC9200/9200D = xxh
[7.:0]	Stepping	R	0x01	Vendor stepping number within the given Vendor RevID: STAC9200/9200D = xxh

5.3.3. Root NodeInfo

Table 8. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 9. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x00	Reserved
[23.:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15.:8]	Rsvd1	R	0x00	Reserved
[7.:0]	TotalNodes	R	0x01	Total number of nodes

5.4. AFG Node (NID = 0x01)

5.4.1. AFG Reset

Table 10. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table
Set1	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 11. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

5.4.2. AFG NodeInfo

Table 12. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 13. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:16]	StartNID	R	0x02	Starting node number for function group subordinate nodes.
[15.:8]	Rsvd1	R	0x0	Reserved
[7.:0]	TotalNodes	R	0x13	Total number of nodes.

5.4.3. AFG Type

Table 14. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table

Table 15. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:9]	Rsvd	R	0x0	Reserved
[8]	Unsol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7.:0]	NodeType	R	0x01	Node type = Audio Function Group

5.4.4. AFG GrpCap

Table 16. AFG GrpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table

Table 17. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15.:12]	Rsvd2	R	0x0	Reserved
[11.:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the Azalia link.
[7.:4]	Rsvd1	R	0x0	Reserved
[3.:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the Azalia link and when it appears as an analog signal at the pin.

5.4.5. AFG FrmtCap

Table 18. AFG FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 19. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15.:12]	Rsvd1	R	0x0	Reserved

Table 19. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2KHz rate (2/1*44.1KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

5.4.6. AFG StreamCap

Table 20. AFG StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 21. AFG StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x0	No support for non-PCM (AC3) data.
[1]	Float32	R	0x0	No support for single-precision floating-point data.
[0]	PCM	R	0x1	PCM-formatted data supported.

5.4.7. AFG PwrCap

Table 22. AFG PwrCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table

Table 23. AFG PwrCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	D3	R	0x1	Power State D3 is supported. Allows for lowest possible power consuming state under software control (and still properly respond to a subsequent Power State command).
[2]	D2	R	0x1	Power State D2 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 ms.
[1]	D1	R	0x1	Power State D1 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 ms, excepting analog pass-through circuits which must remain fully on.
[0]	D0	R	0x1	Power State D0 is supported. Node power state is fully on.

5.4.8. AFG GPIOCap

Table 24. AFG GPIOCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	11	See bitfield table

Table 25. AFG GPIOCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	0x1	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIOs configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	0x1	Unsolicited Response capability. Assuming the Unsolicited Enable Mask controls are enabled, GPIOs configured as inputs can generate an Unsolicited Response on the link when there is a change in level on the pin.
[29.:24]	Rsvd	R	0x0	Reserved
[23.:16]	NumGPIs	R	0x00	Number of GPI pins supported
[15.:8]	NumGPOs	R	0x00	Number of GPO pins supported
[7.:0]	NumGPIOs	R	0x04	Number of GPIO pins supported

5.4.9. AFG OutAmpCap

Table 26. AFG OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 27. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30.:23]	Rsvd3	R	0x0	Reserved
[22.:16]	StepSize	R	0x05	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14.:8]	NumSteps	R	0x1F	Number of steps in the gain range = 32 (-46.5dB to +0dB)

Table 27. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	Rsvd1	R	0x0	Reserved
[6.:0]	Offset	R	0x1F	0dB-step is programmed with this offset

5.4.10. AFG PwrState

Table 28. AFG PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 29. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7.:4]	Act	R	0x2	PS-Act: Actual power state of referenced node.
[3.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	Set	RW	0x2	PS-Set: Current power setting of referenced node. 0: All Powered-On 1: D1 => PR0, PR1 2: D2 => PR0, PR1, PR2, PR6, EAPD 3: D3 => PR6, PR5, PR3, PR2, PR1, PR0, EAPD Note: PR4 is not mapped in Azalia

5.4.11. AFG UnsolResp

Table 30. AFG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 31. AFG UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses.
[6]	Rsvd1	R	0x0	Reserved
[5.:0]	Tag	RW	0x0	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.4.12. AFG GPIO

Table 32. AFG GPIO Command Verb Format

	Verb ID	Payload	Response
Get	F15	00	See bitfield table
Set1	715	See bits [7:0] of bitfield table	0000_0000h

Table 33. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	Data3	RW	0x0	Data for GPIO3 (Pin 47/EAPD). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[2]	Data2	RW	0x0	Data for GPIO2 (Pin 45). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

Table 33. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Data1	RW	0x0	Data for GPIO1 (Pin 34). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[0]	Data0	RW	0x0	Data for GPIO0 (Pin 33). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

5.4.13. AFG GPIOEn

Table 34. AFG GPIOEn Command Verb Format

	Verb ID	Payload	Response
Get	F16	00	See bitfield table
Set1	716	See bits [7:0] of bitfield table	0000_0000h

Table 35. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	Enable for GPIO3: 0= pin is disabled (Hi-Z state); 1= pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0x0	Enable for GPIO2: 0= pin is disabled (Hi-Z state); 1= pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0x0	Enable for GPIO1: 0= pin is disabled (Hi-Z state); 1= pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0x0	Enable for GPIO0: 0= pin is disabled (Hi-Z state); 1= pin is enabled; behavior determined by GPIO Direction control

5.4.14. AFG GPIODir

Table 36. AFG GPIODir Command Verb Format

	Verb ID	Payload	Response
Get	F17	00	See bitfield table
Set1	717	See bits [7:0] of bitfield table	0000_0000h

Table 37. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	Control3	RW	0x0	Direction control for GPIO3 0= GPIO signal is configured as input 1= GPIO signal is configured as output
[2]	Control2	RW	0x0	Direction control for GPIO2 0= GPIO signal is configured as input 1= GPIO signal is configured as output
[1]	Control1	RW	0x0	Direction control for GPIO1 0= GPIO signal is configured as input 1= GPIO signal is configured as output
[0]	Control0	RW	0x0	Direction control for GPIO0 0= GPIO signal is configured as input 1= GPIO signal is configured as output

5.4.15. AFG GPIOWake

Table 38. AFG GPIOWake Command Verb Format

	Verb ID	Payload	Response
Get	F18	00	See bitfield table
Set1	718	See bits [7:0] of bitfield table	0000_0000h

Table 39. AFG GPIOWake Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	En3	RW	0x0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1= when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[2]	En2	RW	0x0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1= when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[1]	En1	RW	0x0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1= when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[0]	En0	RW	0x0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1= when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

5.4.16. AFG GPIOUnsolEn

Table 40. AFG GPIOUnsolEn Command Verb Format

	Verb ID	Payload	Response
Get	F19	00	See bitfield table
Set1	719	See bits [7:0] of bitfield table	0000_0000h

Table 41. AFG GPIOUnsolEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO3 is configured as input and changes state.

Table 41. AFG GPIOUnsolEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	Mask2	RW	0x0	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[1]	Mask1	RW	0x0	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state.
[0]	Mask0	RW	0x0	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

5.4.17. AFG GPIOSticky

Table 42. AFG GPIOSticky Command Verb Format

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table
Set1	71A	See bits [7:0] of bitfield table	0000_0000h

Table 43. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	GPIO3 input type (when configured as input): 0= Non-Sticky (level-sensitive); 1= Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[2]	Mask2	RW	0x0	GPIO2 input type (when configured as input): 0= Non-Sticky (level-sensitive); 1= Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

Table 43. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Mask1	RW	0x0	GPIO1 input type (when configured as input): 0= Non-Sticky (level-sensitive); 1= Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[0]	Mask0	RW	0x0	GPIO0 input type (when configured as input): 0= Non-Sticky (level-sensitive); 1= Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

5.4.18. AFG SysID

Table 44. AFG SysID Command Verb Format

	Verb ID	Payload	Response
Get	F20	00	See bitfield table
Set1	720	See bits [7:0] of bitfield table	0000_0000h
Set2	721	See bits [15:8] of bitfield table	0000_0000h
Set3	722	See bits [23:16] of bitfield table	0000_0000h
Set4	723	See bits [31:24] of bitfield table	0000_0000h

Table 45. AFG SysID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Subsystem3	RW	0x00	Subsystem ID. (Any non-zero value)
[23.:16]	Subsystem2	RW	0x00	
[15.:8]	Subsystem1	RW	0x01	
[7.:0]	Assembly	RW	0x00	Assembly ID. (Not applicable to CODEC vendors)

5.5. DAC0Cnvtr Node (NID = 0x02)

5.5.1. DAC0Cnvtr Frmt

Table 46. DAC0Cnvtr Frmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 47. DAC0Cnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	RateBase	RW	0x0	Sample Base Rate 0= 48 KHz 1= 44.1 KHz
[13.:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000= 48 KHz / 44.1 KHz or less 001= x2 010= Reserved (x3) 011= x4 100-111= Reserved
[10.:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 010= Divide by 3 011= Divide by 4 100= Divide by 5 101= Divide by 6 110= Divide by 7 111= Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 47. DAC0Cnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6.:4]	NumBits	RW	0x3	Bits per Sample 000= 8 bits 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
[3.:0]	NumChan	RW	0x1	Number of Channels in each frame of the stream. 0000= 1 channel 0001 = 2 channels ... 1111= 16 channels

5.5.2. DAC0Cnvtr WCap

Table 48. DAC0Cnvtr WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 49. DAC0Cnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x0	Widget type = Audio Output
[19.:16]	Delay	R	0xD	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter

Table 49. DAC0Cnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.5.3. DAC0Cnvtr PwrState

Table 50. DAC0Cnvtr PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 51. DAC0Cnvtr PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7.:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

5.5.4. DAC0Cnvtr Stream

Table 52. DAC0Cnvtr Stream Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 53. DAC0Cnvtr Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7.:4]	ID	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3.:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

5.6. ADC0Cnvtr Node (NID = 0x03)

5.6.1. ADC0Cnvtr Frmt

Table 54. ADC0Cnvtr Frmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 55. ADC0Cnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	RW	0x0	Stream Type 0= PCM 1= Non-PCM (remaining bits in this verb have other meanings)

Table 55. ADC0Cnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	RateBase	RW	0x0	Sample Base Rate 0= 48 KHz 1= 44.1 KHz
[13.:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000= 48 KHz / 44.1 KHz or less 001= x2 010= Reserved (x3) 011= x4 100-111= Reserved
[10.:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 010= Divide by 3 011= Divide by 4 100= Divide by 5 101= Divide by 6 110= Divide by 7 111= Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6.:4]	NumBits	RW	0x3	Bits per Sample 000= 8 bits 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
[3.:0]	NumChan	RW	0x1	Number of Channels in each frame of the stream. 0000= 1 channel 0001 = 2 channels ... 1111= 16 channels

5.6.2. ADC0Cnvtr WCap

Table 56. ADC0Cnvtr WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 57. ADC0Cnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x1	Widget type = Audio Input
[19.:16]	Delay	R	0xD	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.6.3. ADC0Cnvtr ConnLen

Table 58. ADC0Cnvtr ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 59. ADC0Cnvtr ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.6.4. ADC0Cnvtr ConnLst

Table 60. ADC0Cnvtr ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 61. ADC0Cnvtr ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0A	ADC Mux widget.

5.6.5. ADC0Cnvtr ProcState

Table 62. ADC0Cnvtr ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table
Set1	703	See bits [7:0] of bitfield table	0000_0000h

Table 63. ADC0Cnvtr ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOffsetDis	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	HPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

5.6.6. ADC0Cnvtr PwrState

Table 64. ADC0Cnvtr PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 65. ADC0Cnvtr PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7.:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default powered down)

5.6.7. ADC0Cnvtr Stream

Table 66. ADC0Cnvtr Stream Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 67. ADC0Cnvtr Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7.:4]	ID	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3.:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

5.7. SPDIFinCnvtr Node (NID = 0x04)

5.7.1. SPDIFinCnvtr Frmt

Table 68. SPDIFinCnvtr Frmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 69. SPDIFinCnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	RW	0x0	N/A. (Stream Type) 0= PCM 1= Non-PCM
[14]	RateBase	RW	0x0	Sample Base Rate 0= 48 KHz 1= 44.1 KHz

Table 69. SPDIFinCnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[13.:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000= 48 KHz / 44.1 KHz or less 001= x2 010= Reserved (x3) 011= x4 100-111= Reserved
[10.:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 010= Divide by 3 011= Divide by 4 100= Divide by 5 101= Divide by 6 110= Divide by 7 111= Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6.:4]	NumBits	RW	0x3	Bits per Sample 000= 8 bits 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
[3.:0]	NumChan	RW	0x1	Number of Channels in each frame of the stream. 0000= 1 channel 0001 = 2 channels ... 1111= 16 channels

5.7.2. SPDIFinCnvtr WCap

Table 70. SPDIFinCnvtr WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 71. SPDIFinCnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x1	Widget type = Audio Input

Table 71. SPDIFinCnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0x4	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.7.3. SPDIFinCnvtr FrmtCap

Table 72. SPDIFinCnvtr FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 73. SPDIFinCnvtr FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported

Table 73. SPDIFinCnvtr FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x0	192.0 KHz rate (4/1*48 KHz) NOT supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x0	88.2 KHz rate (2/1*44.1 KHz) NOT supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

5.7.4. SPDIFinCnvtr StreamCap

Table 74. SPDIFinCnvtr StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 75. SPDIFinCnvtr StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

5.7.5. SPDIFinCnvtr ConnLen

Table 76. SPDIFinCnvtr ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 77. SPDIFinCnvtr ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.7.6. SPDIFinCnvtr ConnLst

Table 78. SPDIFinCnvtr ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 79. SPDIFinCnvtr ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.

Table 79. SPDIFinCnvtr ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x08	SPDIF-In Pin widget.

5.7.7. SPDIFinCnvtr Stream

Table 80. SPDIFinCnvtr Stream Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 81. SPDIFinCnvtr Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7.:4]	ID	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3.:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

5.7.8. SPDIFinCnvtr DigCtl

Table 82. SPDIFinCnvtr DigCtl Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table
Set1	70D	See bits [7:0] of bitfield table	0000_0000h
Set2	70E	See bits [15:8] of bitfield table	0000_0000h

Table 83. SPDIFinCnvtr DigCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:15]	Rsvd2	R	0x0	Reserved
[14.:8]	CC	R	0x00	CC[6:0] - Category Code

Table 83. SPDIFinCnvtr DigCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	L	R	0x0	L - Generation Level
[6]	PRO	R	0x0	PRO - Professional
[5]	AUDIO	R	0x0	/AUDIO - Non-Audio
[4]	COPY	R	0x0	COPY - Copyright
[3]	PRE	R	0x0	PRE - Preemphasis
[2]	Rsvd1	R	0x0	Reserved (VCFG bit applies only to output streams)
[1]	V	R	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

5.8. SPDIFoutCnvtr Node (NID = 0x05)

5.8.1. SPDIFoutCnvtr Frmt

Table 84. SPDIFoutCnvtr Frmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 85. SPDIFoutCnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	RW	0x0	Stream Type 0= PCM 1= Non-PCM (remaining bits in this verb have other meanings)
[14]	RateBase	RW	0x0	Sample Base Rate 0= 48 KHz 1= 44.1 KHz

Table 85. SPDIFoutCnvtr Frmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[13.:11]	RateMult	RW	0x0	Sample Base Rate Multiple: 000= 48 KHz / 44.1 KHz or less; 001= x2; 010= Reserved (x3); 011= x4; 100-111= Reserved
[10.:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 010= Divide by 3 011= Divide by 4 100= Divide by 5 101= Divide by 6 110= Divide by 7 111= Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6.:4]	NumBits	RW	0x3	Bits per Sample 000= 8 bits 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
[3.:0]	NumChan	RW	0x1	Number of Channels in each frame of the stream. 0000= 1 channel 0001 = 2 channels ... 1111= 16 channels

5.8.2. SPDIFoutCnvtr WCap

Table 86. SPDIFoutCnvtr WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 87. SPDIFoutCnvtr WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x0	Widget type = Audio Output
[19.:16]	Delay	R	0x4	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.8.3. SPDIFoutCnvtr FrmtCap

Table 88. SPDIFoutCnvtr FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 89. SPDIFoutCnvtr FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x0	192.0 KHz rate (4/1*48 KHz) NOT supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

5.8.4. SPDIFoutCnvtr StreamCap

Table 90. SPDIFoutCnvtr StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 91. SPDIFoutCnvtr StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

5.8.5. SPDIFoutCnvtr Stream

Table 92. SPDIFoutCnvtr Stream Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 93. SPDIFoutCnvtr Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7.:4]	ID	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3.:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

5.8.6. SPDIFoutCnvtr DigCtl

Table 94. SPDIFoutCnvtr DigCtl Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table
Set1	70D	See bits [7:0] of bitfield table	0000_0000h
Set2	70E	See bits [15:8] of bitfield table	0000_0000h

Table 95. SPDIFoutCnvtr DigCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0x0	Reserved
[15]	Rsvd1	R	0x0	Reserved
[14.:8]	CC	RW	0x00	CC[6:0] - Category Code
[7]	L	RW	0x0	L - Generation Level
[6]	PRO	RW	0x0	PRO - Professional
[5]	AUDIO	RW	0x0	/AUDIO - Non-Audio
[4]	COPY	RW	0x0	COPY - Copyright
[3]	PRE	RW	0x0	PRE - Preemphasis
[2]	VCFG	RW	0x0	VCFG - Validity Config
[1]	V	RW	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

5.9. DAC0Mux Node (NID = 0x07)

5.9.1. DAC0Mux WCap

Table 96. DAC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 97. DAC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x3	Widget type = Audio Selector
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved

Table 97. DAC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.9.2. DAC0Mux ConnLen

Table 98. DAC0Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 99. DAC0Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x03	Number of NID entries in connection list.

5.9.3. DAC0Mux ConnSel

Table 100. DAC0Mux ConnSel Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 101. DAC0Mux ConnSel Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	0x0	Reserved
[1.:0]	Index	RW	0x0	Connection select control index.

5.9.4. DAC0Mux ConnLst

Table 102. DAC0Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 103. DAC0Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x0A	ADC Mux widget.
[15.:8]	Entry1	R	0x08	SPDIF-In Pin widget.
[7.:0]	Entry0	R	0x02	DAC Analog converter widget.

5.9.5. DAC0Mux LR

Table 104. DAC0Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 105. DAC0Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1= swap left and right channels of this Widget.
[1.:0]	Rsvd1	R	0x0	Reserved

5.10. DigInPin Node (NID = 0x08)

5.10.1. DigInPin WCap

Table 106. DigInPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 107. DigInPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x3	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 107. DigInPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.10.2. DigInPin Cap

Table 108. DigInPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 109. DigInPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x1	This widget controls EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable. (EAPD not equal to output stream)
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

5.10.3. DigInPin PwrState

Table 110. DigInPin PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 111. DigInPin PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7.:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default powered down)

5.10.4. DigInPin Ctl

Table 112. DigInPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 113. DigInPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1= (CODEC) input path of Pin Widget is enabled
[4.:0]	Rsvd1	R	0x0	Reserved

5.10.5. DigInPin UnsolResp

Table 114. DigInPin UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 115. DigInPin UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon lock or loss-of-lock by SPDIF-in clock recovery circuit.
[6]	Rsvd1	R	0x0	Reserved.
[5.:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.10.6. DigInPin Sense

Table 116. DigInPin Sense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 117. DigInPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Present	R	0x0	1= something is plugged into jack associated with Pin Complex. For this widget, Presence Detect indicates that the SPDIF-in clock recovery circuit has locked onto a valid SPDIF-in sampling frequency. Any change in status will generate an Unsolicited Response, if enabled with verb 708.
[30.:0]	Rsvd	R	0x0	Reserved. Impedance sense not supported for this Pin Complex.

5.10.7. DigInPin EAPD

Table 118. DigInPin EAPD Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 119. DigInPin EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd2	R	0x0	Reserved
[1]	Data	RW	0x0	EAPD value reflected on the EAPD pin. 0= power down external amp; 1= power up external amp if PwrState < 0x2. If PwrState >= 0x2, Pin47 is Hi-Z. An external pull-down is required if EAPD must be low when Pin Widget is powered down.
[0]	Rsvd1	R	0x0	Reserved

5.10.8. DigInPin Config

Table 120. DigInPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h

Table 120. DigInPin Config Command Verb Format

	Verb ID	Payload	Response
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 121. DigInPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x01	Physical location of the jack. Optical jack at mainboard rear.
[23.:20]	Device	RW	0xC	Default Device, indicating intended use of jack. C = SPDIF In
[19.:16]	Connection	RW	0x5	Connection Type. 5 = optical
[15.:12]	Color	RW	0xE	Color of physical jack. E = White
[11.:8]	Misc	RW	0x0	Misc[0] == Jack Detect override.
[7.:4]	Assoc	RW	0x3	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

5.11. DigOutPin Node (NID = 0x09)

5.11.1. DigOutPin WCap

Table 122. DigOutPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 123. DigOutPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.11.2. DigOutPin Cap

Table 124. DigOutPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 125. DigOutPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation N/A since pin complex is not input capable.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

5.11.3. DigOutPin ConnLen

Table 126. DigOutPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 127. DigOutPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x02	Number of NID entries in connection list.

5.11.4. DigOutPin ConnSel

Table 128. DigOutPin ConnSel Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 129. DigOutPin ConnSel Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	0x0	Reserved
[1.:0]	Index	RW	0x0	Connection select control index.

5.11.5. DigOutPin ConnLst

Table 130. DigOutPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 131. DigOutPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x0A	ADC Mux widget.
[7.:0]	Entry0	R	0x05	SPDIF Out converter widget.

5.11.6. DigOutPin Ctl

Table 132. DigOutPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 133. DigOutPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5.:0]	Rsvd1	R	0x0	Reserved

5.11.7. DigOutPin Config

Table 134. DigOutPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 135. DigOutPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x01	Physical location of the jack. Optical jack at mainboard rear.
[23.:20]	Device	RW	0x4	Default Device, indicating intended use of jack. 4 = SPDIF Out
[19.:16]	Connection	RW	0x5	Connection Type. 5 = optical
[15.:12]	Color	RW	0x1	Color of physical jack. 1 = Black
[11.:8]	Misc	RW	0x0	Misc[0] == Jack Detect override.

Table 135. DigOutPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7.:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x2	All Widgets in an association must have unique sequence number.

5.12. ADC0Mux Node (NID = 0x0A)

5.12.1. ADC0Mux VolRight

Table 136. ADC0Mux VolRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 137. ADC0Mux VolRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:4]	Rsvd1	R	0x0	Reserved
[3.:0]	Gain	RW	0x0	Amplifier gain step number

5.12.2. ADC0Mux VolLeft

Table 138. ADC0Mux VolLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 139. ADC0Mux VolLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:4]	Rsvd1	R	0x0	Reserved
[3.:0]	Gain	RW	0x0	Amplifier gain step number

5.12.3. ADC0Mux WCap

Table 140. ADC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 141. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x3	Widget type = Audio Selector
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 141. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.12.4. ADC0Mux OutAmpCap

Table 142. ADC0Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 143. ADC0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30.:23]	Rsvd3	R	0x0	Reserved
[22.:16]	StepSize	R	0x05	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14.:8]	NumSteps	R	0x0F	Number of steps in the gain range = 16 (0dB to +22.5dB)
[7]	Rsvd1	R	0x0	Reserved
[6.:0]	Offset	R	0x00	0dB-step is programmed with this offset

5.12.5. ADC0Mux ConnLen

Table 144. ADC0Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 145. ADC0Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.12.6. ADC0Mux ConnLst

Table 146. ADC0Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 147. ADC0Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0C	Input Port (UnivJack) Mux widget.

5.12.7. ADC0Mux LR

Table 148. ADC0Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 149. ADC0Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	0x0	Reserved

Table 149. ADC0Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	SwapEn	RW	0x0	1= swap left and right channels of this Widget.
[1.:0]	Rsvd1	R	0x0	Reserved

5.13. MasterVol Node (NID = 0x0B)

5.13.1. MasterVol Right

Table 150. MasterVol Right Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 151. MasterVol Right Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:5]	Rsvd1	R	0x0	Reserved
[4.:0]	Gain	RW	0x1F	Amplifier gain step number

5.13.2. MasterVol Left

Table 152. MasterVol Left Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 153. MasterVol Left Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:5]	Rsvd1	R	0x0	Reserved
[4.:0]	Gain	RW	0x1F	Amplifier gain step number

5.13.3. MasterVol WCap

Table 154. MasterVol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 155. MasterVol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x3	Widget type = Audio Selector
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 155. MasterVol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.13.4. MasterVol ConnLen

Table 156. MasterVol ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 157. MasterVol ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.13.5. MasterVol ConnLst

Table 158. MasterVol ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 159. MasterVol ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.

Table 159. MasterVol ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x07	DAC Mux widget.

5.14. InPortMux Node (NID = 0x0C)

5.14.1. InPortMux VolRight

Table 160. InPortMux VolRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 161. InPortMux VolRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2.:0]	Gain	RW	0x0	Amplifier gain step number

5.14.2. InPortMux VolLeft

Table 162. InPortMux VolLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 163. InPortMux VolLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2.:0]	Gain	RW	0x0	Amplifier gain step number

5.14.3. InPortMux WCap

Table 164. InPortMux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 165. InPortMux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x3	Widget type = Audio Selector
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.14.4. InPortMux ConnLen

Table 166. InPortMux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 167. InPortMux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x05	Number of NID entries in connection list.

5.14.5. InPortMux AmpCap

Table 168. InPortMux AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 169. InPortMux AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30.:23]	Rsvd3	R	0x0	Reserved
[22.:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14.:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6.:0]	Offset	R	0x00	0dB-step is programmed with this offset

5.14.6. InPortMux ConnSel

Table 170. InPortMux ConnSel Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 171. InPortMux ConnSel Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0x0	Reserved
[2.:0]	Index	RW	0x0	Connection select control index.

5.14.7. InPortMux ConnLst0

Table 172. InPortMux ConnLst0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 173. InPortMux ConnLst0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x0D	Port A pin widget.
[23.:16]	Entry2	R	0x0E	Port D pin widget.
[15.:8]	Entry1	R	0x0F	Port C pin widget.
[7.:0]	Entry0	R	0x10	Port B pin widget.

5.14.8. InPortMux ConnLst4

Table 174. InPortMux ConnLst4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table

Table 175. InPortMux ConnLst4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x12	CDin pin widget.

5.15. PortAPin Node (NID = 0x0D)

5.15.1. PortAPin WCap

Table 176. PortAPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 177. PortAPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping

Table 177. PortAPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.15.2. PortAPin Cap

Table 178. PortAPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 179. PortAPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

5.15.3. PortAPin ConnLen

Table 180. PortAPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 181. PortAPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.15.4. PortAPin ConnLst

Table 182. PortAPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 183. PortAPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0B	Master Volume widget.

5.15.5. PortAPin Ctl

Table 184. PortAPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 185. PortAPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1= enable the low impedance amplifier associated with the output
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1= (CODEC) input path of Pin Widget is enabled
[4.:0]	Rsvd1	R	0x0	Reserved

5.15.6. PortAPin UnsolResp

Table 186. PortAPin UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 187. PortAPin UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5.:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.15.7. PortAPin Sense

Table 188. PortAPin Sense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 189. PortAPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Present	R	0x0	1= something is plugged into jack associated with Pin Complex.
[30.:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered. Overlaps RightCh.
[0]	RightCh	W	0x0	Set 1= perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0= perform impedance sensing on left channel or tip of the connector

5.15.8. PortAPin Config

Table 190. PortAPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 191. PortAPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x02	Physical location of the jack. 02h = Mainboard, Front
[23.:20]	Device	RW	0x2	Default Device, indicating intended use of jack. 2 = HP Out
[19.:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15.:12]	Color	RW	0x4	Color of physical jack. 4 = Green
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7.:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x1	All Widgets in an association must have unique sequence number.

5.16. PortDPin Node (NID = 0x0E)

5.16.1. PortDPin WCap

Table 192. PortDPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 193. PortDPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 193. PortDPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.16.2. PortDPin Cap

Table 194. PortDPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 195. PortDPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved2
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.

Table 195. PortDPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

5.16.3. PortDPin ConnLen

Table 196. PortDPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 197. PortDPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.16.4. PortDPin ConnLst

Table 198. PortDPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 199. PortDPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0B	Master Volume widget.

5.16.5. PortDPin Ctl

Table 200. PortDPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 201. PortDPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1= enable the low impedance amplifier associated with the output
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1= (CODEC) input path of Pin Widget is enabled
[4.:0]	Rsvd1	R	0x0	Reserved

5.16.6. PortDPin UnsolResp

Table 202. PortDPin UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 203. PortDPin UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5.:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.16.7. PortDPin Sense

Table 204. PortDPin Sense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 205. PortDPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Present	R	0x0	1= something is plugged into jack associated with Pin Complex.
[30.:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered. Overlaps RightCh.
[0]	RightCh	W	0x0	Set 1= perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0= perform impedance sensing on left channel or tip of the connector

5.16.8. PortDPin Config

Table 206. PortDPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 207. PortDPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23.:20]	Device	RW	0x0	Default Device, indicating intended use of jack. 0 = Line Out
[19.:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15.:12]	Color	RW	0x4	Color of physical jack. 4 = Green
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7.:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

5.17. PortCPin Node (NID = 0x0F)

5.17.1. PortCPin WCap

Table 208. PortCPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 209. PortCPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.17.2. PortCPin Cap

Table 210. PortCPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 211. PortCPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved2
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

5.17.3. PortCPin ConnLen

Table 212. PortCPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 213. PortCPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.17.4. PortCPin ConnLst

Table 214. PortCPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 215. PortCPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0B	Master Volume widget.

5.17.5. PortCPin Ctl

Table 216. PortCPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 217. PortCPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1= (CODEC) input path of Pin Widget is enabled
[4.:0]	Rsvd1	R	0x0	Reserved

5.17.6. PortCPin UnsolResp

Table 218. PortCPin UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 219. PortCPin UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5.:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.17.7. PortCPin Sense

Table 220. PortCPin Sense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 221. PortCPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Present	R	0x0	1= something is plugged into jack associated with Pin Complex.
[30.:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered. Overlaps RightCh.

Table 221. PortCPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[0]	RightCh	W	0x0	Set 1= perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0= perform impedance sensing on left channel or tip of the connector

5.17.8. PortCPin Config

Table 222. PortCPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 223. PortCPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x01	Physical location of the jack. 03h = Mainboard, Rear
[23.:20]	Device	RW	0x8	Default Device, indicating intended use of jack. 8 = Line In
[19.:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15.:12]	Color	RW	0x3	Color of physical jack. 3 = Blue
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.

Table 223. PortCPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7.:4]	Assoc	RW	0x2	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x1	All Widgets in an association must have unique sequence number.

5.18. PortBPin Node (NID = 0x10)

5.18.1. PortBPin WCap

Table 224. PortBPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 225. PortBPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 225. PortBPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.18.2. PortBPin Cap

Table 226. PortBPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 227. PortBPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

5.18.3. PortBPin ConnLen

Table 228. PortBPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 229. PortBPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.18.4. PortBPin ConnLst

Table 230. PortBPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 231. PortBPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x0B	Master Volume widget.

5.18.5. PortBPin Ctl

Table 232. PortBPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 233. PortBPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1= (CODEC) input path of Pin Widget is enabled
[4.:3]	Rsvd1	R	0x0	Reserved
[2.:0]	VRefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

5.18.6. PortBPin UnsolResp

Table 234. PortBPin UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 235. PortBPin UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5.:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

5.18.7. PortBPin Sense

Table 236. PortBPin Sense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 237. PortBPin Sense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Present	R	0x0	1= something is plugged into jack associated with Pin Complex.
[30.:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered. Overlaps RightCh.
[0]	RightCh	W	0x0	Set 1= perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0= perform impedance sensing on left channel or tip of the connector

5.18.8. PortBPin Config

Table 238. PortBPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 239. PortBPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = Port Complex is connected to a jack
[29.:24]	Location	RW	0x02	Physical location of the jack. 02h = Mainboard, Front
[23.:20]	Device	RW	0xA	Default Device, indicating intended use of jack. A = Mic In
[19.:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15.:12]	Color	RW	0x9	Color of physical jack. 9 = Pink
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7.:4]	Assoc	RW	0x2	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

5.19. MonoOutPin Node (NID = 0x11)

5.19.1. MonoOutPin Vol

Table 240. MonoOutPin Vol Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 241. MonoOutPin Vol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:5]	Rsvd1	R	0x0	Reserved
[4.:0]	Gain	RW	0x1F	Mono (left) amplifier gain step number

5.19.2. MonoOutPin WCap

Table 242. MonoOutPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 243. MonoOutPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x0	Mono widget

5.19.3. MonoOutPin Cap

Table 244. MonoOutPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 245. MonoOutPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation N/A since pin complex is not input capable.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

5.19.4. MonoOutPin ConnLen

Table 246. MonoOutPin ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 247. MonoOutPin ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.19.5. MonoOutPin ConnLst

Table 248. MonoOutPin ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 249. MonoOutPin ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x13	MonoOut Mix widget.

5.19.6. MonoOutPin Ctl

Table 250. MonoOutPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 251. MonoOutPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1= (CODEC) output path of Pin Widget is enabled
[5.:0]	Rsvd1	R	0x0	Reserved

5.19.7. MonoOutPin Config

Table 252. MonoOutPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 253. MonoOutPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29.:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23.:20]	Device	RW	0x1	Default Device, indicating intended use of jack. 1 = Speaker
[19.:16]	Connection	RW	0x7	Connection Type. 7 = Other Analog
[15.:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.

Table 253. MonoOutPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7.:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x3	All Widgets in an association must have unique sequence number.

5.20. CDPin Node (NID = 0x12)

5.20.1. CDPin WCap

Table 254. CDPin WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 255. CDPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x4	Widget type = Pin Complex
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 255. CDPin WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

5.20.2. CDPin Cap

Table 256. CDPin Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 257. CDPin Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15.:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

5.20.3. CDPin Ctl

Table 258. CDPin Ctl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 259. CDPin Ctl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x1	1= (CODEC) input path of Pin Widget is enabled (un-muted)
[4.:0]	Rsvd1	R	0x0	Reserved

5.20.4. CDPin Config

Table 260. CDPin Config Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 261. CDPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	Port	RW	0x2	External Port Connectivity of the Pin Complex. 2 = fixed function device
[29.:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23.:20]	Device	RW	0x3	Default Device, indicating intended use of jack. 3 = CD

Table 261. CDPin Config Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Connection	RW	0x3	Connection Type. 3 = ATAPI internal
[15.:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11.:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7.:4]	Assoc	RW	0x2	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3.:0]	Sequence	RW	0x2	All Widgets in an association must have unique sequence number.

5.21. MonoOutMix Node (NID = 0x13)

5.21.1. MonoOutMix WCap

Table 262. MonoOutMix WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 263. MonoOutMix WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	0x0	Reserved
[23.:20]	Type	R	0x2	Widget type = Audio Mixer
[19.:16]	Delay	R	0x0	Number of sample delays through widget
[15.:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	Swapping of left and right channels not supported
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response

Table 263. MonoOutMix WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x0	Mono widget

5.21.2. MonoOutMix ConnLen

Table 264. MonoOutMix ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 265. MonoOutMix ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6.:0]	N	R	0x01	Number of NID entries in connection list.

5.21.3. MonoOutMix ConnLst

Table 266. MonoOutMix ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 267. MonoOutMix ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Entry3	R	0x00	Unused list entry.
[23.:16]	Entry2	R	0x00	Unused list entry.
[15.:8]	Entry1	R	0x00	Unused list entry.
[7.:0]	Entry0	R	0x07	DAC Mux widget.

5.22. PCBeep Node (NID = 0x14)

5.22.1. PCBeep Vol

Table 268. PCBeep Vol Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 269. PCBeep Vol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1= mute is active
[6.:2]	Rsvd1	R	0x0	Reserved
[1.:0]	Gain	RW	0x3	Mono (left) amplifier gain step number

5.22.2. PCBeep WCap

Table 270. PCBeep WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 271. PCBeep WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd3	R	0x0	Reserved
[23.:20]	Type	R	0x7	Widget type = Beep Generator
[19.:4]	Rsvd2	R	0x0	Reserved
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	N/A
[0]	Stereo	R	0x0	Mono widget

5.22.3. PCBeep OutAmpCap

Table 272. PCBeep OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 273. PCBeep OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30.:23]	Rsvd3	R	0x0	Reserved
[22.:16]	StepSize	R	0x17	Size of each step in the gain range = 6 dB
[15]	Rsvd2	R	0x0	Reserved
[14.:8]	NumSteps	R	0x03	Number of steps in the gain range = 4 (-18dB to 0dB)
[7]	Rsvd1	R	0x0	Reserved
[6.:0]	Offset	R	0x03	0dB-step is programmed with this offset

5.22.4. PCBeep Gen

Table 274. PCBeep Gen Command Verb Format

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table
Set1	70A	See bits [7:0] of bitfield table	0000_0000h

Table 275. PCBeep Gen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	0x0	Reserved
[7.:0]	Divider	RW	0x00	Enable internal PC-Beep generation. Divider = 00h disables internal PC Beep generation and enables normal operation of the CODEC. Divider not equal to 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The Azalia spec states that the beep tone frequency = (48 KHz Azalia SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 KHz (logarithmic scale). Instead, this part generates tones with frequency = 48000 * (257 - Divider) / 1024, yielding a linear range from 12 KHz to 93.75 Hz in steps of 46.875 Hz. If JackSenseVSR[Rate2x], then the beep tones generated have frequency = 48000 * (513 - Divider) / 1024, yielding a range of 24 KHz to 12093.75 Hz in steps of 46.875 Hz.

6. ORDERING INFORMATION

6.1. STAC9200 Family Options and Part Order Numbers

The +4V Analog voltage is supported by the +5 V version of the STAC9200 or STAC9200D.

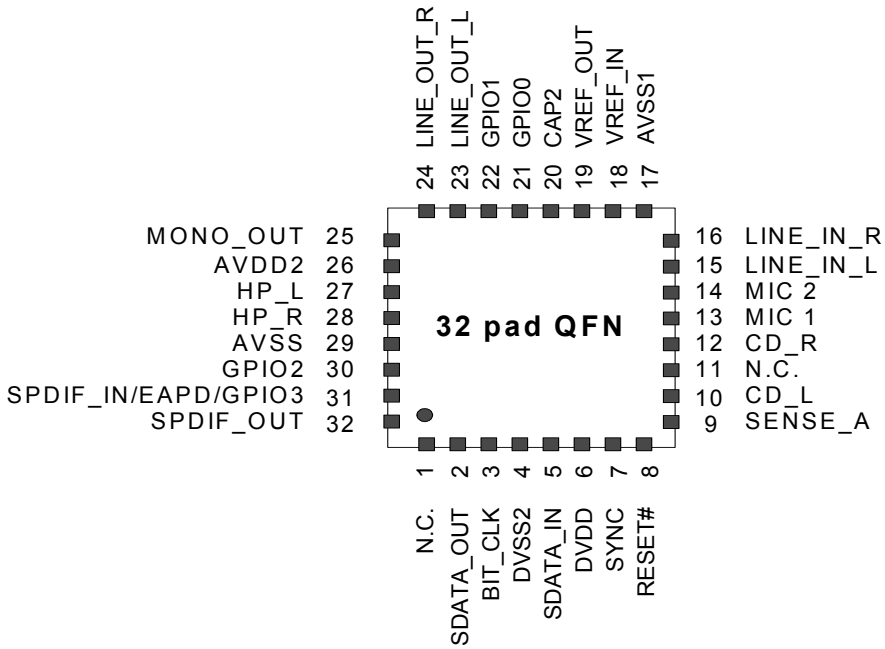
*Dolby requires the 5 V version of this part except for Dolby Digital Live (DDL).

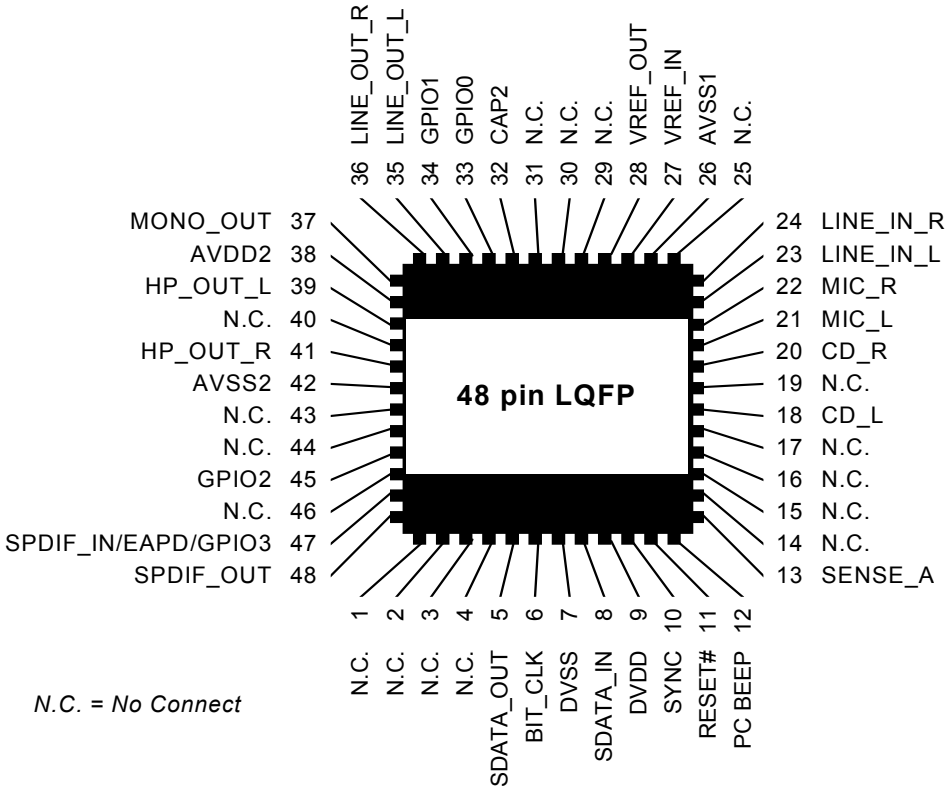
Part Order Number	Voltage	DAC SNR	Dolby*	Pkg Pins
STAC9200D5TAEyy	5 V	100dB	Yes	48 LQFP
STAC9200D5NAEyy	5 V	100dB	Yes	32 QFN
STAC9200X5TAEyy	5 V	100dB	No	48 LQFP
STAC9200X5NAEyy	5 V	100dB	No	32 QFN
STAC9200D3TAEyy	3.3 V	100dB	Yes (DDL)	48 LQFP
STAC9200D3NAEyy	3.3 V	100dB	Yes (DDL)	32 QFN
STAC9200X3TAEyy	3.3 V	100dB	No	48 LQFP
STAC9200X3NAEyy	3.3 V	100dB	No	32 QFN

NOTE: When ordering these parts the “yy” will be replaced with the CODEC revision. Add an “R” to the end of any of these part numbers for delivery on Tape and Reel. The minimum order quantity for Tape and Reel is 2,000 units for both package options.

7. PIN INFORMATION

7.1. Pin Out





N.C. = No Connect

7.2. Pin Table for 48-pin LQFP and 32-pad QFN Packages

Pin Name	Pin Function	I/O	Internal Pull-up/ Pull-down	LQFP 48-pin Location	QFN 32-pin Location
NC	No Connect	-	-	1	-
NC	No Connect	-	-	2	1
NC	No Connect	-	-	3	-
NC	No Connect	-	-	4	-
SDATA_OUT	High Definition Audio “Azalia” Serial Data output (inbound stream)	I/O (Digital)	None	5	2
BIT_CLK	High Definition Audio “Azalia” Bit Clock	I(Digital)	Pull-down	6	3
DVSS	Digital Ground	I(Digital)	None	7	4
SDATA_IN	High Definition Audio “Azalia” Serial Data input (outbound stream)	O(Digital)	Pull-down	8	5
DVDD_CORE3	Digital Vdd = 3.3 V	I(Digital)	None	9	6
SYNC	High Definition Audio “Azalia”Frame Sync	I(Digital)	Pull-down	10	7
RESET#	High Definition Audio “Azalia” Reset	I(Digital)	Pull-down	11	8
PC Beep	PC Beep	I(Analog)	-	12	-
Sense A	Jack insertion detection Ports A, B, C, D	I(Analog)	None	13	9
NC	No Connect	-	-	14	-
NC	No Connect	-	-	15	-
NC	No Connect	-	-	16	-
NC	No Connect	-	-	17	-
CD-L	CD Audio Left Channel	I(Analog)	None	18	10
NC	No Connect	-	-	19	11
CD-R	CD Audio Right Channel	I(Analog)	None	20	12
Port B-L	Analog I/O	I/O(Analog)	None	21	13
Port B-R	Analog I/O	I/O(Analog)	None	22	14
Port C-L	Analog I/O	I/O(Analog)	None	23	15
Port C-R	Analog I/O	I/O(Analog)	None	24	16
NC	No Connect	-	-	25	-
AVSS1	Analog Ground	I(Analog)	None	26	17
VREF IN	Reference Voltage In drive	I(Analog)	None	27	18
VREFOUT	Reference Voltage Out drive	O(Analog)	None	28	19
NC	No Connect	-	-	29	-
NC	No Connect	-	-	30	-
NC	No Connect	-	-	31	-
CAP2	ADC reference Cap	O(Analog)	None	32	20

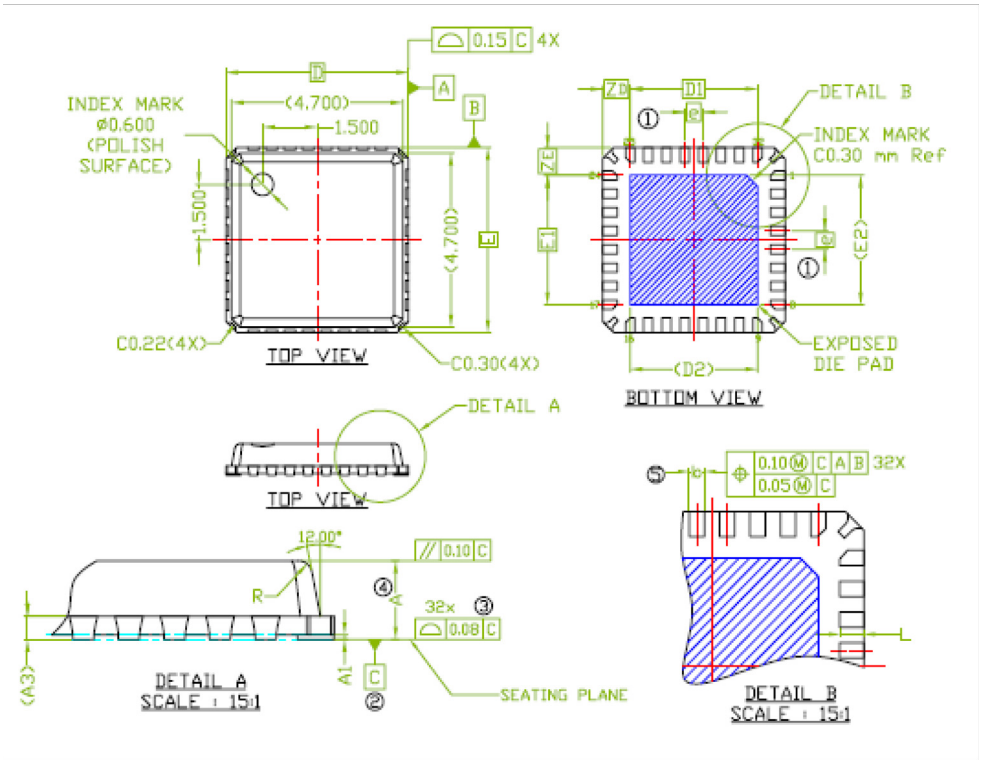
Pin Name	Pin Function	I/O	Internal Pull-up/ Pull-down	LQFP 48-pin Location	QFN 32-pin Location
GPIO0*	General Purpose I/O/Mic Bias	I/O(Analog)	Pull-up 50 KΩ	33	21
GPIO1*	General Purpose I/O/Mic Bias	I/O(Analog)	Pull-up 50 KΩ	34	22
Port D-L	Analog I/O with HP support	I/O(Analog)	None	35	23
Port D-R	Analog I/O with HP support	I/O(Analog)	None	36	24
MONO	Mono Out from DAC	O(Analog)	None	37	25
AVDD2	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	38	26
Port A-L	Analog I/O with HP support	I/O(Analog)	None	39	27
NC	No Connect	-	-	40	-
Port A-R	Analog I/O with HP support	I/O(Analog)	None	41	28
AVSS2	Analog Ground	I(Analog)	None	42	29
NC	No Connect	-	-	43	-
NC	No Connect	-	-	44	-
GPIO2*	General Purpose I/O /Mic Bias	I/O(Digital)	Pull-up 50 KΩ	45	30
NC	No Connect	-	-	46	-
S/PDIFIN/EAPD/ GPIO3*	SPDIF Input, External Amplifier Power Down, General Purpose I/O /Mic Bias	I/O(Digital)	None	47	31
S/PDIF-OUT	SPDIF digital output (50 KΩ internal pull-down)	O(Digital)	50 KΩ internal pull-down	48	32

* GPIO Pins can also be used for Microphone Bias.

8. PACKAGE DRAWINGS

8.1. 32-pin QFN

Figure 3. 32-Pad QFN Package Outline and Package Dimensions



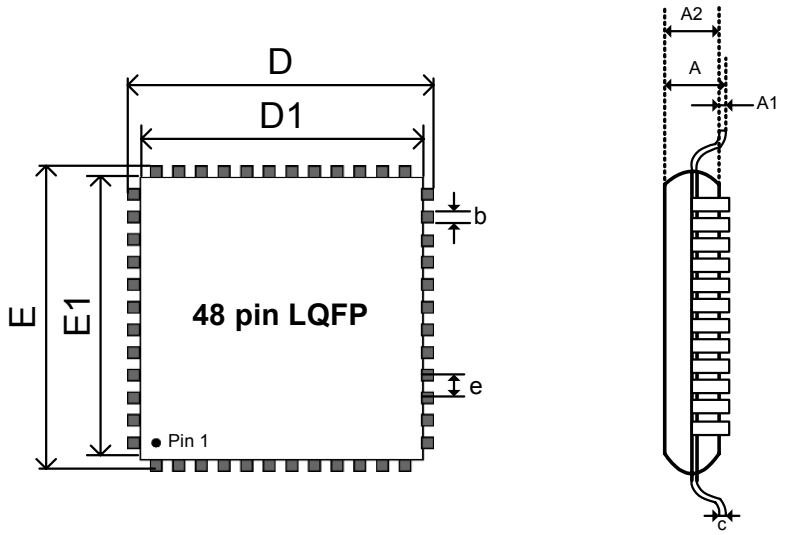
Key	QFN Dimensions in mm		
	Min	Nom	Max
A	-	0.80	0.90
A1	0	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
D1		3.50 BSC	
E		5.00 BSC	
E1		3.50 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
D2	3.20	3.50	3.60
E2	3.20	3.50	3.60
ZD		0.75 BSC	
ZE		0.75 BSC	
R		0.20~0.25	

Note:
① 'e' REPRESENTS THE BASIC TERMINAL PITCH.
SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
② DATUM 'C' IS THE MOUNTING SURFACE, WITH WHICH THE PACKAGE IS IN CONTACT.
③ SPECIFIES THE VERTICAL SHIFT OF THE FLAT PART OF EACH TERMINAL FROM THE MOUNTING SURFACE.
④ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
⑤ DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURE IN THE RADIUS AREA.
6 PACKAGE DIMENSIONS CONFORM TO JEDEC MO-220 REV.J, VARIATIONS VHHD-5, EXCEPT FOR D2 & E2.

NOTE: For more information on the QFN please see IDT QFN Application Note.

8.2. 48-Pin LQFP

Figure 4. 48-Pin LQFP Package Outline and Package Dimensions



Key	LQFP Dimensions in mm		
	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
e		0.50	
C	0.09	-	0.20
b	0.17	0.22	0.27

9. SOLDER REFLOW PROFILE

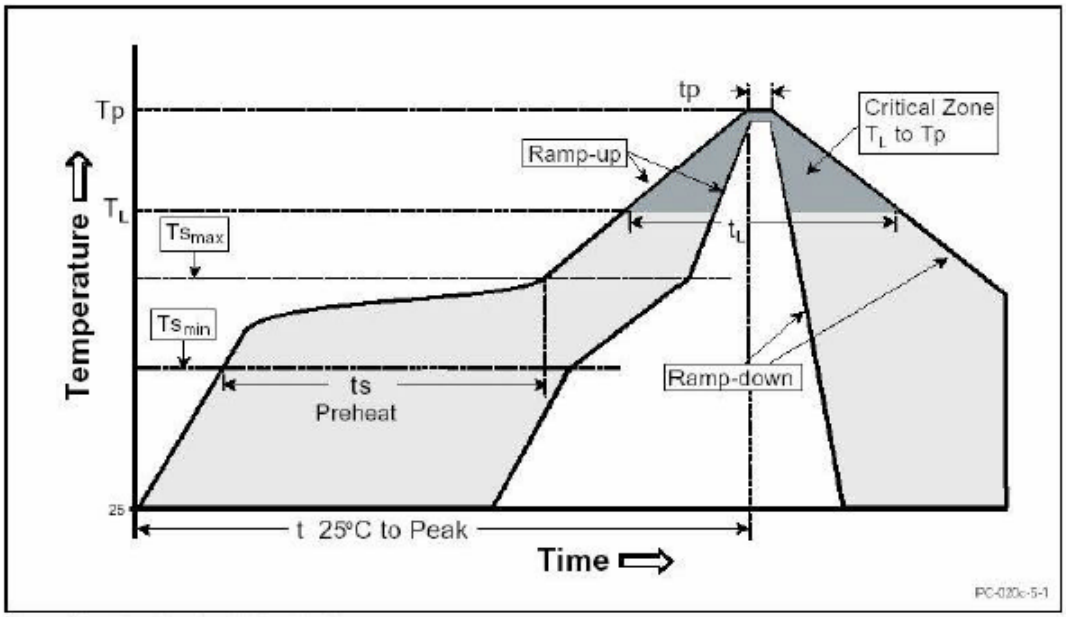
9.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature	Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)	3 °C / second max
Preheat — Temperature Min (Ts_{min})	150 °C
Preheat — Temperature Max (Ts_{max})	200 °C
Preheat — Time (ts_{min} - ts_{max})	60 - 180 seconds
Time maintained above — Temperature (T_L)	217 °C
Time maintained above — Time (t_L)	60 - 150 seconds
Peak / Classification Temperature (Tp)	See "Package Classification Reflow Temperatures" on page 123.
Time within 5 °C of actual Peak Temperature (tp)	20 - 40 seconds
Ramp-Down rate	6 °C / second max
Time 25 °C to Peak Temperature	8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.	

Figure 5. Solder Reflow Profile



9.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
LQFP 48-pin	3	260 ^{o}C*
QFN 32-pad	3	260 ^{o}C*

10. REVISION HISTORY

Revision	Date	Description of Change
		For STAC9200/9200D Revision CA1
0.5	September 2004	Initial release.
0.6	November 2004	Updated the Connection Diagrams
0.7	November 2004	Added Widget Tables
0.8	December 2004	Added 5V Analog Performance Characteristics Table
		FOR STAC9200/9200D Revision CB1
0.9	January 2005	Updated LQFP Package Drawing. Updated QFN Drawing. Updated Reflow profile information. Updated Widget Information- This is for the B1 revision of STAC9200/9200D.
0.91	February 2005	Added Ordering Information. Updated Reflow profile.
0.92	April 2005	Added Dolby part numbers, description and differences section, Added 5V Analog Performance Numbers with note about min/max, Added Power Consumption, Added 4V Analog supply information, Added comment for allowing GPIO to be used as microphone bias
0.93	July 2005	Added in 3.3V Analog performance numbers. Added in 4V performance numbers. Replaced reflow profile- this was only for visual purposes. No changes were made to the Data.
1.0		Updated logo
1.1		Removed “Preliminary”. Added Section 7.4 “Audio Jack Presence Detect.”
1.2	June 2006	Updated 32-pad Package Drawing
1.3	10 October 2006	Released in IDT format.
1.4	December 2006	Updated AIDD Max spec
1.5	April 2007	Corrected 32QFN diagram, removed typical connection diagrams as the reference design should be used instead. Updated table of contents, list of tables and figures.

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