PRODUCT SPECIFICATION

Part Number

PT322435B-TLMWD-EC35

CUSTOMER	
CUSTOMER PART NUMBER	
DESCRIPTION	
APPROVED BY	
DATE	

1. Table of Contents

2. Record of Revisions

Rev.	Comments	Page	Date
1	Preliminary Specification was first issued	All	3/22'13
2	Modify 6 General Specifications	5	5/27'13
2	Modify 8.1 TFT-LCD Module	8	5/27'13
2	Modify 13 Optical Characteristics	29	5/27'13
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3. Module Numbering System

P T ____ __ __ - _ __ _ _ - _ _ _ _ __ _

1. 2. 3. 4. 5. 6. 7. 8. 9 10. 11. 12. 13. 14.

1. P-TEC TFT

2. LENGTH x WIDTH PIXELS
If third character is a zero, it is removed to shorten part number. Example: 240 x 320 = PT3224

3. DIAGONAL DIMENSIONS
Example: 3.5” display = 35 in part number

4. PRODUCT VERSION
Series assigned by P-tec

5. LCD MODE
T: TN
I: IPS
V: VA

6. POLARIZER
LM: Transmissive
LF: Transflective

7. BACKLIGHT COLOR
No Backlight: Left Blank
W: White
B: Blue/Green
S: Yellow/Green

8. VIEWING DIRECTION
D: 6 o’clock
U: 12 o’clock
F: Full Viewing Angle

9. A ~ Z CODE
Assigned by P-tec

11. TEMPERATURE RANGE
Normal: Left Blank
Wide: X

12. LUMINANCE
Blank: Normal (<300 nit)
M: Middle (>/= 300 nit)
H: High (> 600 nit)

13. TOUCH PANEL OPTION
No TP: Left Blank
C: Capacitive TP
R: Resistive TP

14. SPECIAL CHARACTERS
Customer special requirements

4. Application

This specification is applied to the 3.5 inch QVGA supported TFT-LCD module With projected capacitive touch (PCT), and can display 262k colors. The module is designed for PMP, GPS, DMB, other electronic products which require flat panel display of digital signal interface, and used as the input devices for general electric appliances via human's finger.

5. Features

- QVGA (320×240 pixels) resolution.
- System Interface
  8/ 9/ 16/ 18-bit 6800-series / 8080-series Parallel Interface
  Serial Peripheral Interface (SPI)
-Moving picture display interface
  18-/6-bit RGB interface (DEN, DOTCLK, HSYNC, VSYNC, DB[17:0])
  VSYNC interface (system interface + VSYNC)
  WSYNC interface (system interface + WSYNC)
- Line inversion mode with stripe type.
- On-chip voltage generator
- Projected Capacitive Touch
  - I^2C Interface
  - Multi Touch (Ten points)

6. General Specifications

Item	Specifications	Unit
Screen Size	3.5 (Diagonal)	inch
Display Format	320RGB(H)×240(V)	dot
Active Area	70.08(H)×52.56(V)	mm
Dot Pitch	0.073(H)×0.219(V)	mm
Pixel Configuration	RGB Vertical Stripe	-
Display Mode	TN Type Transmissive Mode Normally White	-
Surface Treatment	Clear(7H)	-
Viewing Direction	6 O'clock (The Gray Inversion will appear at this direction)	-
Outline Dimension	76.84(W)×63.84(H)×4.85(D)	mm
DC to DC circuit	Build-in	-
Weight	48.4	g
RoHS Compliance	P-tec certifies this product to be in compliance with European Union Directive 2011/65/EU on the restriction of certain hazardous substances in electrical and electronic equipment.	-

7. Absolute Maximum Ratings

7.1 Absolute Ratings of Environment

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-30	+80	°C	(1)(2)
Operating Ambient Temperature	T_{OP}	-20	+70	°C	(1)(2)

Note1: Background color changes slightly depending on ambient temperature.
This phenomenon is reversible.

Note2: Please refer to item of RELIABILITY.

7.2 Electrical Absolute Ratings

7.2.1 TFT-LCD Module

(Ta=25±2°C, GND=V_{SS}=0V)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Digital Power Supply Voltage	VDDIO	-0.3	4.0	V	-
Input Voltage	VCI	V_{SS}-0.3	5.0	V	-

7.2.2 Backlight Unit

(Ta=25±2°C)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Forward current	If	-	(30)	mA	(1)
Reverse voltage	Vr	-	(30)	V	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.

8. Electrical Characteristics

8.1 TFT-LCD Module

(Ta=25±2°C)

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Digital Power Supply Voltage	VDDIO	1.4	3.3	3.6	V	-
Booster Reference Supply Voltage Range	VCI	2.5 or VDDIO whichever is higher	3.3	3.6	V	-
Input High Threshold Voltage	V_{IH}	$0.8V_{DDIO}$	-	V_{DDIO}	V	-
Input Low Threshold Voltage	V_{IL}	0	-	$0.2V_{DDIO}$	V	-

(GND=V_{SS}=0V)

Parameter	SYMBOL	Condition	Min	Typ	Max	Unit	Remarks
Digital Current	IVDDIO	VDDIO = 3.3V	-	150	300	uA	(1) (2)
Booster Current	IVCI	VCI = 3.3V	-	6.1	8.54	mA	(1) (2)
Total Power Consumption	PCVDDIO	VDDIO = 3.3V	-	495	990	uW	(1) (2)
Total Power Consumption	PCVCI	VCI = 3.3V	-	20.1	28.1	mW	(1) (2)

Note (1) The specified power consumption is under the conditions at VDDIO =3.3V, VCI =3.3V,F_V=60Hz, whereas a power dissipation check pattern below is displayed.

Note (2) 8080-series 16-bit Parallel Interface

Black Pattern / 0 Gray

Active Area

8.2 Backlight Unit

(Ta=25±2°C)

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Voltage	VL	-	(18.6)	20.4	V	(1)(3)
LED Current	IL	-	(20)	-	mA	(1)(3)
Power Consumption	P_{BL}	-	(372)	-	mW	(1)(3)
LED Life Time(25°C)	-	50000	-	-	hr	(2)

Note (1) The driving design of backlight unit is dependent on serial consideration of six LEDs.

Note (2) LED life time is defined as under 25±2°C, when the average brighten decrease to 50% of original brightness

Note (3) BLU Unit Applicable Warrant Period: The period is within Twenty-four months since the date of shipping out under normal using at 25±2°C.

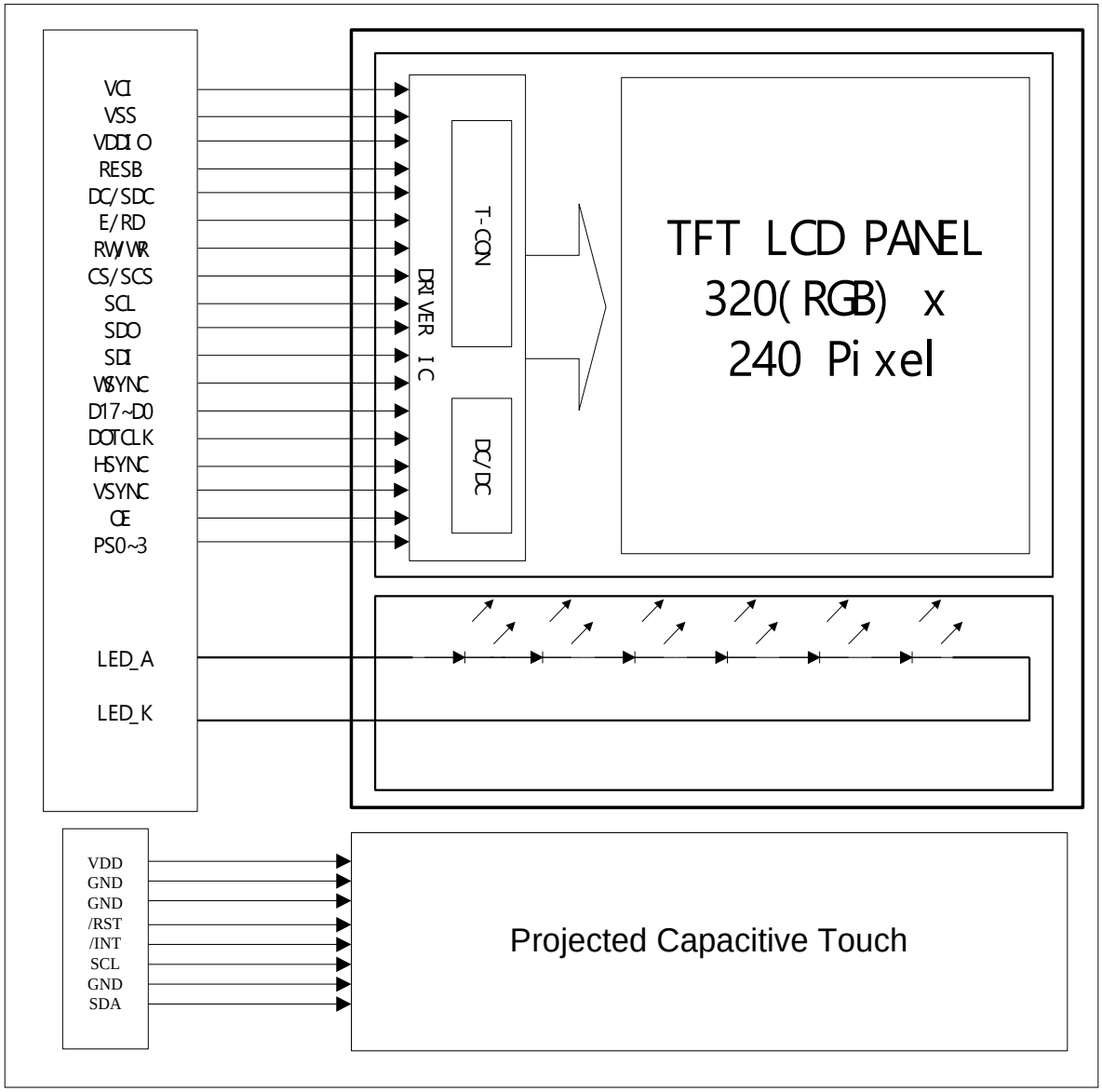
8.3 Projected Capacitive Touch

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.0	3.3	3.6	V	-
Power Supply Current	IDD	-	9.4	13.2	mA	(1)
Input High Threshold Voltage	V_{IH}	0.7VDD	-	VDD	V	-
Input Low Threshold Voltage	V_{IL}	-0.3	-	0.3VDD	V	-
Output High Threshold Voltage	V_{OH}	0.7VDD	-	-	V	-
Output Low Threshold Voltage	V_{OL}	-	-	0.3VDD	V	-
Power Consumption	P_L	-	31.02	43.56	mW	@3.3V
Interface		I^2C				-
Function		Multi Touch				-

Note (1) This test condition is touched with 10 points.

9. Block Diagram

TFT-LCD Module with Backlight Unit



10. Input / Output Terminals Pin Assignment

10.1 TFT-LCD Module

Pin No.	Symbol	I/O	Description
1	VCI	P	Booster input voltage pin.
2	VCI	P	Booster input voltage pin.
3	VSS	P	Ground
4	VDDIO	P	Voltage input pin for logic I/O
5	VSS	P	Ground
6	RESB	I	System reset pin. - An active low pulse at this pin will reset the IC, Connect to VDDIO in normal operation
7	DC/SDC	I	Data or command DC : Parallel Interface SDC : Serial Interface
8	E/RD	I	6800-system : E (enable signal) 8080-system : RD (read strobe signal) Serial mode : Not used and should be connected to VDDIO or Vss
9	RW/WR	I	6800-system : RW (indicates read cycle when High, write cycle when Low) 8080-system : WR (write strobe signal)
10	CS/SCS	I	CS: Chip Selcet pt pin for 6800/8080 Parallel Interface SCS: Chip Selcet pt pin for Serial Mode Interface
11	SCL	I	Serial clock input
12	SDO	O	Data output pin in serial interface
13	SDI	I	Data input pin in serial interface
14	WSYNC	O	Ram Write Synchronization output
15	D17	I/O	For parallel mode, 8/9/16/18 bit interface. Please refer to Tablet 1 Unused pins should connect to VSS.
16	D16	I/O	
17	D15	I/O	
18	D14	I/O	
19	D13	I/O	
20	D12	I/O	
21	D11	I/O	
22	D10	I/O	

Pin No.	Symbol	I/O	Description
23	D9	I/O	
24	D8	I/O	
25	D7	I/O	
26	D6	I/O	
27	D5	I/O	
28	D4	I/O	
29	D3	I/O	
30	D2	I/O	
31	D1	I/O	
32	D0	I/O	
33	VSS	P	Ground
34	DOTCLK	I	Data Colck
35	HSYNC	I	Horizontal synchronous signal
36	VSYNC	I	Vertical synchronous signal
37	OE	I	Data Enable Input
38	VSS	P	Ground
39	PS0	I	Please refer to Tablet 1
40	PS1	I	
41	PS2	I	
42	PS3	I	
43	VSS	P	Ground
44	NC	-	No connection
45	NC	-	No connection
46	NC	-	No connection
47	NC	-	No connection
48	VSS	P	Ground
49	LED_K	P	LED_cathode
50	LED_A	P	LED_anode

Tablet 1

PS3	PS2	PS1	PS0	Interface Mode
0	0	0	0	16-bit 6800 parallel interface
0	0	0	1	8-bit 6800 parallel interface
0	0	1	0	16-bit 8080 parallel interface
0	0	1	1	8-bit 8080 parallel interface
0	1	0	0	9-bit generic D[17:9] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI
0	1	1	1	6-bit generic D[17:12] (262k colour) + 3-wire SPI
1	0	0	0	18-bits 6800 parallel interface
1	0	0	1	9-bits 6800 parallel interface
1	0	1	0	18-bit 8080 parallel interface
1	0	1	1	9-bit 8080 parallel interface
1	1	1	0	3-wire SPI
1	1	1	1	4-wire SPI

10.2 Projected Capacitive Touch

Connector：CVILUX CF25081D0R0-05

Pin No.	Symbol	I/O	Description
1	VDD	I	+3.3V power supply.
2	GND	I	System ground.
3	GND	I	System ground.
4	/RST	I	External reset signal, active low.
5	/INT	O	Interrupt signal, active low, asserted to request Host start a new transcation.
6	SCL	I	I^2C clock signal.
7	GND	I	System ground.
8	SDA	I/O	I^2C data signal.

10.3 Color Data Input Assignment

The brightness of each primary color(red, green and blue) is based on the 6 bit gray scale data input for the color. The higher the binary input, the brighter the color. The table provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		D05	D04	D03	D02	D01	D00	D15	D14	D13	D12	D11	D10	D25	D24	D23	D22	D21	D20
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of RED	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

11. Interface Timing

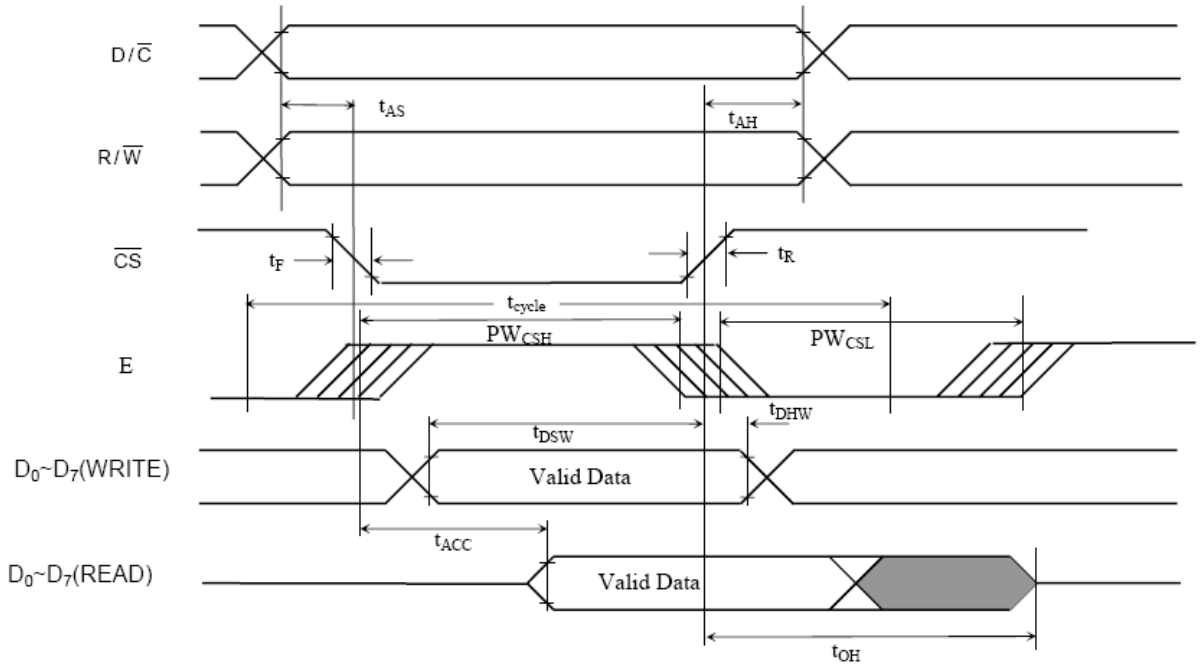
11.1 Input Signal Characteristics

Parallel 6800 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 11-1: Parallel 6800-series Interface Timing Characteristics

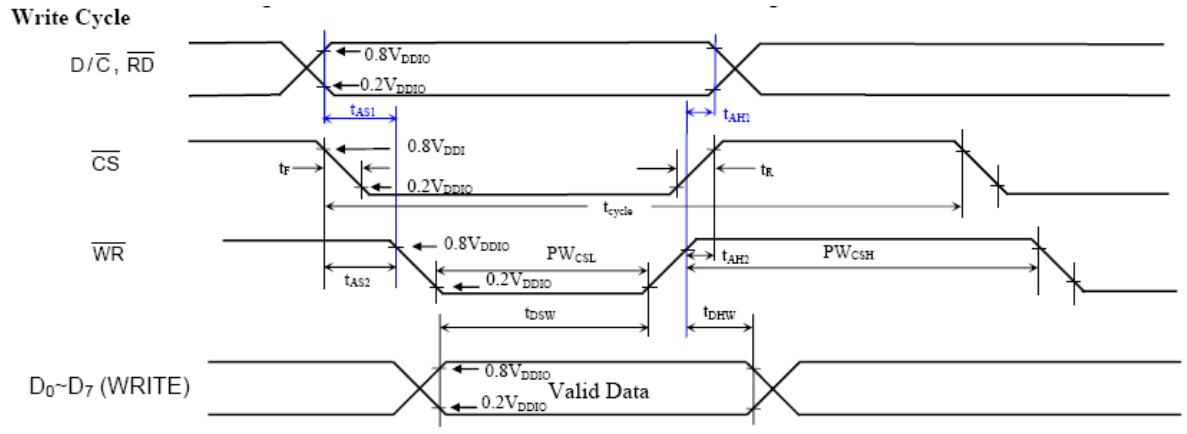


Parallel 8080 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

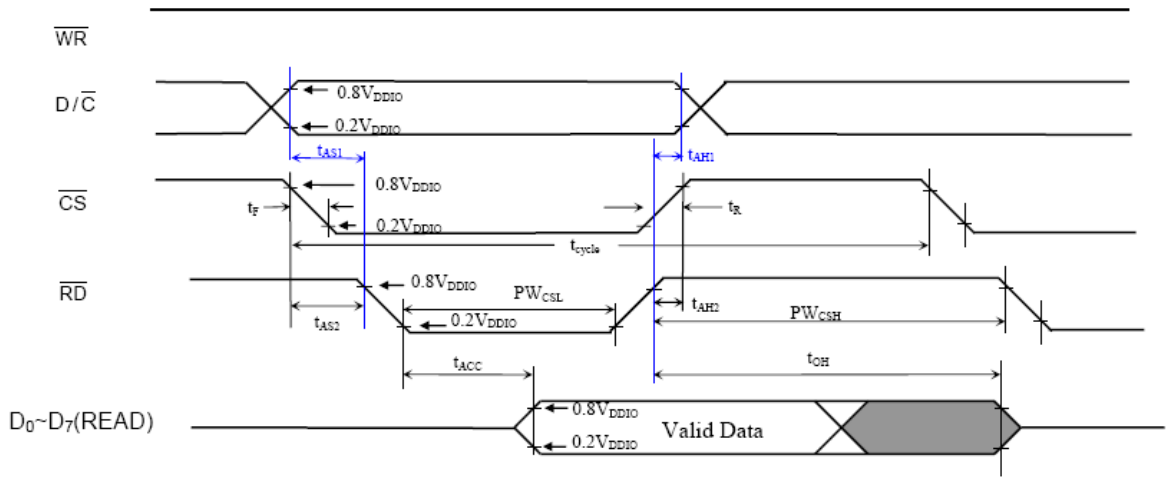
Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 11-2: Parallel 8080-series Interface Timing Characteristics



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

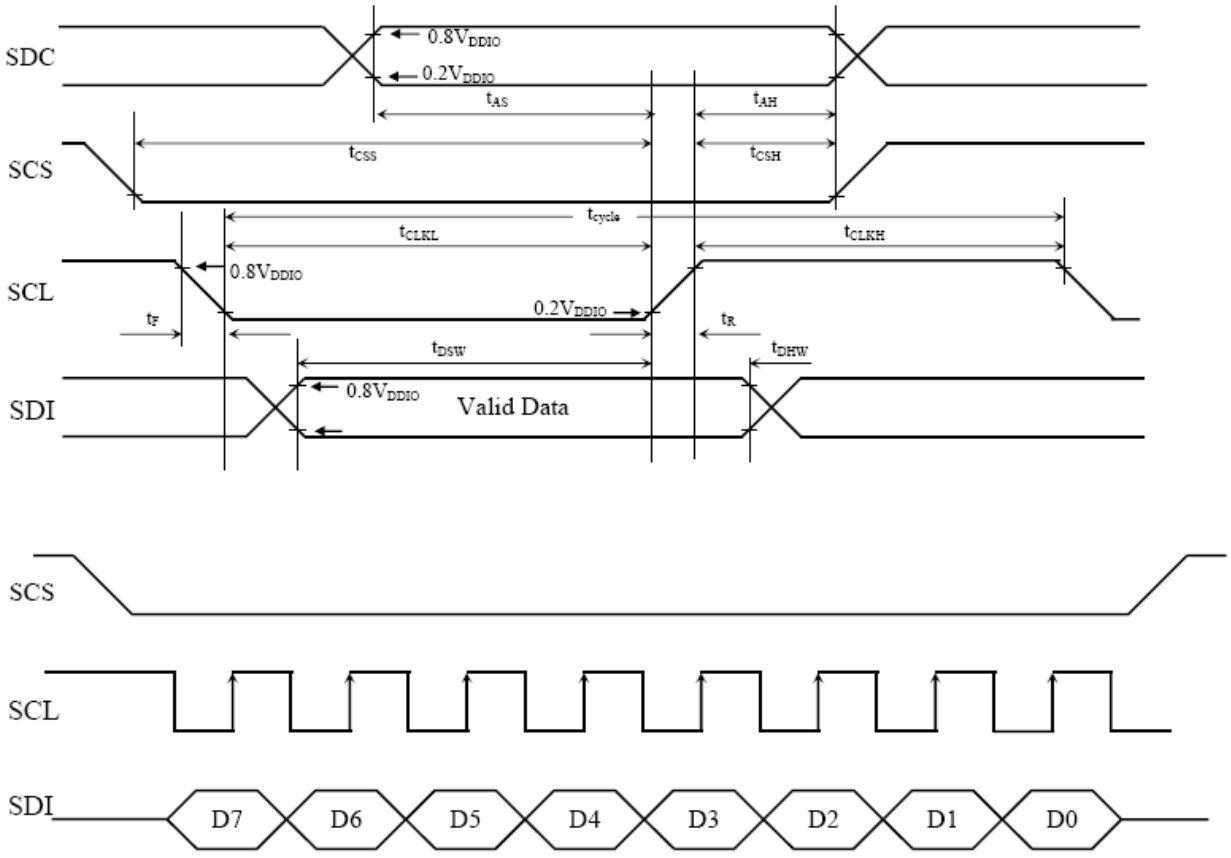
Read Cycle



Serial Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Figure 11-3: 4 wire Serial Timing Characteristics

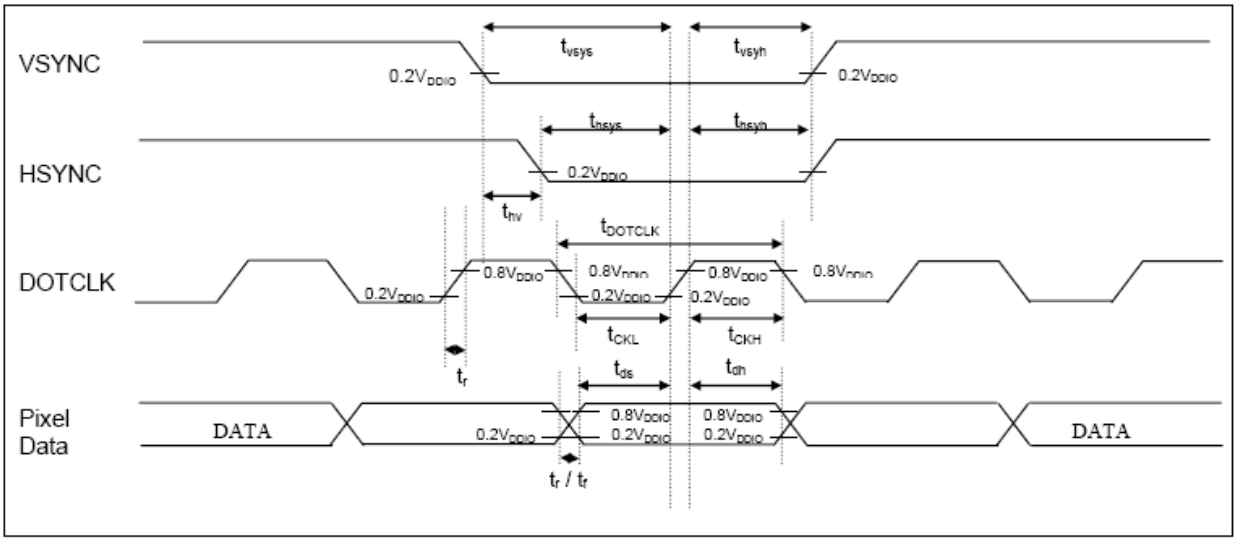


RGB Timing Characteristics

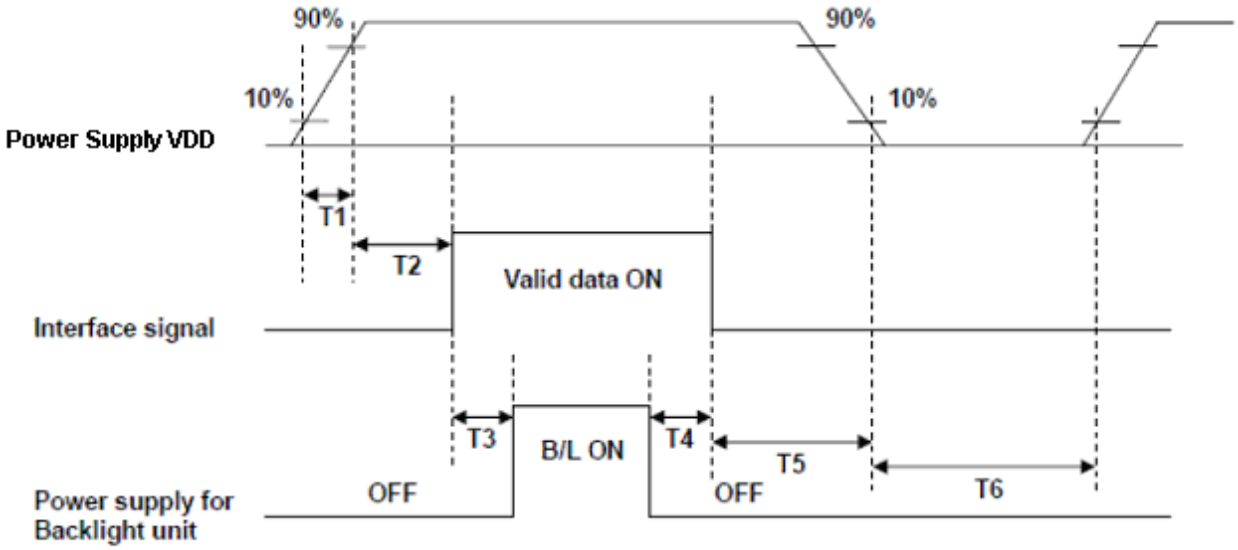
Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119M1. The driver will not operate in absence of the clocking signal.

Figure 11-4: RGB Timing Characteristics



11.2 Power On / Off Sequence

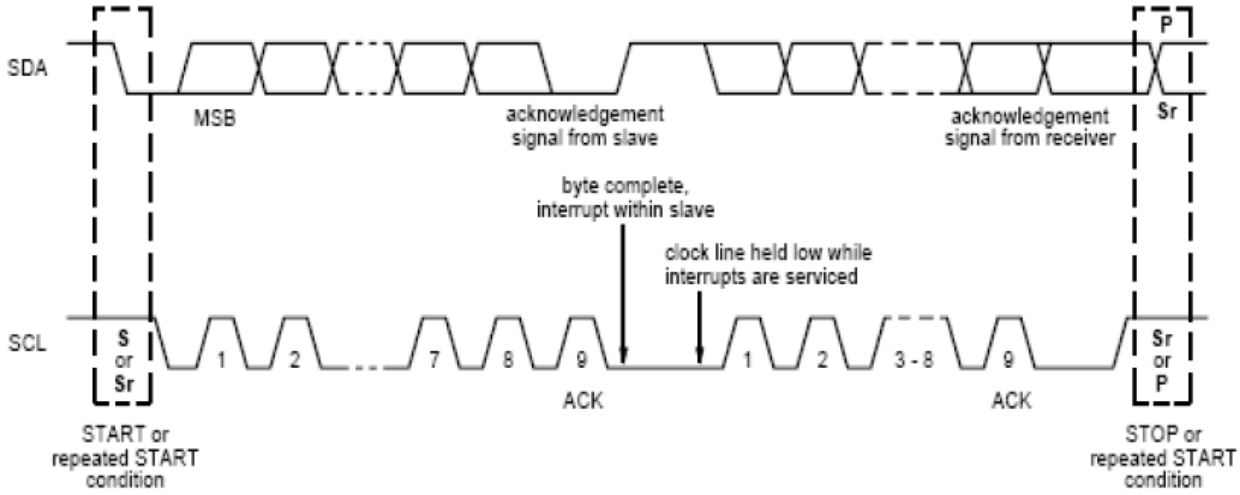


POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ	Max.	
T1	0.5	-	10	ms
T2	5	-	-	ns
T3	200	-	-	ms
T4	200	-	-	ms
T5	2	-	-	ms
T6	1000	-	-	ms

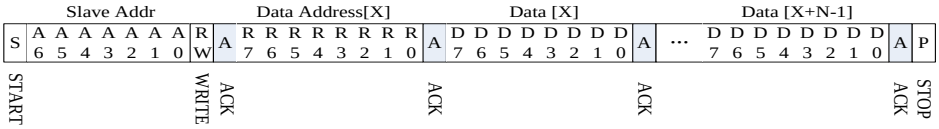
11.3 Timing Requirement of Projected Capacitive Touch

11.3.1 I2C Data Transfer Format

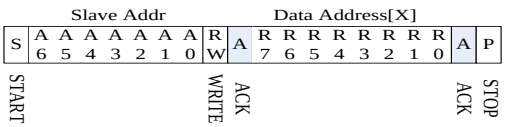


Mnemonics	Description
S	I²C Start or I²C Restart
A[6:0]	Slave Address = 0x70
W	1'b0: Write
R	1'b1: Read
C	ACK
P	STOP: the indicate the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

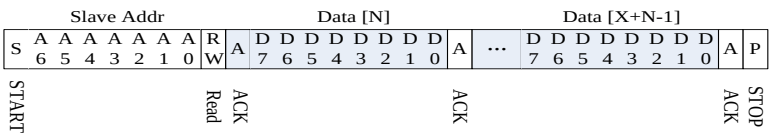
Write N bytes to I2C slave



Set Data Address



Read X bytes from I²C Slave

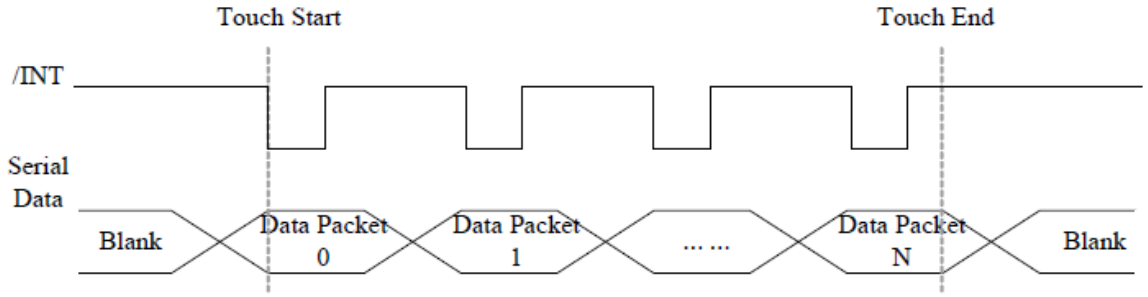


11.3.2 I2C Timing Characteristics

(Ta=25±2°C)

Parameter	Min	Max	Unit
SCL frequency	-	400	kHz
Bus free time between a STOP and START condition	4.7	-	μs
Hold time (repeated) START condition	4.0	-	μs
Data setup time	250	-	ns
Setup time for a repeated START condition	4.7	-	μs
Setup time for STOP condition	4.0	-	μs

11.3.3 Interrupt Trigger Mode



11.3.4 I2C Operating Mode Register Map

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Host Access
Op,00h	DEVICE_MODE		Device Mode[2:0]							RW
Op,01h	Reserved									R
Op,02h	TD_STATUS					Number of touch points[3:0]				R
Op,03h	TOUCH1_YH	1st Event Flag				1st Touch Y Position[11:8]				R
Op,04h	TOUCH1_YL	1st Touch Y Position[7:0]								R
Op,05h	TOUCH1_XH	1st Touch ID[3:0]				1st Touch X Position[11:8]				R
Op,06h	TOUCH1_XL	1st Touch X Position[7:0]								R
Op,07h	Reserved									R

Op,08h	Reserved				R
Op,09h	TOUCH2_YH	2nd Event Flag		2nd Touch Y Position[11:8]	R
Op,0Ah	TOUCH2_YL	2nd touch Y Position[7:0]			R
Op,0Bh	TOUCH2_XH	2nd Touch ID[3:0]		2nd Touch X Position[11:8]	R
Op,0Ch	TOUCH2_XL	2nd Touch X Position[7:0]			R
Op,0Dh	Reserved				R
Op,0Eh	Reserved				R
Op,0Fh	TOUCH3_YH	3rd Event Flag		3rd Touch Y Position[11:8]	R
Op,10h	TOUCH3_YL	3rd Touch Y Position[7:0]			R
Op,11h	TOUCH3_XH	3rd Touch ID[3:0]		3rd Touch X Position[11:8]	R
Op,12h	TOUCH3_XL	3rd Touch X Position[7:0]			R
Op,13h	Reserved				R
Op,14h	Reserved				R
Op,15h	TOUCH4_YH	4th Event Flag		4th Touch Y Position[11:8]	R
Op,16h	TOUCH4_YL	4th Touch Y Position[7:0]			R
Op,17h	TOUCH4_XH	4th Touch ID[3:0]		4th Touch X Position[11:8]	R
Op,18h	TOUCH4_XL	4th Touch X Position[7:0]			R
Op,19h	Reserved				R
Op,1Ah	Reserved				R
Op,1Bh	TOUCH5_YH	5th Event Flag		5th Touch Y Position[11:8]	R
Op,1Ch	TOUCH5_YL	5th Touch Y Position[7:0]			R
Op,1Dh	TOUCH5_XH	5th Touch ID[3:0]		5th Touch X Position[11:8]	R
Op,1Eh	TOUCH5_XL	5th Touch X Position[7:0]			R
Op,1Fh	Reserved				R
Op,20h	Reserved				R
Op,21h	TOUCH6_YH	6th Event Flag		6th Touch Y Position[11:8]	R
Op,22h	TOUCH6_YL	6th Touch Y Position[7:0]			R
Op,23h	TOUCH6_XH	6th Touch ID[3:0]		6th Touch X Position[11:8]	R

Op,24h	TOUCH6_XL	6th Touch X Position[7:0]			R
Op,25h	Reserved				R
Op,26h	Reserved				R
Op,27h	TOUCH7_YH	7thEvent Flag		7th Touch Y Position[11:8]	R
Op,28h	TOUCH7_YL	7thTouch Y Position[7:0]			R
Op,29h	TOUCH7_XH	7th Touch ID[3:0]		7th Touch X Position[11:8]	R
Op,2Ah	TOUCH7_XL	7th Touch X Position[7:0]			R
Op,2Bh	Reserved				R
Op,2Ch	Reserved				R
Op,2Dh	TOUCH8_YH	8thEvent Flag		8th Touch Y Position[11:8]	R
Op,2Eh	TOUCH8_YL	8thTouch Y Position[7:0]			R
Op,2Fh	TOUCH8_XH	8th Touch ID[3:0]		8th Touch X Position[11:8]	R
Op,30h	TOUCH8_XL	8th Touch X Position[7:0]			R
Op,31h	Reserved				R
Op,32h	Reserved				R
Op,33h	TOUCH9_YH	9thEvent Flag		9th Touch Y Position[11:8]	R
Op,34h	TOUCH9_YL	9thTouch Y Position[7:0]			R
Op,35h	TOUCH9_XH	9th Touch ID[3:0]		9th Touch X Position[11:8]	R
Op,36h	TOUCH9_XL	9th Touch X Position[7:0]			R
Op,37h	Reserved				R
Op,38h	Reserved				R
Op,39h	TOUCH10_YH	10thEvent Flag		10th Touch Y Position[11:8]	R
Op,3Ah	TOUCH10_YL	10thTouch Y Position[7:0]			R
Op,3Bh	TOUCH10_XH	10th Touch ID[3:0]		10th Touch X Position[11:8]	R
Op,3Ch	TOUCH10_XL	10th Touch X Position[7:0]			R
Op,3Dh	Reserved				R
Op,3Eh	Reserved				R

11.3.5 DEVICE_MODE

This register is the device mode register, configure it to determine the current mode of the chip.

Address	Bit Address	Register Name	Description
Op,00h	6:4	Device Mode [2:0]	000b Normal operating Mode 001b System Information Mode (Reserved) 100b Test Mode – read raw data (Reserved)

11.3.6 TD_STATUS

This register is the Touch Data status register.

Address	Bit Address	Register Name	Description
Op,02h	3:0	Number of touch points[3:0]	How many points detected. 1-10 is valid.

11.3.7 TOUCHn_YH (n:1-10)

This register describes MSB of the Y coordinate of the nth touch point and the corresponding event flag.

Address	Bit Address	Register Name	Description
Op,03h ~ Op,39h	7:6	Event Flag	00b: Put Down 01b: Put Up 10b: Contact 11b: No event
	5:4		Reserved
	3:0	Touch Y Position [11:8]	MSB of Touch Y Position in pixels

11.3.8 TOUCHn_YL (n:1-10)

This register describes LSB of the Y coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
Op,04h ~ Op,3Ah	7:0	Touch Y Position [7:0]	LSB of the Touch Y Position in pixels

11.3.9 TOUCHn_XH (n:1-10)

This register describes MSB of the X coordinate of the nth touch point and corresponding touch ID.

Address	Bit Address	Register Name	Description
Op,05h ~ Op,3Bh	7:4	Touch ID[3:0]	Touch ID of Touch Point
	3:0	Touch X Position [11:8]	MSB of Touch X Position in pixels

11.3.10 TOUCHn_XL (n:1-10)

This register describes LSB of the X coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
Op,06h ~ Op,3Ch	7:0	Touch X Position [7:0]	LSB of The Touch X Position in pixels

12. Instruction Description

Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0400h)			0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5300h)			0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6230h)			0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0
R12h	Sleep mode	0	1	0	0	DSLP	0	1	1	0	1	1	0	0	1	1	0	0	1
	(0AD9h)			0	0	0	0	1	0	1	0	1	1	0	1	1	0	0	1
R15h	Entry mode	0	1	1	0	1	1	0	0	0	0	0	0	0	1	INVDOT	INVDEN	INVHS	INVVS
	(B010h)			1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
R16h	Horizontal Porch	0	1	0	0	0	0	0	0	0	0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(001Dh)			0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
R17h	Vertical Porch	0	1	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0003h)			0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1
R20h	Uniformity	0	1	1	0	1	1	0	0	0	0	1	1	ENSVIN	0	1	0	1	1
	(B0EBh)			1	0	1	1	0	0	0	0	1	1	1	0	1	0	1	1

(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R26h	Analogue Setting	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0
	(3800h)			0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
R28h R29h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

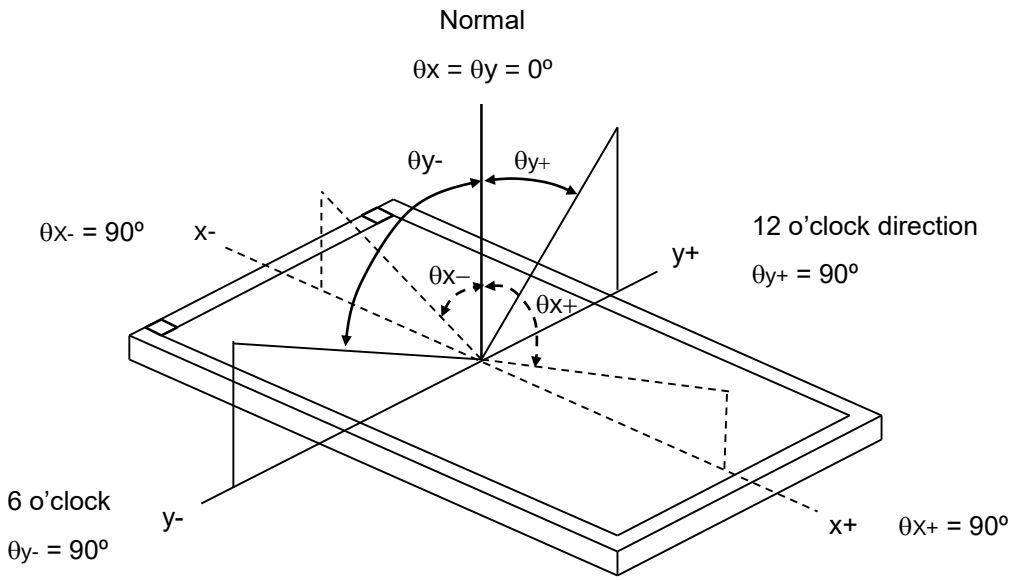
Note: In R01h, bits REV, BGR, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

13. Optical Characteristics

The optical characteristics should be measured in a dark environment (≤ 1 lux) or equivalent state with the methods shown in Note (4).

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	150	(350)	-	-	(2)
Response Time		$T_{R+}T_F$		-	50	-	ms	(3)
Luminance(Center)		Y		200	(250)	-	cd/m^2	(4)
Brightness uniformity		BUNI		80	-	-	%	(5)
Color Chromaticity	Red	Rx		0.575	0.625	0.675	-	(1),(4)
		Ry		0.285	0.335	0.385	-	
	Green	Gx		0.295	0.345	0.395	-	
		Gy		0.550	0.600	0.650	-	
	Blue	Bx		0.095	0.145	0.195	-	
		By		0.030	0.080	0.130	-	
	White	Wx		0.265	0.315	0.365	-	
		Wy		0.265	0.315	0.365	-	
Viewing Angle	Horizontal	θ_X+	CR≥10	55	(70)	-	deg.	
		θ_X-		55	(70)	-		
	Vertical	θ_Y+		40	(55)	-		
		θ_Y-		50	(70)	-		

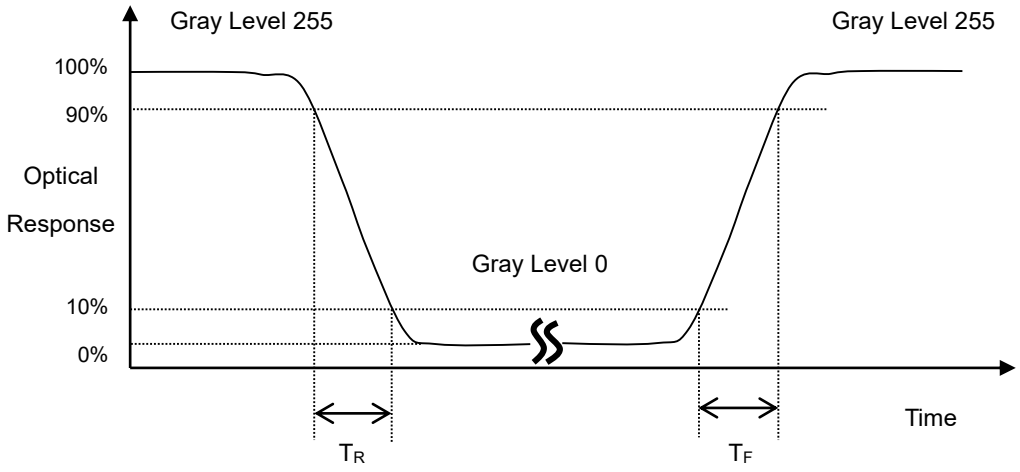
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

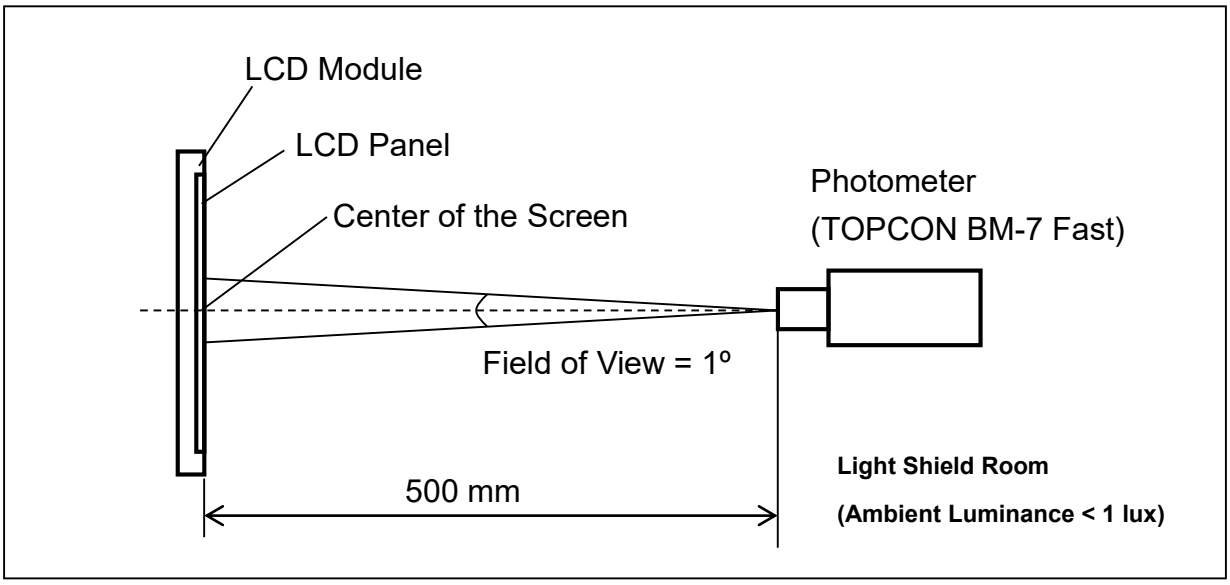
$$CR = \frac{\text{Luminance (brightness) all pixels "White"}}{\text{Luminance (brightness) all pixels "dark"}}$$

Note (3) Definition of Response Time (T_R, T_F):



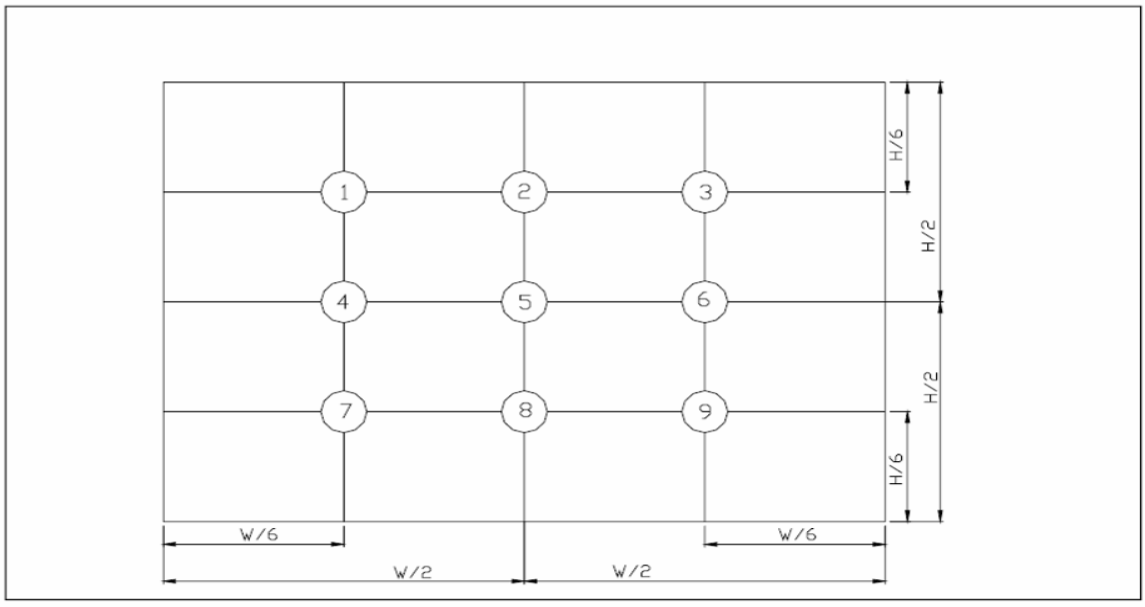
Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a windless room.



Note (5) Definition of brightness uniformity

Brightness uniformity=(Min Luminance of 9 points)/(Max Luminance of 9 points)×100%



(單位 ：mm)

14. Reliability Test

No.	Test Items	Test Condition	Remark
1	High Temperature Storage Test	T_a= 80°C 240 hours	(1),(3),(4)
2	Low Temperature Storage Test	T_a= -30°C 240 hours	(1),(3),(4)
3	High Temperature Operation Test	T_S= 70°C 240 hours	(2),(3),(4)
4	Low Temperature Operation Test	T_a= -20°C 240 hours	(1),(3),(4)
5	High Temperature and High Humidity Operation Test	T_a=60°C 90%RH 240 hours	(3),（4）
6	Electro Static Discharge Test （non-operating）	-Panel Surface/Top Case ：150pF, 330Ω Air：±15kV, Contact: ±8kV	（3）
7	Mechanical Shock Test （non-operating）	Half sine wave, 100G, 6ms 3 times shock of each six surfaces	（3）
8	Vibration Test (non-operating)	Sine wave:10 ~ 55 ~ 10Hz amplitude:1.5mm 3 axis, 2 hours/axis	(3)
9	Thermal Shock Test （non-operating）	-20°C （30min）~ 70°C （30min）,10 cycles	（3）, （4）
10	Drop Test(with Carton)	Height：80㎝ 1 corner, 3 edges, 6 surfaces	（3）

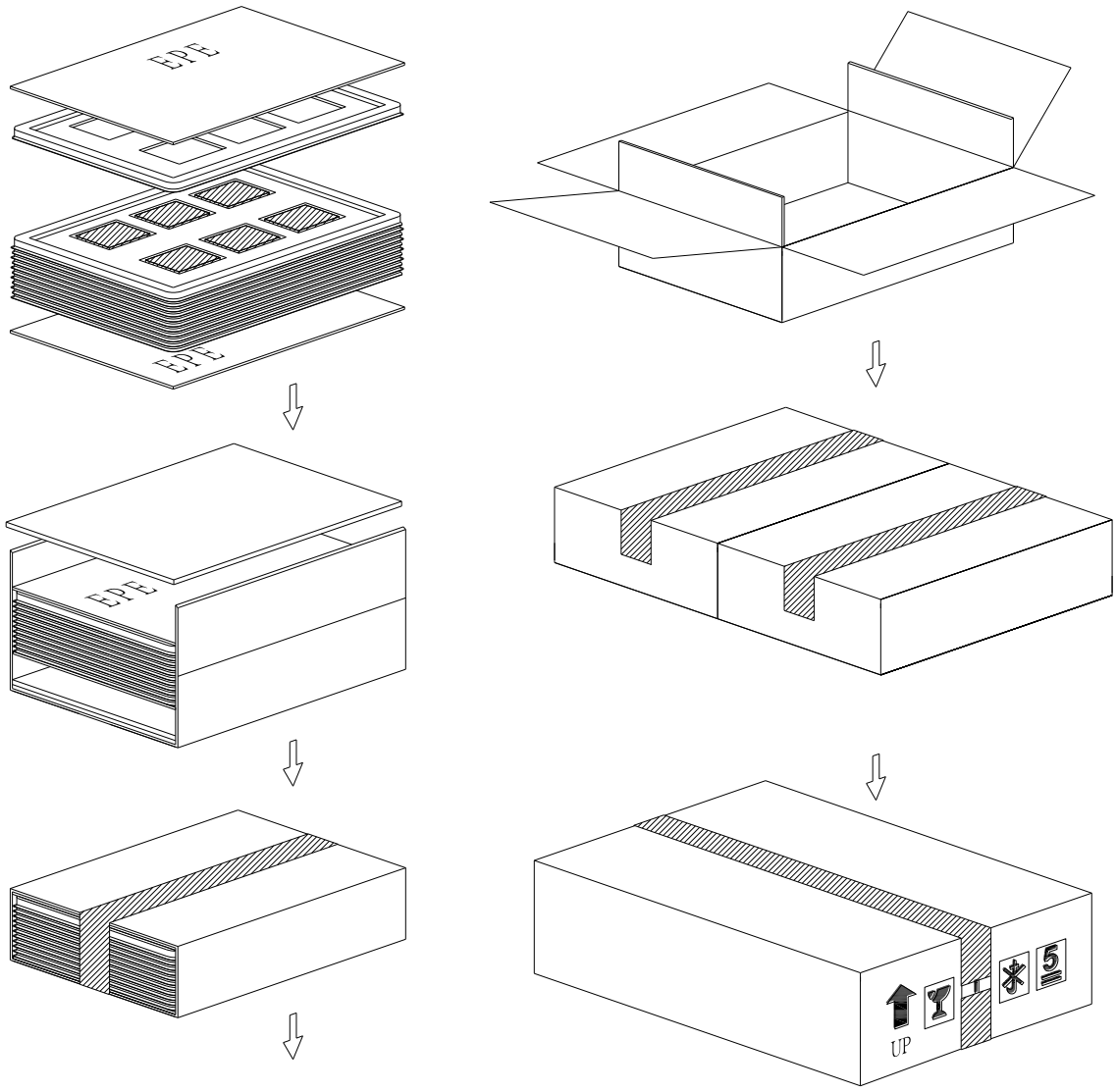
Note 1: Ta is the ambient temperature of samples.

Note 2: Ts is the temperature of panel's surface.

Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

15. Packaging



	PARTS LIST				
	ITEM	SIZE(LxWxH) unit:mm	MATERIAL	Q.T.Y	NOTE
1	TRAY	372.0x262.0x16.6		26	
2	EPE(J46)	372.0x262.0x5.0	EPE	4	
3	CARD BOARD(P01)	816.0x375.0x3.5	CARTON	2	
4	CARD BOARD(P02)	945.0x275.0x3.5	CARTON	2	
5	CARD BOARD(P03)	375.0x265.0x3.5	CARTON	4	
6	INTERNAL BOX(S01)	400.0x290.0x150.0	CARTON	2	
7	EXTERNAL BOX(L28)	600.0x420.0x180.0		1	
8	PRODUCT	76.84x63.84x4.85		144	

16. Precautions

16.1 Assembly and Handling Precautions

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It's recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Don't apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD module in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow.

16.2 Safety Precautions

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the module's end of life, it is not harmful in case of normal operation and storage.

16.3 Terms of Warrant

(1) Acceptance inspection period

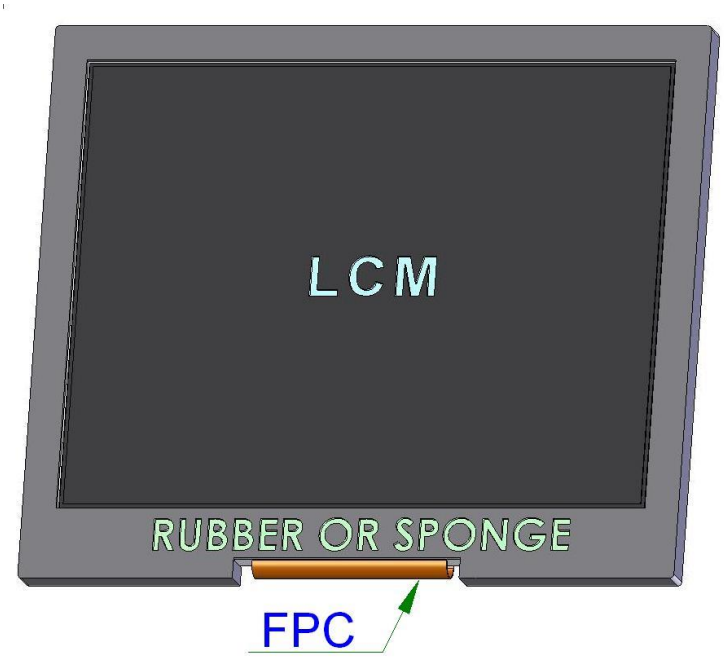
The period is within one month after the arrival of contracted commodity at the buyer's factory site.

(2) Applicable warrant period

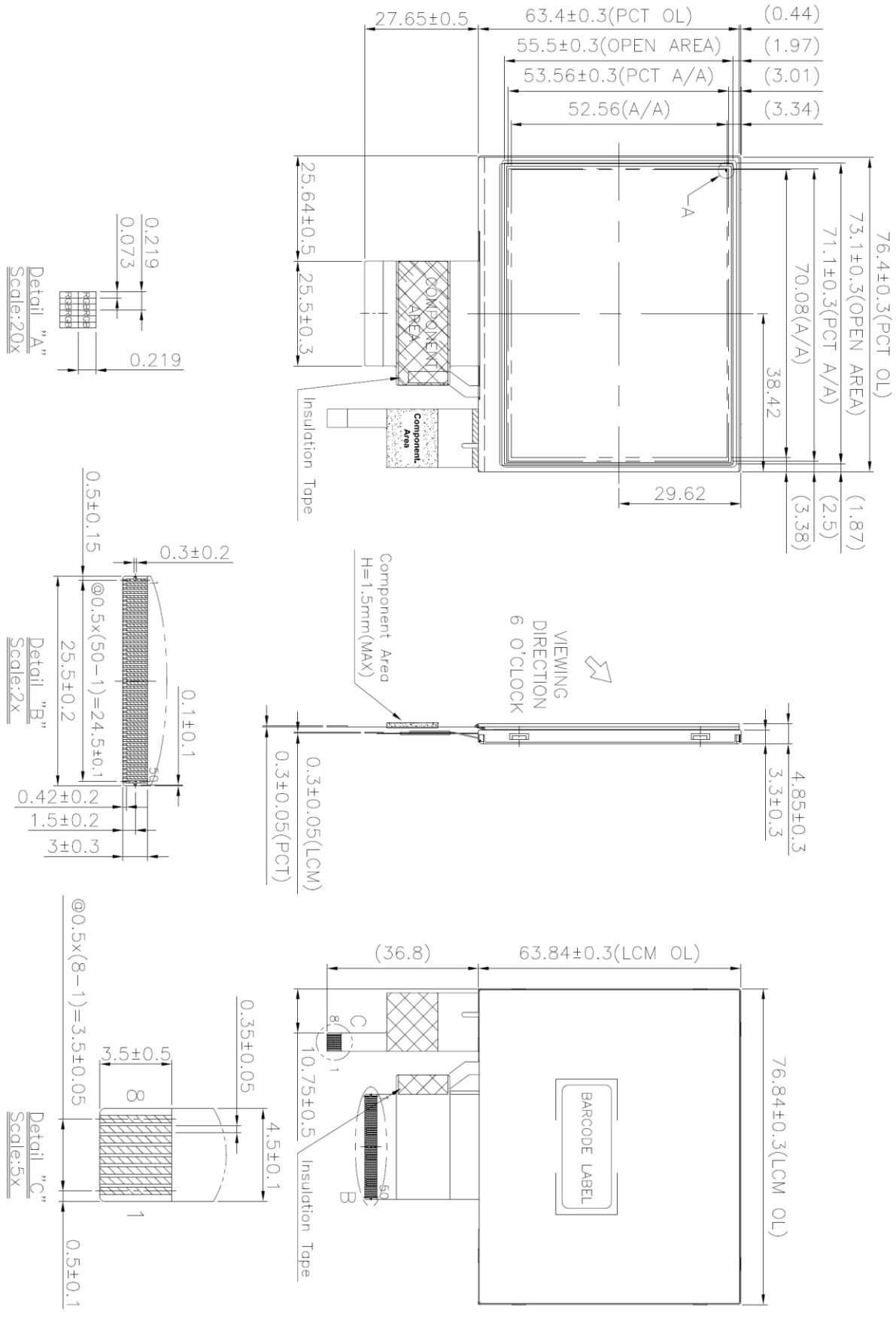
The period is within twelve months since the date of shipping out under normal using and storage conditions.

16.4 Cautions for LCM's installing and assembling

Please keep away the FPC while assembling or fixing the LCM to avoid FPC being damaged or extruded or other related problems. Please see below picture.



17.Outline Drawing



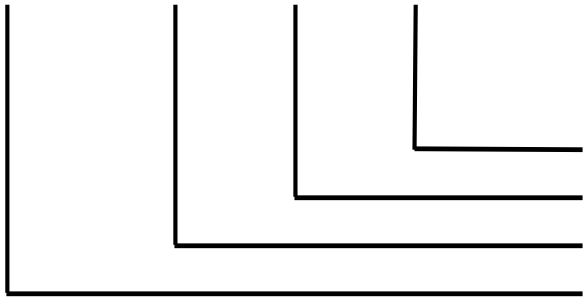
18.Definition of Labels

The bar code nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Module Name: PT322435B-TLMWD-EC35

(b) Serial ID:

A B C D E F G H I J K L



Serial ID includes the information as below:

(a) Screen size (Diagonal): Inch Code (ABCD)

3.5” → 0350

10.4” → 1040

(b) Manufactured Date: Year, Month, Day (EFG)

Year (E)

Year	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009
Mark	0	1	2	3	4	5	6	7	8	9
Year	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
Mark	A	B	C	D	E	F	G	H	I	J

Month (F)

Month	Jan.	Feb.	Mar.	Apr.	May	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

Day (G)

Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Mark	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Day	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Mark	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	

(c) Factory Code (H):

For P-TEC internal use.

(d) Serial No. (IJKL):

Manufacturing sequence of product, for example: 0001~9999.

19. Incoming Inspection Standards

19.1 The environmental condition of inspection

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature 25±5°C

(2) Humidity: 60±5% RH

(3) Viewing distance is approximately 35 ~ 40 cm

(4) Viewing angle is normal to the LCD panel as Fig _1(10°)

(5) Ambient Illumination: 300 ~ 500 Lux for external appearance inspection

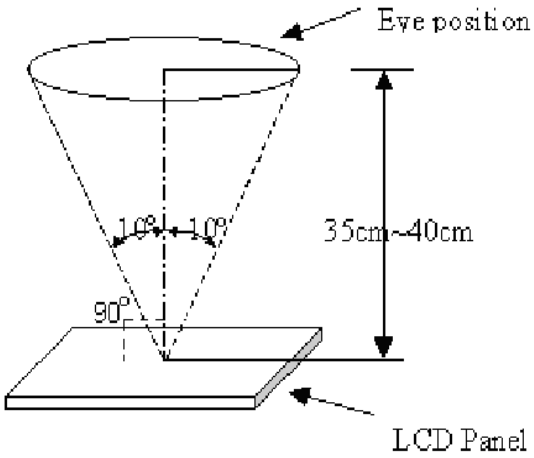


Fig _ 1

19.2 The defects classify of AQL as following:

(1) Test method :According to ANSI/ASQC Z 1.4 .General Inspection Level Ⅱ take a single time

(2) The defects classify of AQL as following:

Class of defects	AQL	Definition
Major	0.65%	It is defect that is likely to result in failure or to reduce materially the usability of the intended function.
Minor	1.5%	It is a defect that will not result in functioning problem with deviation classified.

19.3 Inspection Parameters

<table>
<tr><th colspan="2">Item</th><th colspan="5">Specification/Description</th><th>Note</th></tr>
<tr><td rowspan="2">Display</td><td rowspan="2">Function</td><td colspan="5">No Display</td><td>-</td></tr>
<tr><td colspan="5">Malfunction</td><td>-</td></tr>
<tr><td rowspan="2">Operating</td><td>Contrast ratio</td><td colspan="5">Out of Spec</td><td>-</td></tr>
<tr><td>Line defect</td><td colspan="5">No obvious Vertical and Horizontal line defect in bright , dark and colored.</td><td>-</td></tr>
<tr><td rowspan="6">Operating</td><td rowspan="6">Point Defect (red,green,blue, dark， white)</td><td rowspan="2">Item</td><td colspan="3">Acceptable number</td><td rowspan="2">Note: 1、4、5、6</td></tr>
<tr><td>A</td><td>B</td><td>Total</td></tr>
<tr><td>BRIGHT DOT</td><td>N≦0</td><td>N≦0</td><td rowspan="3">N≦0</td></tr>
<tr><td>DARK DOT</td><td>N≦0</td><td>N≦0</td></tr>
<tr><td>TOTAL DOT</td><td>N≦0</td><td>N≦0</td></tr>
<tr><td>TWO ADJACENT DOT</td><td colspan="3">NOT ALLOWED</td></tr>
<tr><td>THREE OR MORE ADJACENT DOT</td><td colspan="3">NOT ALLOWED</td></tr>
<tr><td rowspan="3">External Inspection (non-operating)</td><td>Scratch on the polarizer</td><td colspan="5"><table><tr><td>L(mm)</td><td>W(mm)</td><td>Acceptable number</td></tr><tr><td>L≦2.5</td><td>W≦0.1</td><td>3</td></tr><tr><td>L＞2.5</td><td>W＞0.1</td><td>0</td></tr></table></td><td>Note:2</td></tr>
<tr><td>Dent or bubble on the polarizer</td><td colspan="5"><table><tr><td>Dimension(mm)</td><td>Acceptable number</td></tr><tr><td>D≦0.3</td><td>3</td></tr><tr><td>D≦0.1</td><td>Disregard</td></tr></table></td><td>Note:3</td></tr>
<tr><td>Foreign material on the polarizer</td><td colspan="5"><table><tr><td>Dimension(mm)</td><td>Acceptable number</td></tr><tr><td>D≦0.5</td><td>2</td></tr><tr><td>D≦0.1</td><td>Disregard</td></tr></table></td><td>Note:3</td></tr>
</table>

Incoming Inspection Touch Panel

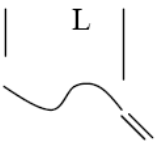
Circular Defects
Linear Defects
Scratch
Air Bubble
Crack

(1) Circular Defects

ϕ =(L+W)/2

Diameter(mm)	Spec
$\phi \leqq 0.2$	No quantity limit
$0.2 < \phi < 0.4$	Max 5defect
$0.4 \leqq \phi$	Reject

(2) Linear Defects



Length	Width	Acceptable
6.0≧L	0.06≧W	Accept
L≧6.0	W≧0.06	Reject

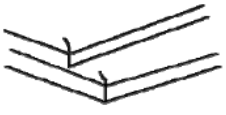
(3)Scratch

Length	Width	Acceptable
12.0≧L	0.06≧W	Accept
L≧12.0	W≧0.06	Reject
The Min distance of defects must be above 5.0mm.		

(4) Air Bubble

Diameter(mm)	Spec
$\phi \leqq 0.2$	No quantity limit
$0.2 < \phi \leqq 0.6$	Max 5 defect
The Min distance of defects must be above 5.0mm.	

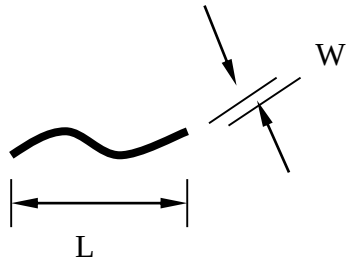
(5)Crack Reject



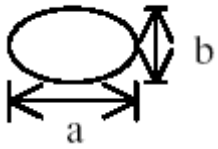
Note1. The definition of dot defect :

The dot defect was judged after repair and the size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

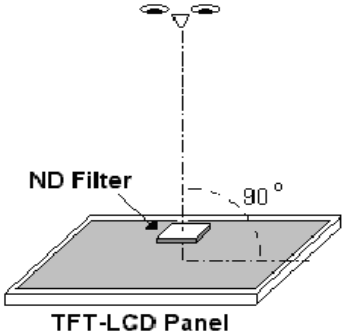
Note2.

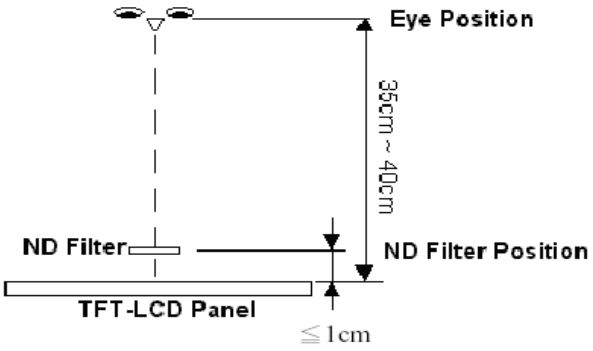


Note3. D：Diameter D=(a+b)/2



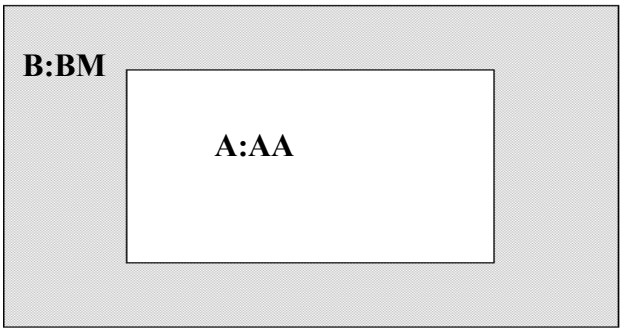
Note4. Bright dot is defined through 6% transmission ND Filter as following.





Note5. ADJACENT DOT

Note6.



19.4 Handling of LCM

(1)Don't give external shock.

(2)Don't apply excessive force on the surface.

(3)Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.

(4)Don't operate it above the absolute maximum rating.

(5)Don't disassemble the LCM.