RA6M4 Group

Renesas Microcontrollers

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High-performance 200 MHz Arm Cortex-M33 core, up to 1 MB code flash memory with Dual-bank, background and SWAP operation, 8 KB Data flash memory, and 256 KB SRAM with Parity/ECC. High-integration with Ethernet MAC controller, USB 2.0 Full-Speed, SDHI, Quad and Octa SPI, and advanced analog. Integrated Secure Crypto Engine with cryptography accelerators, key management support, tamper detection and power analysis resistance in concert with Arm TrustZone for integrated secure element functionality.

# Features

## ■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 200 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

## ■ Memory

- Up to 1-MB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 256-KB SRAM

## ■ Connectivity

- Serial Communications Interface (SCI) × 10
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding (SCI3, SCI4)
- $I^2C$ bus interface (IIC) × 2
- Serial Peripheral Interface (SPI) × 2
- Quad Serial Peripheral Interface (QSPI)
- Octa Serial Peripheral Interface (OSPI)
- USB 2.0 Full-Speed Module (USBFS)
- Control Area Network module (CAN) × 2
- Ethernet MAC/DMA Controller (ETHERC/EDMAC)
- SD/MMC Host Interface (SDHI)
- Serial Sound Interface Enhanced (SSIE)

## ■ Analog

- 12-bit A/D Converter (ADC12) × 2
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

## ■ Timers

- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 6

## ■ Security and Encryption

- Secure Crypto Engine 9
  - Symmetric algorithms: AES
  - Asymmetric algorithms: RSA, ECC, and DSA
  - Hash-value generation: SHA224, SHA256, GHASH
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three or six regions for the code flash, depending on the bank mode
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecyle management
- Pin function
  - Up to three tamper pins
  - Secure pin multiplexing

## ■ System and Power Management

- Low power modes
- Battery backup function (VBATT)
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

## ■ Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSU)

## ■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL/PLL2
- Clock out support

## ■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

## ■ Operating Voltage

- VCC: 2.7 to 3.6 V

## ■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)

# 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 200 MHz with the following features:

- Up to 1 MB code flash memory
- 256 KB SRAM
- Quad Serial Peripheral Interface (QSPI), Octa Serial Peripheral Interface (OSPI)
- Ethernet MAC Controller (ETHERC), USBFS, SD/MMC Host Interface
- Capacitive Touch Sensing Unit (CTSU)
- Analog peripherals
- Security and safety features

## 1.1 Function Outline

**Table 1.1 Arm core**

| Feature | Functional description |
|---|---|
| Arm Cortex-M33 core | • Maximum operating frequency: up to 200 MHz<br>• Arm Cortex-M33 core:<br>– Armv8-M architecture with security extension<br>– Revision: r0p4-00rel0<br>• Arm Memory Protection Unit (Arm MPU)<br>– Protected Memory System Architecture (PMSAv8)<br>– Secure MPU (MPU_S): 8 regions<br>– Non-secure MPU (MPU_NS): 8 regions<br>• SysTick timer<br>– Embeds two Systick timers: Secure and Non-secure instance<br>– Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK)<br>• CoreSight™ ETM-M33 |

**Table 1.2 Memory**

| Feature | Functional description |
|---|---|
| Code flash memory | Maximum 1 MB of code flash memory. |
| Data flash memory | 8 KB of data flash memory. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. |
| SRAM | On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). |

**Table 1.3 System (1 of 2)**

| | Functional description |
|---|---|
| Operating modes | Two operating modes:<br>• Single-chip mode<br>• SCI/USB boot mode |
| Resets | The MCU provides 14 resets. |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. |

**Table 1.3 System (2 of 2)**

| | Functional description |
|---|---|
| Clocks | • Main clock oscillator (MOSC)<br>• Sub-clock oscillator (SOSC)<br>• High-speed on-chip oscillator (HOCO)<br>• Middle-speed on-chip oscillator (MOCO)<br>• Low-speed on-chip oscillator (LOCO)<br>• IWDT-dedicated on-chip oscillator<br>• PLL/PLL2<br>• Clock out support |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. |
| Low power modes | Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. |
| Register write protection | The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). |
| Memory Protection Unit (MPU) | The MCU has one Memory Protection Unit (MPU). |

**Table 1.4 Event link**

| Feature | Functional description |
|---|---|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. |

**Table 1.5 Direct memory access**

| Feature | Functional description |
|---|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. |
| DMA Controller (DMAC) | The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. |

**Table 1.6 External bus interface**

| Feature | Functional description |
|---|---|
| External buses | • CS area (ECBIU): Connected to the external devices (external memory interface)<br>• QSPI area (EQBIU): Connected to the QSPI (external device interface)<br>• OSPI area (EOBIU): Connected to the OSPI (external device interface) |

**Table 1.7 Timers (1 of 2)**

| Feature | Functional description |
|---|---|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 4 channels and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. |
| Port Output Enable for GPT (POEG) | The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state |

**Table 1.7 Timers (2 of 2)**

| Feature | Functional description |
|---|---|
| Low power Asynchronous General Purpose Timer (AGT) | The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. |
| Realtime Clock (RTC) | The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. |
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. |

**Table 1.8 Communication interfaces (1 of 2)**

| Feature | Functional description |
|---|---|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) × 10 channels have asynchronous and synchronous serial interfaces:<br>● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))<br>● 8-bit clock synchronous interface<br>● Simple IIC (master-only)<br>● Simple SPI<br>● Smart card interface<br>● Manchester interface<br>● Extended Serial interface<br>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3 to 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. |
| $I^2C$ bus interface (IIC) | The $I^2C$ bus interface (IIC) has 2 channels. The IIC module conforms with and provides a subset of the NXP $I^2C$ (Inter-Integrated Circuit) bus interface functions. |
| Serial Peripheral Interface (SPI) | The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. |
| Control Area Network (CAN) | The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver. |
| USB 2.0 Full-Speed module (USBFS) | The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. |
| Quad Serial Peripheral Interface (QSPI) | The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. |
| Octa Serial Peripheral Interface (OSPI) | The Octa Serial Peripheral Interface (OSPI) module is a memory controller for connecting OctaFlash and OctaRAM. |

**Table 1.8 Communication interfaces (2 of 2)**

| Feature | Functional description |
|---|---|
| Serial Sound Interface Enhanced (SSIE) | The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting $I^2S$/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. |
| SD/MMC Host Interface (SDHI) | The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit1-bit, and 4-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. |
| Ethernet MAC (ETHERC) | One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. |

**Table 1.9 Analog**

| | Functional description |
|---|---|
| 12-bit A/D Converter (ADC12) | A 12-bit successive approximation A/D converter is provided. Up to 22 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. |
| 12-bit D/A Converter (DAC12) | A 12-bit D/A converter (DAC12) is provided. |
| Temperature Sensor (TSN) | The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application. |

**Table 1.10 Human machine interfaces**

| Feature | Functional description |
|---|---|
| Capacitive Touch Sensing Unit (CTSU) | The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode. |

**Table 1.11 Data processing**

| Feature | Functional description |
|---|---|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. |

## 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

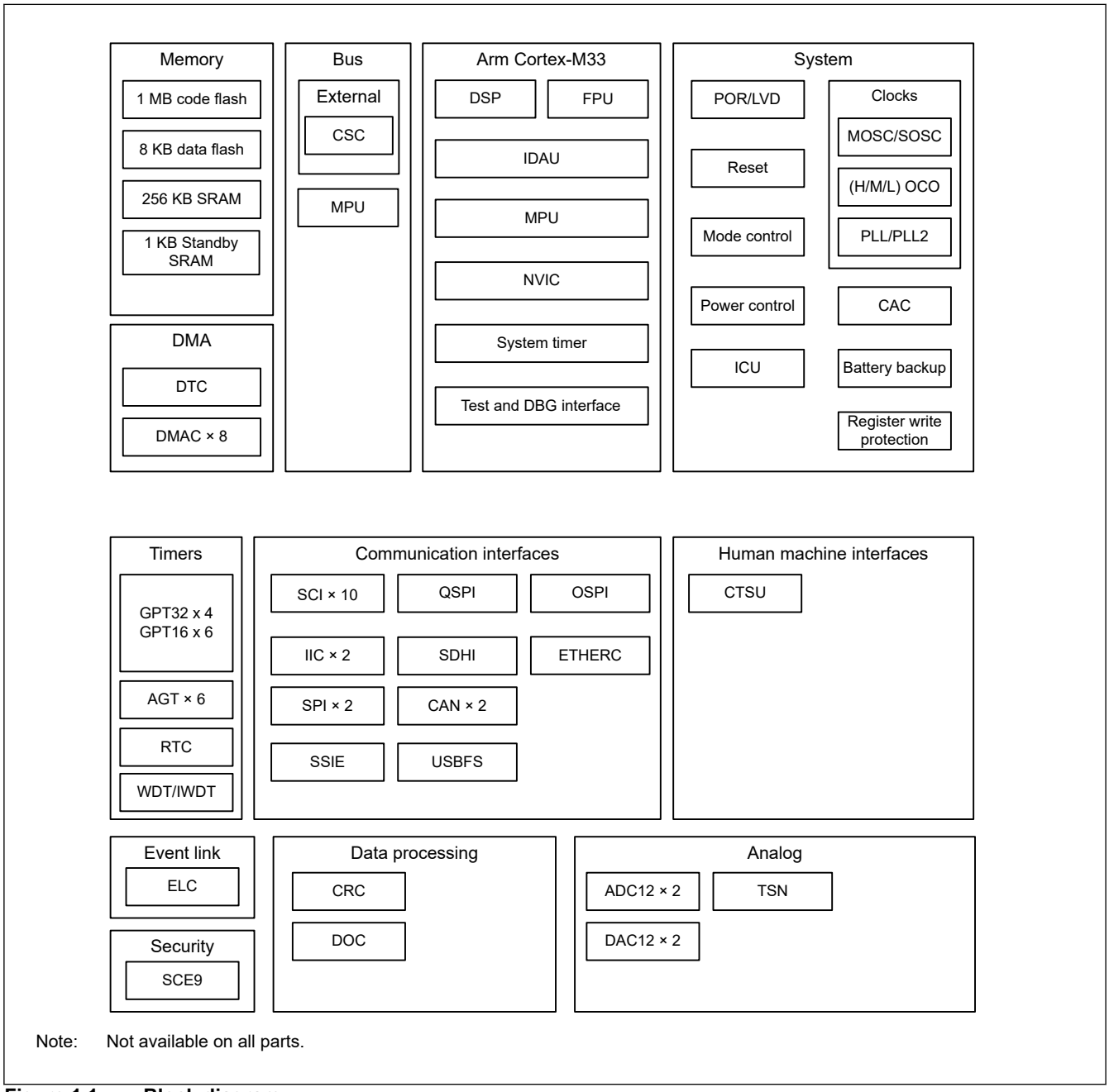



**Figure 1.1 Block diagram**

## 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

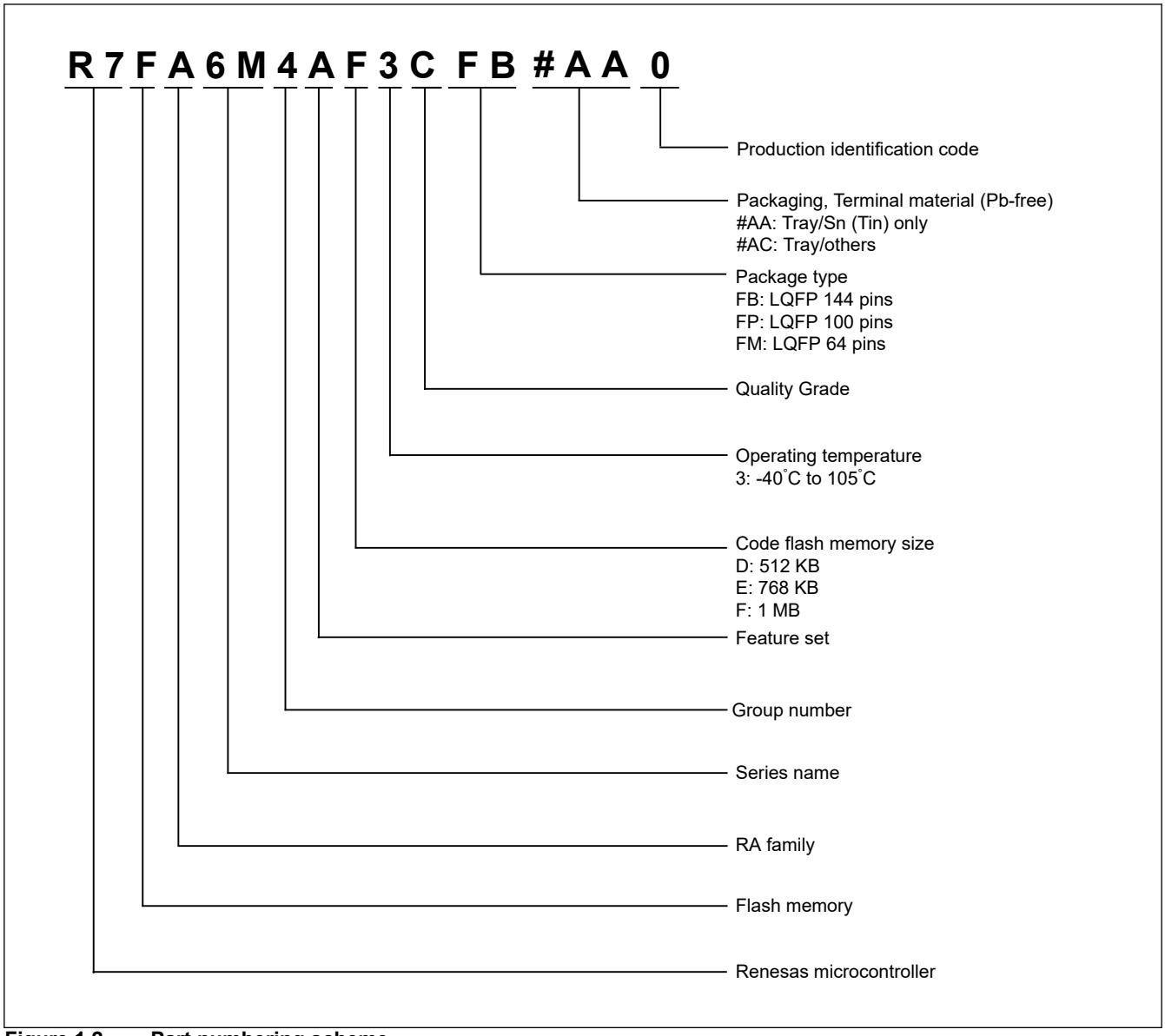



**Figure 1.2 Part numbering scheme**

**Table 1.12 Product list**

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---|---|---|---|---|---|
| R7FA6M4AF3CFB | PLQP0144KA-B | 1 MB | 8 KB | 256 KB | -40 to +105°C |
| R7FA6M4AF3CFP | PLQP0100KB-B | | | | |
| R7FA6M4AF3CFM | PLQP0064KB-C | | | | |
| R7FA6M4AE3CFB | PLQP0144KA-B | 768 KB | 8 KB | 256 KB | -40 to +105°C |
| R7FA6M4AE3CFP | PLQP0100KB-B | | | | |
| R7FA6M4AE3CFM | PLQP0064KB-C | | | | |
| R7FA6M4AD3CFB | PLQP0144KA-B | 512 KB | 8 KB | 256 KB | -40 to +105°C |
| R7FA6M4AD3CFP | PLQP0100KB-B | | | | |
| R7FA6M4AD3CFM | PLQP0064KB-C | | | | |

## 1.4 Function Comparison

**Table 1.13 Function Comparison (1 of 2)**

| Parts number | | R7FA6M4AF3CFB<br>R7FA6M4AE3CFB<br>R7FA6M4AD3CFB | R7FA6M4AF3CFP<br>R7FA6M4AE3CFP<br>R7FA6M4AD3CFP | R7FA6M4AF3CFM<br>R7FA6M4AE3CFM<br>R7FA6M4AD3CFM |
|---|---|---|---|---|
| Pin count | | 144 | 100 | 64 |
| Package | | LQFP | | |
| Code flash memory | | 1 MB<br>768 KB<br>512 KB | | |
| Data flash memory | | 8 KB | | |
| SRAM | | 256 KB | | |
| | Parity | 192 KB | | |
| | ECC | 64 KB | | |
| Standby SRAM | | 1 KB | | |
| DMA | DTC | Yes | | |
| | DMAC | 8 | | |
| BUS | External bus | 16-bit bus | 8-bit bus | No |
| System | CPU clock | 200 MHz (max.) | | |
| | CPU clock sources | MOSC, SOSC, HOCO, MOCO, LOCO, PLL | | |
| | CAC | Yes | | |
| | WDT/IWDT | Yes | | |
| | Backup register | 128 B | | |
| Communication | SCI | 10 | 10 | 8 |
| | IIC | 2 | | |
| | SPI | 2 | | |
| | CAN | 2 | | |
| | USBFS | Yes | | |
| | QSPI | Yes | | |
| | OSPI | Yes | | No |
| | SSIE | Yes | | No |
| | SDHI/MMC | Yes | | No |
| | ETHERC | Yes | | No |
| Timers | GPT32[*1] | 4 | | |
| | GPT16[*1] | 6 | | |
| | AGT[*1] | 6 | | |
| | RTC | Yes | | |
| Analog | ADC12 | Unit 0: 12<br>Unit 1: 10 | Unit 0: 11<br>Unit 1: 9 | Unit 0: 7<br>Unit 1: 4 |
| | DAC12 | 2 | | |
| | TSN | Yes | | |
| HMI | CTSU | 20 | 12 | 7 |
| Data processing | CRC | Yes | | |
| | DOC | Yes | | |
| Event control | ELC | Yes | | |

**Table 1.13 Function Comparison (2 of 2)**

| Parts number | R7FA6M4AF3CFB<br>R7FA6M4AE3CFB<br>R7FA6M4AD3CFB | R7FA6M4AF3CFP<br>R7FA6M4AE3CFP<br>R7FA6M4AD3CFP | R7FA6M4AF3CFM<br>R7FA6M4AE3CFM<br>R7FA6M4AD3CFM |
|---|---|---|---|
| Security | SCE9, TrustZone, and Lifecycle management | | |

Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.

## 1.5 Pin Functions

**Table 1.14 Pin functions (1 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin. |
| | VCL/VCL0 | I/O | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Battery Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCOUT | Output | |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| On-chip emulator | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TCLK | Output | Output clock for synchronization with the trace data |
| | TDATA0 to TDATA3 | Output | Trace data output |
| | SWO | Output | Serial wire trace output pin |
| | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQn | Input | Maskable interrupt request pins |
| | IRQn-DS | Input | Maskable interrupt request pins that can also be used in Deep Software Standby mode |

**Table 1.14 Pin functions (2 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| External bus interface | RD | Output | Strobe signal indicating that reading from the external bus interface space is in progress, active-low |
| | WR | Output | Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low |
| | WRn | Output | Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active-low |
| | BCn | Output | Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active-low |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT | Input | Input pin for wait request signals in access to the external space, active-low |
| | CSn | Output | Select signals for CS areas, active-low |
| | A00 to A20 | Output | Address bus |
| | D00 to D15 | I/O | Data bus |
| | A00/D00 to A15/D15 | I/O | Address/data multiplexed bus |
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pins |
| | GTIOCnA, GTIOCnB | I/O | Input capture, output compare, or PWM output pins |
| | GTIU | Input | Hall sensor input pin U |
| | GTIV | Input | Hall sensor input pin V |
| | GTIW | Input | Hall sensor input pin W |
| | GTOUUP | Output | 3-phase PWM output for BLDC motor control (positive U phase) |
| | GTOULO | Output | 3-phase PWM output for BLDC motor control (negative U phase) |
| | GTOVUP | Output | 3-phase PWM output for BLDC motor control (positive V phase) |
| | GTOVLO | Output | 3-phase PWM output for BLDC motor control (negative V phase) |
| | GTOWUP | Output | 3-phase PWM output for BLDC motor control (positive W phase) |
| | GTOWLO | Output | 3-phase PWM output for BLDC motor control (negative W phase) |
| AGT | AGTEEn | Input | External event input enable signals |
| | AGTIOn | I/O | External event input and pulse output pins |
| | AGTOn | Output | Pulse output pins |
| | AGTOAn | Output | Output compare match A output pins |
| | AGTOBn | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock |
| | RTCICn | Input | Time capture event input pins |

**Table 1.14 Pin functions (3 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| SCI | SCKn | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXDn | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXDn | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTSn_RTSn | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low. |
| | CTSn | Input | Input for the start of transmission. |
| | SCLn | I/O | Input/output pins for the IIC clock (simple IIC mode) |
| | SDAn | I/O | Input/output pins for the IIC data (simple IIC mode) |
| | SCKn | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISOn | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSIn | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| | SSn | Input | Chip-select input pins (simple SPI mode), active-low |
| | RXDXn | Input | Input pins for received data (Extended Serial Mode) |
| | TXDXn | Output | Output pins for transmitted data (Extended Serial Mode) |
| | SIOXn | I/O | Input/output pins for receivde or tramsmitted data (Extended Serial Mode) |
| IIC | SCLn | I/O | Input/output pins for the clock |
| | SDAn | I/O | Input/output pins for data |
| SPI | RSPCKA, RSPCKB | I/O | Clock input/output pin |
| | MOSIA, MOSIB | I/O | Input or output pins for data output from the master |
| | MISOA, MISOB | I/O | Input or output pins for data output from the slave |
| | SSLA0, SSLB0 | I/O | Input or output pin for slave selection |
| | SSLA1 to SSLA3, SSLB1 to SSLB3 | Output | Output pins for slave selection |
| CAN | CRXn | Input | Receive data |
| | CTXn | Output | Transmit data |

**Table 1.14 Pin functions (4 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| USBFS | VCC_USB | Input | Power supply pin |
| | VSS_USB | Input | Ground pin |
| | USB_DP | I/O | D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus. |
| | USB_DM | I/O | D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus. |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller. |
| | USB_EXICEN | Output | Low-power control signal for external power supply (OTG) chip |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA, USB_OVRCURB | Input | Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_OVRCURA-DS, USB_OVRCURB-DS | Input | Overcurrent pins for USBFS that can also be used in Deep Software Standby mode.<br>Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_ID | Input | Connect the MicroAB connector ID input signal to this pin during operation in OTG mode |
| QSPI | QSPCLK | Output | QSPI clock output pin |
| | QSSL | Output | QSPI slave output pin |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |
| OSPI | OM_SCLK | Output | Clock output (OCTACLK divided by 2) |
| | OM_CSn | Output | Chip select signal for an OctaFlash device, active-low |
| | OM_DQS | I/O | Read data strobe/write data mask signal |
| | OM_SIOn | I/O | Data input/output |
| | OM_RESET | Output | Reset signal for both OctaFlash and OctaRAM devices, active-low |
| | OM_ECS | Input | ECC error detection signal from the external memory, active-low |
| SSIE | SSIBCK0 | I/O | SSIE serial bit clock pins |
| | SSILRCK0/SSIFS0 | I/O | LR clock/frame synchronization pins |
| | SSITXD0 | Output | Serial data output pin |
| | SSIRXD0 | Input | Serial data input pin |
| | SSIDATA0 | I/O | Serial data input/output pins |
| | AUDIO_CLK | Input | External clock pin for audio (input oversampling clock) |
| SDHI/MMC | SD0CLK | Output | SD clock output pins |
| | SD0CMD | I/O | Command output pin and response input signal pins |
| | SD0DAT0 to SD0DAT73 | I/O | SD and MMC data bus pins |
| | SD0CD | Input | SD card detection pins |
| | SD0WP | Input | SD write-protect signals |

**Table 1.14 Pin functions (5 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| ETHERC | REF50CK0 | Input | 50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode. |
| | RMII0_CRS_DV | Input | Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode<br>. |
| | RMII0_TXDn | Output | 2-bit transmit data in RMII mode |
| | RMII0_RXDn | Input | 2-bit receive data in RMII mode |
| | RMII0_TXD_EN | Output | Output pin for data transmit enable signal in RMII mode |
| | RMII0_RX_ER | Input | Indicates an error occurred during reception of data in RMII mode |
| | ET0_CRS | Input | Carrier detection/data reception enable signal |
| | ET0_RX_DV | Input | Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0 |
| | ET0_EXOUT | Output | General-purpose external output pin |
| | ET0_LINKSTA | Input | Input link status from the PHY-LSI |
| | ET0_ETXDn | Output | 4 bits of MII transmit data |
| | ET0_ERXDn | Input | 4 bits of MII receive data |
| | ET0_TX_EN | Output | Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0. |
| | ET0_TX_ER | Output | Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission. |
| | ET0_RX_ER | Output | Receive error pin. Functions as signal to recognize an error during reception. |
| | ET0_TX_CLK | Input | Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER. |
| | ET0_RX_CLK | Input | Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER. |
| | ET0_COL | Input | Input collision detection signal |
| | ET0_WOL | Output | Receive Magic packets |
| | ET0_MDC | Output | Output reference clock signal for information transfer through ET0_MDIO |
| | ET0_MDIO | I/O | Input or output bidirectional signal for exchange of management data with PHY-LSI |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin. |
| | AVSS0 | Input | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin. |
| | VREFH0 | Input | Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0). |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0). |
| | VREFH | Input | Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1) and D/A Converter. |
| | VREFL | Input | Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1) and D/A Converter. |

**Table 1.14 Pin functions (6 of 6)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| ADC12 | ANmn | Input | Input pins for the analog signals to be processed by the A/D converter.<br>(m: ADC unit number, n: pin number) |
| | ADTRGm | Input | Input pins for the external trigger signals that start the A/D conversion, active-low. |
| DAC12 | DAn | Output | Output pins for the analog signals processed by the D/A converter. |
| CTSU | TSn | Input | Capacitive touch detection pins (touch pins) |
| | TSCAP | I/O | Secondary power supply pin for the touch driver |
| I/O ports | Pmn | I/O | General-purpose input/output pins<br>(m: port number, n: pin number) |
| | P200 | Input | General-purpose input pin |

## 1.6 Pin Assignments

The following figures show the pin assignments from the top view.

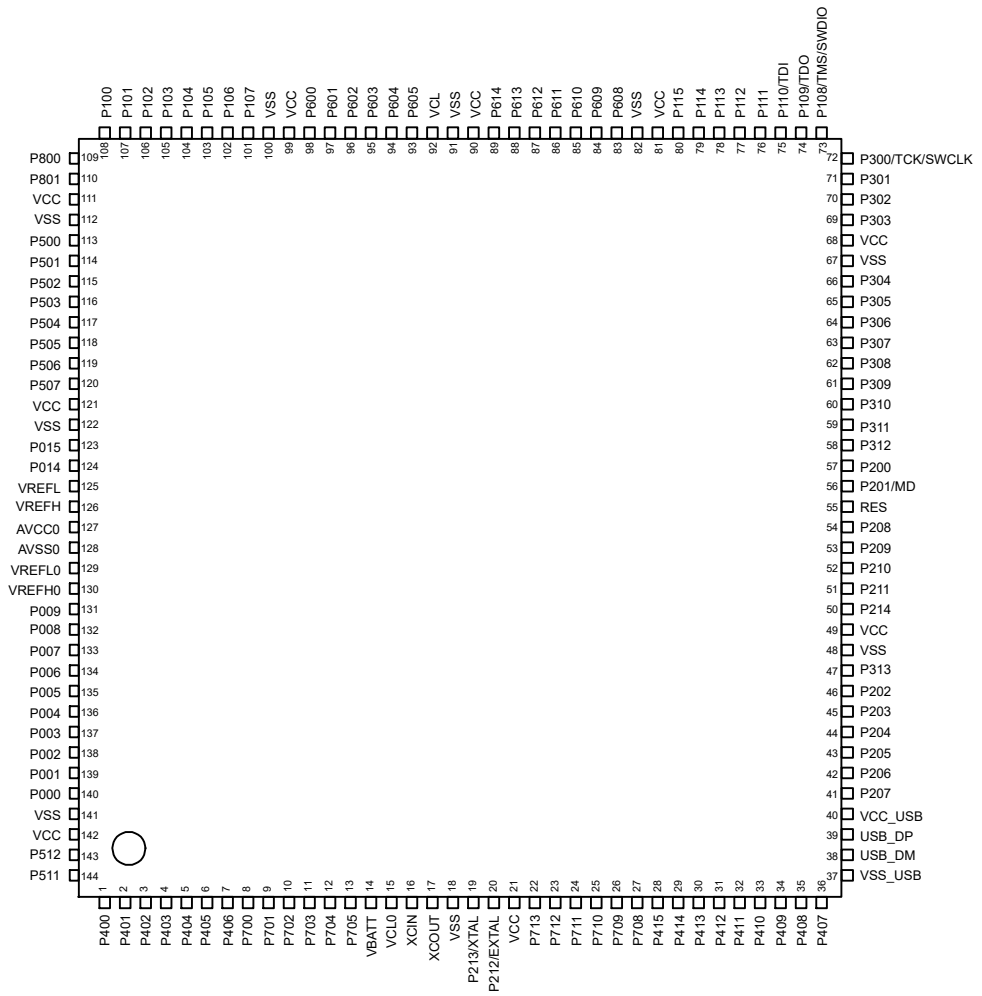



**Figure 1.3 Pin assignment for LQFP 144-pin**

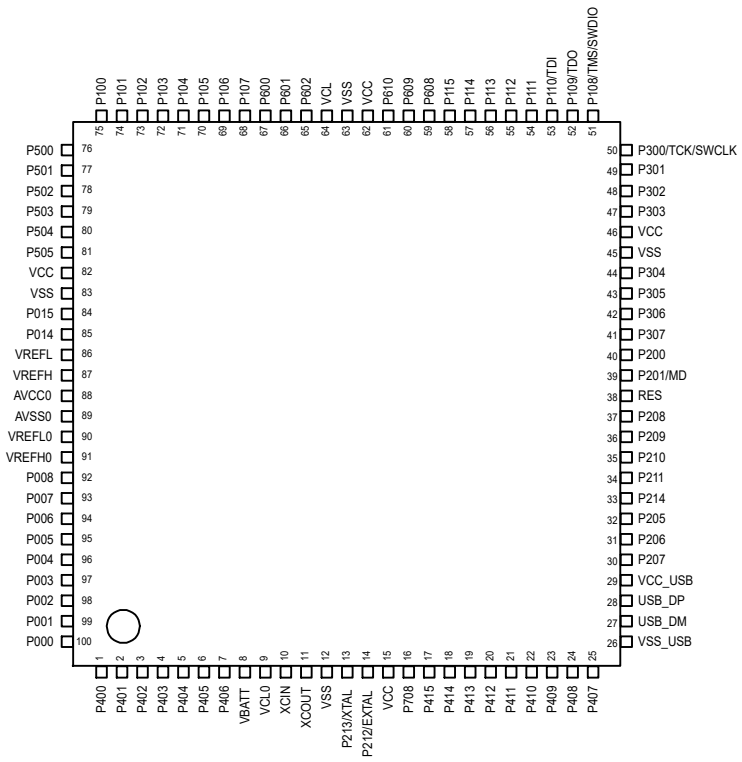



**Figure 1.4 Pin assignment for LQFP 100-pin**

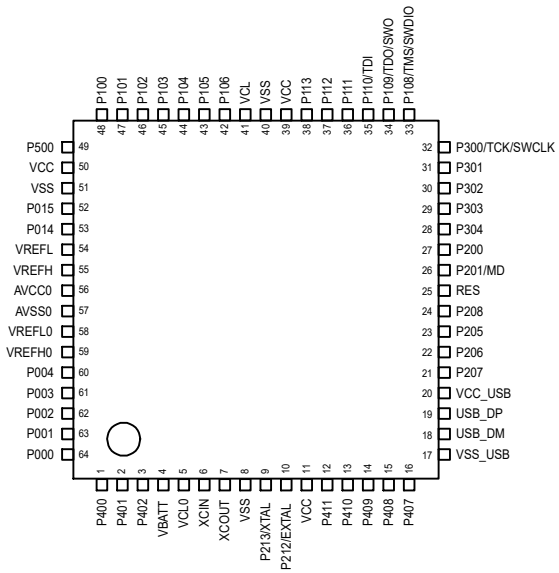



**Figure 1.5 Pin assignment for LQFP 64-pin**

## 1.7 Pin Lists

**Table 1.15 Pin list (1 of 4)**

| LPQFP144 | LPQFP100 | LPQFP64 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Bus | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/OSPI/SSIE/ SDHI/MMC/EHTERC(MII,RMII) | GPT/AGT/RTC | ADC12/DAC12 | CTSU |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | — | P400 | — | IRQ0 | SCK4/SCK7/SCL0_A/AUDIO_CLK/ET0_WOL/ ET0_WOL | GTIOC6A/AGTIO1 | ADTRG1 | — |
| 2 | 2 | 2 | — | P401 | — | IRQ5-DS | CTS4_RTS4/TXD7/SDA0_A/CTX0/ET0_MDC/ ET0_MDC | GTETRGA/GTIOC6B | — | — |
| 3 | 3 | 3 | CACREF | P402 | — | IRQ4-DS | CTS4/RXD7/CRX0/AUDIO_CLK/ET0_MDIO/ ET0_MDIO | AGTIO0/AGTIO1/AGTIO2/ AGTIO3/RTCIC0 | — | — |
| 4 | 4 | — | — | P403 | — | IRQ14-DS | CTS7_RTS7/SSIBCK0_A/ET0_LINKSTA/ ET0_LINKSTA | GTIOC3A/AGTIO0/AGTIO1/ AGTIO2/AGTIO3/RTCIC1 | — | — |
| 5 | 5 | — | — | P404 | — | IRQ15-DS | CTS7/SSILRCK0_A/ET0_EXOUT/ET0_EXOUT | GTIOC3B/AGTIO0_G/AGTIO1/ AGTIO2/AGTIO3/RTCIC2 | — | — |
| 6 | 6 | — | — | P405 | — | — | SSITXD0_A/ET0_TX_EN/RMII0_TXD_EN_B | GTIOC1A | — | — |
| 7 | 7 | — | — | P406 | — | — | SSLA3_C/SSIRXD0_A/ET0_RX_ER/RMII0_TXD1_B | GTIOC1B/AGTO5 | — | — |
| 8 | — | — | — | P700 | — | — | MISOA_C/ET0_ETXD1/RMII0_TXD0_B | GTIOC5A/AGTO4 | — | — |
| 9 | — | — | — | P701 | — | — | MOSIA_C/ET0_ETXD0/REF50CK0_B | GTIOC5B/AGTO3 | — | — |
| 10 | — | — | — | P702 | — | — | RSPCKA_C/ET0_ERXD1/RMII0_RXD0_B | GTIOC6A/AGTO2 | — | — |
| 11 | — | — | — | P703 | — | — | SSLA0_C/ET0_ERXD0/RMII0_RXD1_B | GTIOC6B/AGTO1 | — | — |
| 12 | — | — | — | P704 | — | — | SSLA1_C/CTX0/ET0_RX_CLK/RMII0_RX_ER_B | AGTO0 | — | — |
| 13 | — | — | — | P705 | — | — | CTS3/SSLA2_C/CRX0/ET0_CRS/RMII0_CRS_DV_B | AGTIO0 | — | — |
| 14 | 8 | 4 | VBATT | — | — | — | — | — | — | — |
| 15 | 9 | 5 | VCL0 | — | — | — | — | — | — | — |
| 16 | 10 | 6 | XCIN | — | — | — | — | — | — | — |
| 17 | 11 | 7 | XCOUT | — | — | — | — | — | — | — |
| 18 | 12 | 8 | VSS | — | — | — | — | — | — | — |
| 19 | 13 | 9 | XTAL | P213 | — | IRQ2 | TXD1 | GTETRGC/GTIOC0A/AGTEE2 | ADTRG1 | — |
| 20 | 14 | 10 | EXTAL | P212 | — | IRQ3 | RXD1 | GTETRGD/GTIOC0B/AGTEE1 | — | — |
| 21 | 15 | 11 | VCC | — | — | — | — | — | — | — |
| 22 | — | — | — | P713 | — | — | — | GTIOC2A/AGTOA0 | — | TS17 |
| 23 | — | — | — | P712 | — | — | — | GTIOC2B/AGTOB0 | — | TS16 |
| 24 | — | — | — | P711 | — | — | CTS1_RTS1/ET0_TX_CLK | AGTEE0 | — | TS15 |
| 25 | — | — | — | P710 | — | — | SCK1/ET0_TX_ER | — | — | TS14 |
| 26 | — | — | — | P709 | — | IRQ10 | TXD1/ET0_ETXD2 | — | — | TS13 |
| 27 | 16 | — | CACREF | P708 | — | IRQ11 | RXD1/SSLB3_B/AUDIO_CLK/ET0_ETXD3 | — | — | TS12 |
| 28 | 17 | — | — | P415 | — | IRQ8 | SSLB2_B/USB_VBUSEN/SD0CD/ET0_TX_EN/ RMII0_TXD_EN_A | GTIOC0A/AGTIO4 | — | TS11 |
| 29 | 18 | — | — | P414 | — | IRQ9 | CTS0/SSLB1_B/SD0WP/ET0_RX_ER/ RMII0_TXD1_A | GTIOC0B/AGTIO5 | — | TS10 |
| 30 | 19 | — | — | P413 | — | — | CTS0_RTS0/SSLB0_B/SD0CLK_A/ET0_ETXD1/ RMII0_TXD0_A | GTOUUP/AGTEE3 | — | TS09 |
| 31 | 20 | — | — | P412 | — | — | SCK0/CTS3/RSPCKB_B/SD0CMD_A/ET0_ETXD0/ REF50CK0_A | GTOULO/AGTEE1 | — | TS08 |
| 32 | 21 | 12 | — | P411 | — | IRQ4 | TXD0/CTS3_RTS3/MOSIB_B/SD0DAT0_A/ ET0_ERXD1/RMII0_RXD0_A | GTOVUP/GTIOC9A/AGTOA1 | — | TS07 |
| 33 | 22 | 13 | — | P410 | — | IRQ5 | RXD0/SCK3/MISOB_B/SD0DAT1_A/ET0_ERXD0/ RMII0_RXD1_A | GTOVLO/GTIOC9B/AGTOB1 | — | TS06 |
| 34 | 23 | 14 | — | P409 | — | IRQ6 | TXD3/USB_EXICEN/ET0_RX_CLK/RMII0_RX_ER_A | GTOWUP/AGTOA2 | — | TS05 |
| 35 | 24 | 15 | — | P408 | — | IRQ7 | CTS4/RXD3/SCL0_B/USB_ID/ET0_CRS/ RMII0_CRS_DV_A | GTOWLO/GTIOC6B/AGTOB2 | — | TS04 |
| 36 | 25 | 16 | — | P407 | — | — | CTS4_RTS4/SDA0_B/SSLA3_A/USB_VBUS/ ET0_EXOUT/ET0_EXOUT | GTIOC6A/AGTIO0/RTCOUT | ADTRG0 | TS03 |
| 37 | 26 | 17 | VSS_USB | — | — | — | — | — | — | — |
| 38 | 27 | 18 | USB_DM | — | — | — | — | — | — | — |
| 39 | 28 | 19 | USB_DP | — | — | — | — | — | — | — |
| 40 | 29 | 20 | VCC_USB | — | — | — | — | — | — | — |

**Table 1.15 Pin list (2 of 4)**

| LPQFP144 | LPQFP100 | LPQFP64 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Bus | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/OSPI/SSIE/ SDHI/MMC/EHTERC(MII,RMII) | GPT/AGT/RTC | ADC12/DAC12 | CTSU |
|---|---|---|---|---|---|---|---|---|---|---|
| 41 | 30 | 21 | — | P207 | A17 | — | TXD4/SSLA2_A/QSSL | — | — | TSCAP |
| 42 | 31 | 22 | — | P206 | WAIT | IRQ0-DS | RXD4/CTS9/SDA1_B/SSLA1_A/USB_VBUSEN/ SSIDATA0_C/SD0DAT2_A/ET0_LINKSTA/ ET0_LINKSTA | GTIU | — | TS02 |
| 43 | 32 | 23 | CLKOUT | P205 | A16 | IRQ1-DS | TXD4/CTS9_RTS9/SCL1_B/SSLA0_A/ USB_OVRCURA-DS/SSILRCK0_C/SD0DAT3_A/ ET0_WOL/ET0_WOL | GTIV/GTIOC4A/AGTO1 | — | TS01 |
| 44 | — | — | CACREF | P204 | A18 | — | SCK4/SCK9/RSPCKA_A/USB_OVRCURB-DS/ SSIBCK0_C/SD0DAT4_A/ET0_RX_DV | GTIW/GTIOC4B/AGTIO1 | — | TS00 |
| 45 | — | — | — | P203 | A19 | IRQ2-DS | CTS2_RTS2/TXD9/MOSIA_A/CTX0/SD0DAT5_A/ ET0_COL | GTIOC5A/AGTOA3 | — | TS18 |
| 46 | — | — | — | P202 | WR1/BC1 | IRQ3-DS | SCK2/RXD9/MISOA_A/CRX0/SD0DAT6_A/ ET0_ERXD2 | GTIOC5B/AGTOB3 | — | TS19 |
| 47 | — | — | — | P313 | A20 | — | SD0DAT7_A/ET0_ERXD3 | — | — | — |
| 48 | — | — | VSS | — | — | — | — | — | — | — |
| 49 | — | — | VCC | — | — | — | — | — | — | — |
| 50 | 33 | — | TCLK | P214 | — | — | QSPCLK/SD0CLK_B/ET0_MDC/ET0_MDC | GTIU/AGTO5 | — | — |
| 51 | 34 | — | TDATA0 | P211 | CS7 | — | QIO0/SD0CMD_B/ET0_MDIO/ET0_MDIO | GTIV/AGTOA5 | — | — |
| 52 | 35 | — | TDATA1 | P210 | CS6 | — | QIO1/SD0CD/ET0_WOL/ET0_WOL | GTIW/AGTOB5 | — | — |
| 53 | 36 | — | TDATA2 | P209 | CS5 | — | QIO2/SD0WP/ET0_EXOUT/ET0_EXOUT | GTOVUP/AGTEE5 | — | — |
| 54 | 37 | 24 | TDATA3 | P208 | CS4 | — | QIO3/SD0DAT0_B/ET0_LINKSTA/ET0_LINKSTA | GTOVLO | — | — |
| 55 | 38 | 25 | RES | — | — | — | — | — | — | — |
| 56 | 39 | 26 | MD | P201 | — | — | — | — | — | — |
| 57 | 40 | 27 | — | P200 | — | NMI | — | — | — | — |
| 58 | — | — | — | P312 | CS3 | — | CTS3_RTS3 | AGTOA1 | — | — |
| 59 | — | — | — | P311 | CS2 | — | SCK3 | AGTOB1 | — | — |
| 60 | — | — | — | P310 | A15 | — | TXD3/QIO3 | AGTEE1 | — | — |
| 61 | — | — | — | P309 | A14 | — | RXD3/QIO2 | AGTOA4 | — | — |
| 62 | — | — | — | P308 | A13 | — | CTS6/CTS3/QIO1 | AGTOB4 | — | — |
| 63 | 41 | — | — | P307 | A12 | — | CTS6_RTS6/QIO0 | GTOUUP_D/AGTEE4 | — | — |
| 64 | 42 | — | — | P306 | A11 | — | SCK6/QSSL | GTOULO_D/AGTOA2 | — | — |
| 65 | 43 | — | — | P305 | A10 | IRQ8 | TXD6/QSPCLK | GTOWUP/AGTOB2 | — | — |
| 66 | 44 | 28 | — | P304 | A9 | IRQ9 | RXD6 | GTOWLO/GTIOC7A/AGTEE2 | — | — |
| 67 | 45 | — | VSS | — | — | — | — | — | — | — |
| 68 | 46 | — | VCC | — | — | — | — | — | — | — |
| 69 | 47 | 29 | — | P303 | A8 | — | CTS9 | GTIOC7B | — | — |
| 70 | 48 | 30 | — | P302 | A7 | IRQ5 | TXD2/SSLA3_B | GTOUUP/GTIOC4A | — | — |
| 71 | 49 | 31 | — | P301 | A6 | IRQ6 | RXD2/CTS9_RTS9/SSLA2_B | GTOULO/GTIOC4B/AGTIO0 | — | — |
| 72 | 50 | 32 | TCK/SWCLK | P300 | — | — | SSLA1_B | GTOUUP/GTIOC0A | — | — |
| 73 | 51 | 33 | TMS/SWDIO | P108 | — | — | CTS9_RTS9/SSLA0_B | GTOULO/GTIOC0B/AGTOA3 | — | — |
| 74 | 52 | 34 | TDO/SWO/CLKOUT | P109 | — | — | TXD9/MOSIA_B/CTX1 | GTOVUP/GTIOC1A/AGTOB3 | — | — |
| 75 | 53 | 35 | TDI | P110 | — | IRQ3 | CTS2_RTS2/RXD9/MISOA_B/CRX1 | GTOVLO/GTIOC1B/AGTEE3 | — | — |
| 76 | 54 | 36 | — | P111 | A5 | IRQ4 | SCK2/SCK9/RSPCKA_B | GTIOC3A/AGTOA5 | — | — |
| 77 | 55 | 37 | — | P112 | A4 | — | TXD2/SCK1/SSLA0_B/QSSL/OM_CS1/SSISCK0_B | GTIOC3B/AGTOB5 | — | — |
| 78 | 56 | 38 | — | P113 | A3 | — | RXD2/SSILRCK0_B | GTIOC2A/AGTEE5 | — | — |
| 79 | 57 | — | — | P114 | A2 | — | CTS9/SSIRXD0_B | GTIOC2B/AGTIO5 | — | — |
| 80 | 58 | — | — | P115 | A1 | — | SSITXD0_B | GTIOC4A | — | — |
| 81 | — | — | VCC | — | — | — | — | — | — | — |
| 82 | — | — | VSS | — | — | — | — | — | — | — |
| 83 | 59 | — | — | P608 | A0/BC0 | — | — | GTIOC4B | — | — |
| 84 | 60 | — | — | P609 | CS1 | — | CTX1/OM_ECS | GTIOC5A/AGTO5 | — | — |
| 85 | 61 | — | — | P610 | CS0 | — | CTS7/CRX1/OM_CS0 | GTIOC5B/AGTO4 | — | — |

**Table 1.15 Pin list (3 of 4)**

| LPQFP144 | LPQFP100 | LPQFP64 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Bus | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/OSPI/SSIE/ SDHI/MMC/EHTERC(MII,RMII) | GPT/AGT/RTC | ADC12/DAC12 | CTSU |
|---|---|---|---|---|---|---|---|---|---|---|
| 86 | — | — | CACREF/CLKOUT | P611 | — | — | CTS7_RTS7 | AGTO3 | — | — |
| 87 | — | — | — | P612 | D8 | — | SCK7 | AGTO2 | — | — |
| 88 | — | — | — | P613 | D9 | — | TXD7 | AGTO1 | — | — |
| 89 | — | — | — | P614 | D10 | — | RXD7 | AGTO0 | — | — |
| 90 | 62 | 39 | VCC | — | — | — | — | — | — | — |
| 91 | 63 | 40 | VSS | — | — | — | — | — | — | — |
| 92 | 64 | 41 | VCL | — | — | — | — | — | — | — |
| 93 | — | — | — | P605 | D11 | — | CTS8 | GTIOC8A/AGTO4 | — | — |
| 94 | — | — | — | P604 | D12 | — | CTS9 | GTIOC8B/AGTEE4 | — | — |
| 95 | — | — | — | P603 | D13 | — | CTS9_RTS9 | GTIOC7A/AGTIO4 | — | — |
| 96 | 65 | — | — | P602 | BCLK | — | TXD9/OM_CS1 | GTIOC7B/AGTO3 | — | — |
| 97 | 66 | — | — | P601 | WR/WR0 | — | RXD9/OM_SIO2 | GTIOC6A/AGTEE3 | — | — |
| 98 | 67 | — | CACREF/CLKOUT | P600 | RD | — | SCK9/OM_SIO4 | GTIOC6B/AGTIO3 | — | — |
| 99 | — | — | VCC | — | — | — | — | — | — | — |
| 100 | — | — | VSS | — | — | — | — | — | — | — |
| 101 | 68 | — | — | P107 | D7 | — | CTS8_RTS8/OM_SIO3 | GTIOC8A/AGTOA0 | — | — |
| 102 | 69 | 42 | — | P106 | D6 | — | SCK8/SSLB3_A/OM_SIO0 | GTIOC8B/AGTOB0 | — | — |
| 103 | 70 | 43 | — | P105 | D5 | IRQ0 | TXD8/SSLB2_A/OM_SIO5 | GTETRGA/GTIOC1A/AGTO2 | — | — |
| 104 | 71 | 44 | — | P104 | D4 | IRQ1 | RXD8/SSLB1_A/QIO2/OM_DQS | GTETRGB/GTIOC1B/AGTEE2 | — | — |
| 105 | 72 | 45 | — | P103 | D3 | — | CTS0_RTS0/SSLB0_A/CTX0/QIO3/OM_SIO6 | GTOWUP/GTIOC2A/AGTIO2 | — | — |
| 106 | 73 | 46 | — | P102 | D2 | — | SCK0/RSPCKB_A/CRX0/QIO0/OM_SIO1 | GTOWLO/GTIOC2B/AGTO0 | ADTRG0 | — |
| 107 | 74 | 47 | — | P101 | D1 | IRQ1 | TXD0/CTS1_RTS1/MOSIB_A/QIO1/OM_SIO7 | GTETRGB/GTIOC5A/AGTEE0 | — | — |
| 108 | 75 | 48 | — | P100 | D0 | IRQ2 | RXD0/SCK1/MISOB_A/QSPCLK/OM_SCLK | GTETRGA/GTIOC5B/AGTIO0 | — | — |
| 109 | — | — | — | P800 | D14 | — | CTS0 | AGTOA4 | — | — |
| 110 | — | — | — | P801 | D15 | — | CTS8 | AGTOB4 | — | — |
| 111 | — | — | VCC | — | — | — | — | — | — | — |
| 112 | — | — | VSS | — | — | — | — | — | — | — |
| 113 | 76 | 49 | CACREF | P500 | — | — | CTS5/USB_VBUSEN/QSPCLK | GTIU/AGTOA0 | AN116 | — |
| 114 | 77 | — | — | P501 | — | IRQ11 | TXD5/USB_OVRCURA/QSSL | GTIV/AGTOB0 | AN117 | — |
| 115 | 78 | — | — | P502 | — | IRQ12 | CTS6/RXD5/USB_OVRCURB/QIO0 | GTIW/AGTOA2 | AN118 | — |
| 116 | 79 | — | — | P503 | — | — | CTS6_RTS6/SCK5/USB_EXICEN/QIO1 | GTETRGC/AGTOB2 | AN119 | — |
| 117 | 80 | — | — | P504 | ALE | — | SCK6/CTS5_RTS5/USB_ID/QIO2 | GTETRGD/AGTOA3 | AN120 | — |
| 118 | 81 | — | — | P505 | — | IRQ14 | RXD6/QIO3 | AGTOB3 | AN121 | — |
| 119 | — | — | — | P506 | — | IRQ15 | TXD6 | — | AN122 | — |
| 120 | — | — | — | P507 | — | — | SCK6/SCK5 | — | — | — |
| 121 | 82 | 50 | VCC | — | — | — | — | — | — | — |
| 122 | 83 | 51 | VSS | — | — | — | — | — | — | — |
| 123 | 84 | 52 | — | P015 | — | IRQ13 | — | — | AN013/DA1 | — |
| 124 | 85 | 53 | — | P014 | — | — | — | — | AN012/DA0 | — |
| 125 | 86 | 54 | VREFL | — | — | — | — | — | — | — |
| 126 | 87 | 55 | VREFH | — | — | — | — | — | — | — |
| 127 | 88 | 56 | AVCC0 | — | — | — | — | — | — | — |
| 128 | 89 | 57 | AVSS0 | — | — | — | — | — | — | — |
| 129 | 90 | 58 | VREFL0 | — | — | — | — | — | — | — |
| 130 | 91 | 59 | VREFH0 | — | — | — | — | — | — | — |
| 131 | — | — | — | P009 | — | IRQ13-DS | — | — | AN009 | — |
| 132 | 92 | — | — | P008 | — | IRQ12-DS | — | — | AN008 | — |
| 133 | 93 | — | — | P007 | — | — | — | — | AN007 | — |
| 134 | 94 | — | — | P006 | — | IRQ11-DS | — | — | AN006 | — |

**Table 1.15 Pin list (4 of 4)**

| LPQFP144 | LPQFP100 | LPQFP64 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Bus | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/OSPI/SSIE/ SDHI/MMC/EHTERC(MII,RMII) | GPT/AGT/RTC | ADC12/DAC12 | CTSU |
|---|---|---|---|---|---|---|---|---|---|---|
| 135 | 95 | — | — | P005 | — | IRQ10-DS | — | — | AN005 | — |
| 136 | 96 | 60 | — | P004 | — | IRQ9-DS | — | — | AN004 | — |
| 137 | 97 | 61 | — | P003 | — | — | — | — | AN003 | — |
| 138 | 98 | 62 | — | P002 | — | IRQ8-DS | — | — | AN002/AN102 | — |
| 139 | 99 | 63 | — | P001 | — | IRQ7-DS | — | — | AN001/AN101 | — |
| 140 | 100 | 64 | — | P000 | — | IRQ6-DS | — | — | AN000/AN100 | — |
| 141 | — | — | VSS | — | — | — | — | — | — | — |
| 142 | — | — | VCC | — | — | — | — | — | — | — |
| 143 | — | — | — | P512 | — | IRQ14 | TXD4/SCL1_A/CTX1 | GTIOC0A | — | — |
| 144 | — | — | — | P511 | — | IRQ15 | RXD4/SDA1_A/CRX1 | GTIOC0B | — | — |

Note: Several pin names have the added suffix of _A, _B, and _C. The suffix can be ignored when assigning functionality.

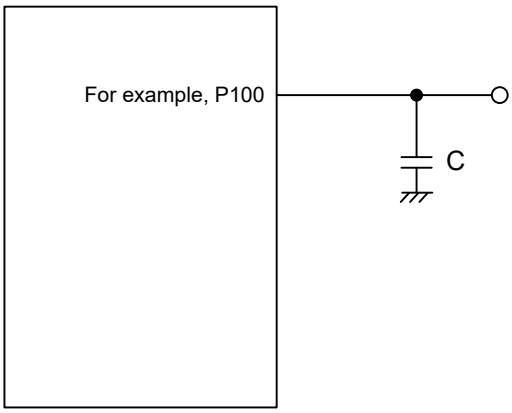
# 2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.




$V_{OH}$ = VCC × 0.7, $V_{OL}$ = VCC × 0.3
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3
Load capacitance C = 30 pF

**Figure 2.1 Input or output timing measurement conditions**

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VCC, VCC_USB*2 | –0.3 to +4.0 | V |
| VBATT power supply voltage | VBATT | –0.3 to +4.0 | V |
| Input voltage (except for 5 V-tolerant ports*1) | $V_{in}$ | –0.3 to VCC + 0.3 | V |
| Input voltage (5 V-tolerant ports*1) | $V_{in}$ | –0.3 to + VCC + 4.0 (max. 5.8) | V |
| Reference power supply voltage | VREFH/VREFH0 | –0.3 to VCC + 0.3 | V |
| Analog power supply voltage | AVCC0*2 | –0.3 to +4.0 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to AVCC0 + 0.3 | V |
| Operating temperature*3 *4 | $T_{opr}$ | –40 to +105 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, and P708 to P713 are 5 V tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

**Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.**

**Table 2.2 Recommended operating conditions**

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC | When USB is not used | 2.7 | — | 3.6 | V |
| | | When USB is used | 3.0 | — | 3.6 | V |
| | VSS | | — | 0 | — | V |
| USB power supply voltages | VCC_USB | | — | VCC | — | V |
| | VSS_USB | | — | 0 | — | V |
| VBATT power supply voltage | VBATT | | 1.8 | — | 3.6 | V |
| Analog power supply voltages | AVCC0*1 | | — | VCC | — | V |
| | AVSS0 | | — | 0 | — | V |

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

**Table 2.3 DC characteristics**

Conditions: Products with operating temperature ($T_a$) -40 to +105°C

| Parameter | Symbol | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Permissible junction temperature | $T_j$ | — | 125 | °C | High-speed mode<br>Low-speed mode<br>Subosc-speed mode |

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

### 2.2.2 I/O $V_{IH}$, $V_{IL}$

**Table 2.4 I/O $V_{IH}$, $V_{IL}$ (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL (external clock input), WAIT, SPI (except RSPCK), OSPI (except ECS) | $V_{IH}$ | VCC × 0.8 | — | — | V |
| | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | D00 to D15 | $V_{IH}$ | VCC × 0.7 | — | — | |
| | | | $V_{IL}$ | — | — | VCC × 0.3 | |
| | | ETHERC | $V_{IH}$ | 2.3 | — | — | |
| | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | IIC (SMBus) | $V_{IH}$ | 2.1 | — | VCC + 3.6 (max 5.8) | |
| | | | $V_{IL}$ | — | — | 0.8 | |

**Table 2.4 I/O $V_{IH}$, $V_{IL}$ (2 of 2)**

| Parameter | | | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | Peripheral function pin | IIC (except for SMBus) | | | $V_{IH}$ | VCC × 0.7 | — | VCC + 3.6 (max 5.8) | V |
| | | | | | $V_{IL}$ | — | — | VCC × 0.3 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | — | — | |
| | | 5 V-tolerant ports*1 *5 | | | $V_{IH}$ | VCC × 0.8 | — | VCC + 3.6 (max 5.8) | |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | — | — | |
| | | RTCIC0, RTCIC1, RTCIC2 | When using the Battery Backup Function | When VBATT power supply is selected | $V_{IH}$ | $V_{BATT}$ × 0.8 | — | $V_{BATT}$ + 0.3 | |
| | | | | | $V_{IL}$ | — | — | $V_{BATT}$ × 0.2 | |
| | | | | | $\Delta V_T$ | $V_{BATT}$ × 0.05 | — | — | |
| | | | | When VCC power supply is selected | $V_{IH}$ | VCC × 0.8 | — | Higher voltage either VCC + 0.3 V or $V_{BATT}$ + 0.3 V | |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | — | — | |
| | | | When not using the Battery Backup Function | | $V_{IH}$ | VCC × 0.8 | — | VCC + 0.3 | |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | — | — | |
| | | Other input pins*2 | | | $V_{IH}$ | VCC × 0.8 | — | — | |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | — | — | |
| | Ports | 5 V-tolerant ports*3 *5 | | | $V_{IH}$ | VCC × 0.8 | — | VCC + 3.6 (max 5.8) | V |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |
| | | Other input pins*4 | | | $V_{IH}$ | VCC × 0.8 | — | — | |
| | | | | | $V_{IL}$ | — | — | VCC × 0.2 | |

Note 1. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 22 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 21 pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

### 2.2.3 I/O $I_{OH}$, $I_{OL}$

**Table 2.5 I/O $I_{OH}$, $I_{OL}$ (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (average value per pin) | Ports P000 to P009, P014, P015, P201 | — | $I_{OH}$ | — | — | –2.0 | mA |
| | | | $I_{OL}$ | — | — | 2.0 | mA |
| | Ports P205, P206, P407 to P415, P708 to P713 (total 17 pins) | Low drive*1 | $I_{OH}$ | — | — | –2.0 | mA |
| | | | $I_{OL}$ | — | — | 2.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –20 | mA |
| | | | $I_{OL}$ | — | — | 20 | mA |
| | Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins) | Low drive*1 | $I_{OH}$ | — | — | –2.0 | mA |
| | | | $I_{OL}$ | — | — | 2.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –16 | mA |
| | | | $I_{OL}$ | — | — | 16 | mA |
| | | High spped high drive*4 | $I_{OH}$ | — | — | –20 | mA |
| | | | $I_{OL}$ | — | — | 20 | mA |
| | Other output pins*5 | Low drive*1 | $I_{OH}$ | — | — | –2.0 | mA |
| | | | $I_{OL}$ | — | — | 2.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –16 | mA |
| | | | $I_{OL}$ | — | — | 16 | mA |

**Table 2.5 I/O $I_{OH}$, $I_{OL}$ (2 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (max value per pin) | Ports P000 to P009, P014, P015, P201 | — | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | Ports P205, P206, P407 to P415, P708 to P713 (total 17 pins) | Low drive*1 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –8.0 | mA |
| | | | $I_{OL}$ | — | — | 8.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –40 | mA |
| | | | $I_{OL}$ | — | — | 40 | mA |
| | Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins) | Low drive*1 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –8.0 | mA |
| | | | $I_{OL}$ | — | — | 8.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –32 | mA |
| | | | $I_{OL}$ | — | — | 32 | mA |
| | | High spped high drive*4 | $I_{OH}$ | — | — | –40 | mA |
| | | | $I_{OL}$ | — | — | 40 | mA |
| | Other output pins*5 | Low drive*1 | $I_{OH}$ | — | — | –4.0 | mA |
| | | | $I_{OL}$ | — | — | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | — | — | –8.0 | mA |
| | | | $I_{OL}$ | — | — | 8.0 | mA |
| | | High drive*3 | $I_{OH}$ | — | — | –32 | mA |
| | | | $I_{OL}$ | — | — | 32 | mA |
| Permissible output current (maxvalue of total of all pins) | Maximum of all output pins | | $\Sigma I_{OH\ (max)}$ | — | — | –80 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | — | — | 80 | mA |

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. This is the value when high speed high driving ability is selected in the Port Drive Capability in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. Except for P200, which is an input port.

**Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.**

### 2.2.4 I/O $V_{OH}$, $V_{OL}$, and Other Characteristics

**Table 2.6 I/O $V_{OH}$, $V_{OL}$, and other characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Output voltage | IIC | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 3.0 mA |
| | | $V_{OL}$ | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | IIC*1 | $V_{OL}$ | — | — | 0.4 | | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | $V_{OL}$ | — | 0.4 | — | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| | ETHERC | $V_{OH}$ | VCC – 0.5 | — | — | | $I_{OH}$ = –1.0 mA |
| | | $V_{OL}$ | — | — | 0.4 | | $I_{OL}$ = 1.0 mA |
| | Ports P205, P206, P407 to P415, P708 to P713 (total of 17 pins)*2 | $V_{OH}$ | VCC – 1.0 | — | — | | $I_{OH}$ = –20 mA<br>VCC = 3.3 V |
| | | $V_{OL}$ | — | — | 1.0 | | $I_{OL}$ = 20 mA<br>VCC = 3.3 V |
| | Other output pins | $V_{OH}$ | VCC – 0.5 | — | — | | $I_{OH}$ = –1.0 mA |
| | | $V_{OL}$ | — | — | 0.5 | | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES | $\|I_{in}\|$ | — | — | 5.0 | μA | $V_{in}$ = 0 V<br>$V_{in}$ = 5.5 V |
| | Port P200 | | — | — | 1.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | 5 V-tolerant ports | $\|I_{TSI}\|$ | — | — | 5.0 | μA | $V_{in}$ = 0 V<br>$V_{in}$ = 5.5 V |
| | Other ports (except for port P200) | | — | — | 1.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Input pull-up MOS current | Ports P0 to P8 | $I_p$ | –300 | — | –10 | μA | VCC = 2.7 to 3.6 V<br>$V_{in}$ = 0 V |
| Input capacitance | USB_DP, USB_DM, and ports P014, P015, P400, P401, P511, P512 | $C_{in}$ | — | — | 16 | pF | Vbias = 0 V<br>Vamp = 20 mV<br>f = 1 MHz<br>Ta = 25°C |
| | Other input pins | | — | — | 8 | | |

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

## 2.2.5 Operating and Standby Current

**Table 2.7 Operating and standby current (1 of 2)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed mode | Maximum*2 | | $I_{CC}$*3 | — | — | 115 | mA | ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz BCLK = 100 MHz |
| | | CoreMark®*5, *6 | | | — | 20 | — | | |
| | | Normal mode | All peripheral clocks enabled, while (1) code executing from flash*4 | | — | 30 | — | | |
| | | | All peripheral clocks disabled, while (1) code executing from flash*5, *6 | | — | 17 | — | | |
| | | Sleep mode*5, *6 | | | — | 10 | 47 | | |
| | | Increase during BGO operation | Data flash P/E | | — | 6 | — | | |
| | | | Code flash P/E | | — | 8 | — | | |
| | Low-speed mode*5 *9 | | | | — | 1.9 | — | | ICLK = 1 MHz |
| | Subosc-speed mode*5 *10 | | | | — | 1.7 | — | | ICLK = 32.768 kHz |
| | Software Standby mode | | SNZCR.RXDREQEN = 1 | | — | — | 34 | | — |
| | | | SNZCR.RXDREQEN = 0 | | — | 1.6 | — | | — |
| | Deep Software Standby mode | Power supplied to Standby SRAM and USB resume detecting unit | | | — | 16.9 | 131 | μA | — |
| | | Power not supplied to SRAM or USB resume detecting unit | Power-on reset circuit low power function disabled | | — | 11.8 | 31 | | — |
| | | | Power-on reset circuit low power function enabled | | — | 4.8 | 21 | | — |
| | | Increase when the RTC and AGT are operating | When the low-speed on-chip oscillator (LOCO) is in use | | — | 4.0 | — | | — |
| | | | When a crystal oscillator for low clock loads is in use | | — | 1.2 | — | | — |
| | | | When a crystal oscillator for standard clock loads is in use | | — | 1.5 | — | | — |
| | RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | | — | 0.9 | — | | $V_{BATT}$ = 1.8 V, VCC = 0 V |
| | | | | | — | 1.3 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | | | When a crystal oscillator for standard clock loads is in use | | — | 1.0 | — | | $V_{BATT}$ = 1.8 V, VCC = 0 V |
| | | | | | — | 1.7 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | Inrush current on returning from deep software standby mode | | Inrush current*7 | $I_{RUSH}$ | — | 160 | — | mA | |
| | | | Energy of inrush current*7 | $E_{RUSH}$ | — | 1.0 | — | μC | |
| Analog power supply current | During 12-bit A/D conversion | | | $AI_{CC}$ | — | 0.8 | 1.1 | mA | — |
| | Temperature sensor | | | | — | 0.1 | 0.2 | mA | — |
| | During D/A conversion (per unit) | | Without AMP output | | — | 0.1 | 0.2 | mA | — |
| | | | With AMP output | | — | 0.6 | 1.1 | mA | — |
| | Waiting for A/D, D/A conversion (all units) | | | | — | 0.9 | 1.6 | mA | — |
| | ADC12, DAC12 in standby modes (all units)*8 | | | | — | 2 | 8 | μA | — |

**Table 2.7 Operating and standby current (2 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Reference power supply current (VREFH0) | During 12-bit A/D conversion (unit 0) | | $AI_{REFH0}$ | — | 70 | 120 | μA | — |
| | Waiting for 12-bit A/D conversion (unit 0) | | | — | 0.07 | 0.5 | μA | — |
| | ADC12 in standby modes (unit 0) | | | — | 0.07 | 0.5 | μA | — |
| Reference power supply current (VREFH) | During 12-bit A/D conversion (unit 1) | | $AI_{REFH}$ | — | 70 | 120 | μA | — |
| | During D/A conversion (per unit) | Without AMP output | | — | 0.1 | 0.4 | mA | — |
| | | With AMP ouput | | — | 0.1 | 0.4 | mA | — |
| | Waiting for 12-bit A/D (unit 1), D/A (all units) conversion | | | — | 0.07 | 0.8 | μA | — |
| | ADC12 unit 1 in standby modes | | | — | 0.07 | 0.8 | μA | — |
| USB operating current | Low speed | USB | $I_{CCUSBLS}$ | — | 3.5 | 6.5 | mA | VCC_USB |
| | Full speed | USB | $I_{CCUSBFS}$ | — | 4.0 | 10.0 | mA | VCC_USB |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. $I_{CC}$ depends on f (ICLK) as follows.
$I_{CC}$ Max. = 0.37 × f + 42 (max. operation in high-speed mode)
$I_{CC}$ Typ. = 0.07 × f + 3.6 (normal operation in high-speed mode, all peripheral clocks disabled)
$I_{CC}$ Typ. = 0.2 × f + 1.7 (low-speed mode)
$I_{CC}$ Max. = 0.03 × f + 42 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 7. Reference value
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D converter 1 module stop bit) are in the module-stop state.
Note 9. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 10. BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.

**Table 2.8 Coremark and normal mode current**

| Parameter | | | Symbol | Typ | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Supply Current*1 | Coremark | | $I_{CC}$ | 99 | μA/MHz | ICLK = 200MHz<br>PCLKA =<br>PCLKB =<br>PCLKC =<br>PCLKD =<br>FCLK =<br>BCLK =<br>3.125MHz |
| | Normal mode | All peripheral clocks disabled, cache on, while (1) code executing from flash*2 | | 95 | | |
| | | All peripheral clocks disabled, cache off, while (1) code executing from flash*2 | | 82 | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

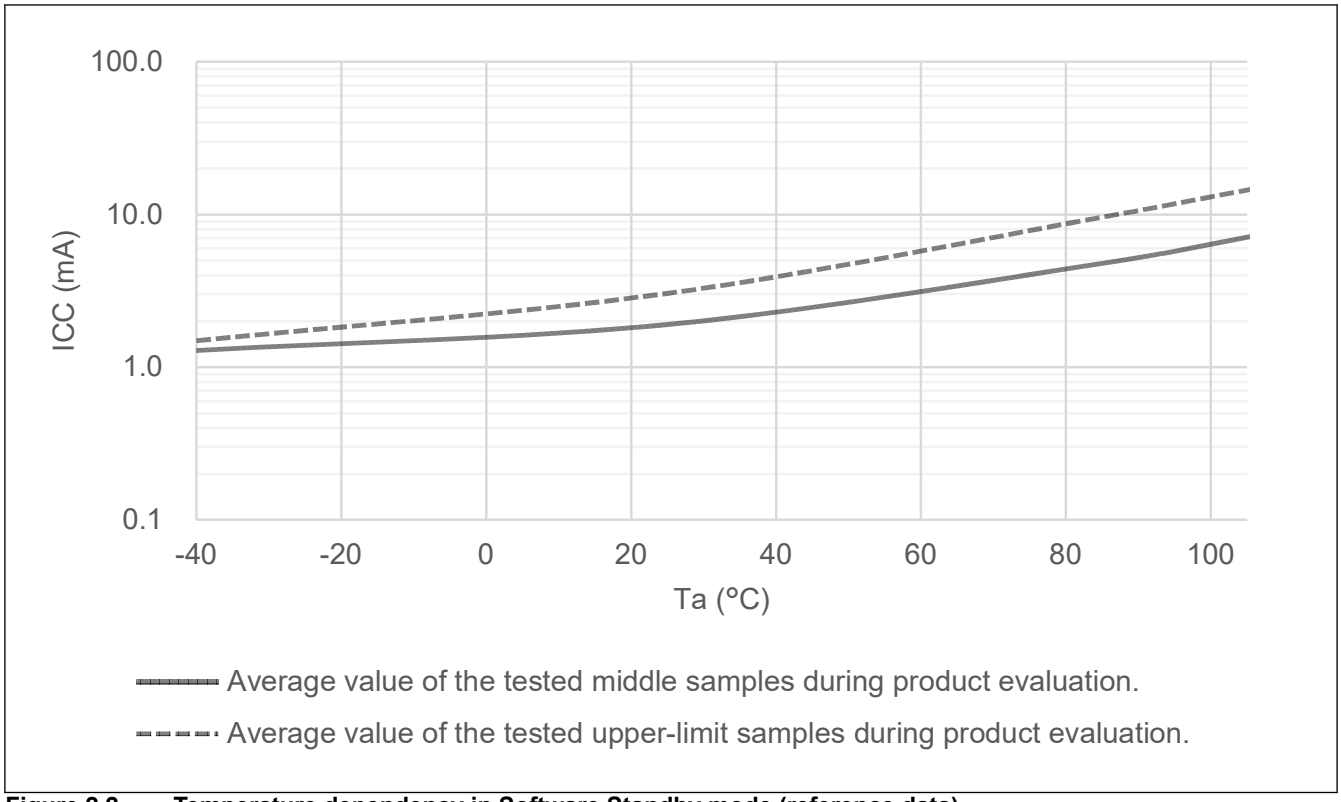



**Figure 2.2 Temperature dependency in Software Standby mode (reference data)**

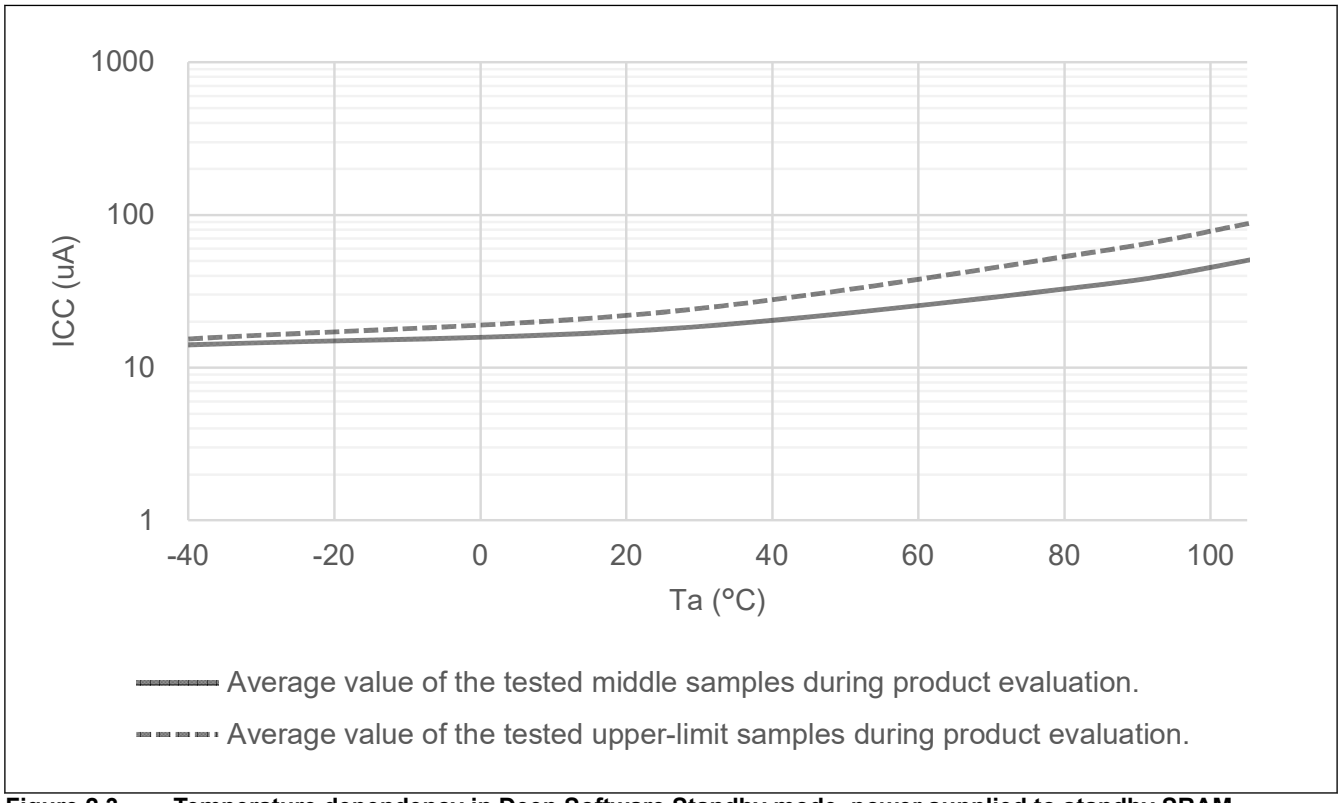



**Figure 2.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)**

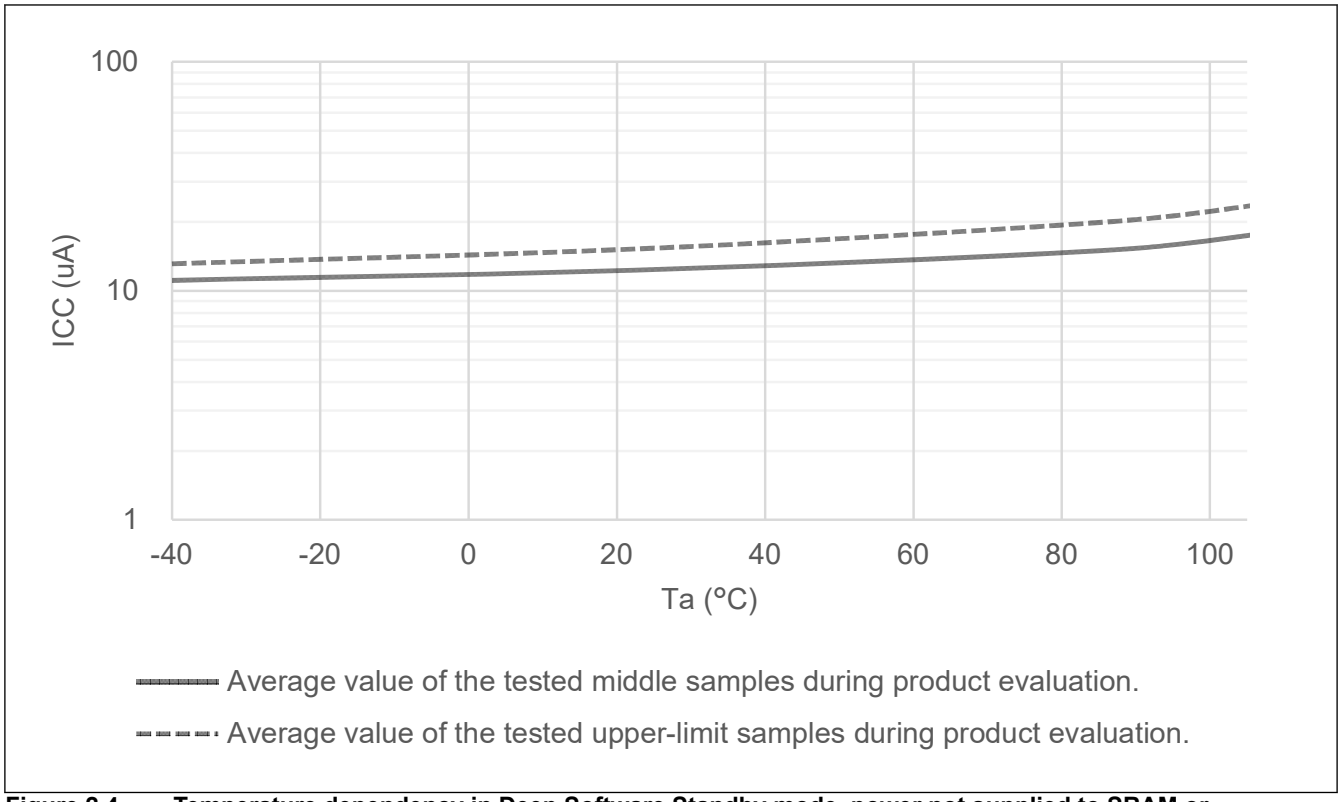



**Figure 2.4 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)**

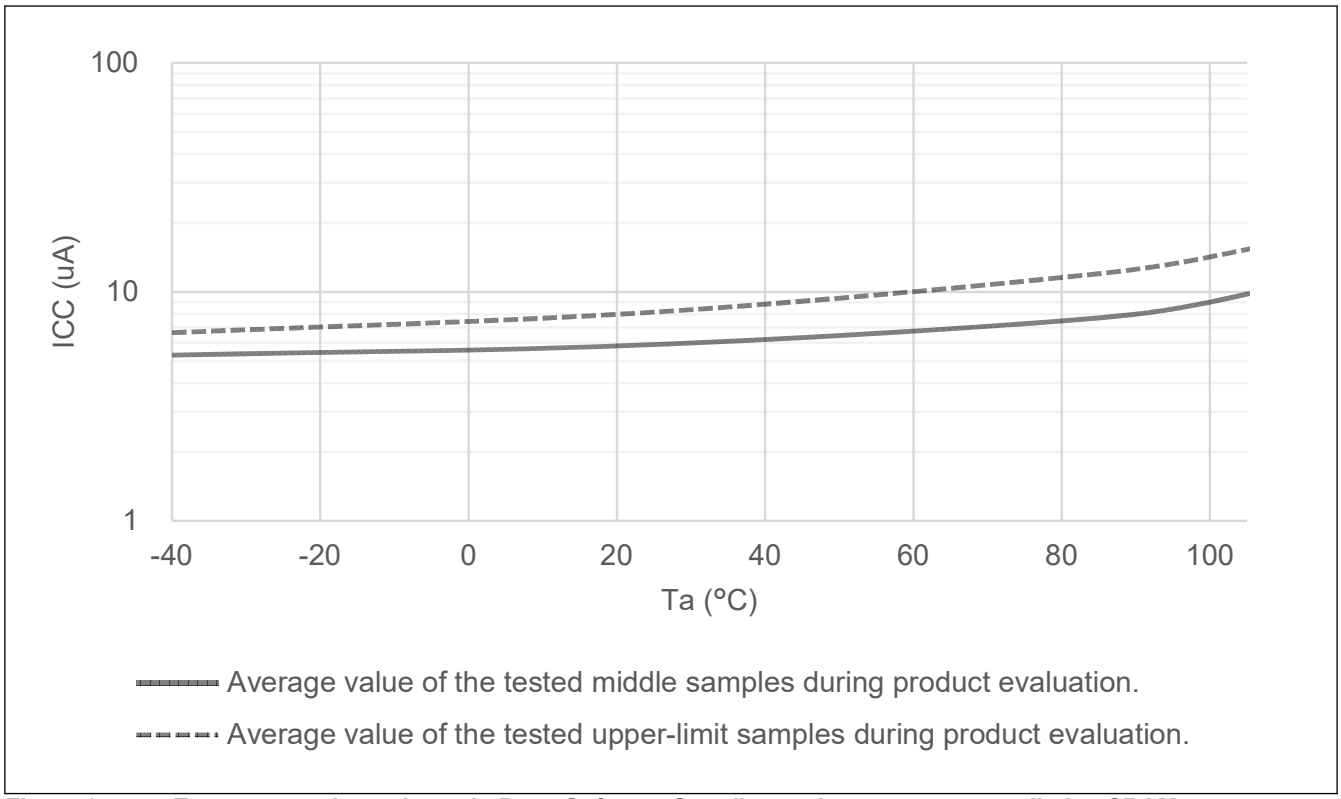



**Figure 2.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)**

### 2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.9 Rise and fall gradient characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.0084 | — | 20 | ms/V | — |
| | Voltage monitor 0 reset enabled at startup | | 0.0084 | — | — | | — |
| | SCI/USB boot mode*1 | | 0.0084 | — | 20 | | — |
| VCC falling gradient*2 | | SfVCC | 0.0084 | — | — | ms/V | — |

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

**Table 2.10 Rising and falling gradient and ripple frequency characteristics**

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Allowable ripple frequency | $f_{r\ (VCC)}$ | — | — | 10 | kHz | Figure 2.6<br>$V_{r\ (VCC)} \leq VCC \times 0.2$ |
| | | — | — | 1 | MHz | Figure 2.6<br>$V_{r\ (VCC)} \leq VCC \times 0.08$ |
| | | — | — | 10 | MHz | Figure 2.6<br>$V_{r\ (VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | dt/dVCC | 1.0 | — | — | ms/V | When VCC change exceeds VCC ±10% |

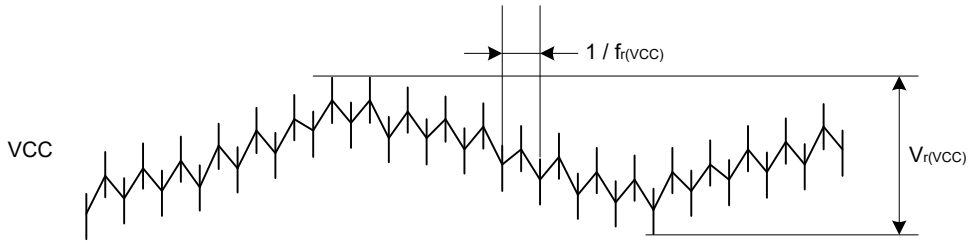



**Figure 2.6 Ripple waveform**

### 2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 2.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)

  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ ($I_{OL}$ × $V_{OL}$) /Voltage + Σ (|$I_{OH}$| × |VCC – $V_{OH}$|) /Voltage
- Dynamic current of IO = Σ IO ($C_{in}$ + $C_{load}$) × IO switching frequency × Voltage
  - $C_{in}$: Input capacitance
  - $C_{load}$: Output capacitance

Regarding θja and Ψjt, refer to Table 2.11.

**Table 2.11 Thermal Resistance**

| Parameter | Package | Symbol | Value*1 | Unit | Test conditions |
|---|---|---|---|---|---|
| Thermal Resistance | 64-pin LQFP (PLQP0064KB-C) | θja | 38.0 | °C/W | JESD 51-2 and 51-7 compliant |
| | 100-pin LQFP (PLQP0100KB-B) | | 35.0 | | |
| | 144-pin LQFP (PLQP0144KA-B) | | 33.0 | | |
| | 64-pin LQFP (PLQP0064KB-C) | Ψjt | 0.80 | °C/W | JESD 51-2 and 51-7 compliant |
| | 100-pin LQFP (PLQP0100KB-B) | | 0.76 | | |
| | 144-pin LQFP (PLQP0144KA-B) | | 0.63 | | |

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

### 2.2.7.1 Calculation guide of $I_{CC}$max

Table 2.12 shows the power consumption of each unit.

**Table 2.12 Power consumption of each unit (1 of 2)**

| Dynamic current/ Leakage current | MCU Domain | Category | Item | Frequency [MHz] | Current [uA/MHz] | Current*1 [mA] |
|---|---|---|---|---|---|---|
| Leakage current | Analog | LDO and Leak*2 | Ta = 75 °C*3 | — | — | 21.22 |
| | | | Ta = 85 °C*3 | — | — | 25.22 |
| | | | Ta = 95 °C*3 | — | — | 30.22 |
| | | | Ta = 105 °C*3 | — | — | 37.42 |

**Table 2.12 Power consumption of each unit (2 of 2)**

| Dynamic current/ Leakage current | MCU Domain | Category | Item | Frequency [MHz] | Current [uA/MHz] | Current*1 [mA] |
|---|---|---|---|---|---|---|
| Dynamic current | CPU | Operation with Flash and SRAM | Coremark | 200 | 86.357 | 17.27 |
| | Peripheral Unit | Timer | GPT16 (6ch)*4 | 100 | 5.300 | 0.53 |
| | | | GPT32 (4ch)*4 | 100 | 3.946 | 0.39 |
| | | | POEG (4 Groups)*4 | 50 | 1.378 | 0.07 |
| | | | AGT (6ch)*4 | 50 | 10.095 | 0.50 |
| | | | RTC | 50 | 5.239 | 0.26 |
| | | | WDT | 50 | 0.722 | 0.04 |
| | | | IWDT | 50 | 0.267 | 0.01 |
| | | Communication interfaces | ETHERC | 100 | 7.651 | 0.77 |
| | | | USBFS | 50 | 8.788 | 0.44 |
| | | | SCI (10ch)*4 | 100 | 25.595 | 2.56 |
| | | | IIC (2ch)*4 | 50 | 3.014 | 0.15 |
| | | | CAN (2ch)*4 | 50 | 3.843 | 0.19 |
| | | | SPI (2ch)*4 | 100 | 6.770 | 0.68 |
| | | | OSPI | 50 | 32.530 | 1.63 |
| | | | QSPI | 100 | 2.587 | 0.26 |
| | | | SSIE | 50 | 3.131 | 0.16 |
| | | | SDHI | 50 | 7.074 | 0.35 |
| | | Analog | ADC12 (2 Units)*4 | 100 | 4.697 | 0.47 |
| | | | DAC12 (2ch)*4 | 100 | 3.543 | 0.35 |
| | | | TSN | 50 | 0.166 | 0.01 |
| | | Human machine interfaces | CTSU | 50 | 0.678 | 0.03 |
| | | Event link | ELC | 50 | 1.016 | 0.05 |
| | | Security | SCE9 | 100 | 218.100 | 21.81 |
| | | Data processing | CRC | 100 | 0.521 | 0.05 |
| | | | DOC | 100 | 0.358 | 0.04 |
| | | System | CAC | 50 | 0.909 | 0.05 |
| | | DMA | DMAC | 200 | 4.045 | 0.81 |
| | | | DTC | 200 | 3.720 | 0.74 |

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 shows the outline of operation for each unit.

**Table 2.13 Outline of operation for each unit (1 of 2)**

| Peripheral | Outline of operation |
|---|---|
| GPT | Operating modes is set to saw-wave PWM mode.<br>GPT is operating with PCLKD. |
| POEG | Only clear module stop bit. |

**Table 2.13 Outline of operation for each unit (2 of 2)**

| Peripheral | Outline of operation |
|---|---|
| AGT | AGT is operating with PCLKB. |
| RTC | RTC is operating with LOCO. |
| WDT | WDT is operating with PCLKB. |
| IWDT | IWDT is operating with IWDTCLK. |
| ETHERC | Operation modes is set to full-duplex mode.<br>ETHERC is operating using Reduced Media Independent Interface (RMII). |
| USBFS | Transfer types is set to bulk transfer.<br>USBFS is operating using Full-speed transfer (12 Mbps). |
| SCI | SCI is transmitting data in clock synchronous mode. |
| IIC | Communication format is set to I2C-bus format.<br>IIC is transmitting data in master mode. |
| CAN | CAN is transmitting and receiving data in self-test mode 1. |
| SPI | SPI mode is set to SPI operation (4-wire method).<br>SPI master/slave mode is set to master mode.<br>SPI is transmitting 8-bit width data. |
| OSPI | Transfer mode is single continuous write mode.<br>OSPI is issuing memory write command to OctaRAM. |
| QSPI | QSPI is issuing Fast Read Quad I/O Instruction. |
| SSIE | Communication mode is set to Master.<br>System word length is set to 32 bits.<br>Data word length is set to 20 bits.<br>SSIE is transmitting data using I2S format. |
| SDHI | Transfer bus mode is set to 4-bit wide bus mode.<br>SDHI is issuing CMD24 (single-block write). |
| ADC12 | Resolution is set to 12-bit accuracy.<br>Data registers is set to A/D-converted value addition mode.<br>ADC12 is converting the analog input in continuous scan mode. |
| DAC12 | DAC12 is outputting the conversion result while updating the value of data register. |
| TSN | TSN is operating. |
| CTSU | CTSU is operating in self-capacitance single scan mode. |
| ELC | Only clear module stop bit. |
| SCE9 | SCE9 is executing built-in self test. |
| CRC | CRC is generating CRC code using 32-bit CRC32-C polynomial. |
| DOC | DOC is operating in data addition mode. |
| CAC | Measurement target clocks is set to PCLKB.<br>Measurement reference clocks is set to PCLKB.<br>CAC is measuring the clock frequency accuracy. |
| DMAC | Bit length of transfer data is set to 32 bits.<br>Transfer mode is set to block transfer mode.<br>DMAC is transferring data from SRAM0 to SRAM0. |
| DTC | Bit length of transfer data is set to 32 bits.<br>Transfer mode is set to block transfer mode.<br>DTC is transferring data from SRAM0 to SRAM0. |

### 2.2.7.2 Example of $T_j$ calculation

Assumption :

- Package 144-pin LQFP : θja = 33.0 °C/W
- Ta = 100 °C

- $I_{CC}$max = 70 mA
- VCC = 3.5 V (VCC = AVCC = VCC_USB)
- $I_{OH}$ = 1 mA, $V_{OH}$ = VCC – 0.5 V, 12 Outputs
- $I_{OL}$ = 20 mA, $V_{OL}$ = 1.0 V, 8 Outputs
- $I_{OL}$ = 1 mA, $V_{OL}$ = 0.5 V, 12 Outputs
- $C_{in}$ = 8 pF, 32 pins, Input frequency = 10 MHz
- $C_{load}$ = 30 pF, 32 pins, Output frequency = 10 MHz

Leakage current of IO = Σ ($V_{OL}$ × $I_{OL}$) / Voltage + Σ ((VCC - $V_{OH}$) × $I_{OH}$) / Voltage
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

Dynamic current of IO = Σ IO ($C_{in}$ + $C_{load}$) × IO switching frequency × Voltage
= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V
= 42.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (70 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V
= 566 mW (0.566 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 33.0 °C/W × 0.566W
= 118.7 °C

## 2.3 AC Characteristics

### 2.3.1 Frequency

**Table 2.14 Operation frequency value in high-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | — | — | 200 | MHz |
| | Peripheral module clock (PCLKA) | | — | — | 100 | |
| | Peripheral module clock (PCLKB) | | — | — | 50 | |
| | Peripheral module clock (PCLKC) | | —*2 | — | 50 | |
| | Peripheral module clock (PCLKD) | | — | — | 100 | |
| | Flash interface clock (FCLK) | | —*1 | — | 50 | |
| | External bus clock (BCLK) | | — | — | 100 | |
| | EBCLK pin output | | — | — | 50 | |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

**Table 2.15 Operation frequency value in low-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | — | — | 1 | MHz |
| | Peripheral module clock (PCLKA) | | — | — | 1 | |
| | Peripheral module clock (PCLKB) | | — | — | 1 | |
| | Peripheral module clock (PCLKC) *2 | | —*2 | — | 1 | |
| | Peripheral module clock (PCLKD) | | — | — | 1 | |
| | Flash interface clock (FCLK)*1 | | — | — | 1 | |
| | External bus clock (BCLK) | | — | — | 1 | |
| | EBCLK pin output | | — | — | 1 | |

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

**Table 2.16 Operation frequency value in Subosc-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | 29.4 | — | 36.1 | kHz |
| | Peripheral module clock (PCLKA) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKB) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKC) *2 | | — | — | 36.1 | |
| | Peripheral module clock (PCLKD) | | — | — | 36.1 | |
| | Flash interface clock (FCLK)*1 | | 29.4 | — | 36.1 | |
| | External bus clock (BCLK) | | — | — | 36.1 | |
| | EBCLK pin output | | — | — | 36.1 | |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. The ADC12 cannot be used.

## 2.3.2 Clock Timing

**Table 2.17 Clock timing except for sub-clock oscillator (1 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| EBCLK pin output cycle time | $t_{Bcyc}$ | 20 | — | — | ns | Figure 2.7 |
| EBCLK pin output high pulse width | $t_{CH}$ | 3.3 | — | — | ns | |
| EBCLK pin output low pulse width | $t_{CL}$ | 3.3 | — | — | ns | |
| EBCLK pin output rise time | $t_{Cr}$ | — | — | 5.0 | ns | |
| EBCLK pin output fall time | $t_{Cf}$ | — | — | 5.0 | ns | |
| EXTAL external clock input cycle time | $t_{EXcyc}$ | 41.66 | — | — | ns | Figure 2.8 |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 15.83 | — | — | ns | |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 15.83 | — | — | ns | |
| EXTAL external clock rise time | $t_{EXr}$ | — | — | 5.0 | ns | |
| EXTAL external clock fall time | $t_{EXf}$ | — | — | 5.0 | ns | |
| Main clock oscillator frequency | $f_{MAIN}$ | 8 | — | 24 | MHz | — |
| Main clock oscillation stabilization wait time (crystal)*1 | $t_{MAINOSCWT}$ | — | — | —*1 | ms | Figure 2.9 |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 29.4912 | 32.768 | 36.0448 | kHz | — |
| LOCO clock oscillation stabilization wait time | $t_{LOCOWT}$ | — | — | 60.4 | μs | Figure 2.10 |

**Table 2.17 Clock timing except for sub-clock oscillator (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| ILOCO clock oscillation frequency | | $f_{ILOCO}$ | 13.5 | 15 | 16.5 | kHz | — |
| MOCO clock oscillation frequency | | $F_{MOCO}$ | 6.8 | 8 | 9.2 | MHz | — |
| MOCO clock oscillation stabilization wait time | | $t_{MOCOWT}$ | — | — | 15.0 | μs | — |
| HOCO clock oscillator oscillation frequency | Without FLL | $f_{HOCO16}$ | 15.78 | 16 | 16.22 | MHz | –20 ≤ Ta ≤ 105°C |
| | | $f_{HOCO18}$ | 17.75 | 18 | 18.25 | | |
| | | $f_{HOCO20}$ | 19.72 | 20 | 20.28 | | |
| | | $f_{HOCO16}$ | 15.71 | 16 | 16.29 | | –40 ≤ Ta ≤ –20°C |
| | | $f_{HOCO18}$ | 17.68 | 18 | 18.32 | | |
| | | $f_{HOCO20}$ | 19.64 | 20 | 20.36 | | |
| | With FLL | $f_{HOCO16}$ | 15.960 | 16 | 16.040 | | –40 ≤ Ta ≤ 105°C<br>Sub-clock frequency accuracy is ±50 ppm. |
| | | $f_{HOCO18}$ | 17.955 | 18 | 18.045 | | |
| | | $f_{HOCO20}$ | 19.950 | 20 | 20.050 | | |
| HOCO clock oscillation stabilization wait time[*2] | | $t_{HOCOWT}$ | — | — | 64.7 | μs | — |
| HOCO period jitter | | — | — | ±85 | — | ps | — |
| FLL stabilization wait time | | $t_{FLLWT}$ | — | — | 1.8 | ms | — |
| PLL clock frequency | | $f_{PLL}$ | 120 | — | 200 | MHz | — |
| PLL2 clock frequency | | $f_{PLL2}$ | 120 | — | 240 | MHz | — |
| PLL/PLL2 clock oscillation stabilization wait time | | $t_{PLLWT}$ | — | — | 174.9 | μs | Figure 2.11 |
| PLL/PLL2 period jitter | | — | — | ±100 | — | ps | — |
| PLL/PLL2 long term jitter | | — | — | ±300 | — | ps | Term: 1μs, 10μs |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency ($f_{HOCO}$) reaches the range for guaranteed operation.

**Table 2.18 Clock timing for the sub-clock oscillator**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Sub-clock frequency | $f_{SUB}$ | — | 32.768 | — | kHz | — |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | —[*1] | s | Figure 2.12 |

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

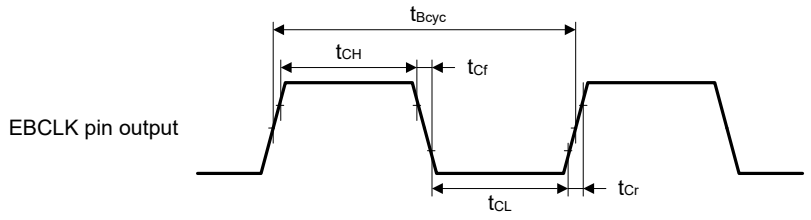



**Figure 2.7 EBCLK output timing**

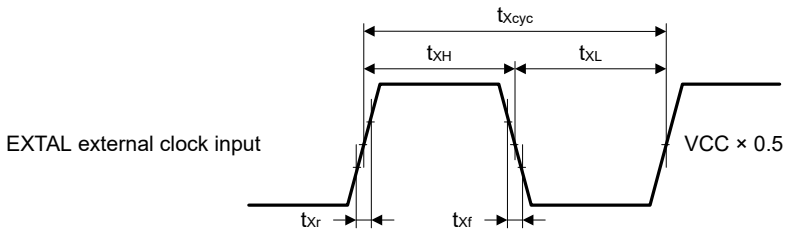



**Figure 2.8 EXTAL external clock input timing**

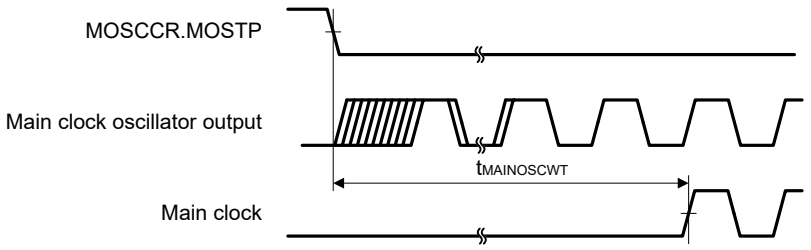



**Figure 2.9 Main clock oscillation start timing**

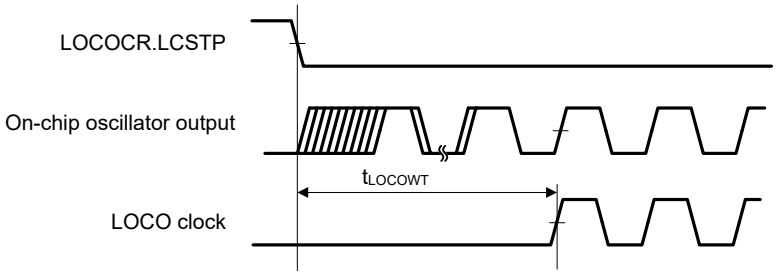



**Figure 2.10 LOCO clock oscillation start timing**

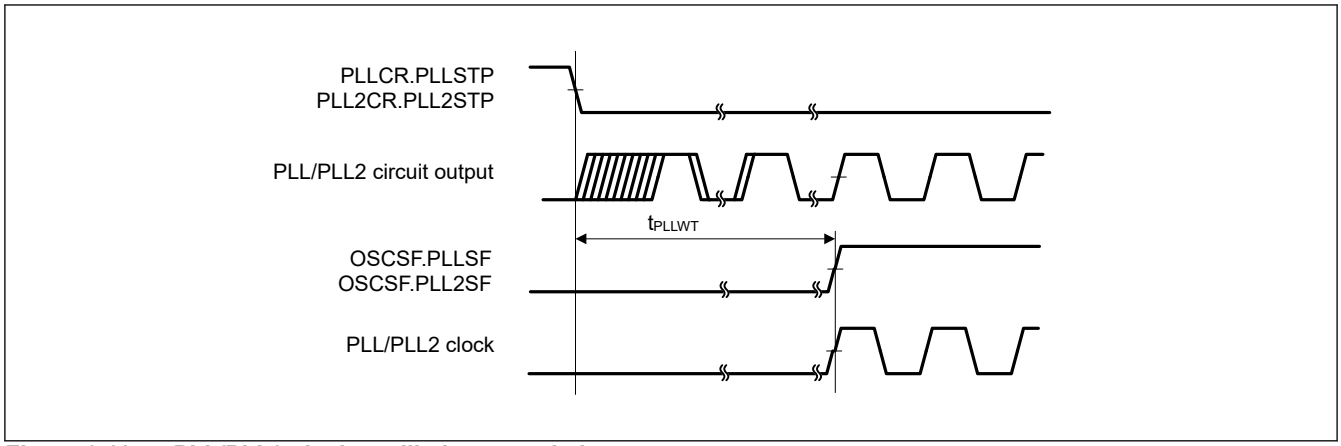



**Figure 2.11 PLL/PLL2 clock oscillation start timing**

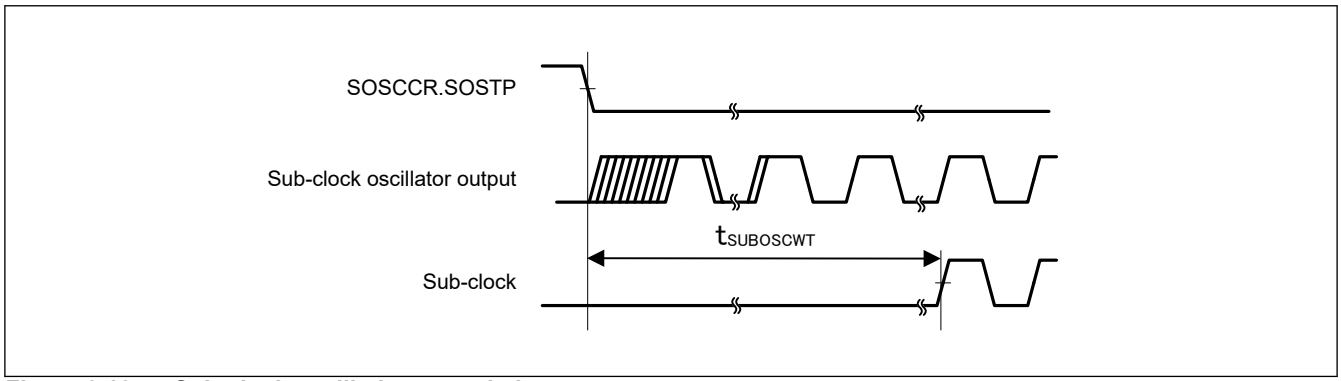



**Figure 2.12 Sub-clock oscillation start timing**

## 2.3.3 Reset Timing

**Table 2.19 Reset timing**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| RES pulse width | Power-on | $t_{RESWP}$ | 0.7 | — | — | ms | Figure 2.13 |
| | Deep Software Standby mode | $t_{RESWD}$ | 0.6 | — | — | ms | Figure 2.14 |
| | Software Standby mode, Subosc-speed mode | $t_{RESWS}$ | 0.3 | — | — | ms | |
| | All other | $t_{RESW}$ | 200 | — | — | μs | |
| Wait time after RES cancellation | | $t_{RESWT}$ | — | 37.3 | 41.2 | μs | Figure 2.13 |
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset) | | $t_{RESW2}$ | — | 324 | 397.7 | μs | — |

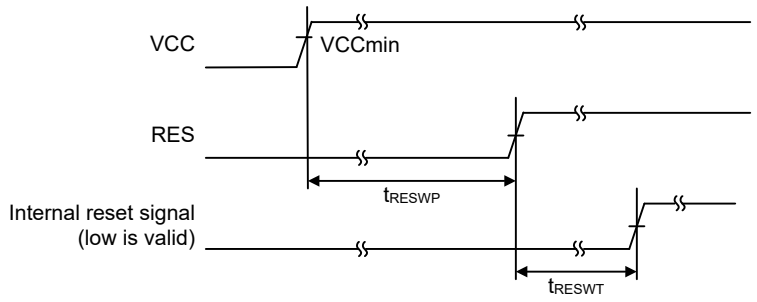



**Figure 2.13 RES pin input timing under the condition that VCC exceeds $V_{POR}$ voltage threshold**

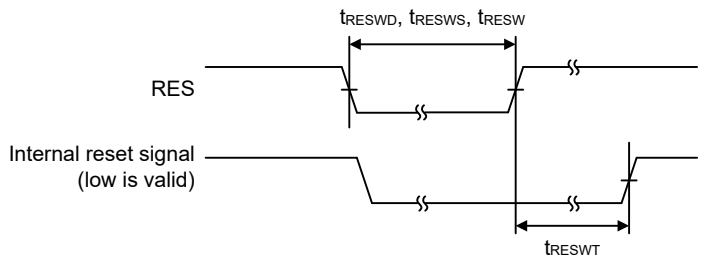



**Figure 2.14 Reset input timing**

## 2.3.4 Wakeup Timing

**Table 2.20 Timing of recovery from low power modes (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator*2 | $t_{SBYMC}$*13 | — | 2.1 | 2.4 | ms | Figure 2.15 The division ratio of all oscillators is 1. |
| | | System clock source is PLL with main clock oscillator*3 | $t_{SBYPC}$*13 | — | 2.2 | 2.6 | ms | |
| | External clock input to main clock oscillator | System clock source is main clock oscillator*4 | $t_{SBYEX}$*13 | — | 45 | 125 | μs | |
| | | System clock source is PLL with main clock oscillator*5 | $t_{SBYPE}$*13 | — | 170 | 255 | μs | |
| | System clock source is sub-clock oscillator*6 *11 | | $t_{SBYSC}$*13 | — | 0.7 | 0.8 | ms | |
| | System clock source is LOCO*7 *11 | | $t_{SBYLO}$*13 | — | 0.7 | 0.9 | ms | |
| | System clock source is HOCO clock oscillator*8 | | $t_{SBYHO}$*13 | — | 55 | 130 | μs | |
| | System clock source is PLL with HOCO*9 | | $t_{SBYPH}$*13 | — | 175 | 265 | μs | |
| | System clock source is MOCO clock oscillator*10 | | $t_{SBYMO}$*13 | — | 35 | 65 | μs | |
| Recovery time from Deep Software Standby mode | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E | | $t_{DSBY}$ | — | 0.38 | 0.54 | ms | Figure 2.16 |
| | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19 | | $t_{DSBY}$ | — | 0.55 | 0.73 | ms | |
| Wait time after cancellation of Deep Software Standby mode | | | $t_{DSBYWT}$ | 56 | — | 57 | $t_{cyc}$ | |

**Table 2.20 Timing of recovery from low power modes (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode to Snooze mode | High-speed mode when system clock source is HOCO (20 MHz) | $t_{SNZ}$ | — | 35*12 | 70*12 | μs | Figure 2.17 |
| | High-speed mode when system clock source is MOCO (8 MHz) | $t_{SNZ}$ | — | 11*12 | 14*12 | μs | |

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 μs (typical), 48 μs (maximum).
Note 13. The recovery time can be calcurated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the fol-lowing value and equation. For n, the greatest value is selected from among the internal clock division settings.

| Wakeup time | TYP | | MAX | | Unit |
|---|---|---|---|---|---|
| | tSBYOSCWT | tSBYSEQ | tSBYOSCWT | tSBYSEQ | |
| tSBYMC | (MSTS[7:0]*32 + 3) / 0.262 | 35 + 18 / fICLK + 4n / fMAIN | (MSTS[7:0]*32 + 14 / 0.236 | 62 + 18 / fICLK + 4n / fMAIN | μs |
| tSBYPC | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / fICLK + 4n / fPLL | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / fICLK + 4n / fPLL | μs |
| tSBYEX | 10 | 35 + 18 / fICLK + 4n / fEXMAIN | 62 | 62 + 18 / fICLK + 4n / fEXMAIN | μs |
| tSBYPE | 135 | 35 + 18 / fICLK + 4n / fPLL | 192 | 62 + 18 / fICLK + 4n / fPLL | μs |
| tSBYSC | 0 | 35 + 18 / fICLK + 4n / fSUB | 0 | 62 + 18 / fICLK + 4n / fSUB | μs |
| tSBYLO | 0 | 35 + 18 / fICLK + 4n / fLOCO | 0 | 62 + 18 / fICLK + 4n / fLOCO | μs |
| tSBYHO | 20 | 35 + 18 / fICLK + 4n / fHOCO | 67 | 62 + 18 / fICLK + 4n / fHOCO | μs |
| tSBYPH | 140 | 35 + 18 / fICLK + 4n / fPLL | 202 | 62 + 18 / fICLK + 4n / fPLL | μs |
| tSBYMO | 0 | 35 + 18 / fICLK + 4n / fMOCO | 0 | 62 + 18 / fICLK + 4n / fMOCO | μs |

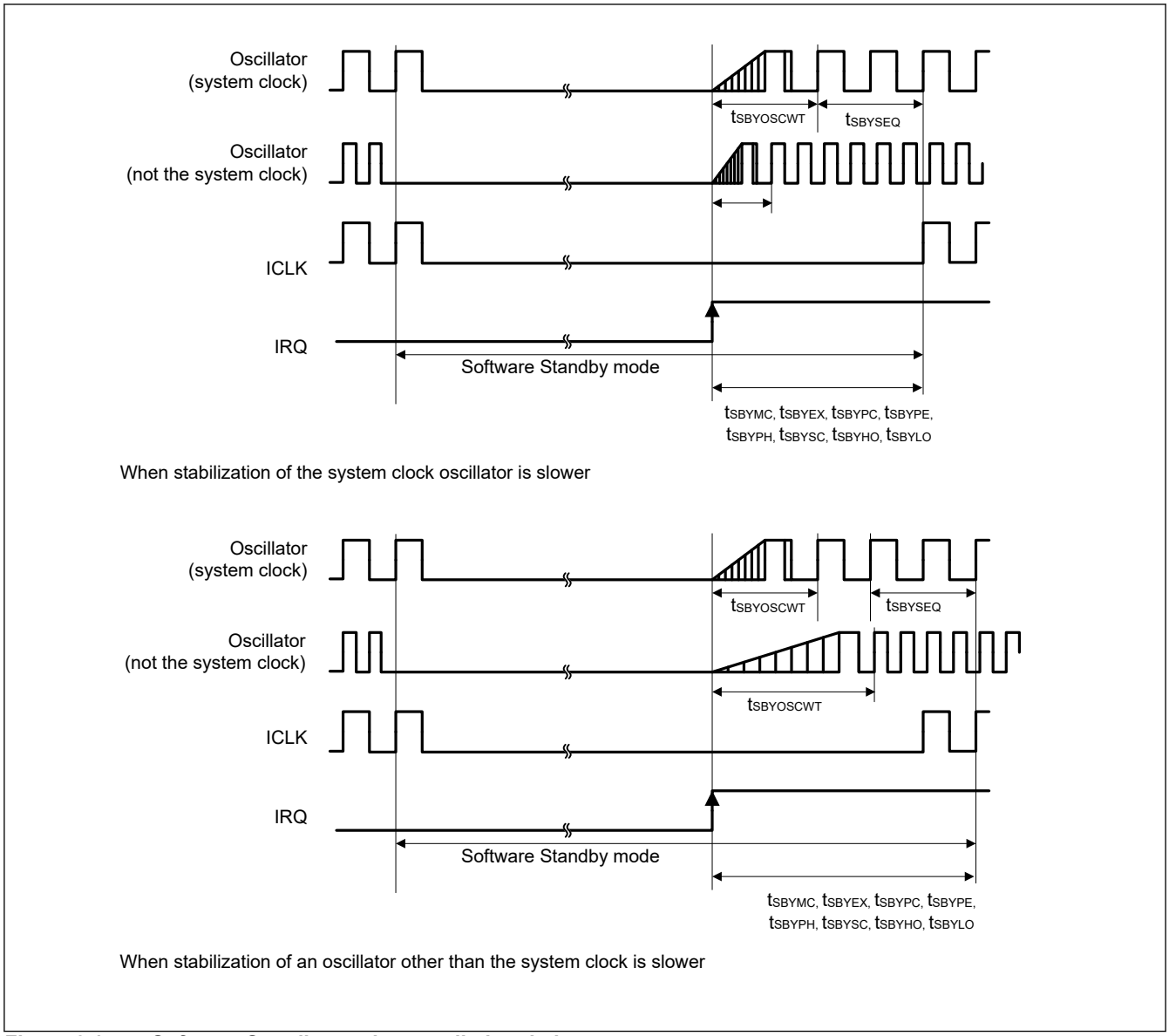



**Figure 2.15 Software Standby mode cancellation timing**

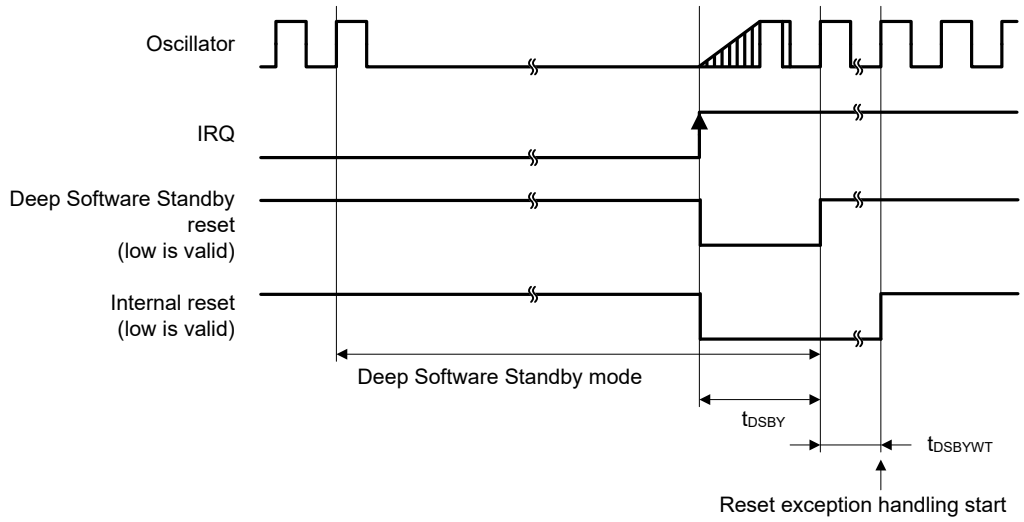
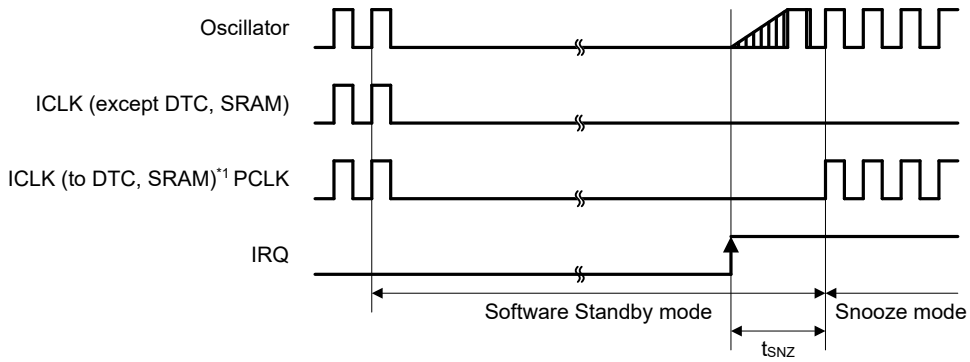



**Figure 2.16 Deep Software Standby mode cancellation timing**




Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

**Figure 2.17 Recovery timing from Software Standby mode to Snooze mode**

## 2.3.5 NMI and IRQ Noise Filter

**Table 2.21 NMI and IRQ noise filter**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | — | — | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | — | — | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. $t_{Pcyc}$ indicates the PCLKB cycle.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock.

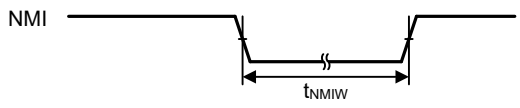



**Figure 2.18 NMI interrupt input timing**

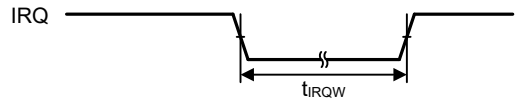



**Figure 2.19 IRQ interrupt input timing**

## 2.3.6 Bus Timing

**Table 2.22 Bus timing**

Condition:
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.
EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Address delay | $t_{AD}$ | — | 12.5 | ns | Figure 2.22 to Figure 2.25 |
| Byte control delay | $t_{BCD}$ | — | 12.5 | ns | |
| CS delay | $t_{CSD}$ | — | 12.5 | ns | |
| ALE delay time | $t_{ALED}$ | — | 12.5 | ns | |
| RD delay | $t_{RSD}$ | — | 12.5 | ns | |
| Read data setup time | $t_{RDS}$ | 12.5 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR/WRn delay | $t_{WRD}$ | — | 12.5 | ns | |
| Write data delay | $t_{WDD}$ | — | 12.5 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT setup time | $t_{WTS}$ | 12.5 | — | ns | Figure 2.26 |
| WAIT hold time | $t_{WTH}$ | 0 | — | ns | |

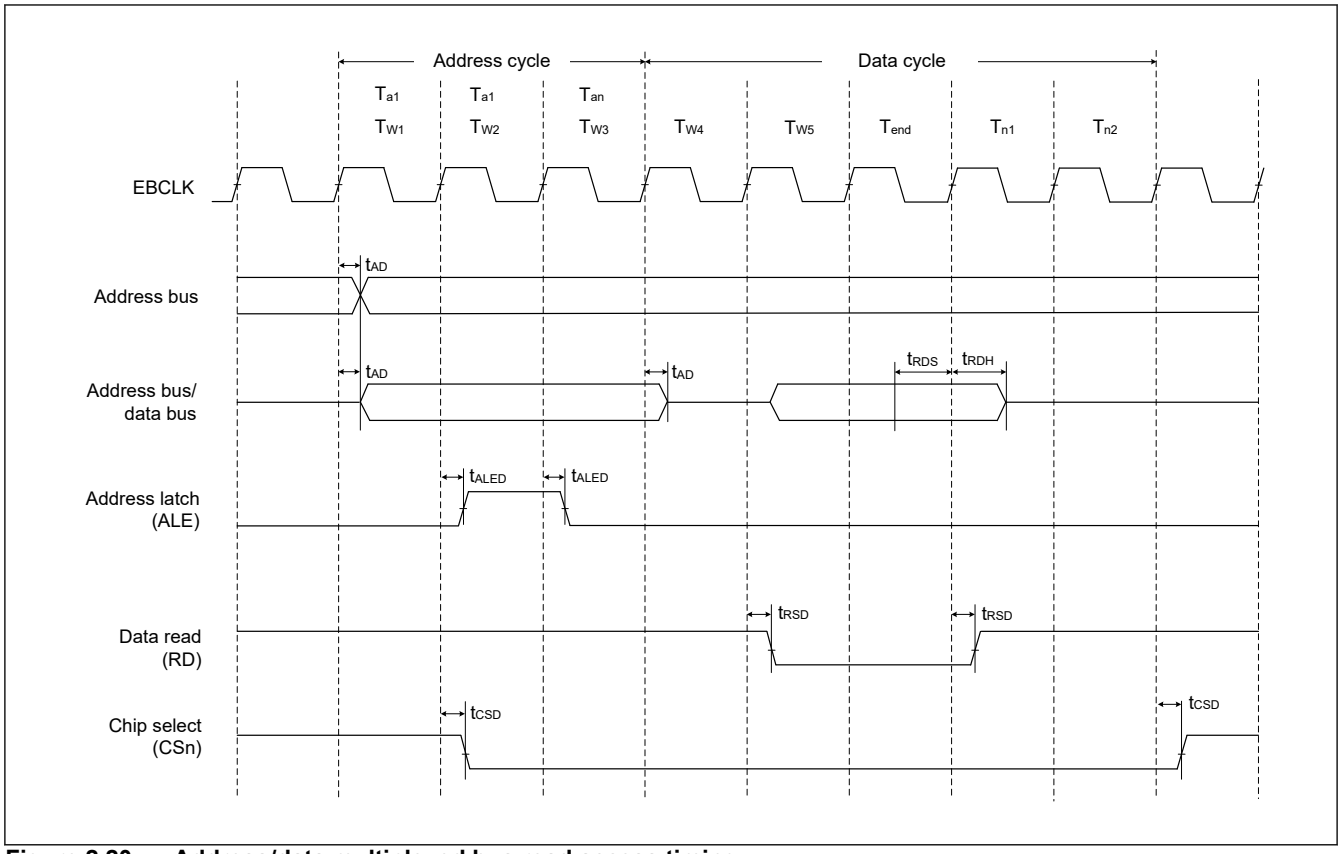



**Figure 2.20 Address/data multiplexed bus read access timing**

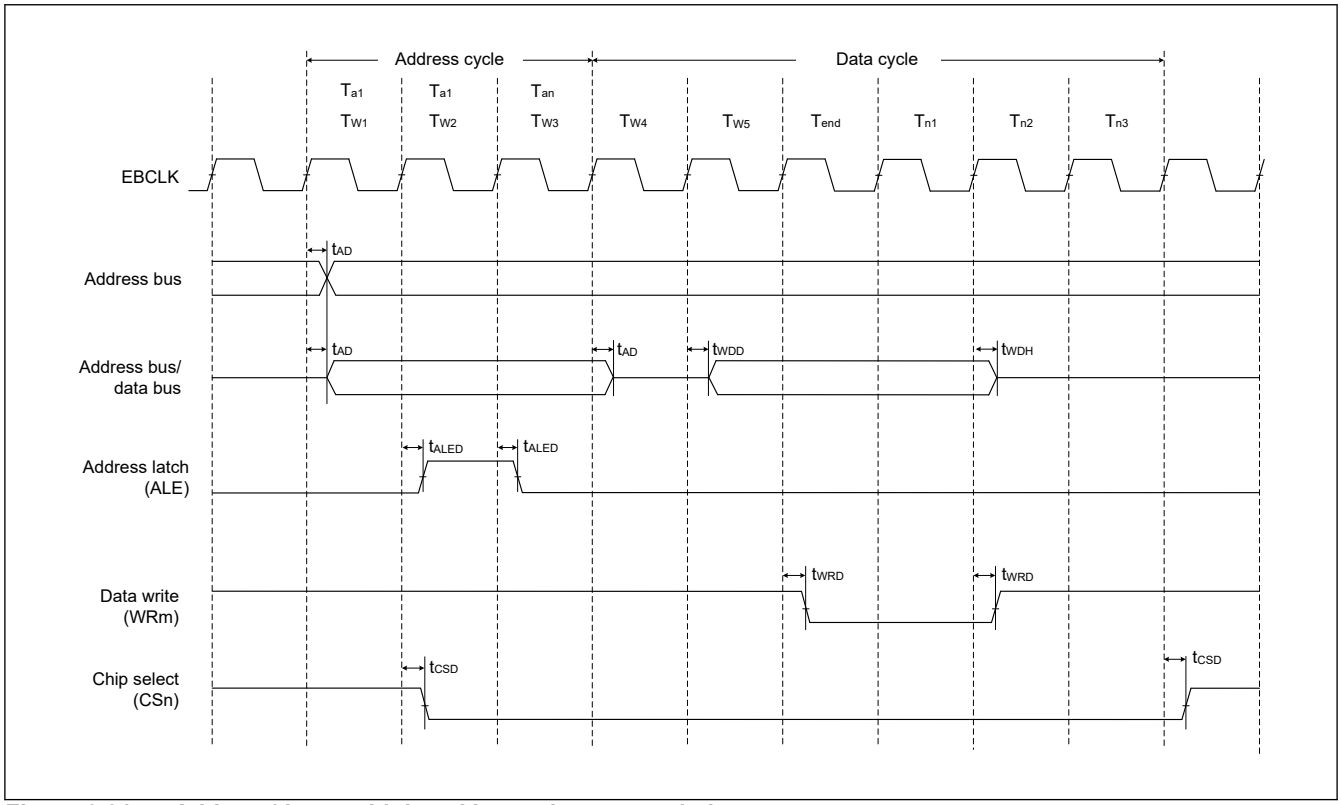



**Figure 2.21 Address/data multiplexed bus write access timing**

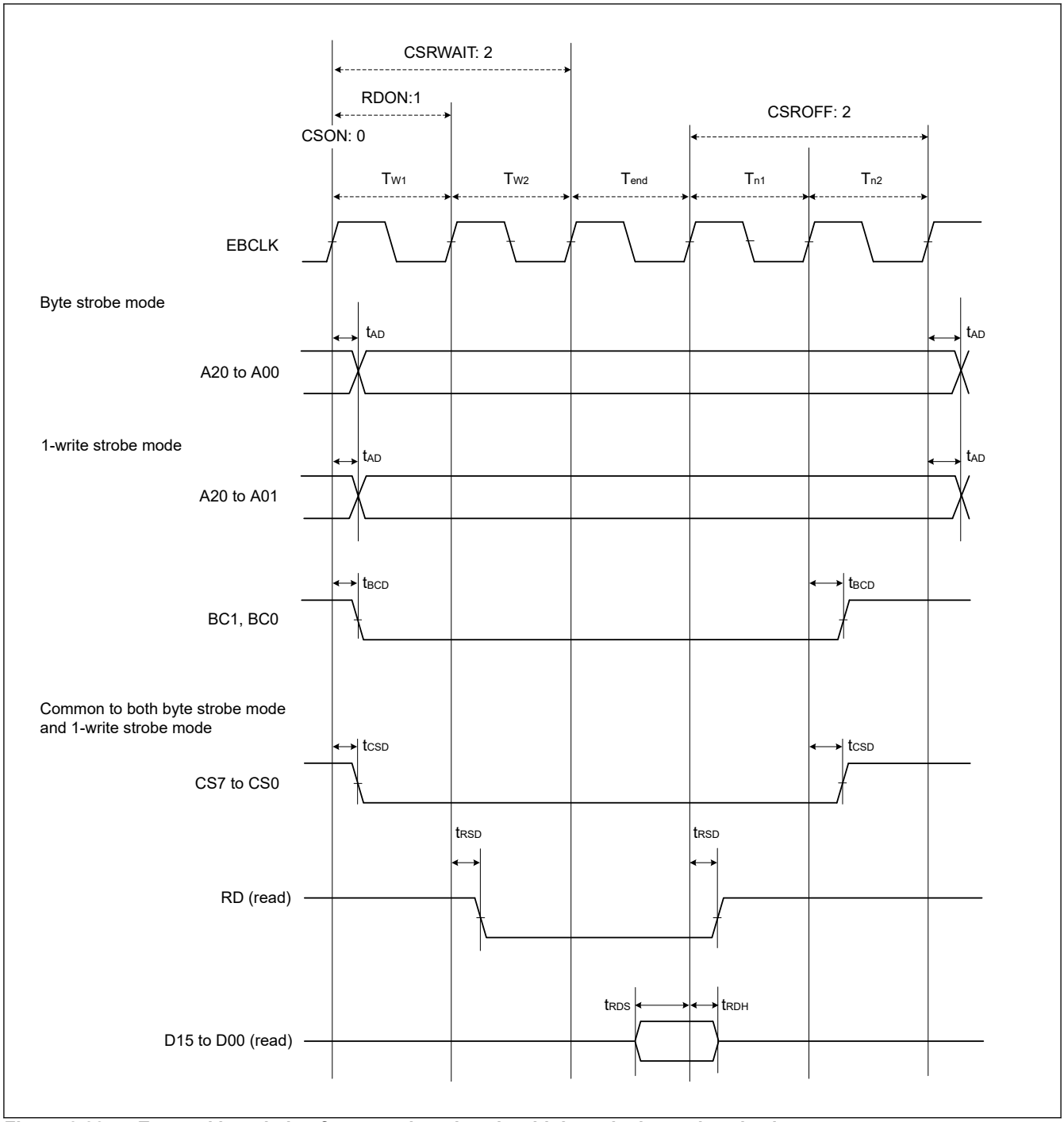
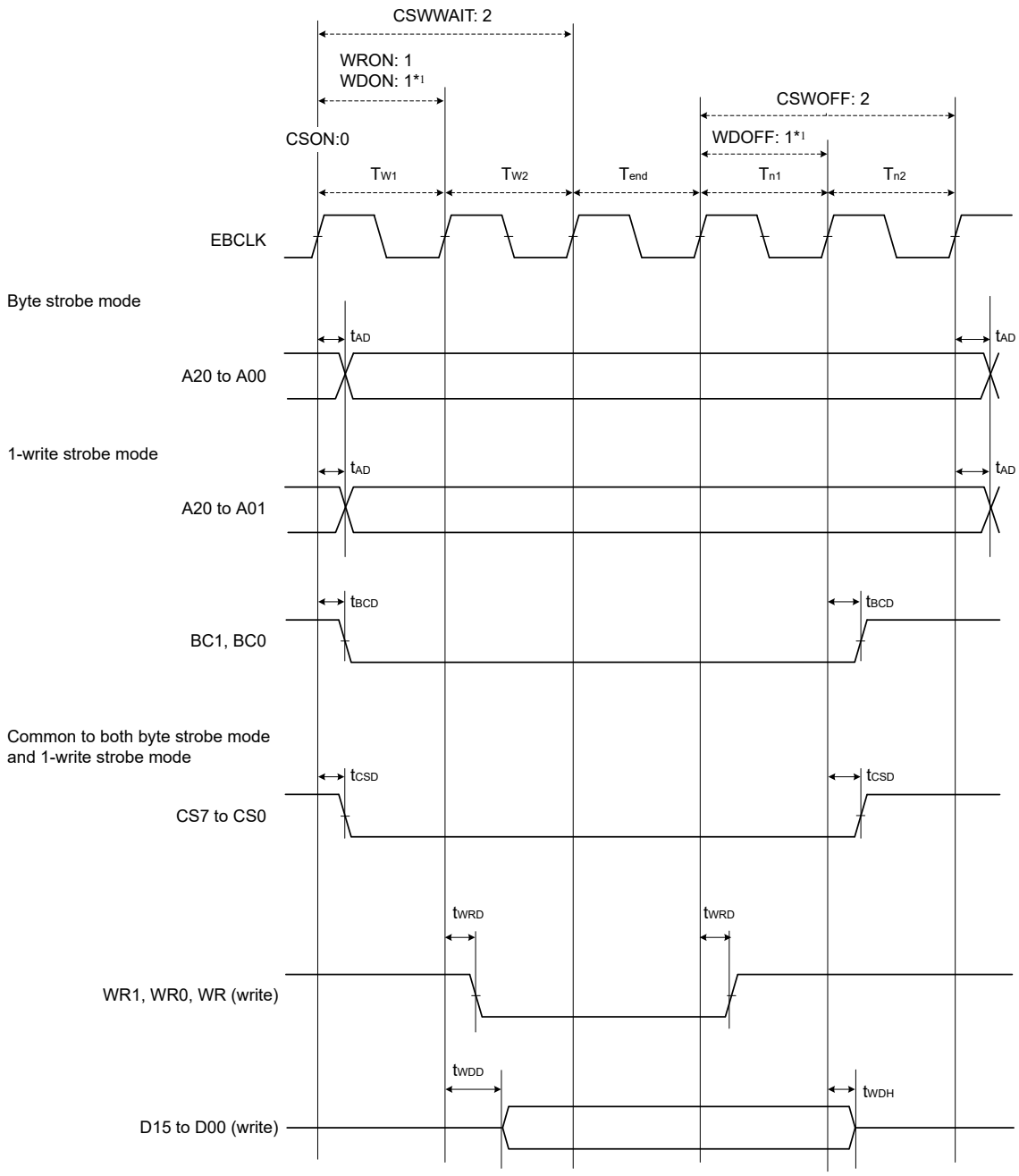



**Figure 2.22 External bus timing for normal read cycle with bus clock synchronized**




Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

**Figure 2.23 External bus timing for normal write cycle with bus clock synchronized**

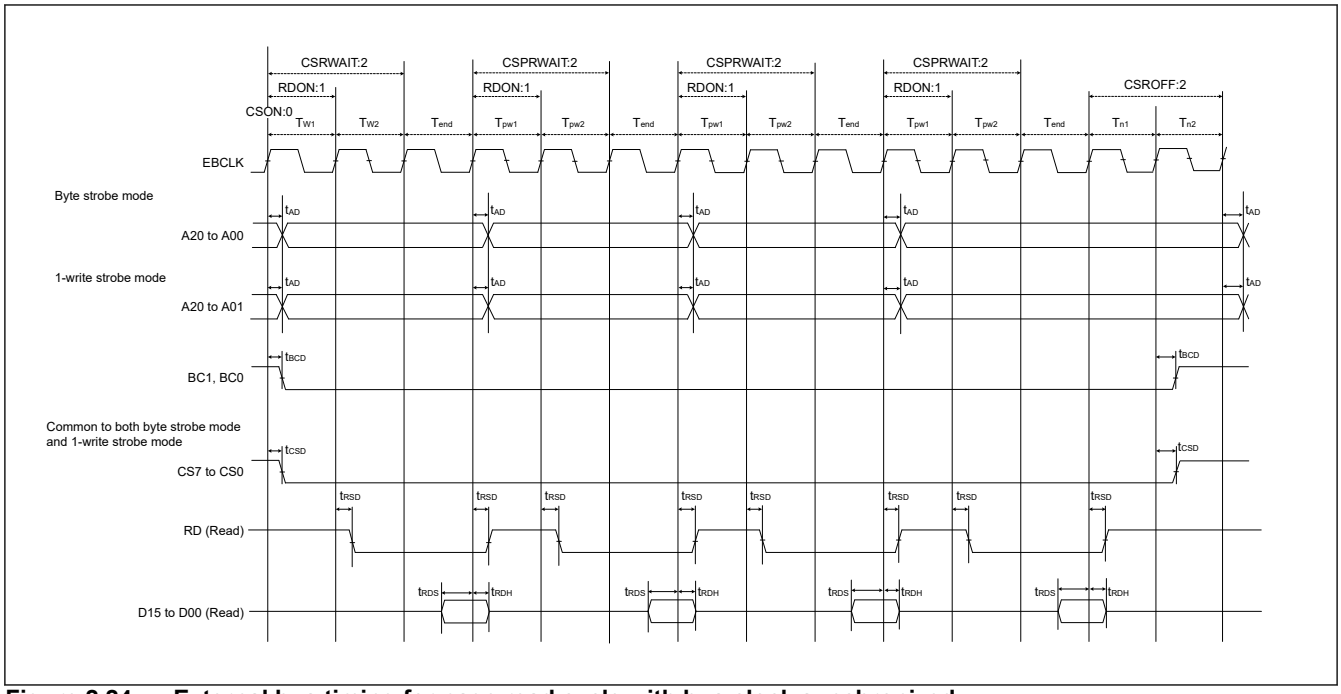
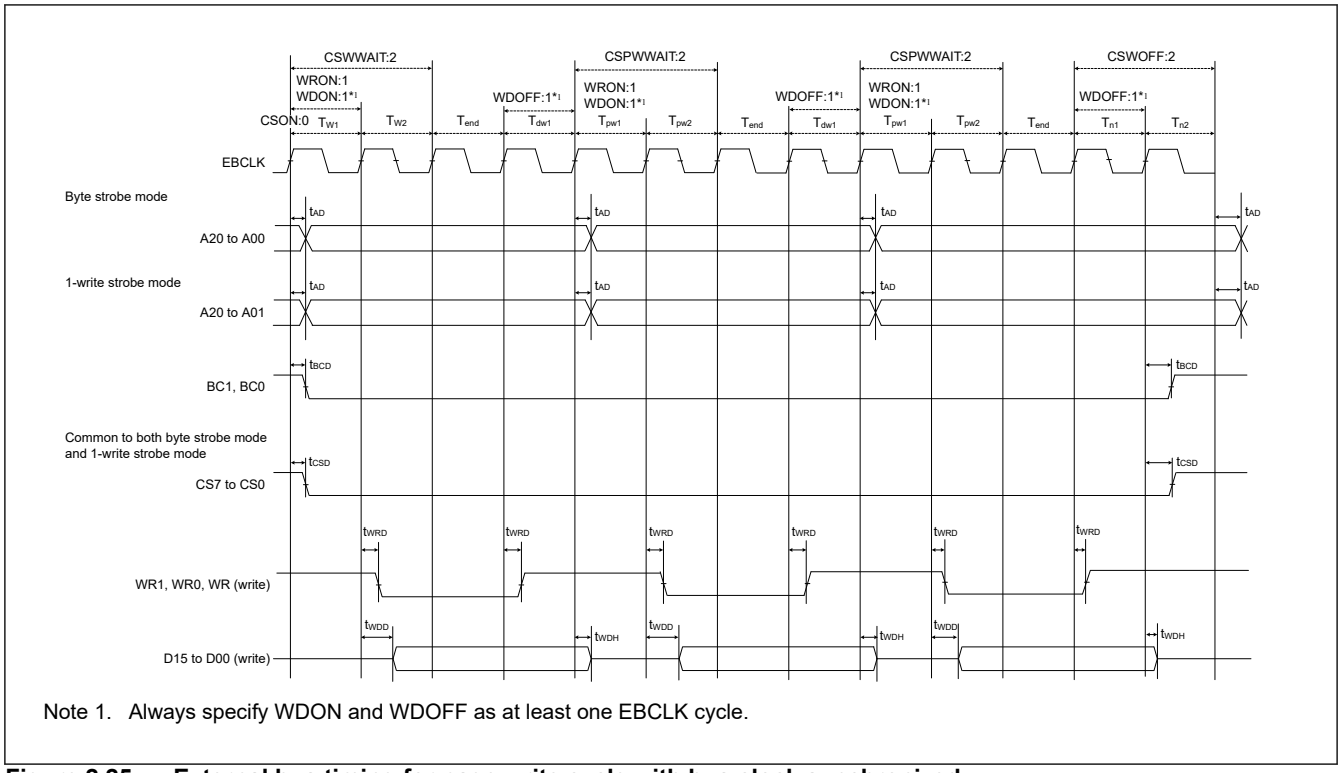



**Figure 2.24 External bus timing for page read cycle with bus clock synchronized**




Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

**Figure 2.25 External bus timing for page write cycle with bus clock synchronized**

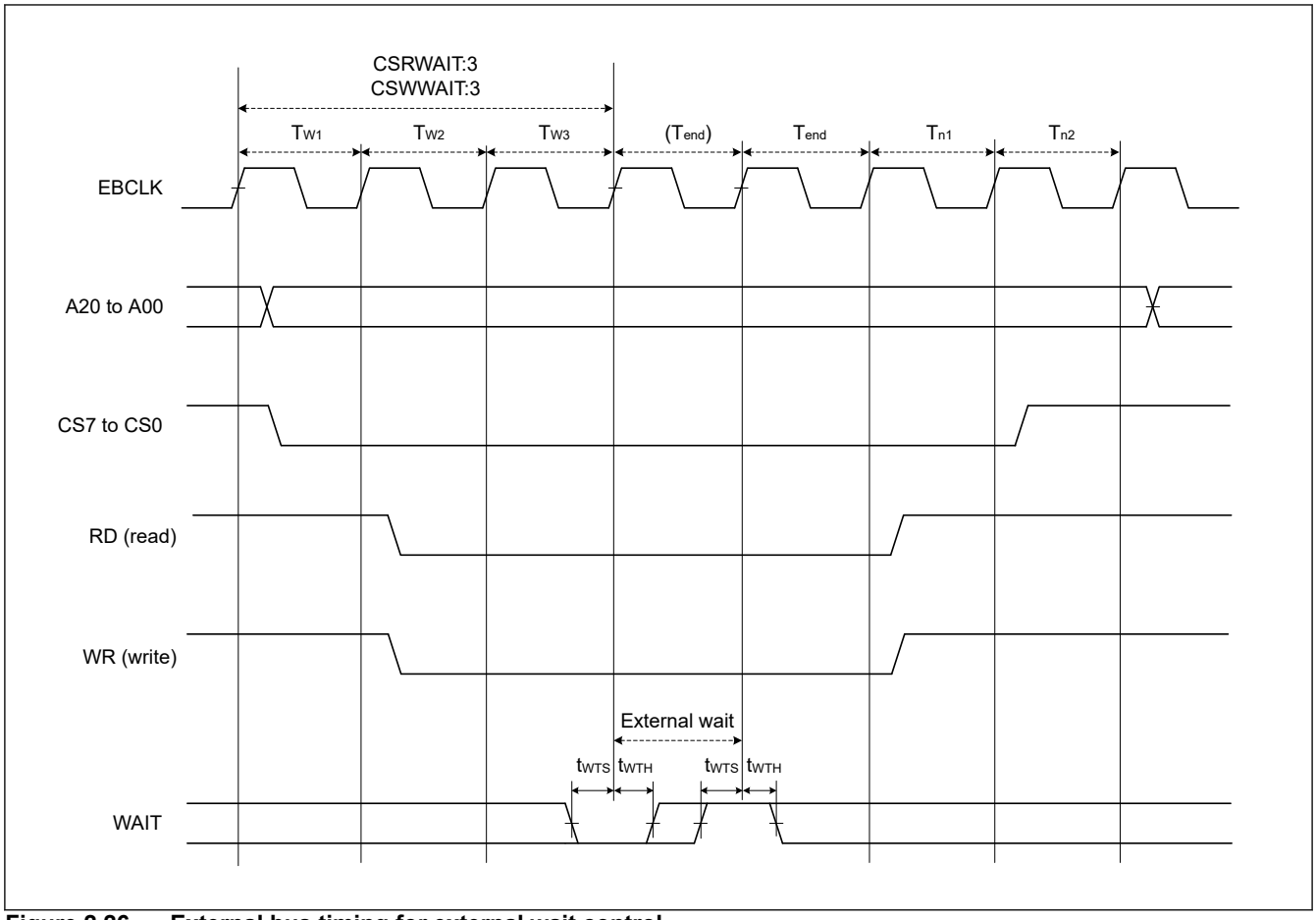



**Figure 2.26 External bus timing for external wait control**

## 2.3.7 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

**Table 2.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (1 of 2)**

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 2.27 |
| POEG | POEG input trigger pulse width | | $t_{POEW}$ | 3 | — | $t_{Pcyc}$ | Figure 2.28 |
| GPT | Input capture pulse width | Single edge | $t_{GTICW}$ | 1.5 | — | $t_{PDcyc}$ | Figure 2.29 |
| | | Dual edge | | 2.5 | — | | |
| | GTIOCxY output skew (x = 0 to 3, Y = A or B) | Middle drive buffer | $t_{GTISK}$ *1 | — | 4 | ns | Figure 2.30 |
| | | High drive buffer | | — | 4 | | |
| | GTIOCxY output skew (x = 4 to 9, Y = A or B) | Middle drive buffer | | — | 4 | | |
| | | High drive buffer | | — | 4 | | |
| | GTIOCxY output skew (x = 0 to 9, Y = A or B) | Middle drive buffer | | — | 6 | | |
| | | High drive buffer | | — | 6 | | |
| | OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO | | $t_{GTOSK}$ | — | 5 | ns | Figure 2.31 |

**Table 2.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (2 of 2)**

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| AGT | AGTIO, AGTEE input cycle | $t_{ACYC}$ *2 | 100 | — | ns | Figure 2.32 |
| | AGTIO, AGTEE input high width, low width | $t_{ACKWH}$, $t_{ACKWL}$ | 40 | — | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | $t_{ACYC2}$ | 62.5 | — | ns | |
| ADC12 | ADC12 trigger input pulse width | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 2.33 |

Note: $t_{Pcyc}$: PCLKB cycle, $t_{PDcyc}$: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

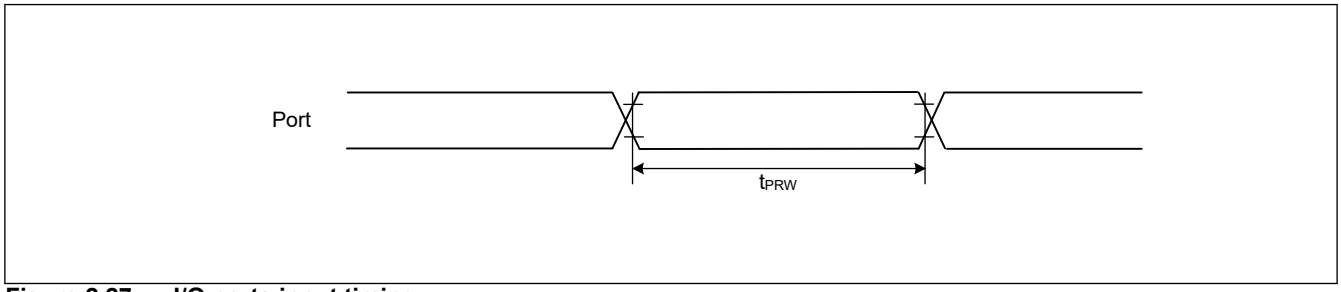



**Figure 2.27 I/O ports input timing**

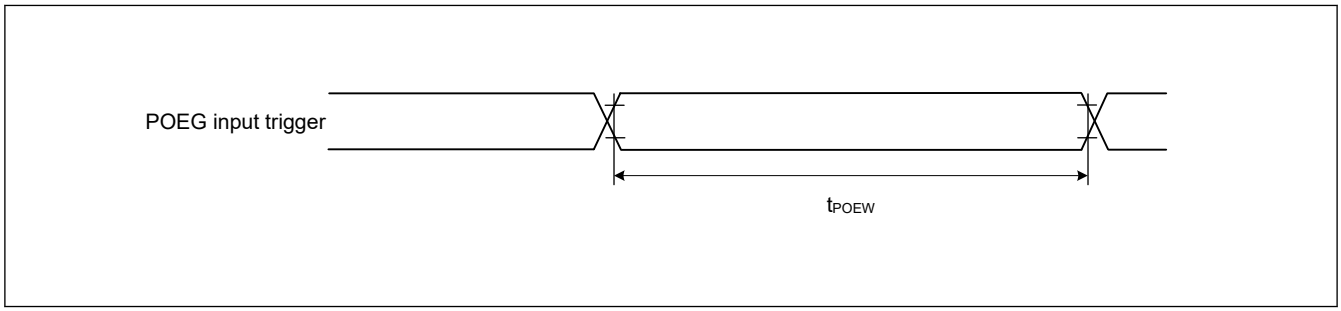



**Figure 2.28 POEG input trigger timing**

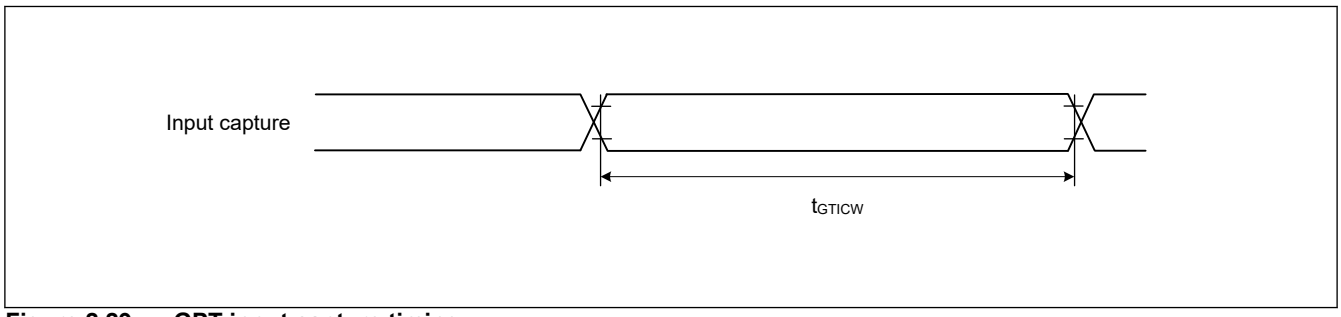



**Figure 2.29 GPT input capture timing**

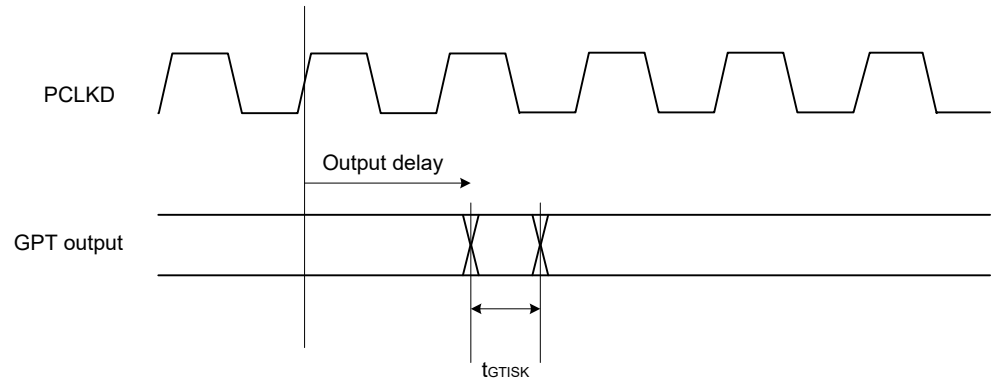



**Figure 2.30 GPT output delay skew**

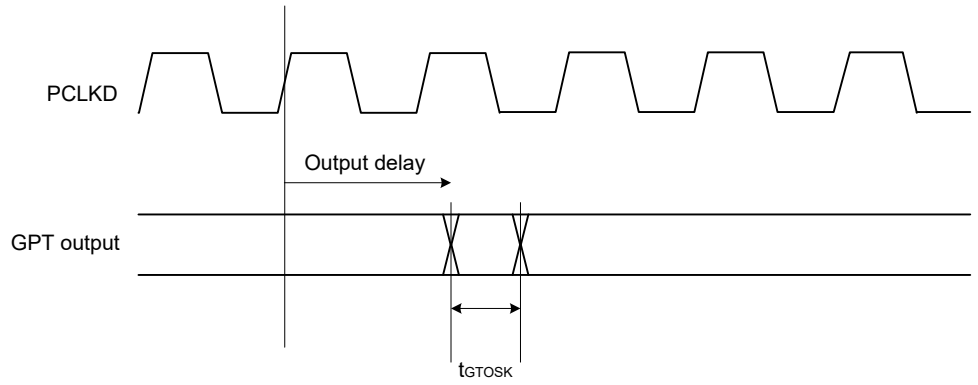



**Figure 2.31 GPT output delay skew for OPS**

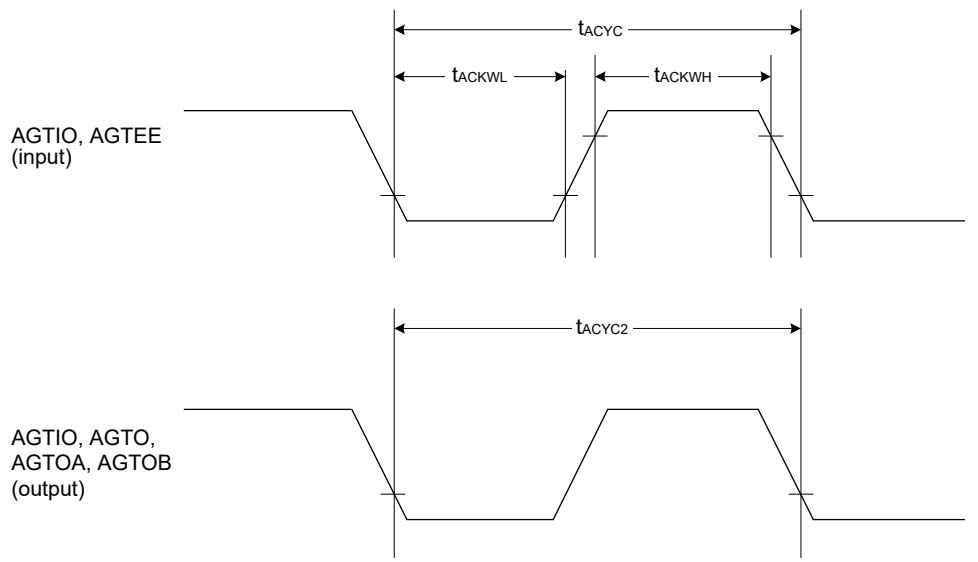



**Figure 2.32 AGT input/output timing**

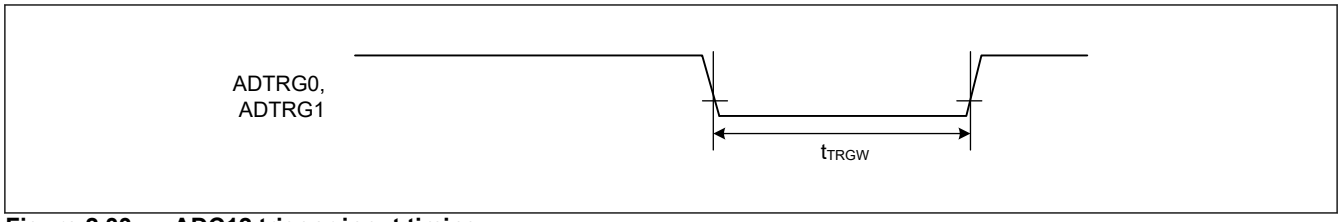



**Figure 2.33 ADC12 trigger input timing**

## 2.3.8 CAC Timing

**Table 2.24 CAC timing**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}$ *1 | $t_{CACREF}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | — | — | ns | — |
| | | $t_{PBcyc} > t_{cac}$ *1 | | $5 \times t_{cac} + 6.5 \times t_{PBcyc}$ | — | — | ns | |

Note: $t_{PBcyc}$: PCLKB cycle.
Note 1. $t_{cac}$: CAC count clock source cycle.

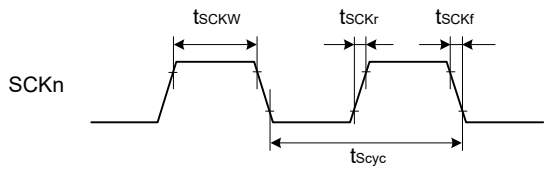
## 2.3.9 SCI Timing

**Table 2.25 SCI timing (1)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

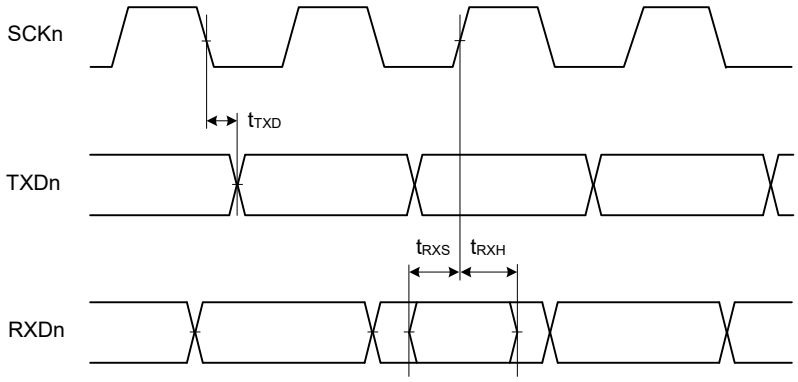
| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | Figure 2.34 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 6 (other than SCI1, SCI2)<br>8 (SCI1, SCI2) | — | $t_{Pcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay | Clock synchronous master mode (internal clock) | $t_{TXD}$ | — | 5 | ns | Figure 2.35 |
| | | Clock synchronous slave mode (external clock) | $t_{TXD}$ | — | 25 | ns | |
| | Receive data setup time | Clock synchronous master mode (internal clock) | $t_{RXS}$ | 15 | — | ns | |
| | | Clock synchronous slave mode (external clock) | $t_{RXS}$ | 5 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | ns | |

Note: $t_{Pcyc}$: PCLKA cycle.




Note: n = 0 to 9

**Figure 2.34 SCK clock input/output timing**




Note: n = 0 to 9

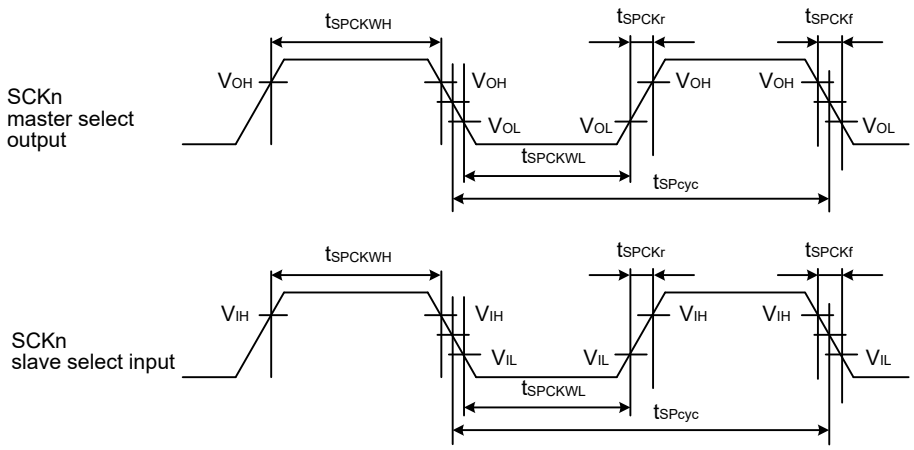
**Figure 2.35 SCI input/output timing in clock synchronous mode**

**Table 2.26 SCI timing (2)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | | $t_{SPcyc}$ | 4 | 65536 | $t_{Pcyc}$ | Figure 2.36 |
| | SCK clock cycle input (slave) | | | 6 | 65536 | | |
| | SCK clock high pulse width | | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise and fall time | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | |
| | Data input setup time | master | $t_{SU}$ | 15 | — | ns | Figure 2.37 to Figure 2.40 |
| | | slave | | 5 | — | ns | |
| | Data input hold time | | $t_H$ | 5 | — | ns | |
| | SS input setup time | | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay | master | $t_{OD}$ | — | 5 | ns | |
| | | slave | | — | 25 | ns | |
| | Data output hold time | | $t_{OH}$ | -5 | — | ns | |
| | Data rise and fall time | | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | |
| | SS input rise and fall time | | $t_{SSLr}$, $t_{SSLf}$ | — | 5 | ns | |
| | Slave access time | | $t_{SA}$ | — | $3 \times t_{Pcyc} + 25$ | ns | Figure 2.40 |
| | Slave output release time | | $t_{REL}$ | — | $3 \times t_{Pcyc} + 25$ | ns | |

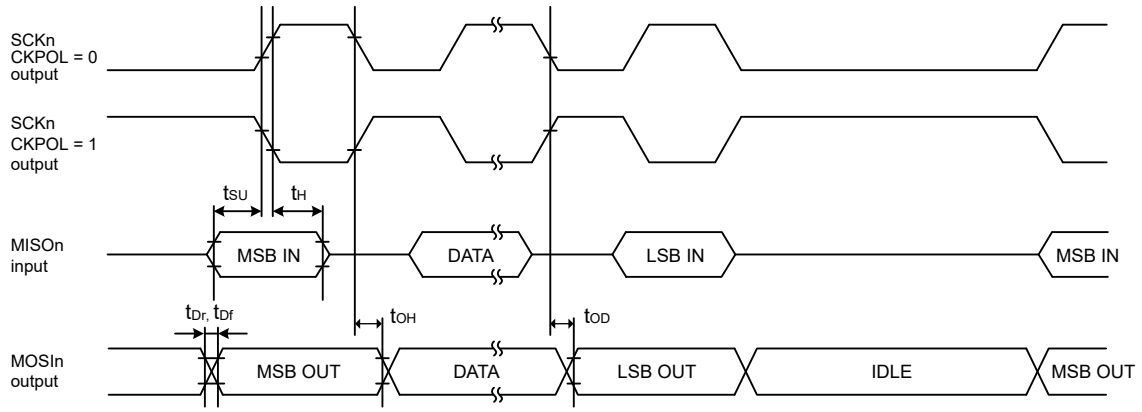
Note: $t_{Pcyc}$: PCLKA cycle.




$V_{OH} = 0.7 \times VCC$, $V_{OL} = 0.3 \times VCC$, $V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$

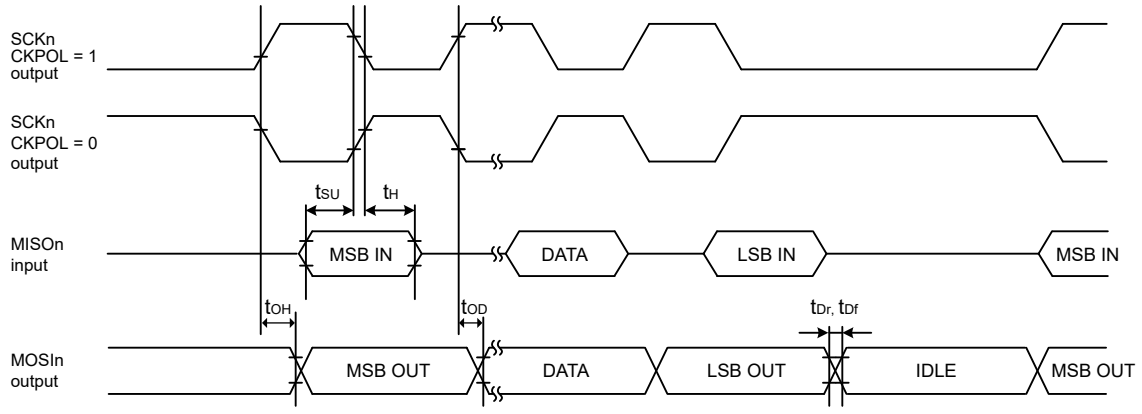
Note: n = 0 to 9

**Figure 2.36 SCI simple SPI mode clock timing**



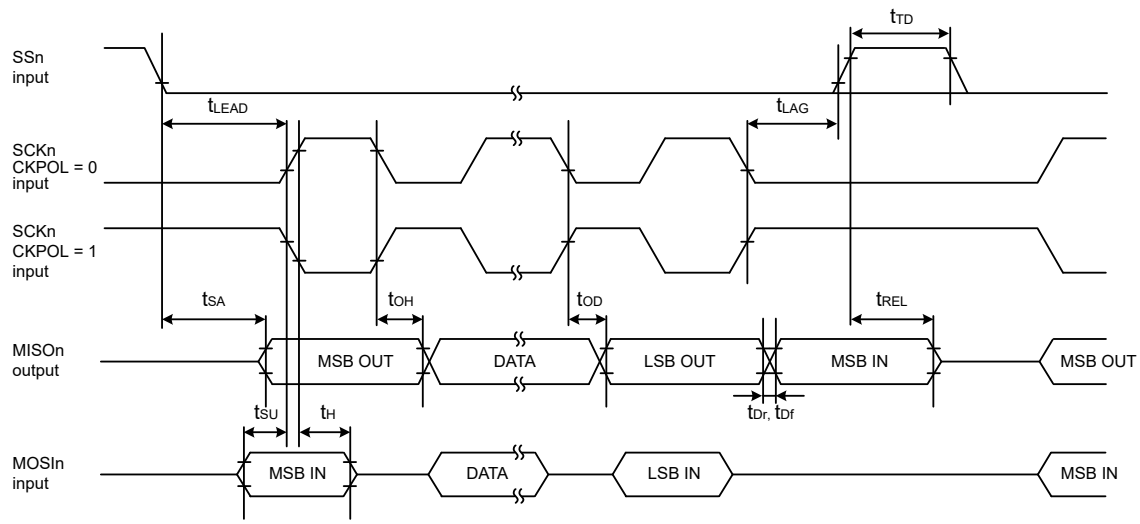

Note: n = 0 to 9

**Figure 2.37 SCI simple SPI mode timing for master when CKPH = 1**



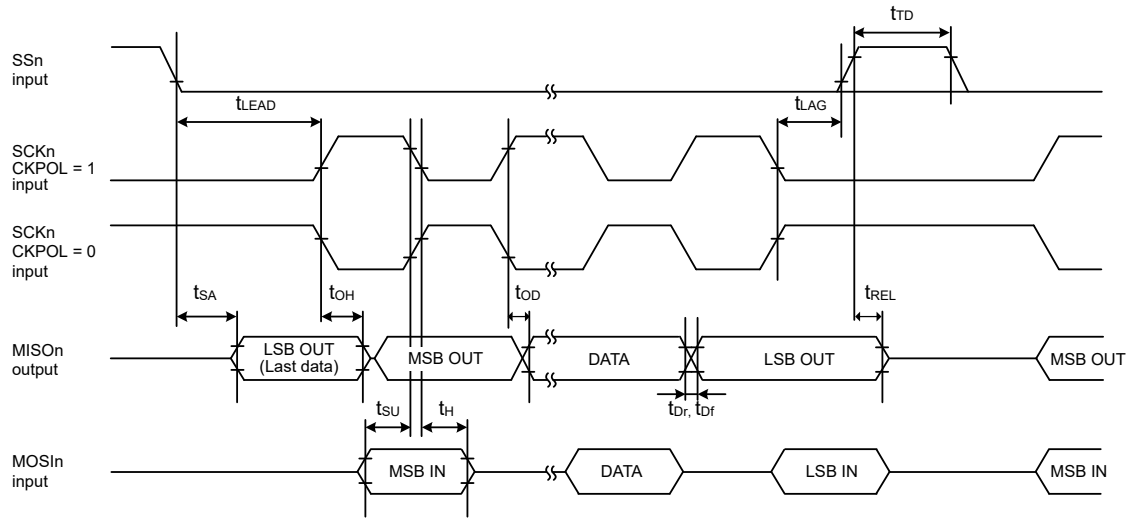

Note: n = 0 to 9

**Figure 2.38 SCI simple SPI mode timing for master when CKPH = 0**




Note: n = 0 to 9

**Figure 2.39 SCI simple SPI mode timing for slave when CKPH = 1**




Note: n = 0 to 9

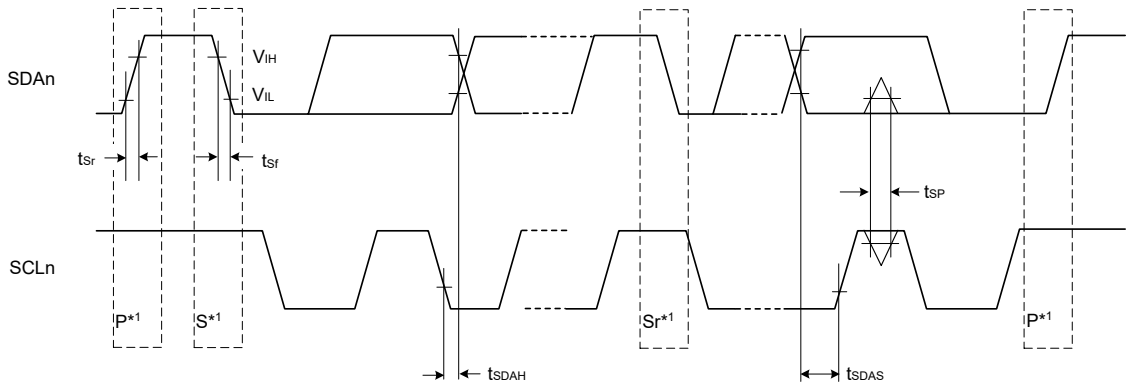
**Figure 2.40 SCI simple SPI mode timing for slave when CKPH = 0**

**Table 2.27 SCI timing (3)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard mode) | SDA input rise time | $t_{Sr}$ | — | 1000 | ns | Figure 2.41 |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ *1 | — | 400 | pF | |
| Simple IIC (Fast mode) | SDA input rise time | $t_{Sr}$ | — | 300 | ns | Figure 2.41 |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ *1 | — | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle.
Note 1. $C_b$ indicates the total capacity of the bus line.




Test conditions:
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA

Note: n = 0 to 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

**Figure 2.41 SCI simple IIC mode timing**

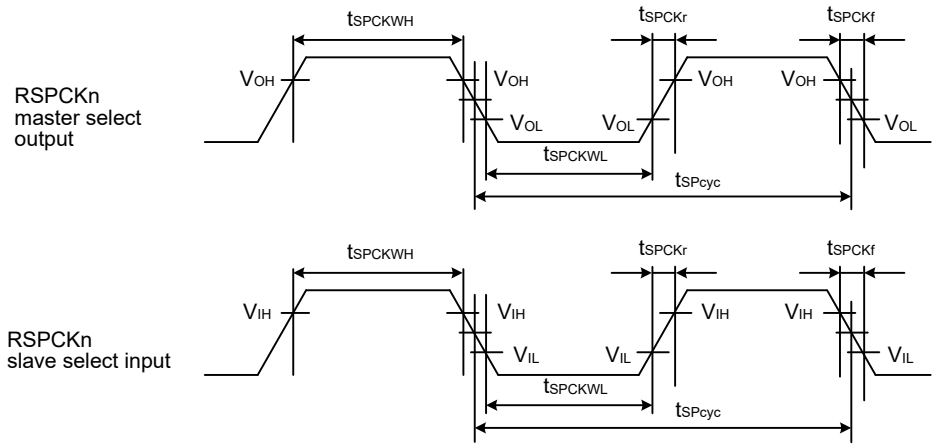
## 2.3.10 SPI Timing

**Table 2.28 SPI timing**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| SPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ | Figure 2.42 |
| | | Slave | | 4 | 4096 | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | RSPCK clock rise and fall time | Master | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | |
| | | Slave | | — | 1 | μs | |
| | Data input setup time | Master | $t_{SU}$ | 4 | — | ns | Figure 2.43 to Figure 2.48 |
| | | Slave | | 5 | — | | |
| | Data input hold time | Master (PCLKA division ratio set to 1/2) | $t_{HF}$ | 0 | — | ns | |
| | | Master (PCLKA division ratio set to a value other than 1/2) | $t_H$ | $t_{Pcyc}$ | — | | |
| | | Slave | $t_H$ | 20 | — | | |
| | SSL setup time | Master | $t_{LEAD}$ | $N \times t_{SPcyc} - 10$ *1 | $N \times t_{SPcyc} + 100$ *1 | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | ns | |
| | SSL hold time | Master | $t_{LAG}$ | $N \times t_{SPcyc} - 10$ *2 | $N \times t_{SPcyc} + 100$ *2 | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | ns | |
| | Data output delay | Master | $t_{OD1}$ | — | 6.3 | ns | |
| | | | $t_{OD2}$ | | 6.3 | | |
| | | Slave | $t_{OD}$ | — | 20 | | |
| | Data output hold time | Master | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | 0 | — | | |
| | Successive transmission delay | Master | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | | | |
| | MOSI and MISO rise and fall time | Output | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | |
| | | Input | | — | 1 | μs | |
| | SSL rise and fall time | Output | $t_{SSLr}$, $t_{SSLf}$ | — | 5 | ns | |
| | | Input | | — | 1 | μs | |
| | Slave access time | | $t_{SA}$ | — | 25 | ns | Figure 2.47 and Figure 2.48 |
| | Slave output release time | | $t_{REL}$ | — | 25 | | |

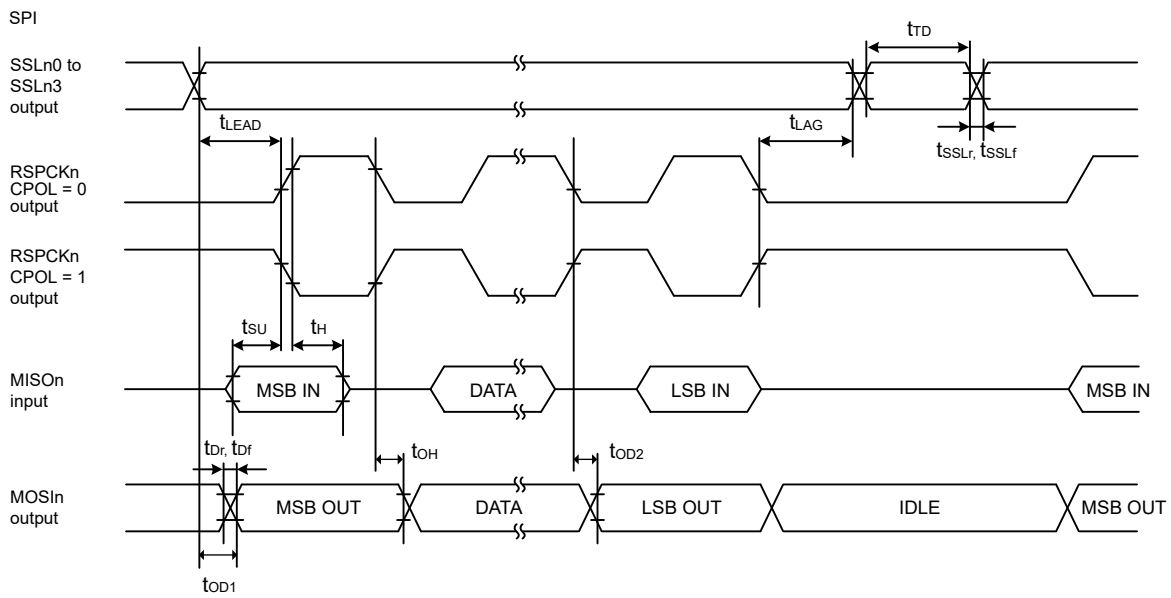
Note: $t_{Pcyc}$: PCLKA cycle.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.




$V_{OH}$ = 0.7 × VCC, $V_{OL}$ = 0.3 × VCC, $V_{IH}$ = 0.7 × VCC, $V_{IL}$ = 0.3 × VCC

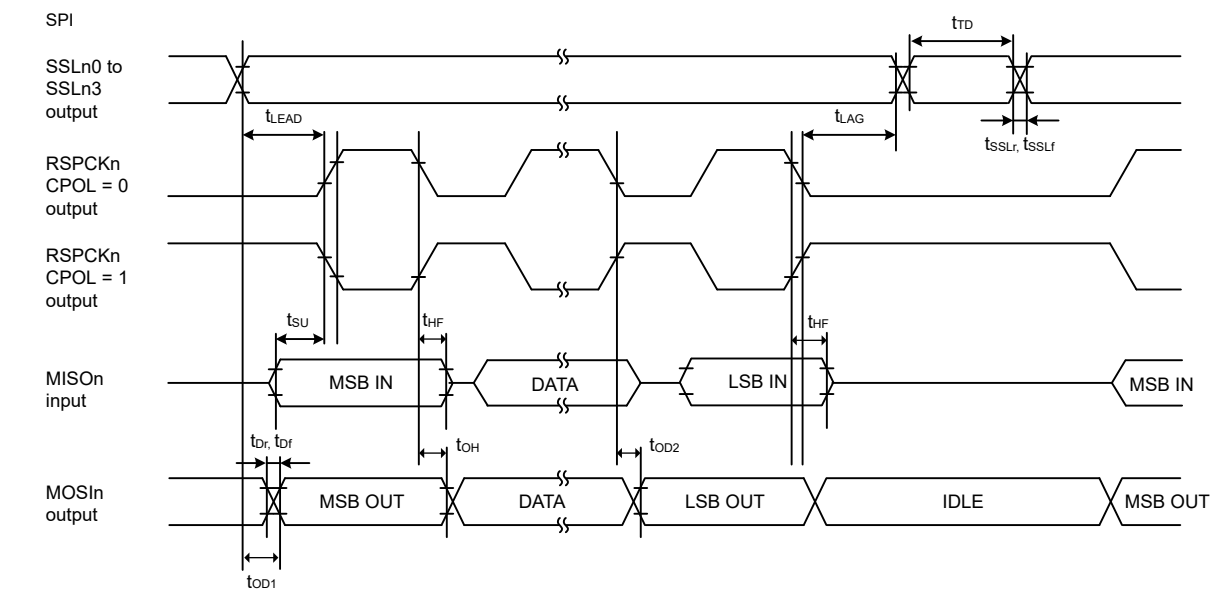
Note: n = A or B

**Figure 2.42 SPI clock timing**



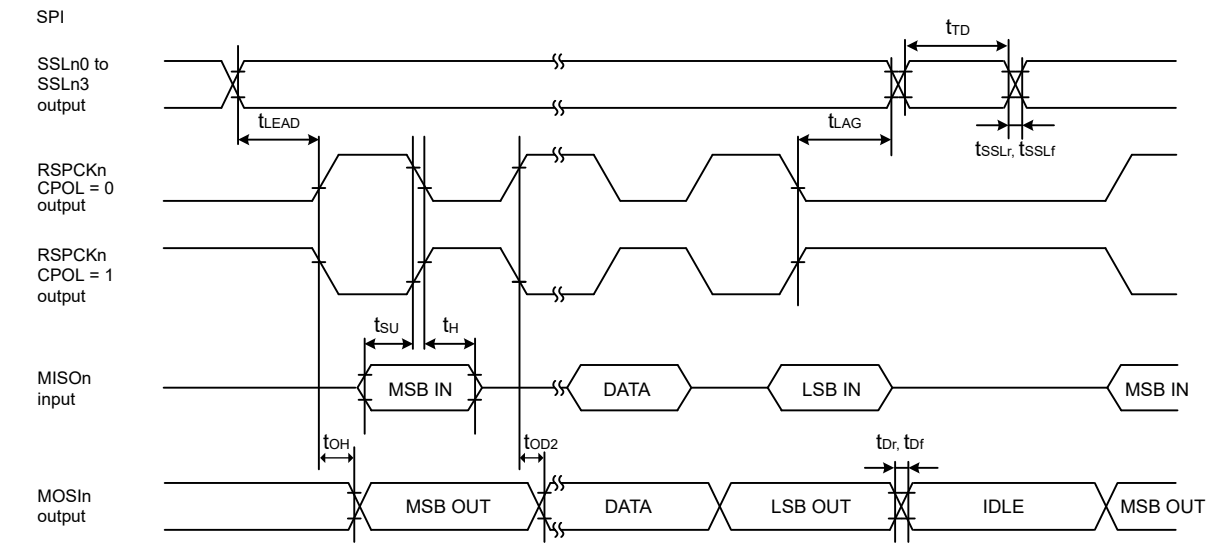

Note: n = A or B

**Figure 2.43 SPI timing for master when CPHA = 0**




Note: n = A or B

**Figure 2.44 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2**




Note: n = A or B

**Figure 2.45 SPI timing for master when CPHA = 1**

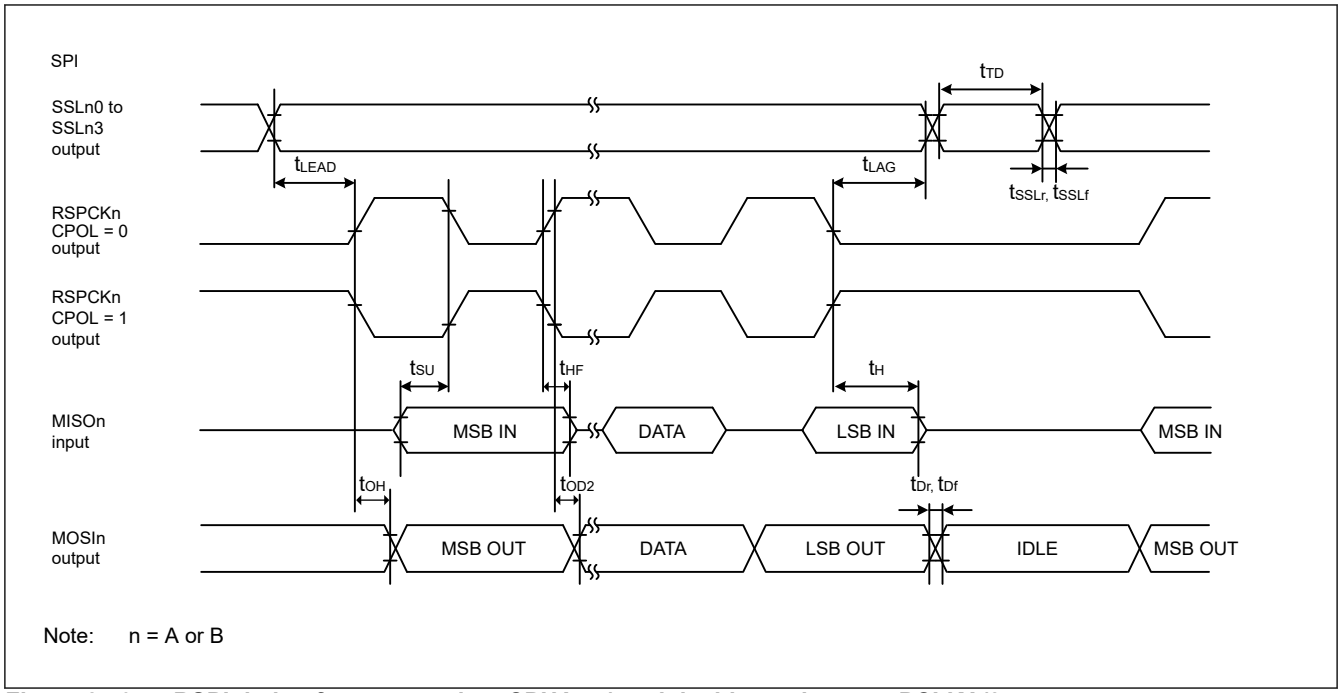



**Figure 2.46 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2**

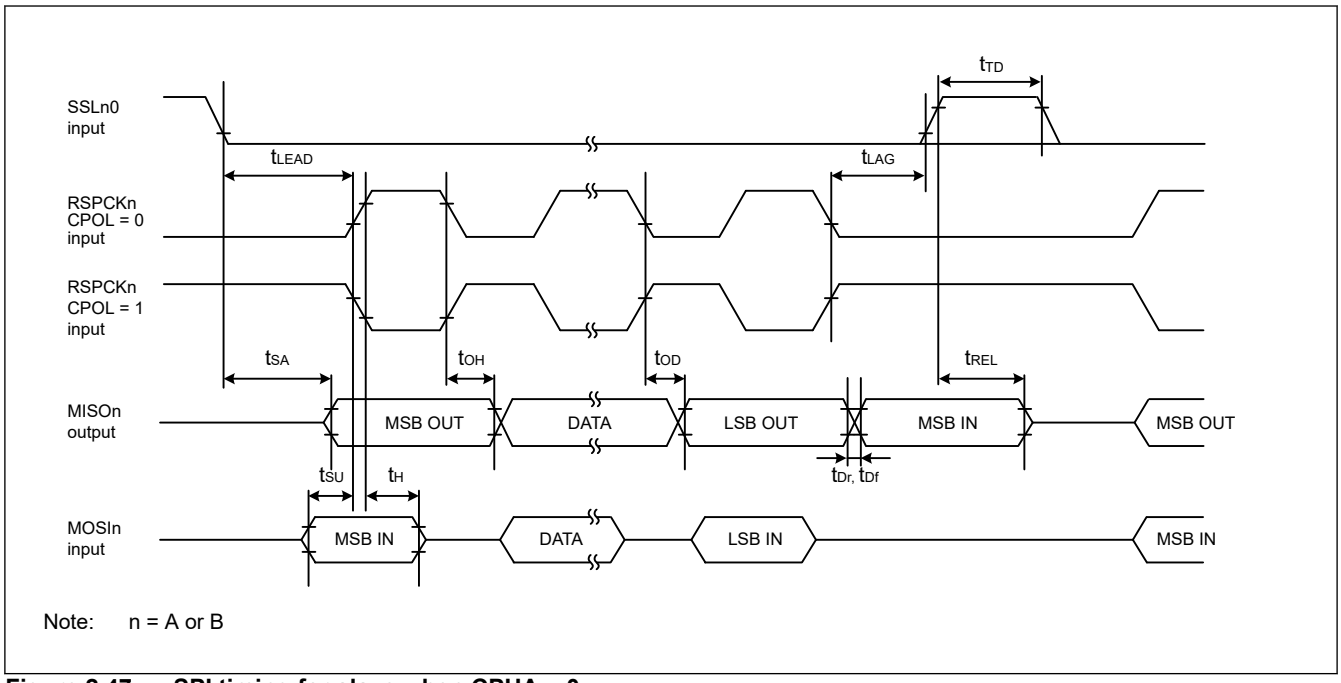
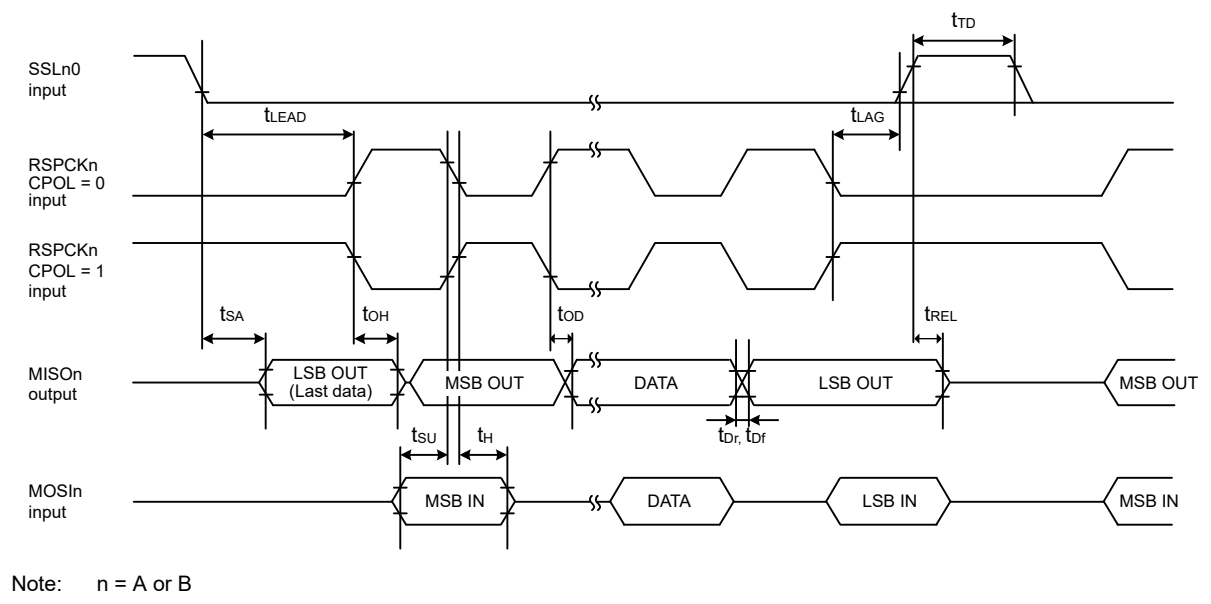



**Figure 2.47 SPI timing for slave when CPHA = 0**




Note: n = A or B

**Figure 2.48 SPI timing for slave when CPHA = 1**

## 2.3.11 QSPI Timing

**Table 2.29 QSPI timing**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| QSPI | QSPCK clock cycle | $t_{QScyc}$ | 2 | 48 | $t_{Pcyc}$ | Figure 2.49 |
| | QSPCK clock high pulse width | $t_{QSWH}$ | $t_{QScyc}$ × 0.4 | — | ns | |
| | QSPCK clock low pulse width | $t_{QSWL}$ | $t_{QScyc}$ × 0.4 | — | ns | |
| | Data input setup time | $t_{Su}$ | 10 | — | ns | Figure 2.50 |
| | Data input hold time | $t_{IH}$ | 0 | — | ns | |
| | QSSL setup time | $t_{LEAD}$ | (N + 0.5) × $t_{Qscyc}$ - 5*1 | (N + 0.5) × $t_{Qscyc}$ + 100*1 | ns | |
| | QSSL hold time | $t_{LAG}$ | (N + 0.5) × $t_{Qscyc}$ - 5*2 | (N + 0.5) × $t_{Qscyc}$ + 100*2 | ns | |
| | Data output delay | $t_{OD}$ | — | 4 | ns | |
| | Data output hold time | $t_{OH}$ | –3.3 | — | ns | |
| | Successive transmission delay | $t_{TD}$ | 1 | 16 | $t_{QScyc}$ | |

Note: $t_{Pcyc}$: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

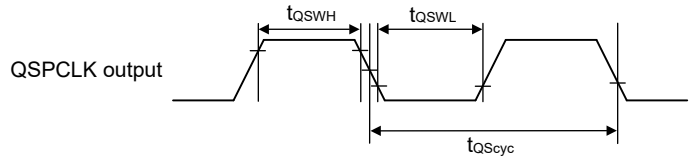



**Figure 2.49 QSPI clock timing**

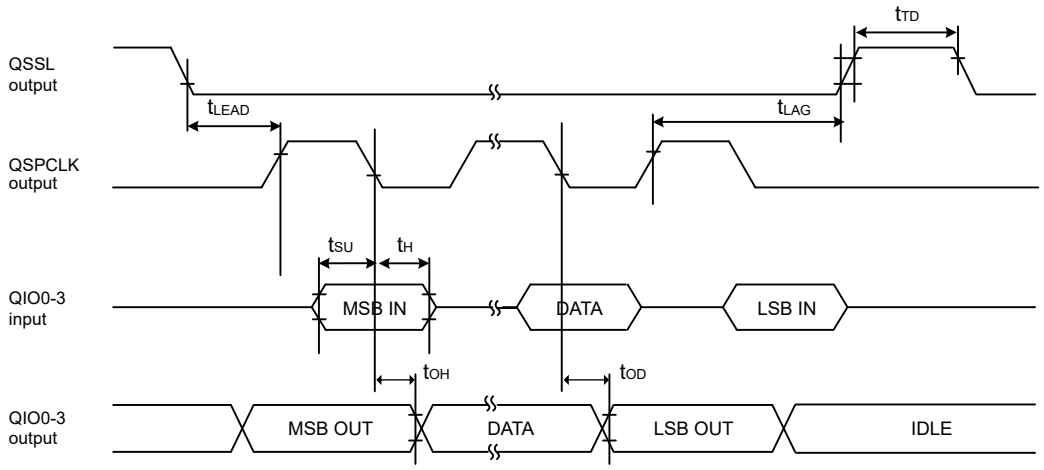



**Figure 2.50 Transmit and receive timing**

## 2.3.12 OSPI Timing

**Table 2.30 OSPI timing (1 of 2)**

(1) Conditions: High speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_SCLK, OM_DQS, OM_SIO0-7.
(2) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_CS0, OM_CS1.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| OM_SCLK clock frequency | SPI | $f_{OCcyc}$ | — | 50 | MHz | Figure 2.51 |
| | SOPI/DOPI | $f_{OCcyc}$ | — | 100 | MHz | |
| OM_SCLK high pulse width | | $t_{OCwh}$ | 0.475 | 0.525 | $t_{OCcyc}$ | |
| OM_SCLK low pulse width | | $t_{OCwl}$ | 0.475 | 0.525 | $t_{OCcyc}$ | |
| OM_SCLK rise time | | $t_{OCr}$ | — | 1.8 | ns | |
| OM_SCLK fall time | | $t_{OCf}$ | — | 1.8 | ns | |
| OM_CS setup time | SPI/SOPI | $t_{OCLEAD}$ | $1.5 \times t_{OCcyc} - 10.4$ (Minimum register settings) | $2.5 \times t_{OCcyc} + 6.9$ (Maximum register settings) | ns | Figure 2.52, Figure 2.53 |
| | DOPI | $t_{OCLEAD}$ | $1.25 \times t_{OCcyc} - 7.9$ (Minimum register settings) | $2.25 \times t_{OCcyc} + 4.4$ (Maximum register settings) | ns | Figure 2.54 |

**Table 2.30 OSPI timing (2 of 2)**

(1) Conditions: High speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_SCLK, OM_DQS, OM_SIO0-7.
(2) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_CS0, OM_CS1.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| OM_CS hold time | SPI/SOPI | $t_{OCLAG}$ | 1 × $t_{OCcyc}$ – 6.9 (Minimum register settings) | 4.5 × $t_{OCcyc}$ + 10.4 (Maximum register settings) | ns | Figure 2.52, Figure 2.53 |
| | DOPI read | $t_{OCLAG}$ | 3.25 × $t_{OCcyc}$ – 4.4 (Minimum register settings) | 4.25 × $t_{OCcyc}$ + 7.9 (Maximum register settings) | ns | Figure 2.54 |
| | DOPI write | $t_{OCLAG}$ | 0.75 × $t_{OCcyc}$ – 4.4 (Minimum register settings) | 4.25 × $t_{OCcyc}$ + 7.9 (Maximum register settings) | ns | |
| Continuous transfer delay time | | $t_{OCTD}$ | 1 × $t_{OCcyc}$ – 1 (Minimum register settings) | 8.5 × $t_{OCcyc}$ + 1 (Maximum register settings) | ns | Figure 2.52, Figure 2.53, Figure 2.54 |
| Data input setup time | SPI SCLK base point | $t_{SU}$ | 10.5 | — | ns | Figure 2.52 |
| Data input hold time | | $t_H$ | 0.5 | — | ns | |
| Data input setup time | SOPI/DOPI DQS base point*1 | $t_{SU}$ | -1.3 | — | ns | Figure 2.53, Figure 2.54 |
| Data input hold time | | $t_H$ | 3.25 | — | ns | |
| Skew of Clock to Data Strobe | | $t_{CKDS}$ | — | 20 | ns | |
| Data output delay time | SPI/SOPI | $t_{OD}$ | — | 2.65 | ns | Figure 2.52, Figure 2.53 |
| Data output hold time | | $t_{OH}$ | -2.65 | — | ns | |
| Data output buffer off time | SOPI | $t_{BOFF}$ | 2.1 | — | ns | Figure 2.53 |
| Data output delay time | DOPI*1 | $t_{OD}$ | — | 3.65 | ns | Figure 2.54, Figure 2.55 |
| Data output hold time | | $t_{OH}$ | 1.1 | — | ns | |
| Data output buffer off time | DOPI | $t_{BOFF}$ | 1.1 | — | ns | Figure 2.54 |
| DQS refresh input setup time | | $t_{DQSS}$ | 20 | — | ns | Figure 2.56 |
| DQS refresh input hold time | | $t_{DQSH}$ | 0.5 × tOCcyc | — | ns | |

Note: $t_{OCcyc}$ indicates the OM_SCLK cycle.
Note 1. OM_SCLK frequency: 100 MHz

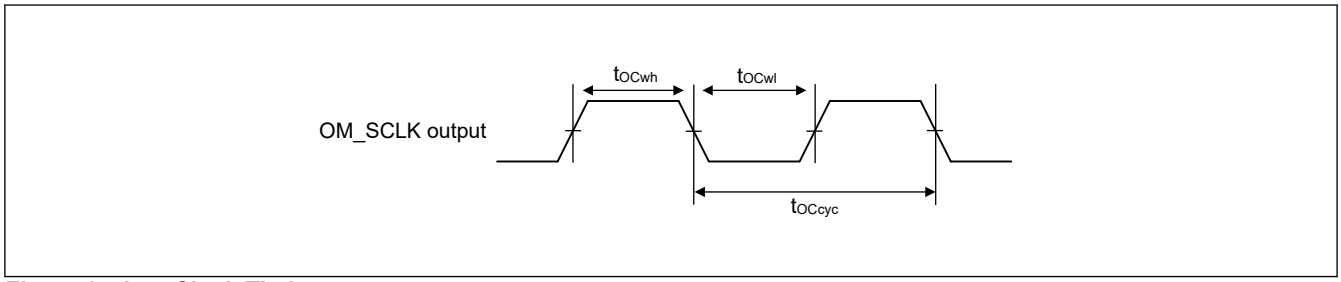



**Figure 2.51 Clock Timing**

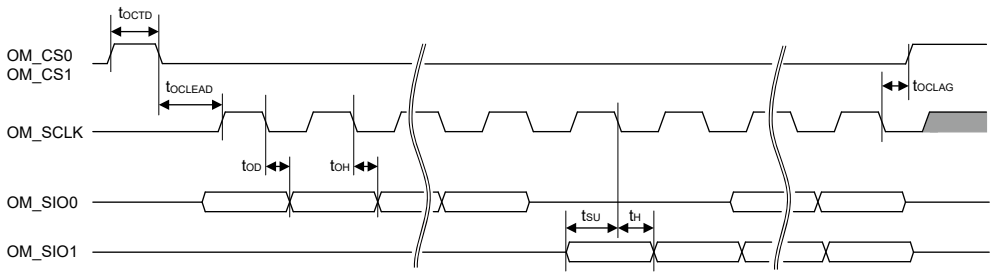



**Figure 2.52 SPI Transfer Format Transmission and Reception Timing**

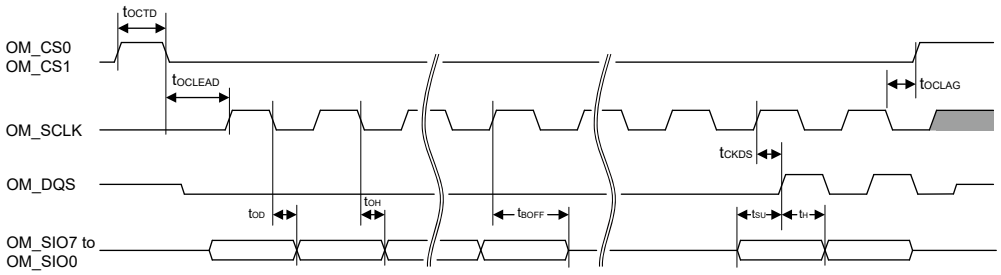



**Figure 2.53 SOPI Transfer Format Transmission and Reception Timing**

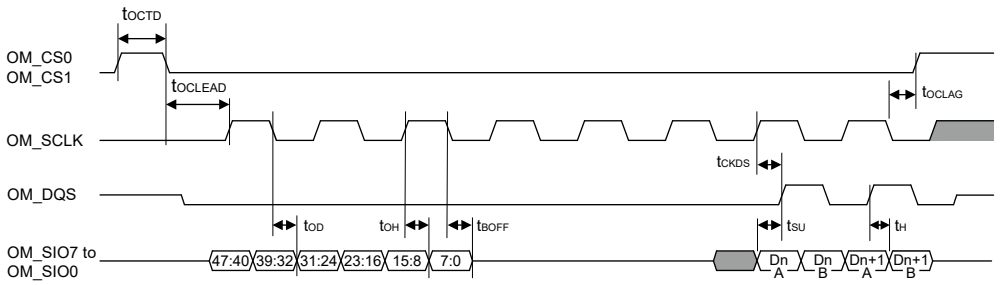



**Figure 2.54 DOPI Transfer Format Transmission and Reception Timing**

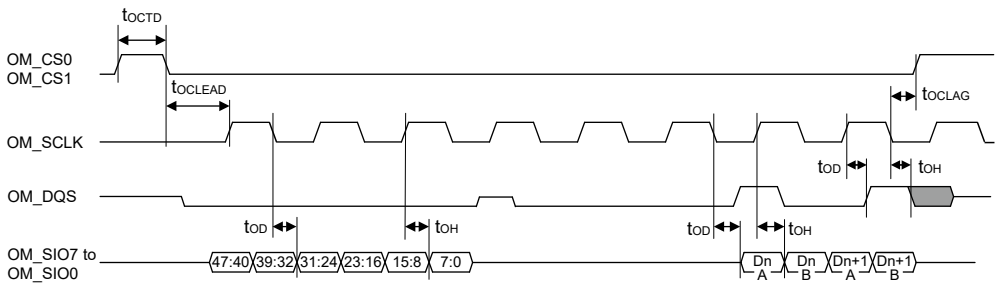



**Figure 2.55 DOPI Transfer Format Transmission Timing**

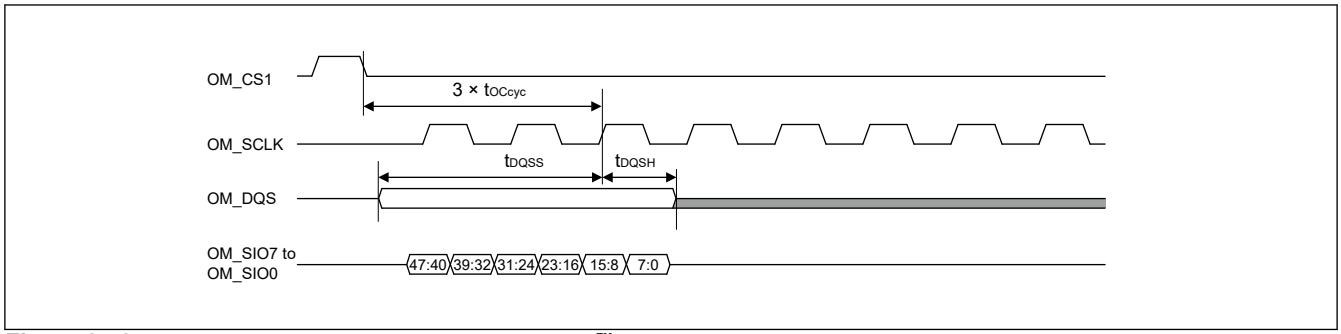



**Figure 2.56 DQS Refresh input Timing (OctaRAM™ Read/Write)**

## 2.3.13 IIC Timing

**Table 2.31 IIC timing (1) (1 of 2)**

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 2.57 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | — | ns | |
| | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | — | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

**Table 2.31 IIC timing (1) (2 of 2)**

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | — | ns | Figure 2.57 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA rise time | $t_{Sr}$ | 20 × (external pullup voltage/5.5V)*1 | 300 | ns | |
| | SCL, SDA fall time | $t_{Sf}$ | 20 × (external pullup voltage/5.5V)*1 | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | — | ns | |
| | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | — | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

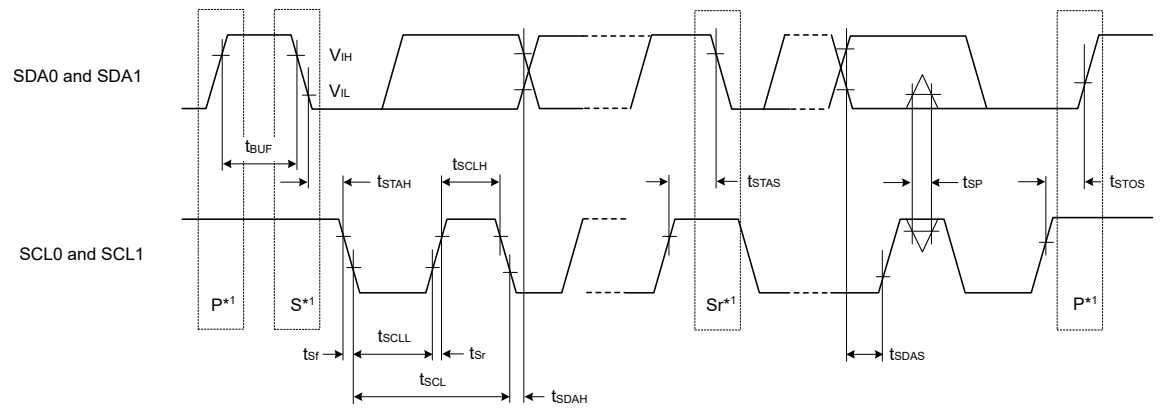
Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, and SDA1_A.

**Table 2.32 IIC timing (2)**

Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 240 | — | ns | Figure 2.57 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL, SDA rise time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA fall time | $t_{Sf}$ | 20 × (external pullup voltage/ 5.5V) | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × tIICcyc | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 120 | — | ns | |
| | Start condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 120 | — | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 120 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 120 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 30 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ *1 | — | 550 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 1. Cb indicates the total capacity of the bus line.




Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

**Figure 2.57 I²C bus interface input/output timing**

## 2.3.14 SSIE Timing

**Table 2.33 SSIE timing**

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | | Symbol | Target specification | | Unit | Comments |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| SSIBCK0 | Cycle | Master | $t_O$ | 80 | — | ns | Figure 2.58 |
| | | Slave | $t_I$ | 80 | — | ns | |
| | High level/ low level | Master | $t_{HC}/t_{LC}$ | 0.35 | — | $t_O$ | |
| | | Slave | | 0.35 | — | $t_I$ | |
| | Rising time/ falling time | Master | $t_{RC}/t_{FC}$ | — | 0.15 | $t_O$ / $t_I$ | |
| | | Slave | | — | 0.15 | $t_O$ / $t_I$ | |
| SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0, SSIDATA0 | Input set up time | Master | $t_{SR}$ | 12 | — | ns | Figure 2.60, Figure 2.61 |
| | | Slave | | 12 | — | ns | |
| | Input hold time | Master | $t_{HR}$ | 8 | — | ns | |
| | | Slave | | 15 | — | ns | |
| | Output delay time | Master | $t_{DTR}$ | -10 | 5 | ns | |
| | | Slave | | 0 | 20 | ns | Figure 2.60, Figure 2.61 |
| | Output delay time from SSILRCK0/ SSIFS0 change | Slave | $t_{DTRW}$ | — | 20 | ns | Figure 2.62*1 |
| GTIOC2A, AUDIO_CLK | Cycle | | $t_{EXcyc}$ | 20 | — | ns | Figure 2.59 |
| | High level/ low level | | $t_{EXL}/t_{EXH}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA0 pin.

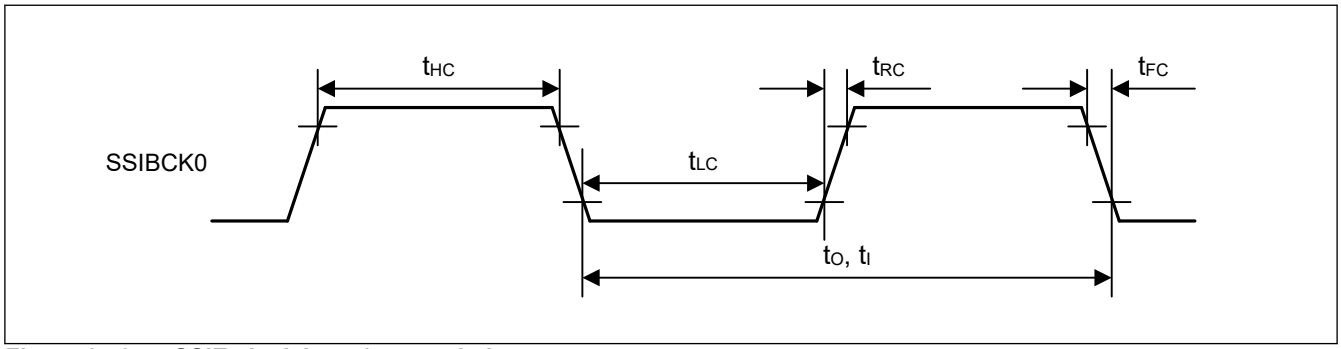



**Figure 2.58 SSIE clock input/output timing**

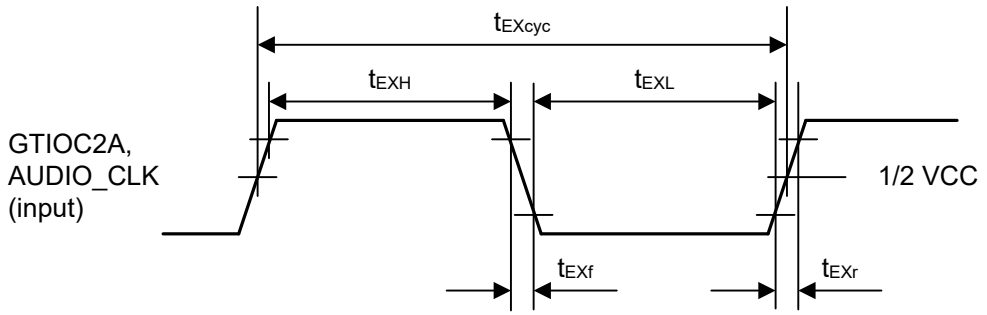



**Figure 2.59 Clock input timing**

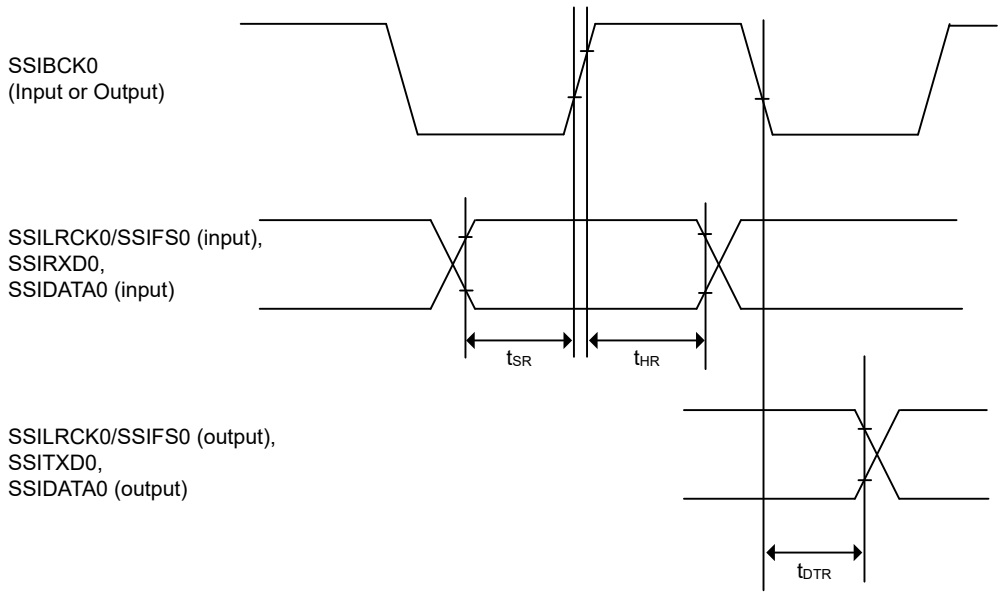



**Figure 2.60 SSIE data transmit and receive timing when SSICR.BCKP = 0**

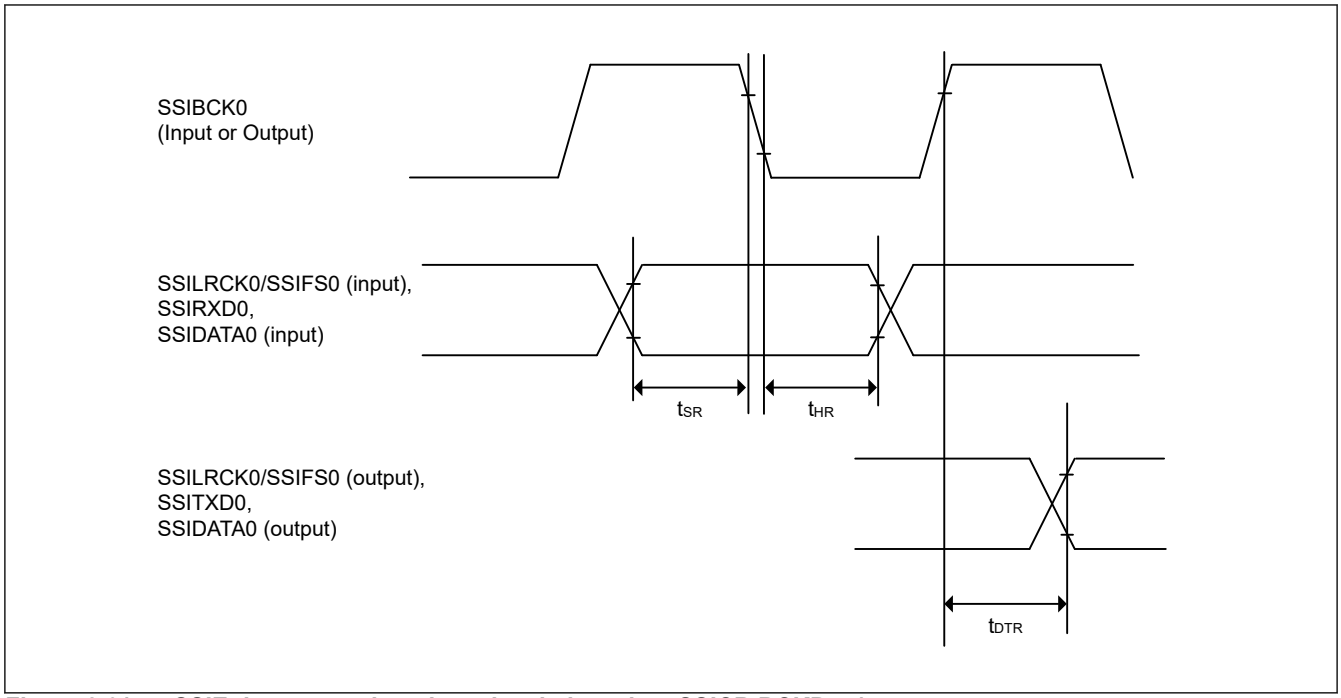



**Figure 2.61 SSIE data transmit and receive timing when SSICR.BCKP = 1**

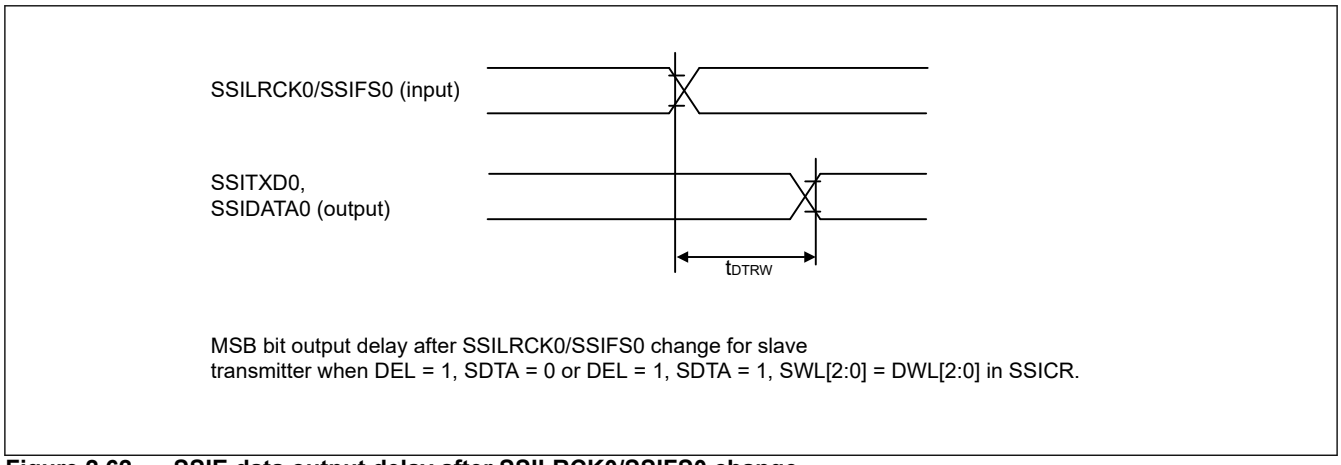



**Figure 2.62 SSIE data output delay after SSILRCK0/SSIFS0 change**

## 2.3.15 SD/MMC Host Interface Timing

**Table 2.34 SD/MMC Host Interface signal timing**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Clock duty ratio is 50%.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| SDCLK clock cycle | $T_{SDCYC}$ | 20 | — | ns | Figure 2.63 |
| SDCLK clock high pulse width | $T_{SDWH}$ | 6.5 | — | ns | |
| SDCLK clock low pulse width | $T_{SDWL}$ | 6.5 | — | ns | |
| SDCLK clock rise time | $T_{SDLH}$ | — | 3 | ns | |
| SDCLK clock fall time | $T_{SDHL}$ | — | 3 | ns | |
| SDCMD/SDDAT output data delay | $T_{SDODLY}$ | –7 | 4 | ns | |
| SDCMD/SDDAT input data setup | $T_{SDIS}$ | 4.5 | — | ns | |
| SDCMD/SDDAT input data hold | $T_{SDIH}$ | 1.5 | — | ns | |

Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

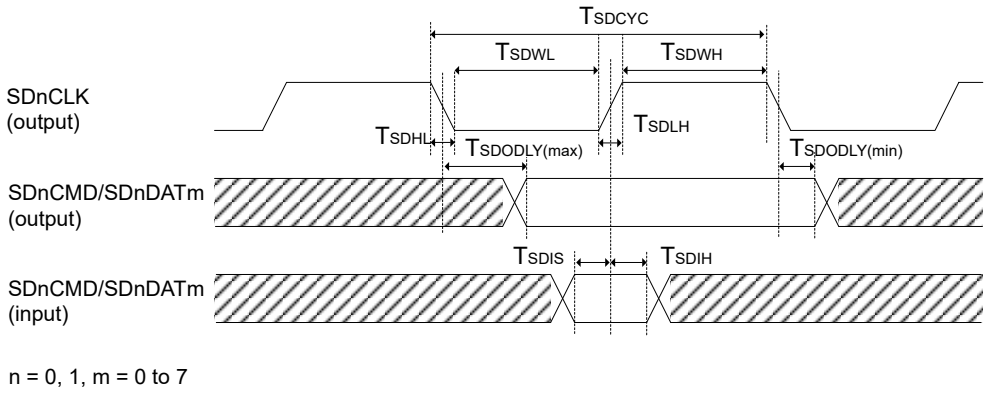



**Figure 2.63 SD/MMC Host Interface signal timing**

## 2.3.16 ETHERC Timing

**Table 2.35 ETHERC timing (1 of 2)**

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

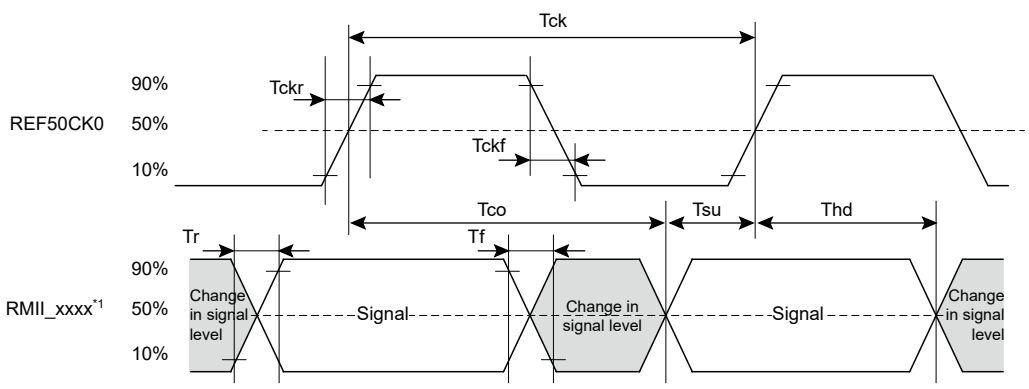
| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| ETHERC (RMII) | REF50CK0 cycle time | $T_{ck}$ | 20 | — | ns | Figure 2.64 to Figure 2.67 |
| | REF50CK0 frequency, typical 50 MHz | — | — | 50 + 100 ppm | MHz | |
| | REF50CK0 duty | — | 35 | 65 | % | |
| | REF50CK0 rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII_xxxx*1 output delay | $T_{co}$ | 2.5 | 12.0 | ns | |
| | RMII_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII_xxxx*1, *2 rise/fall time | $T_r/T_f$ | 0.5 | 4 | ns | |
| | ET0_WOL output delay | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 2.68 |

**Table 2.35 ETHERC timing (2 of 2)**

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| ETHERC (MII) | ET0_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET0_TX_EN output delay | $t_{TENd}$ | 1 | 20 | ns | Figure 2.69 |
| | ET0_ETXD0 to ET_ETXD3 output delay | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET0_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET0_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET0_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 2.70 |
| | ET0_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET0_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET0_RX_DV setup time | $t_{RDVs}$ | 10 | — | ns | Figure 2.71 |
| | ET0_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET0_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 2.72 |
| | ET0_RX_ER hold time | $t_{RESh}$ | 10 | — | ns | |
| | ET0_WOL output delay | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 2.73 |

Note: The following pins must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B.
Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.




Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

**Figure 2.64 REF50CK0 and RMII signal timing**

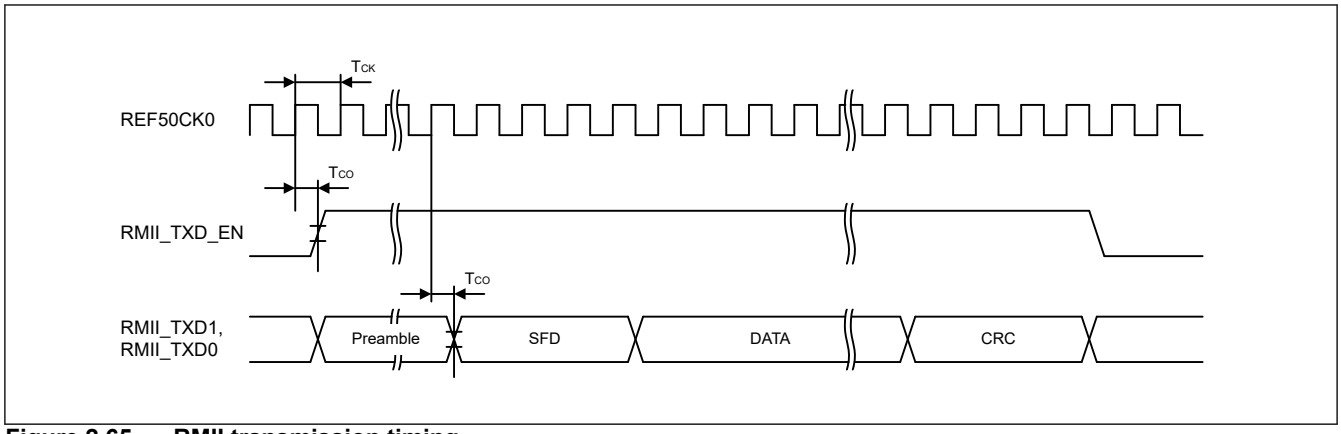



**Figure 2.65 RMII transmission timing**

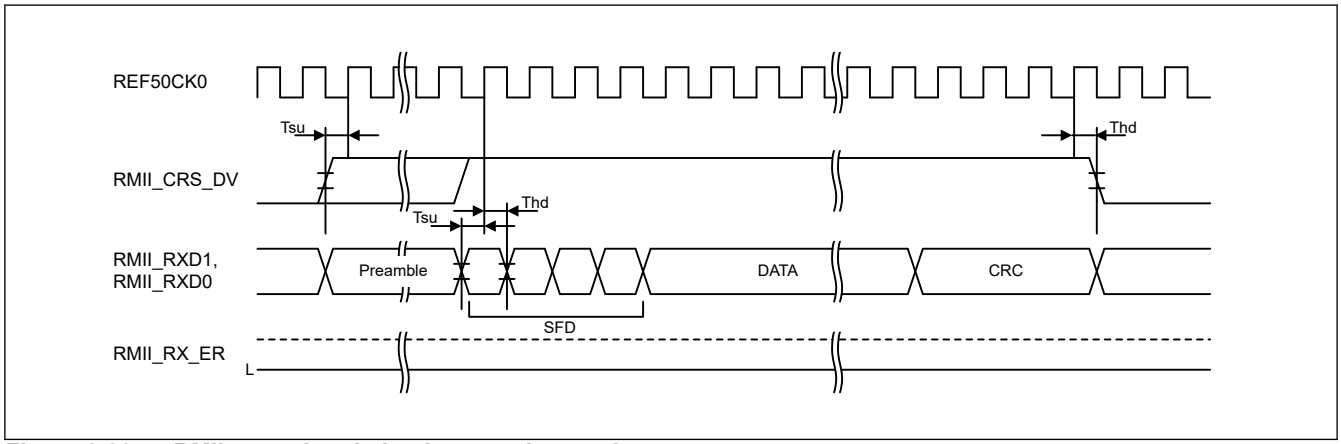



**Figure 2.66 RMII reception timing in normal operation**

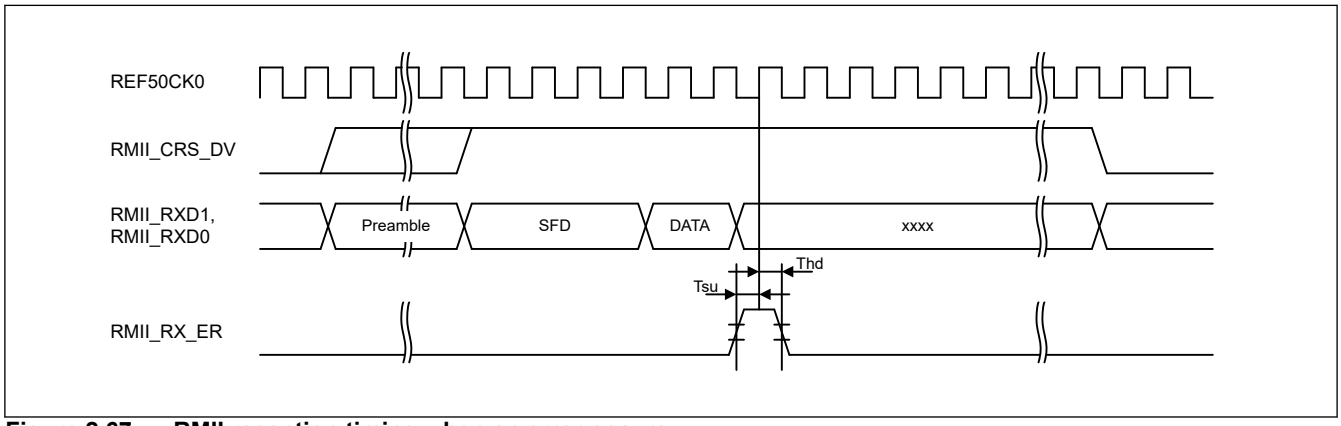



**Figure 2.67 RMII reception timing when an error occurs**

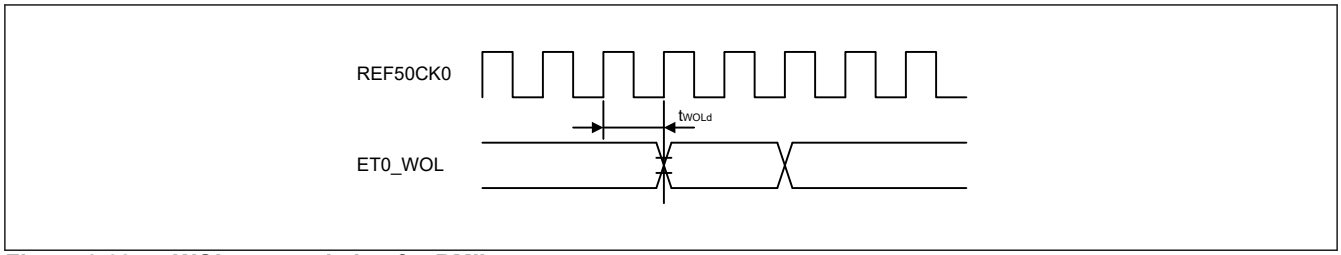



**Figure 2.68 WOL output timing for RMII**

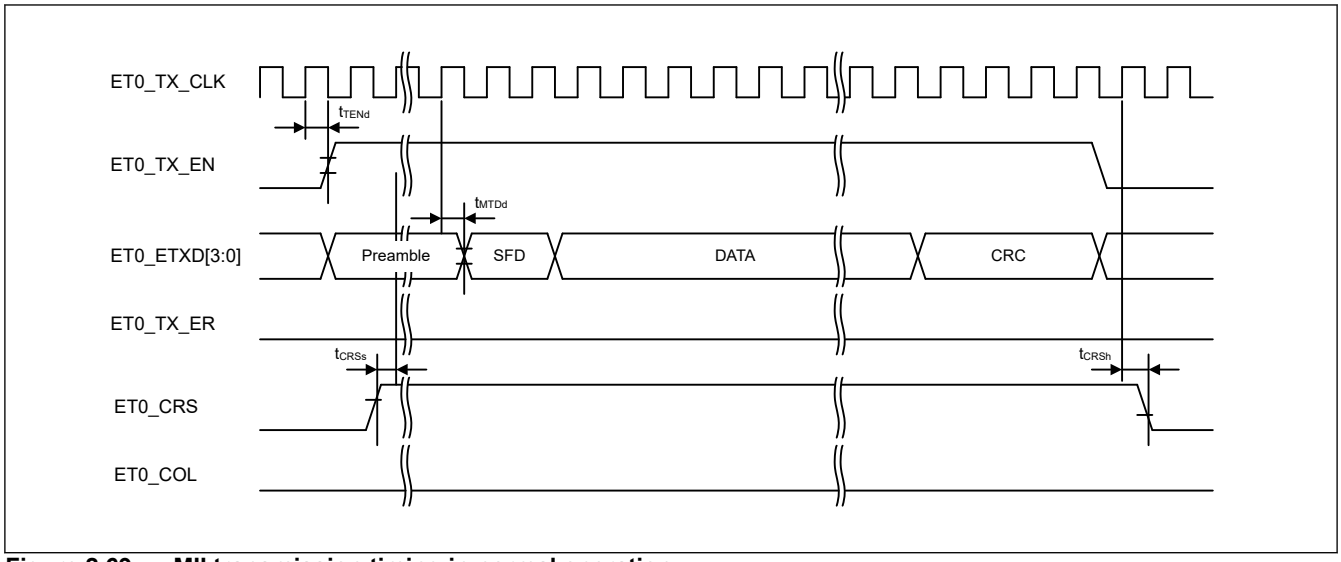



**Figure 2.69 MII transmission timing in normal operation**

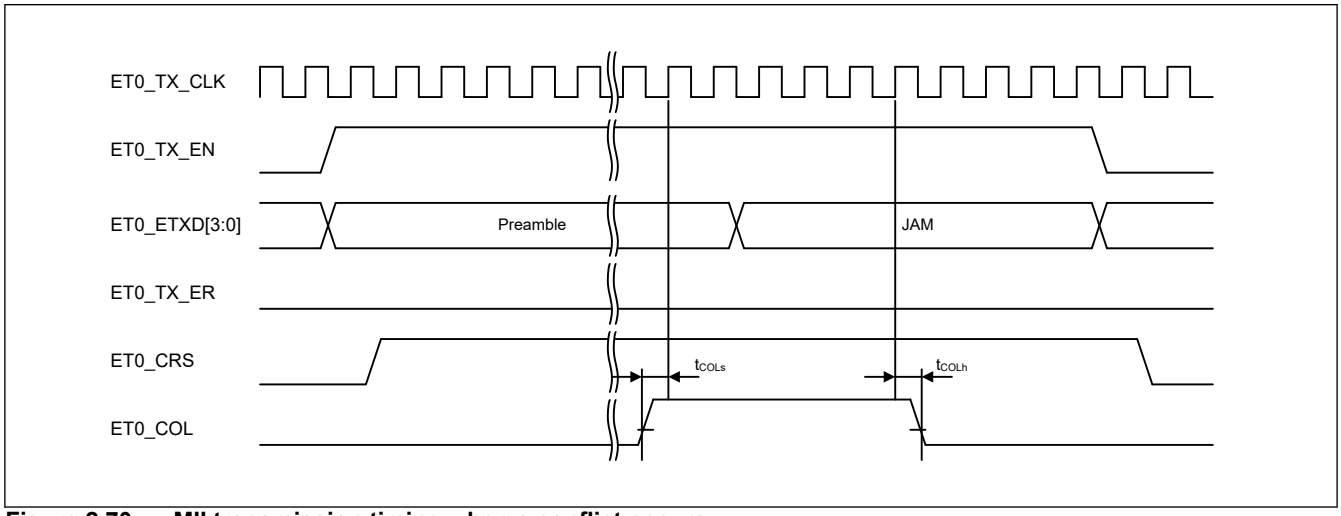



**Figure 2.70 MII transmission timing when a conflict occurs**

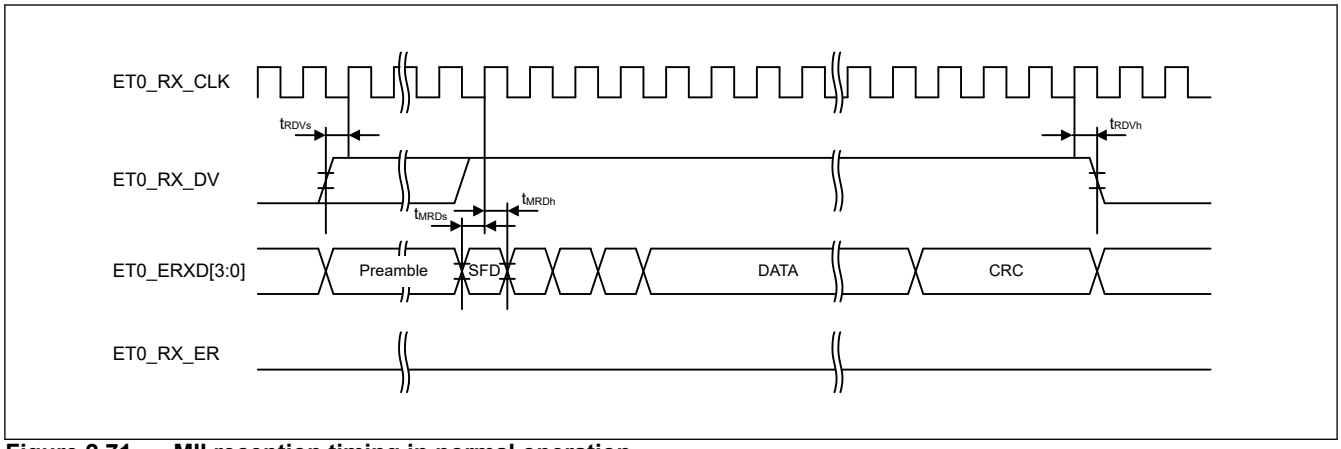



**Figure 2.71 MII reception timing in normal operation**

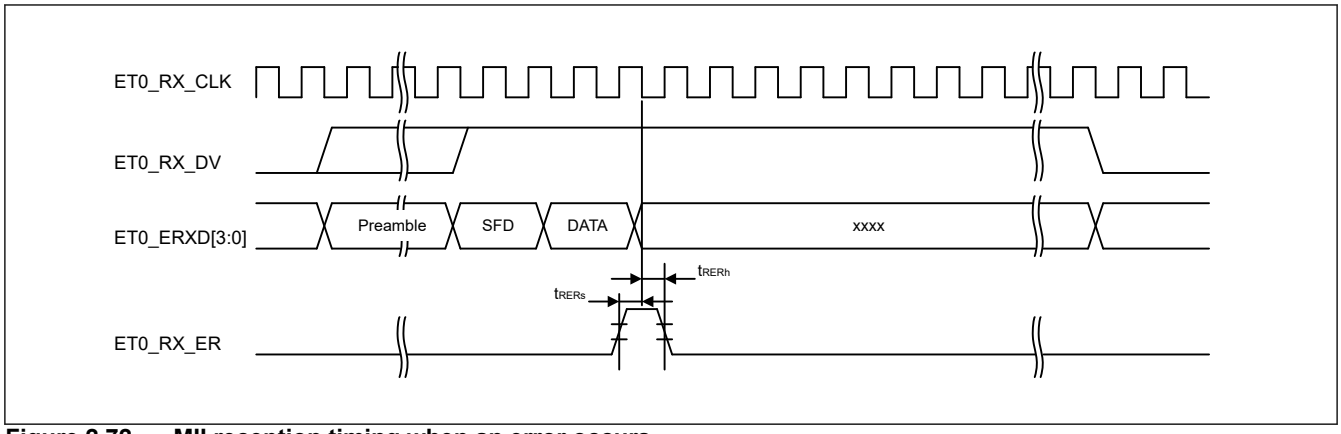



**Figure 2.72 MII reception timing when an error occurs**

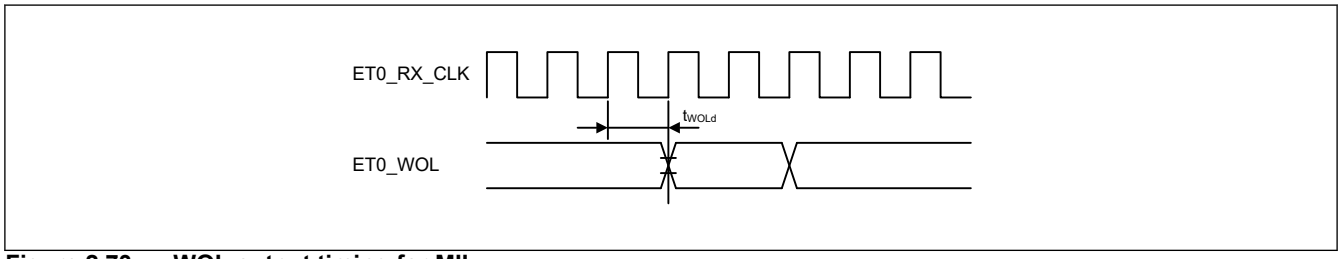



**Figure 2.73 WOL output timing for MII**

## 2.4 USB Characteristics

### 2.4.1 USBFS Timing

**Table 2.36 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)**

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high voltage | $V_{IH}$ | 2.0 | — | — | V | — |
| | Input low voltage | $V_{IL}$ | — | — | 0.8 | V | — |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| USB_DP - USB_DM \| |
| | Differential common-mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | — |
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 μA |
| | Output low voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 2.74 |
| | Rise time | $t_{LR}$ | 75 | — | 300 | ns | |
| | Fall time | $t_{LF}$ | 75 | — | 300 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 80 | — | 125 | % | $t_{LR}$/ $t_{LF}$ |
| Pull-up and pull-down characteristics | USB_DP and USB_DM pull-down resistance in host controller mode | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | — |

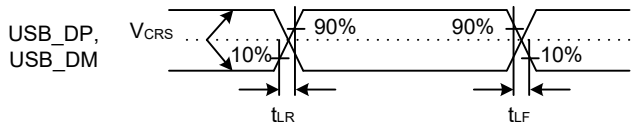



**Figure 2.74 USB_DP and USB_DM output timing in low-speed mode**

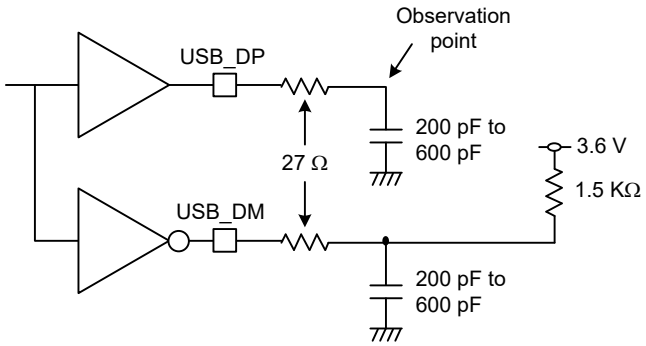



**Figure 2.75 Test circuit in low-speed mode**

**Table 2.37 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)**

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high voltage | $V_{IH}$ | 2.0 | — | — | V | — |
| | Input low voltage | $V_{IL}$ | — | — | 0.8 | V | — |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| USB_DP - USB_DM \| |
| | Differential common-mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | — |
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 μA |
| | Output low voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 2.76 |
| | Rise time | $t_{LR}$ | 4 | — | 20 | ns | |
| | Fall time | $t_{LF}$ | 4 | — | 20 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 90 | — | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | — | 44 | Ω | USBFS: Rs = 27 Ω included |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | $R_{pu}$ | 0.900 | — | 1.575 | kΩ | During idle state |
| | | | 1.425 | — | 3.090 | kΩ | During transmission and reception |
| | USB_DP and USB_DM pull-down resistance in host controller mode | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | — |

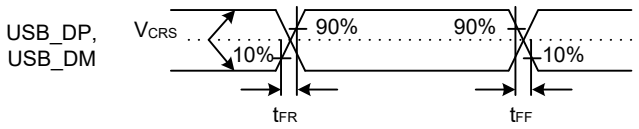



**Figure 2.76 USB_DP and USB_DM output timing in full-speed mode**

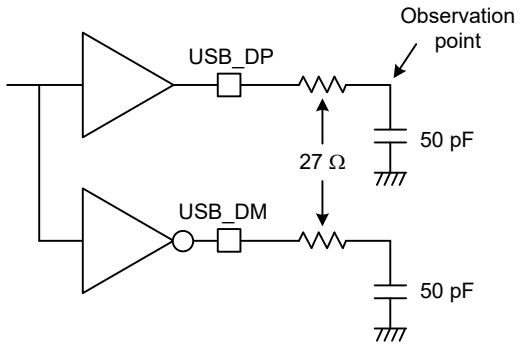



**Figure 2.77 Test circuit in full-speed mode**

**Table 2.38 USBFS characteristics (USB_DP and USB_DM pin characteristics)**

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Battery Charging Specification | D+ sink current | $I_{DP_SINK}$ | 25 | — | 175 | μA | — |
| | D- sink current | $I_{DM_SINK}$ | 25 | — | 175 | μA | — |
| | DCD source current | $I_{DP_SRC}$ | 7 | — | 13 | μA | — |
| | Data detection voltage | $V_{DAT_REF}$ | 0.25 | — | 0.4 | V | — |
| | D+ source voltage | $V_{DP_SRC}$ | 0.5 | — | 0.7 | V | Outout current = 250 μA |
| | D- source voltage | $V_{DM_SRC}$ | 0.5 | — | 0.7 | V | Outout current = 250 μA |

## 2.5 ADC12 Characteristics

**Table 2.39 A/D conversion characteristics for unit 0 (1 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Frequency | 1 | — | 50 | MHz | — |
| Analog input capacitance | — | — | 30 | pF | — |
| Quantization error | — | ±0.5 | — | LSB | — |
| Resolution | — | — | 12 | Bits | — |

**Table 2.39 A/D conversion characteristics for unit 0 (2 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| High-precision high-speed channels (AN000 to AN005) | Conversion time*1 (operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.52 (0.26)*2 | — | — | μs | Sampling in 13 states |
| | | Max. = 400 Ω | 0.40 (0.14)*2 | — | — | μs | Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±2.5 | LSB | — |
| High-precision normal-speed channels (AN006 to AN009, AN012, AN013) | Conversion time*1 (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66)*2 | — | — | μs | Sampling in 33 states |
| | Offset error | | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±2.5 | LSB | — |

Note: These specification values apply when there is no access to the external memory during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note: When both unit0 and unit1 are used, do not select the following analog input combinations at the same time except the interleave function. If selected, values might not fall within the indicated ranges.
- AN100 and AN000 or AN001 or AN002
- AN101 and AN000 or AN001 or AN002 or AN003
- AN102 and AN000 or AN001 or AN002 or AN003 or AN004

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

**Table 2.40 A/D conversion characteristics for unit 1 (1 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Frequency | 1 | — | 50 | MHz | — |
| Analog input capacitance | — | — | 30 | pF | — |
| Quantization error | — | ±0.5 | — | LSB | — |
| Resolution | — | — | 12 | Bits | — |

**Table 2.40 A/D conversion characteristics for unit 1 (2 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| High-precision high-speed channels (AN100 to AN102) | Conversion time*1 (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.52 (0.26)*2 | — | — | μs | Sampling in 13 states |
| | | Max. = 400 Ω | 0.40 (0.14)*2 | — | — | μs | Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0 |
| | Offset error | | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±2.5 | LSB | — |
| Normal-precision normal-speed channels (AN116 to AN122) | Conversion time*1 (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66)*2 | — | — | μs | Sampling in 33 states |
| | Offset error | | — | ±1.0 | ±5.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±5.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±7.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±4.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±5.5 | LSB | — |

Note: These specification values apply when there is no access to the external memory during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note: When both unit0 and unit1 are used, do not select the following analog input combinations at the same time except the interleave function. If selected, values might not fall within the indicated ranges.
- AN100 and AN000 or AN001 or AN002
- AN101 and AN000 or AN001 or AN002 or AN003
- AN102 and AN000 or AN001 or AN002 or AN003 or AN004

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

**Table 2.41 A/D conversion characteristics for interleaving (1 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Frequency | 1 | — | 50 | MHz | — |
| Analog input capacitance | — | — | 30 | pF | — |
| Quantization error | — | ±0.5 | — | LSB | — |
| Resolution | — | — | 12 | Bits | — |

**Table 2.41 A/D conversion characteristics for interleaving (2 of 2)**

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| High-precision high-speed channels (AN000 & AN100, AN001 & AN101, AN002 & AN102)) | Conversion time*1 (operation at PCLKC = 50 MHz) | Max. = 400 Ω | 0.22 | — | — | μs | Sampling in 9 states<br>VCC = AVCC0 = 3.0 to 3.6 V<br>3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±4.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±4.5 | LSB | — |

Note: These specification values apply when there is no access to the external memory during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

**Table 2.42 A/D internal reference voltage characteristics**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | — |
| Sampling time | 4.15 | — | — | μs | — |

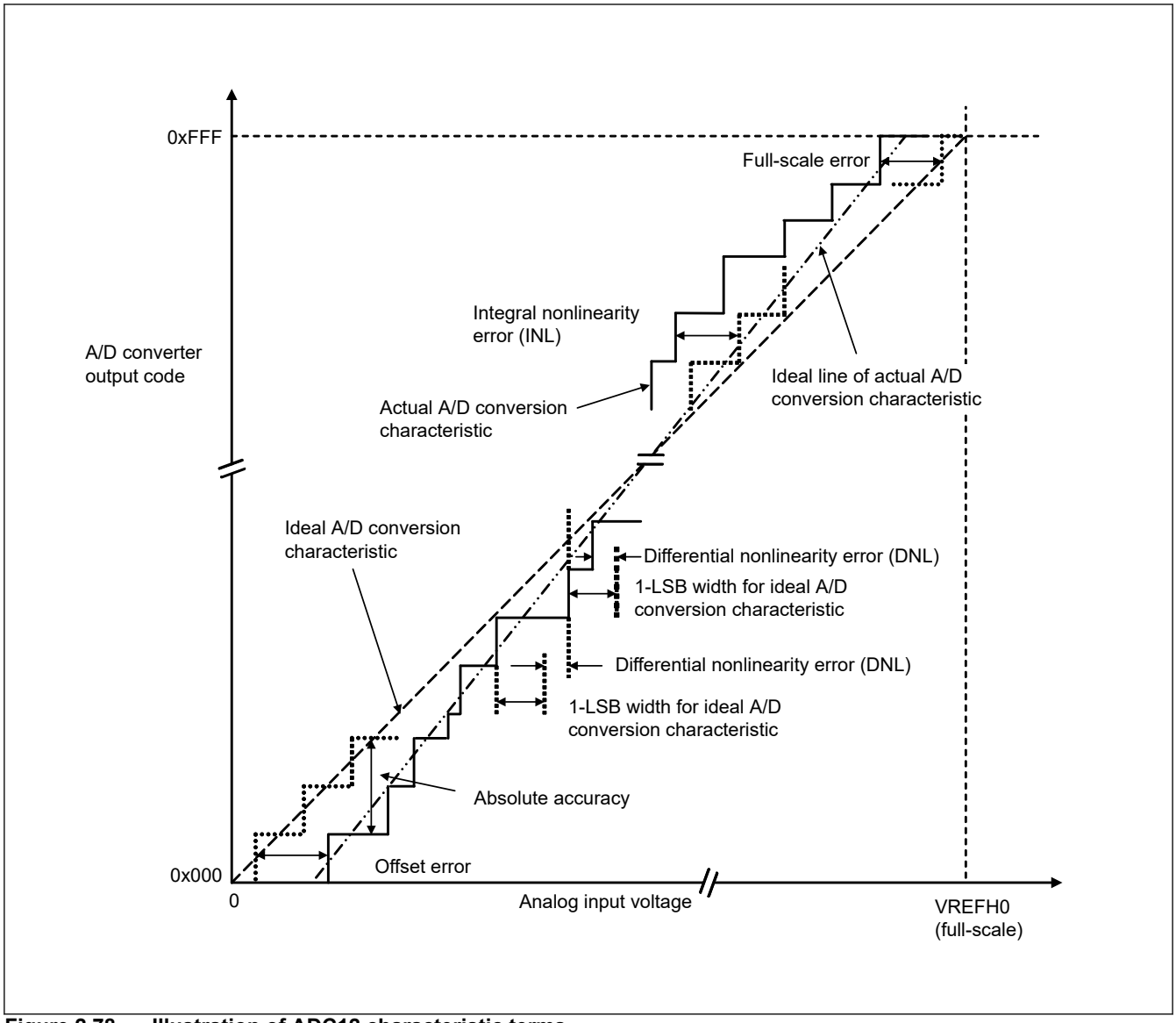



**Figure 2.78 Illustration of ADC12 characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

## 2.6 DAC12 Characteristics

**Table 2.43 D/A conversion characteristics**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | — | — | 12 | Bits | — |
| Without output amplifier | | | | | |
| Absolute accuracy | — | — | ±24 | LSB | Resistive load 2 MΩ |
| INL | — | ±2.0 | ±8.0 | LSB | Resistive load 2 MΩ |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Output impedance | — | 8.5 | — | kΩ | — |
| Conversion time | — | — | 3 | μs | Resistive load 2 MΩ, Capacitive load 20 pF |
| Output voltage range | 0 | — | VREFH | V | — |
| With output amplifier | | | | | |
| INL | — | ±2.0 | ±4.0 | LSB | — |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Conversion time | — | — | 4.0 | μs | — |
| Resistive load | 5 | — | — | kΩ | — |
| Capacitive load | — | — | 50 | pF | — |
| Output voltage range | 0.2 | — | VREFH – 0.2 | V | — |

## 2.7 TSN Characteristics

**Table 2.44 TSN characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Relative accuracy | — | — | ± 1.0 | — | °C | — |
| Temperature slope | — | — | 4.0 | — | mV/°C | — |
| Output voltage (at 25 °C) | — | — | 1.24 | — | V | — |
| Temperature sensor start time | $t_{START}$ | — | — | 30 | μs | — |
| Sampling time | — | 4.15 | — | — | μs | — |

## 2.8 OSC Stop Detect Characteristics

**Table 2.45 Oscillation stop detection circuit characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 2.79 |

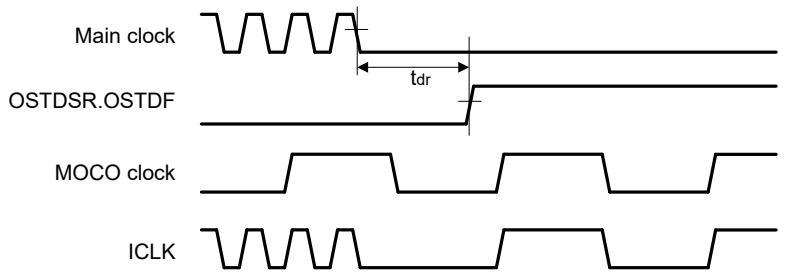



**Figure 2.79 Oscillation stop detection timing**

## 2.9 POR and LVD Characteristics

**Table 2.46 Power-on reset circuit and voltage detection circuit characteristics (1)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | $V_{POR}$ | 2.5 | 2.6 | 2.7 | V | Figure 2.80 |
| | | DPSBYCR.DEEPCUT[1:0] = 11b. | | 1.8 | 2.25 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | $V_{det0_1}$ | 2.84 | 2.94 | 3.04 | | Figure 2.81 |
| | | | $V_{det0_2}$ | 2.77 | 2.87 | 2.97 | | |
| | | | $V_{det0_3}$ | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | | $V_{det1_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.82 |
| | | | $V_{det1_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det1_3}$ | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | | $V_{det2_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.83 |
| | | | $V_{det2_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det2_3}$ | 2.75 | 2.85 | 2.95 | | |
| Internal reset time | Power-on reset time | | $t_{POR}$ | — | 4.5 | — | ms | Figure 2.80 |
| | LVD0 reset time | | $t_{LVD0}$ | — | 0.51 | — | | Figure 2.81 |
| | LVD1 reset time | | $t_{LVD1}$ | — | 0.38 | — | | Figure 2.82 |
| | LVD2 reset time | | $t_{LVD2}$ | — | 0.38 | — | | Figure 2.83 |
| Minimum VCC down time*1 | | | $t_{VOFF}$ | 200 | — | — | μs | Figure 2.80, Figure 2.81 |
| Response delay | | | $t_{det}$ | — | — | 200 | μs | Figure 2.81 to Figure 2.83 |
| LVD operation stabilization time (after LVD is enabled) | | | $t_{d(E-A)}$ | — | — | 10 | μs | Figure 2.82, Figure 2.83 |
| Hysteresis width (LVD1 and LVD2) | | | $V_{LVH}$ | — | 70 | — | mV | |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det0}$, $V_{det1}$, and $V_{det2}$ for POR and LVD.

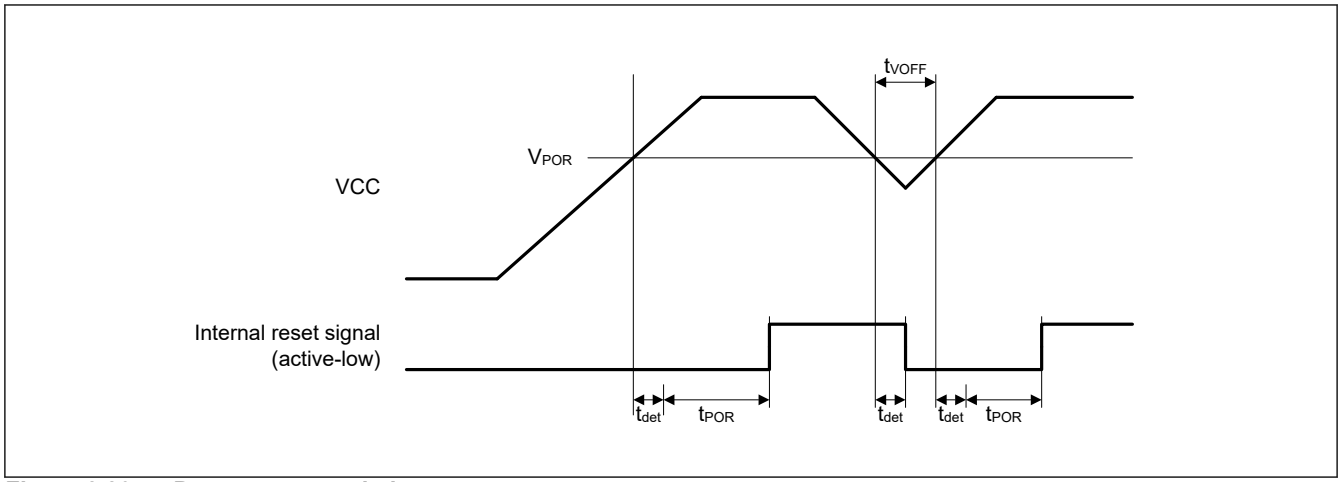



**Figure 2.80 Power-on reset timing**

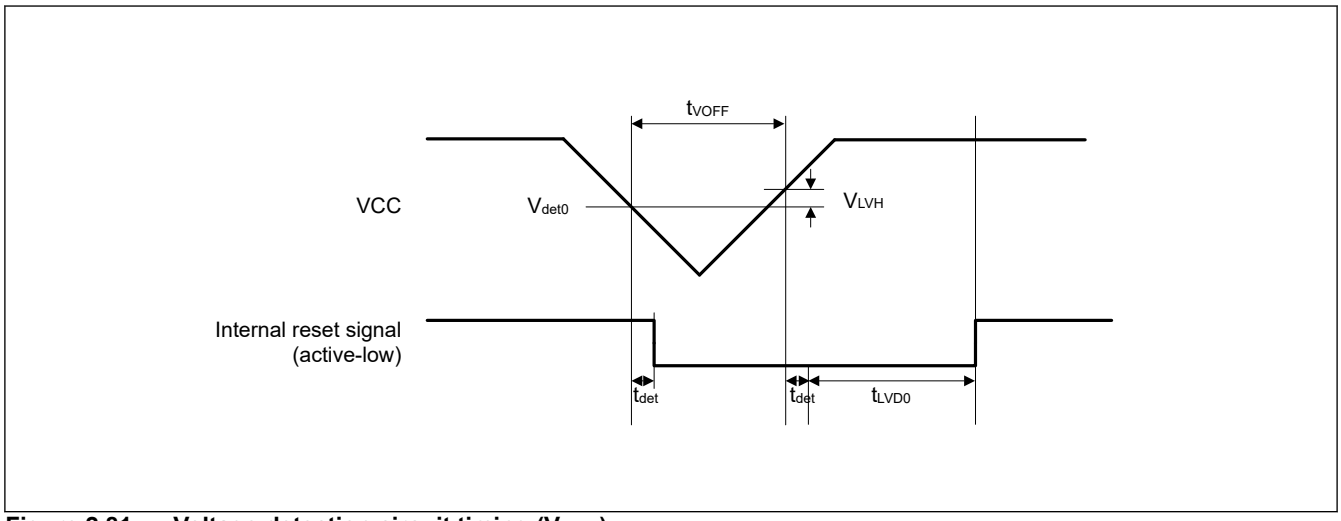



**Figure 2.81 Voltage detection circuit timing ($V_{det0}$)**

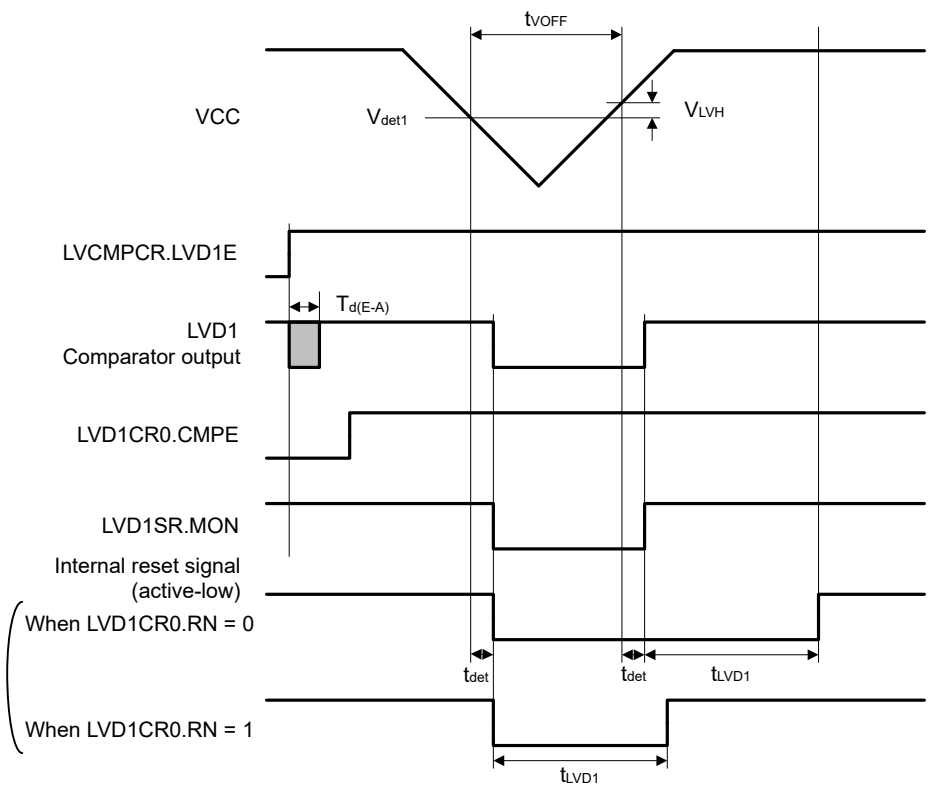



**Figure 2.82 Voltage detection circuit timing ($V_{det1}$)**

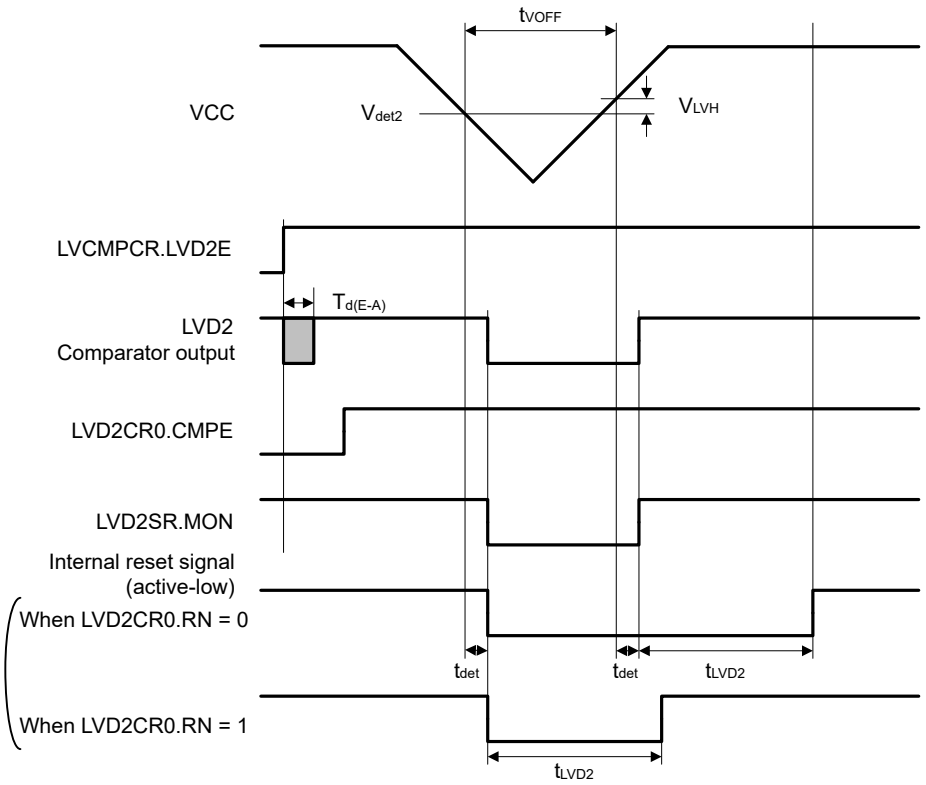



**Figure 2.83 Voltage detection circuit timing ($V_{det2}$)**

## 2.10 VBATT Characteristics

**Table 2.47 Battery backup function characteristics**

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.84 |
| Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop | $V_{BATTSW}$ | 2.70 | — | — | V | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | — | — | μs | |
| VBATT low voltage detection level | $V_{battldet}$ | 1.8 | 1.9 | 2.0 | V | Figure 2.85 |
| Minimum VBATT down time | $t_{BATTOFF}$ | 200 | — | — | μs | |
| Response delay | $t_{BATTdet}$ | — | — | 200 | μs | |
| VBATT monitor operation stabilization time (after VBATTMNSELR.VBATTMNSEL is changed to 1) | $t_{d(E-A)}$ | — | — | 20 | μs | |
| VBATT current increase (when VBATTMNSELR.VBATTMNSEL is 1 compared to the case that VBATTMNSELR.VBATTMNSEL is 0) | $I_{VBATTSEL}$ | — | 140 | 350 | nA | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

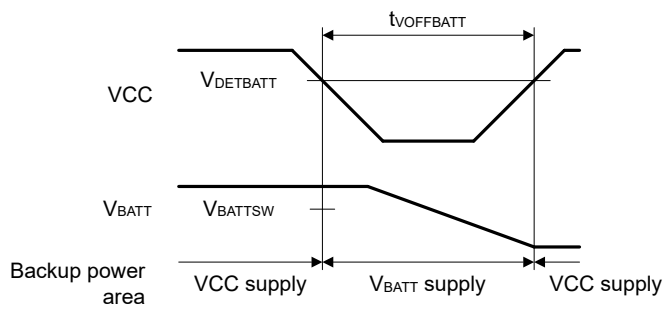



**Figure 2.84 Battery backup function characteristics**

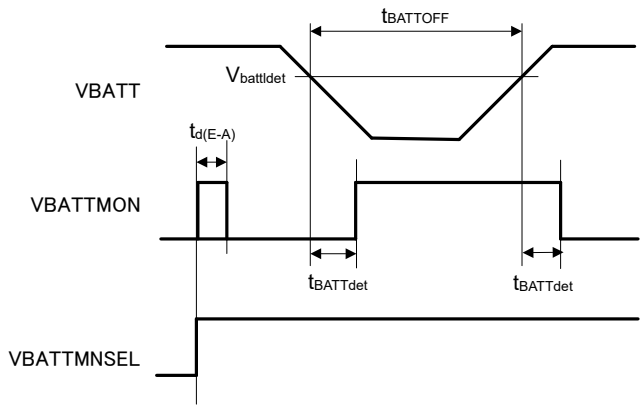



**Figure 2.85 Battery backup function characteristics**

## 2.11 CTSU Characteristics

**Table 2.48 CTSU characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| External capacitance connected to TSCAP pin | $C_{tscap}$ | 9 | 10 | 11 | nF | — |
| TS pin capacitive load | $C_{base}$ | — | — | 50 | pF | — |
| Permissible output high current | $\Sigma_{IoH}$ | — | — | -40 | mA | When the mutual capacitance method is applied |

## 2.12 Flash Memory Characteristics

### 2.12.1 Code Flash Memory Characteristics

**Table 2.49 Code flash memory characteristics (1 of 2)**

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ*6 | Max | Min | Typ*6 | Max | | |
| Programming time $N_{PEC}$ ≤ 100 times | 128-byte | $t_{P128}$ | — | 0.75 | 13.2 | — | 0.34 | 6.0 | ms | |
| | 8-KB | $t_{P8K}$ | — | 49 | 176 | — | 22 | 80 | ms | |
| | 32-KB | $t_{P32K}$ | — | 194 | 704 | — | 88 | 320 | ms | |

**Table 2.49 Code flash memory characteristics (2 of 2)**

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ*6 | Max | Min | Typ*6 | Max | | |
| Programming time $N_{PEC}$ > 100 times | 128-byte | $t_{P128}$ | — | 0.91 | 15.8 | — | 0.41 | 7.2 | ms | |
| | 8-KB | $t_{P8K}$ | — | 60 | 212 | — | 27 | 96 | ms | |
| | 32-KB | $t_{P32K}$ | — | 234 | 848 | — | 106 | 384 | ms | |
| Erasure time $N_{PEC}$ ≤ 100 times | 8-KB | $t_{E8K}$ | — | 78 | 216 | — | 43 | 120 | ms | |
| | 32-KB | $t_{E32K}$ | — | 283 | 864 | — | 157 | 480 | ms | |
| Erasure time $N_{PEC}$ > 100 times | 8-KB | $t_{E8K}$ | — | 94 | 260 | — | 52 | 144 | ms | |
| | 32-KB | $t_{E32K}$ | — | 341 | 1040 | — | 189 | 576 | ms | |
| Reprogramming/erasure cycle*4 | | $N_{PEC}$ | 10000*1 | — | — | 10000*1 | — | — | Times | |
| Suspend delay during programming | | $t_{SPD}$ | — | — | 264 | — | — | 120 | μs | |
| Programming resume time | | $t_{PRT}$ | — | — | 110 | — | — | 50 | μs | |
| First suspend delay during erasure in suspend priority mode | | $t_{SESD1}$ | — | — | 216 | — | — | 120 | μs | |
| Second suspend delay during erasure in suspend priority mode | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | ms | |
| Suspend delay during erasure in erasure priority mode | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | ms | |
| First erasing resume time during erasure in suspend priority mode*5 | | $t_{REST1}$ | — | — | 1.7 | — | — | 1.7 | ms | |
| Second erasing resume time during erasure in suspend priority mode | | $t_{REST2}$ | — | — | 144 | — | — | 80 | μs | |
| Erasing resume time during erasure in erasure priority mode | | $t_{REET}$ | — | — | 144 | — | — | 80 | μs | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 20 | μs | |
| Data hold time*2 | | $t_{DRP}$ | 10*2 *3 | — | — | 10*2 *3 | — | — | Years | |
| | | | 30*2 *3 | — | — | 30*2 *3 | — | — | | Ta = +85°C |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

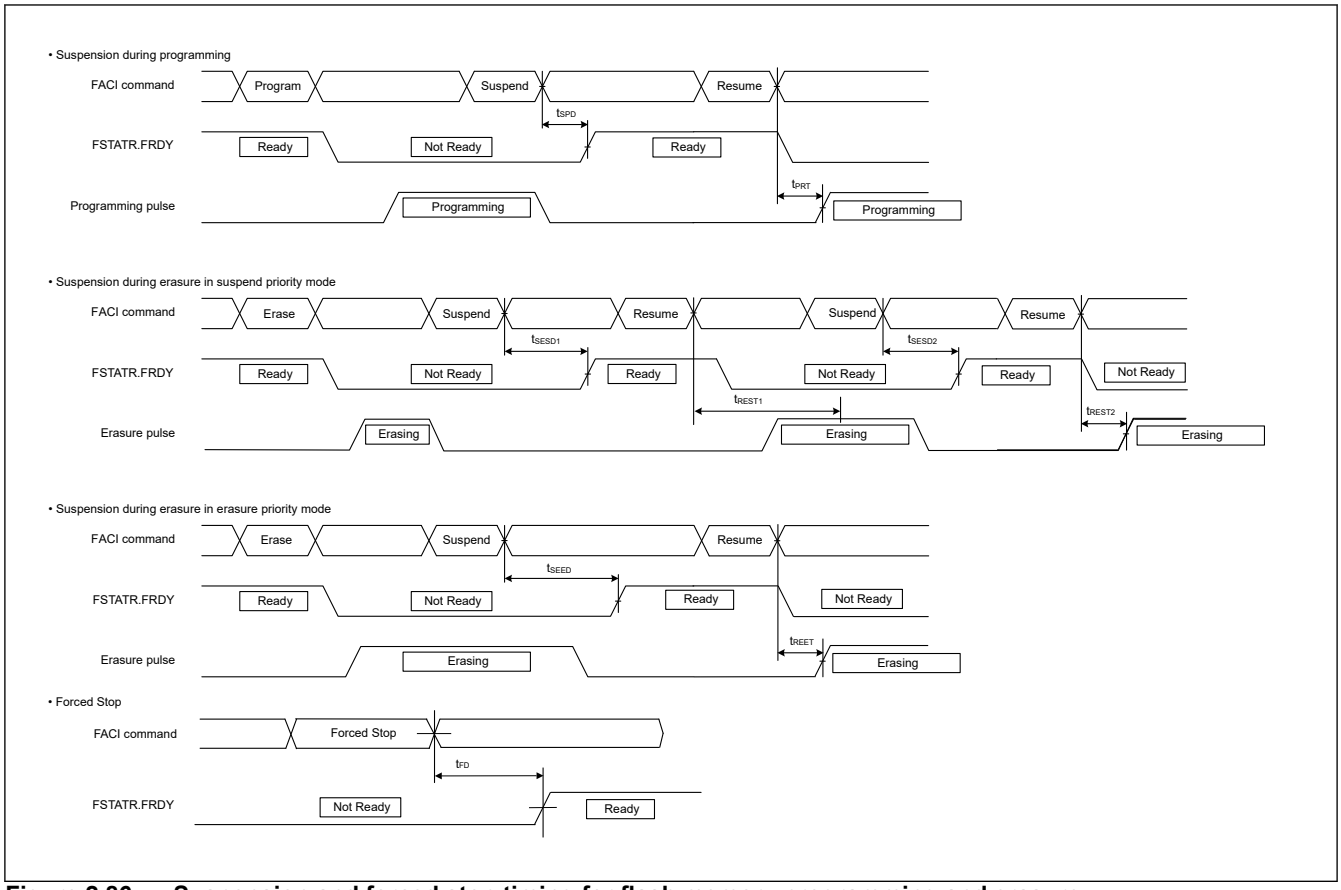



**Figure 2.86 Suspension and forced stop timing for flash memory programming and erasure**

## 2.12.2 Data Flash Memory Characteristics

**Table 2.50 Data flash memory characteristics (1 of 2)**

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ*6 | Max | Min | Typ*6 | Max | | |
| Programming time | 4-byte | $t_{DP4}$ | — | 0.36 | 3.8 | — | 0.16 | 1.7 | ms | |
| | 8-byte | $t_{DP8}$ | — | 0.38 | 4.0 | — | 0.17 | 1.8 | | |
| | 16-byte | $t_{DP16}$ | — | 0.42 | 4.5 | — | 0.19 | 2.0 | | |
| Erasure time | 64-byte | $t_{DE64}$ | — | 3.1 | 18 | — | 1.7 | 10 | ms | |
| | 128-byte | $t_{DE128}$ | — | 4.7 | 27 | — | 2.6 | 15 | | |
| | 256-byte | $t_{DE256}$ | — | 8.9 | 50 | — | 4.9 | 28 | | |
| Blank check time | 4-byte | $t_{DBC4}$ | — | — | 84 | — | — | 30 | μs | |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 125000*2 | — | — | 125000*2 | — | — | — | |
| Suspend delay during programming | 4-byte | $t_{DSPD}$ | — | — | 264 | — | — | 120 | μs | |
| | 8-byte | | — | — | 264 | — | — | 120 | | |
| | 16-byte | | — | — | 264 | — | — | 120 | | |
| Programming resume time | | $t_{DPRT}$ | — | — | 110 | — | — | 50 | μs | |
| First suspend delay during erasure in suspend priority mode | 64-byte | $t_{DSESD1}$ | — | — | 216 | — | — | 120 | μs | |
| | 128-byte | | — | — | 216 | — | — | 120 | | |
| | 256-byte | | — | — | 216 | — | — | 120 | | |

**Table 2.50 Data flash memory characteristics (2 of 2)**

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ*6 | Max | Min | Typ*6 | Max | | |
| Second suspend delay during erasure in suspend priority mode | 64-byte | $t_{DSESD2}$ | — | — | 300 | — | — | 300 | μs | |
| | 128-byte | | — | — | 390 | — | — | 390 | | |
| | 256-byte | | — | — | 570 | — | — | 570 | | |
| Suspend delay during erasing in erasure priority mode | 64-byte | $t_{DSEED}$ | — | — | 300 | — | — | 300 | μs | |
| | 128-byte | | — | — | 390 | — | — | 390 | | |
| | 256-byte | | — | — | 570 | — | — | 570 | | |
| First erasing resume time during erasure in suspend priority mode*5 | | $t_{DREST1}$ | — | — | 300 | — | — | 300 | μs | |
| Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode | | $t_{DREST2}$ | — | — | 126 | — | — | 70 | μs | |
| Erasing resume time during erasure in erasure priority mode | | $t_{DREET}$ | — | — | 126 | — | — | 70 | μs | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 20 | μs | |
| Data hold time*3 | | $t_{DRP}$ | 10*3 *4 | — | — | 10*3 *4 | — | — | Year | |
| | | | 30*3 *4 | — | — | 30*3 *4 | — | — | | Ta = +85°C |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

## 2.12.3 Option Setting Memory Characteristics

**Table 2.51 Option setting memory characteristics**

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ*4 | Max | Min | Typ*4 | Max | | |
| Programming time $N_{OPC}$ ≤ 100 times | $t_{OP}$ | — | 83 | 309 | — | 45 | 162 | ms | |
| Programming time $N_{OPC}$ > 100 times | $t_{OP}$ | — | 100 | 371 | — | 55 | 195 | ms | |
| Reprogramming cycle | $N_{OPC}$ | 20000*1 | — | — | 20000*1 | — | — | Times | |
| Data hold time*2 | $t_{DRP}$ | 10*2 *3 | — | — | 10*2 *3 | — | — | Years | |
| | | 30*2 *3 | — | — | 30*2 *3 | — | — | | Ta = +85°C |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

## 2.13 Boundary Scan

**Table 2.52 Boundary scan characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 2.87 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rise time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | — | — | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 2.88 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay | $t_{TDOD}$ | — | — | 40 | ns | |
| Boundary scan circuit startup time*1 | $T_{BSSTUP}$ | $t_{RESWP}$ | — | — | — | Figure 2.89 |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

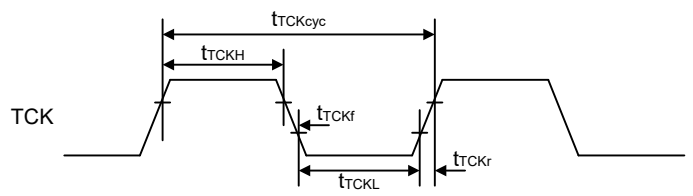



**Figure 2.87 Boundary scan TCK timing**

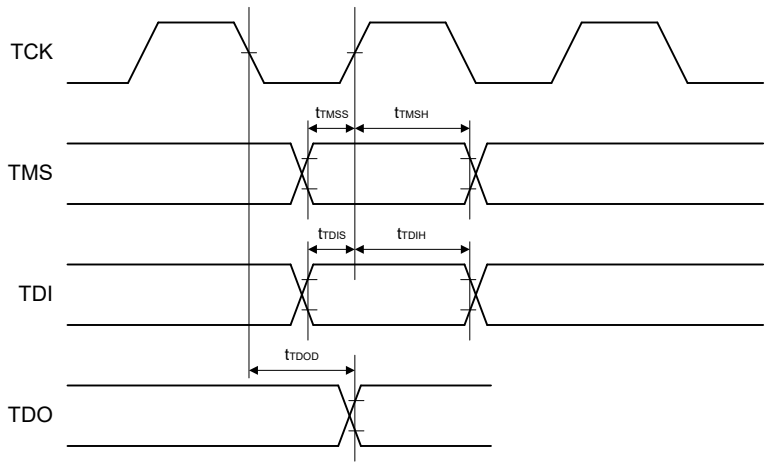



**Figure 2.88 Boundary scan input/output timing**

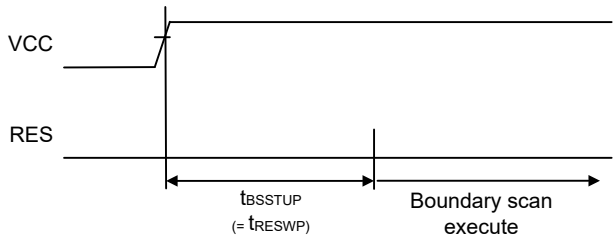



**Figure 2.89 Boundary scan circuit startup timing**

## 2.14 Joint European Test Action Group (JTAG)

**Table 2.53 JTAG**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 40 | — | — | ns | Figure 2.90 |
| TCK clock high pulse width | $t_{TCKH}$ | 15 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 15 | — | — | ns | |
| TCK clock rise time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | — | — | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 8 | — | — | ns | Figure 2.91 |
| TMS hold time | $t_{TMSH}$ | 8 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 8 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 8 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 20 | ns | |

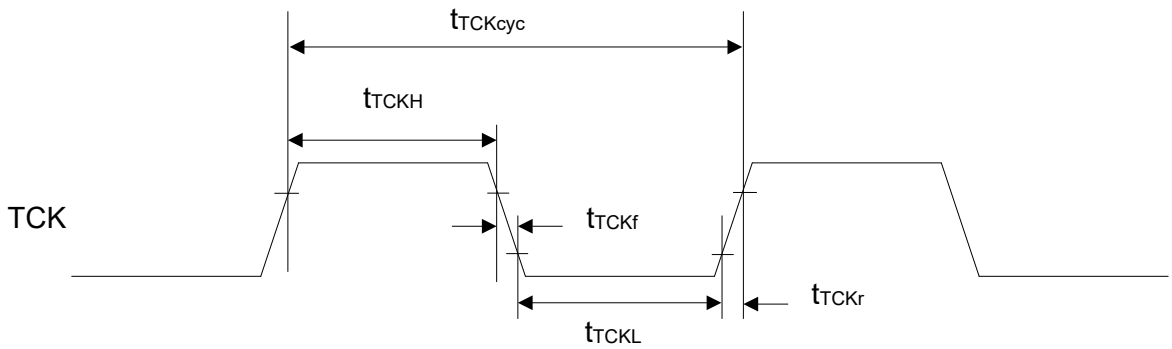



**Figure 2.90 JTAG TCK timing**

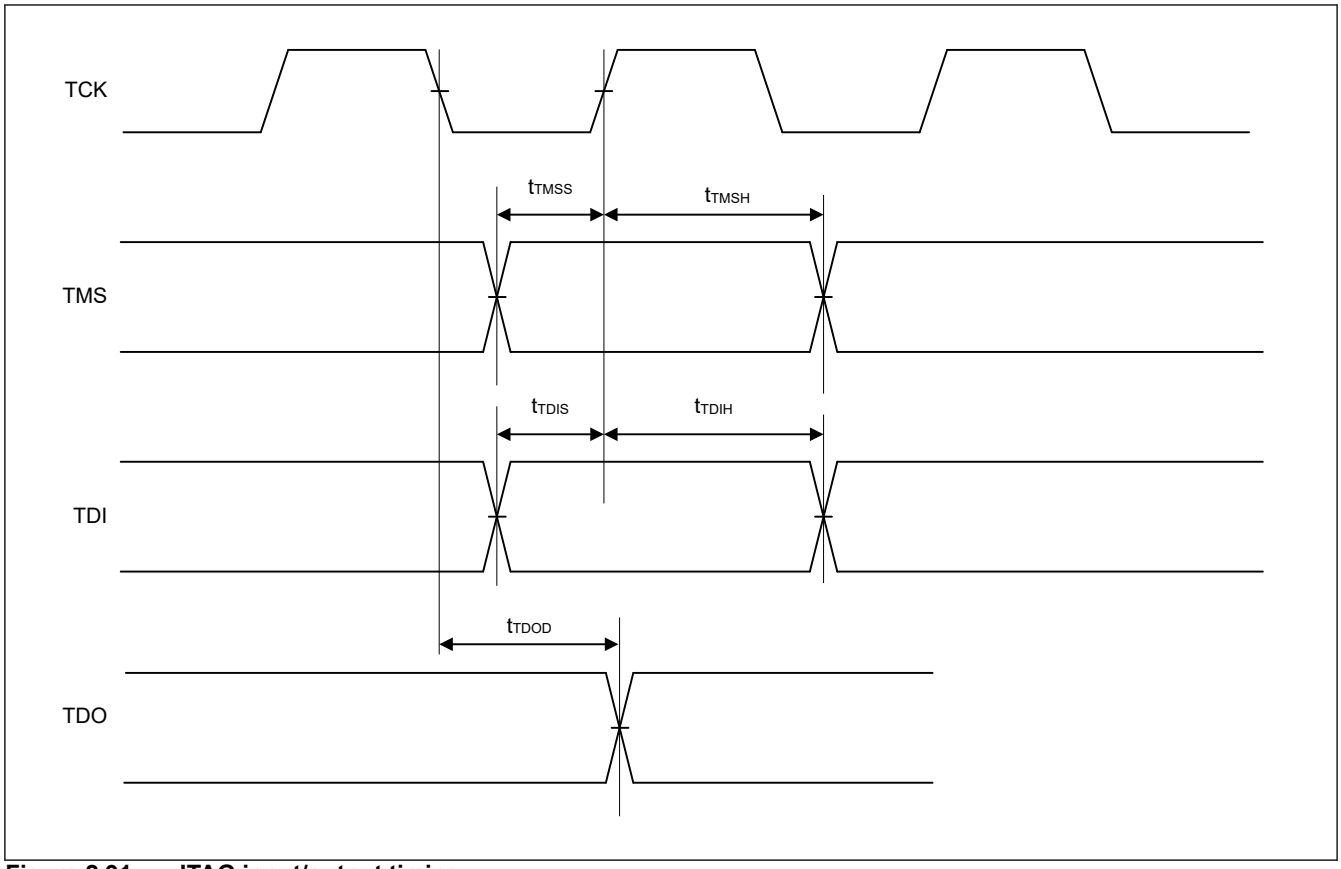



**Figure 2.91 JTAG input/output timing**

## 2.15 Serial Wire Debug (SWD)

**Table 2.54 SWD**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 40 | — | — | ns | Figure 2.92 |
| SWCLK clock high pulse width | $t_{SWCKH}$ | 15 | — | — | ns | |
| SWCLK clock low pulse width | $t_{SWCKL}$ | 15 | — | — | ns | |
| SWCLK clock rise time | $t_{SWCKr}$ | — | — | 5 | ns | |
| SWCLK clock fall time | $t_{SWCKf}$ | — | — | 5 | ns | |
| SWDIO setup time | $t_{SWDS}$ | 8 | — | — | ns | Figure 2.93 |
| SWDIO hold time | $t_{SWDH}$ | 8 | — | — | ns | |
| SWDIO data delay time | $t_{SWDD}$ | 2 | — | 28 | ns | |

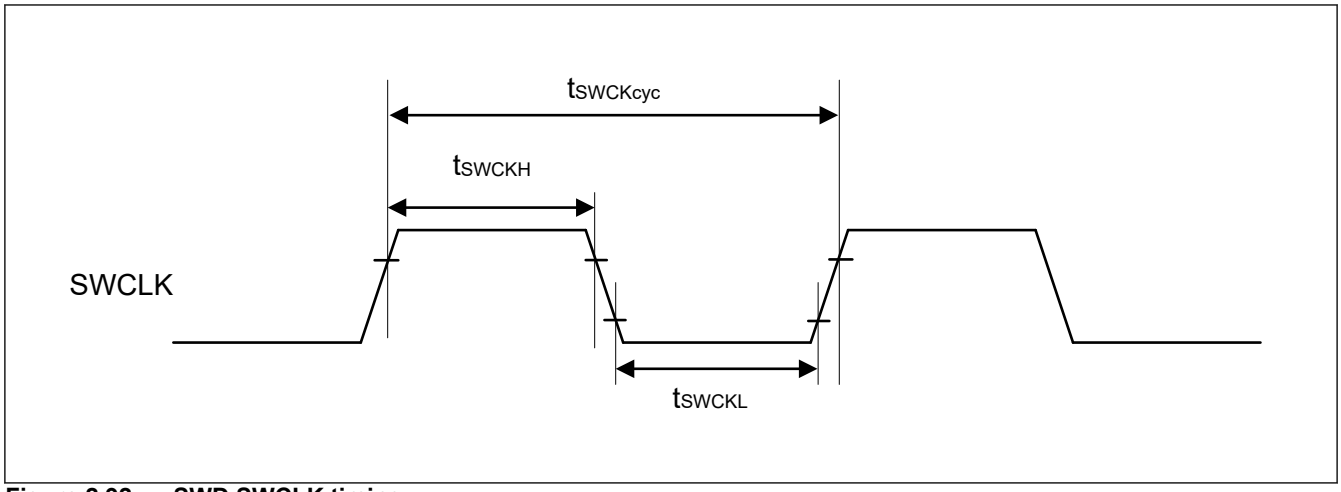



**Figure 2.92 SWD SWCLK timing**

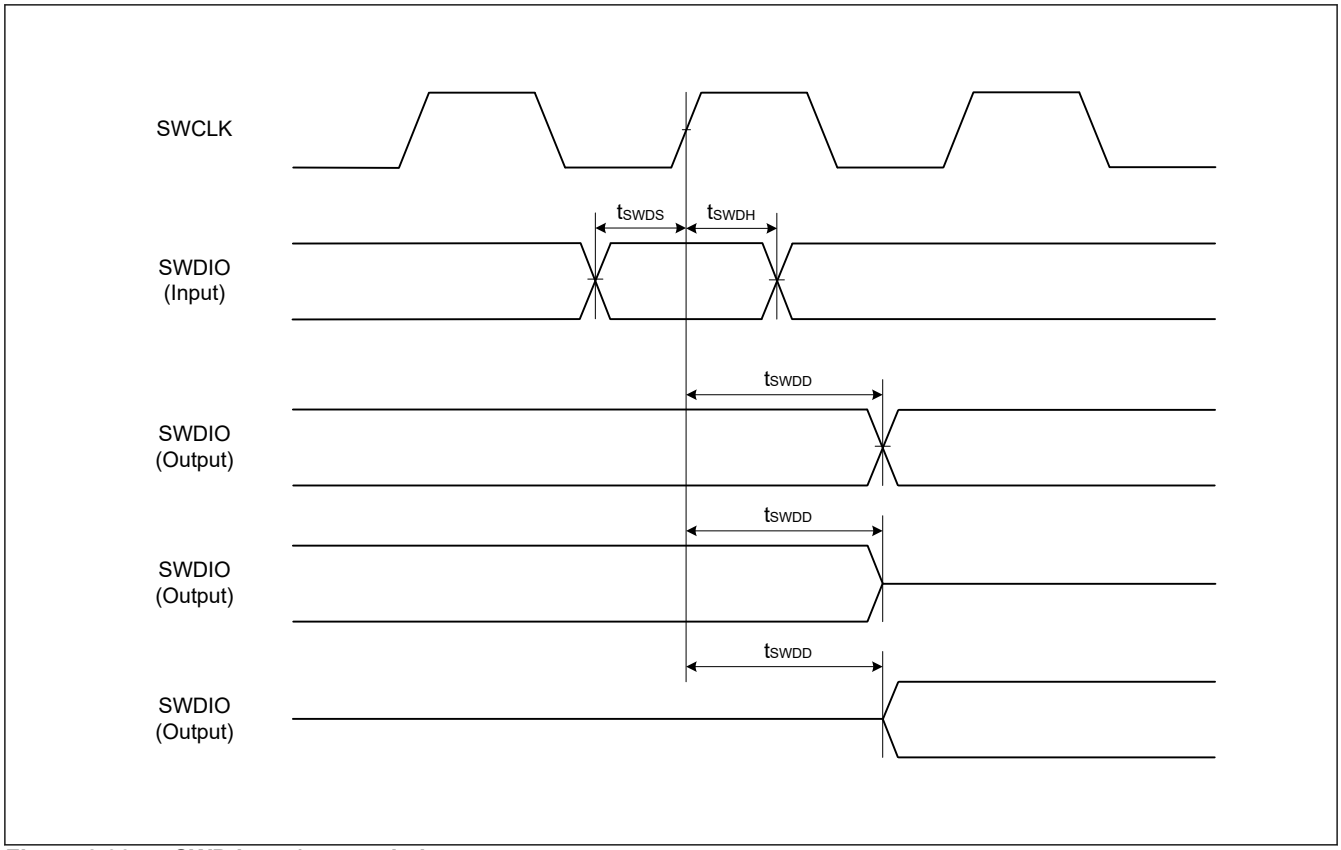



**Figure 2.93 SWD input/output timing**

## 2.16 Embedded Trace Macro Interface (ETM)

**Table 2.55 ETM**

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCLK clock cycle time | $t_{TCLKcyc}$ | 20 | — | — | ns | Figure 2.94 |
| TCLK clock high pulse width | $t_{TCLKH}$ | 9 | — | — | ns | |
| TCLK clock low pulse width | $t_{TCLKL}$ | 9 | — | — | ns | |
| TCLK clock rise time | $t_{TCLKr}$ | — | — | 1 | ns | |
| TCLK clock fall time | $t_{TCLKf}$ | — | — | 1 | ns | |
| TDATA[3:0] output setup time | $t_{TRDS}$ | 2.5 | — | — | ns | Figure 2.95 |
| TDATA[3:0] output hold time | $t_{TRDH}$ | 1.5 | — | — | ns | |

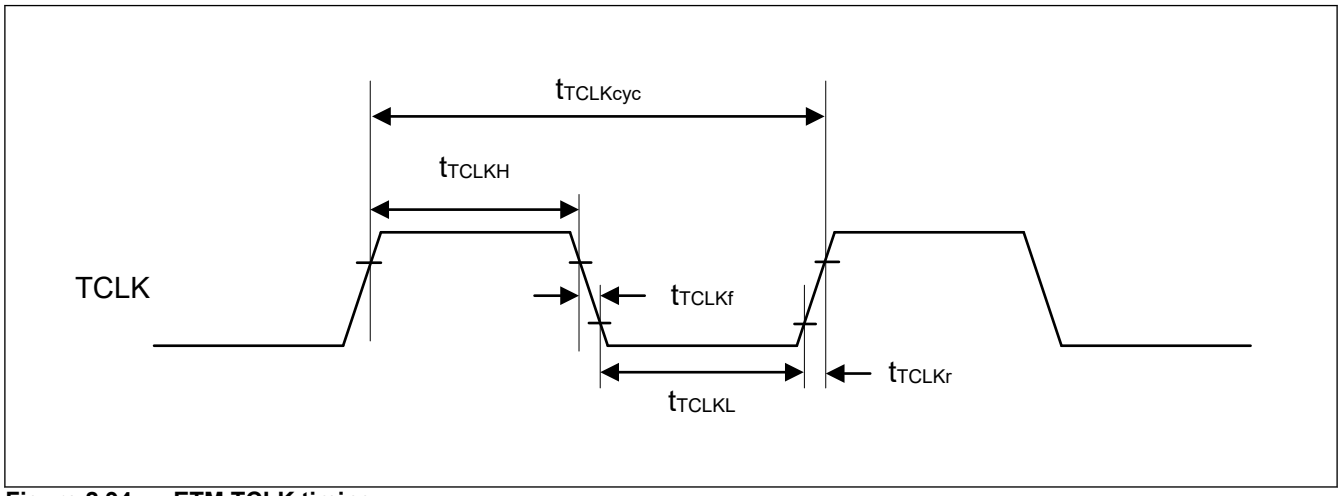



**Figure 2.94 ETM TCLK timing**

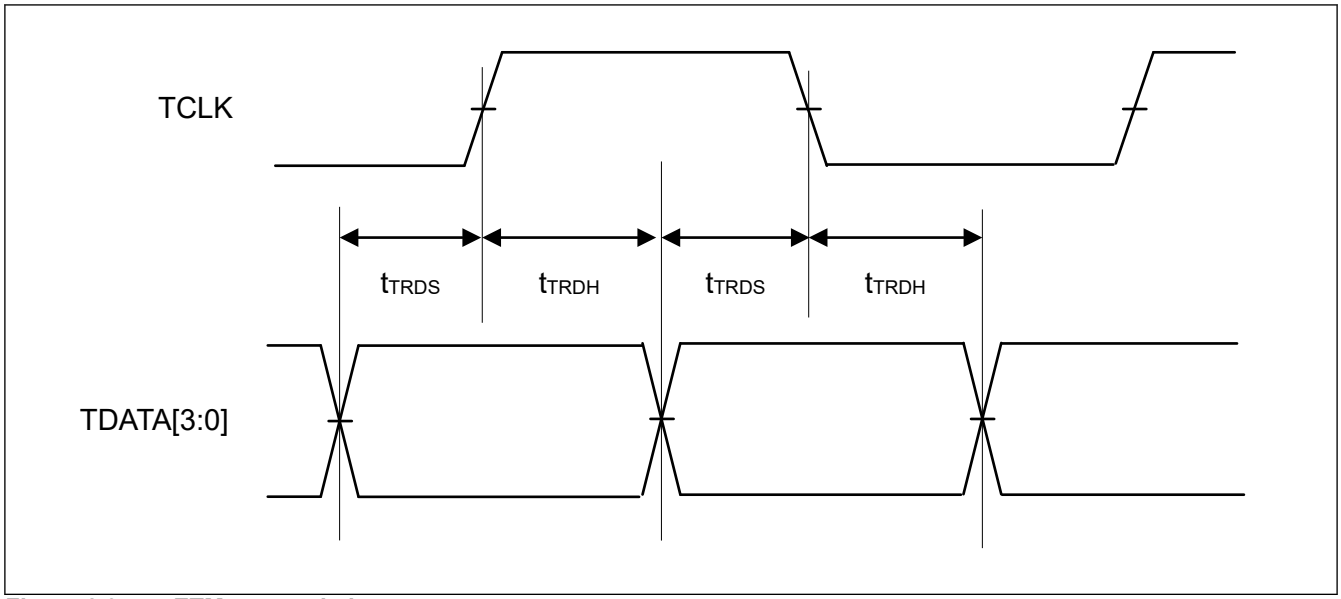



**Figure 2.95 ETM output timing**

# Appendix 1. Port States in Each Processing Mode

| Function | Pin function | Reset | Software Standby mode | | Deep Software Standby mode | After Deep Software Standby mode is canceled (return to startup mode) | |
|---|---|---|---|---|---|---|---|
| | | | OPE=0 | OPE=1 | | IOKEEP = 0 | IOKEEP = 1[*1] |
| Mode | MD | Pull-up | Keep-O | | Keep | Hi-Z | Keep |
| JTAG | TCK/TMS/TDI | Pull-up | Keep-O | | Keep | Hi-Z | Keep |
| | TDO | output | Keep-O | | Keep | TDO output | Keep |
| IRQ | IRQx | Hi-Z | Keep-O[*2] | | Keep | Hi-Z | Keep |
| | IRQx-DS | Hi-Z | Keep-O[*2] | | Keep[*3] | Hi-Z | Keep |
| AGT | AGTIOn | Hi-Z | Keep-O[*2] | | Keep | Hi-Z | Keep |
| | AGTIOn (n=1,3) | Hi-Z | Keep-O[*2] | | Keep[*3] | Hi-Z | Keep |
| SCI | RXD0 | Hi-Z | Keep-O[*2] | | Keep | Hi-Z | Keep |
| IIC | SCLn/SDAn | Hi-Z | Keep-O[*2] | | Keep | Hi-Z | Keep |
| USBFS | USB_OVRCURx | Hi-Z | Keep-O[*2] | | Keep | Hi-Z | Keep |
| | USB_OVRCURx-DS/ USB_VBUS | Hi-Z | Keep-O[*2] | | Keep[*3] | Hi-Z | Keep |
| | USB_DP/USB_DM | Hi-Z | Keep-O[*4] | | Keep[*3] | Hi-Z | Keep |
| RTC | RTCICx | Hi-Z | Keep-O[*2] | | Keep[*3] | Hi-Z | Keep |
| | RTCOUT | Hi-Z | [RTCOUT selected] RTCOUT output | | Keep | Hi-Z | Keep |
| CLKOUT | CLKOUT | Hi-Z | [CLKOUT selected] CLKOUT output | | Keep | Hi-Z | Keep |
| DAC | DAn | Hi-Z | [DAn output (DAOE = 1)] D/A output retained | | Keep | Hi-Z | Keep |
| External bus (CS area) | EBCLK | Hi-Z | [EBCLK output] H | | Keep | Hi-Z | Keep |
| | Dx | Hi-Z | [Dx output] Hi-Z | | Keep | Hi-Z | Keep |
| | Ax | Hi-Z | [Ax output] Hi-Z | [Ax output] Keep-O | Keep | Hi-Z | Keep |
| | BCx/CSx/RD/WRx | Hi-Z | [BCx/CSx/RD/WRx output] Hi-Z | [BCx/CSx/RD/WRx output] H | Keep | Hi-Z | Keep |
| | ALE | Hi-Z | [ALE output] Hi-Z | [ALE output] L | Keep | Hi-Z | Keep |
| Others | — | Hi-Z | Keep-O | | Keep | Hi-Z | Keep |

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

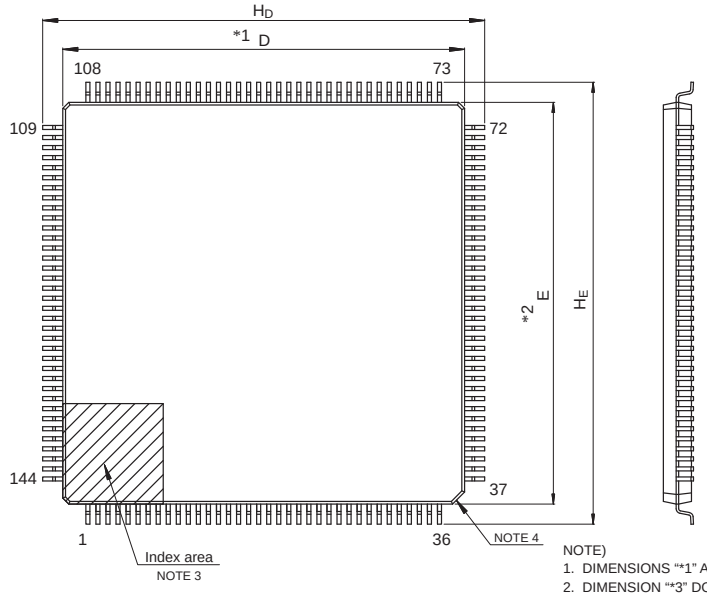
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input pin.

# Appendix 2. Package Dimensions

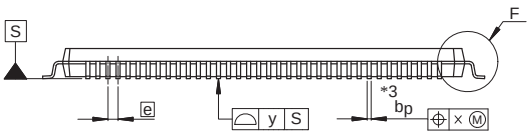
Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

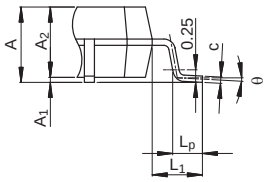
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP144-20x20-0.50 | PLQP0144KA-B | — | 1.2 |

Unit: mm




NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.




Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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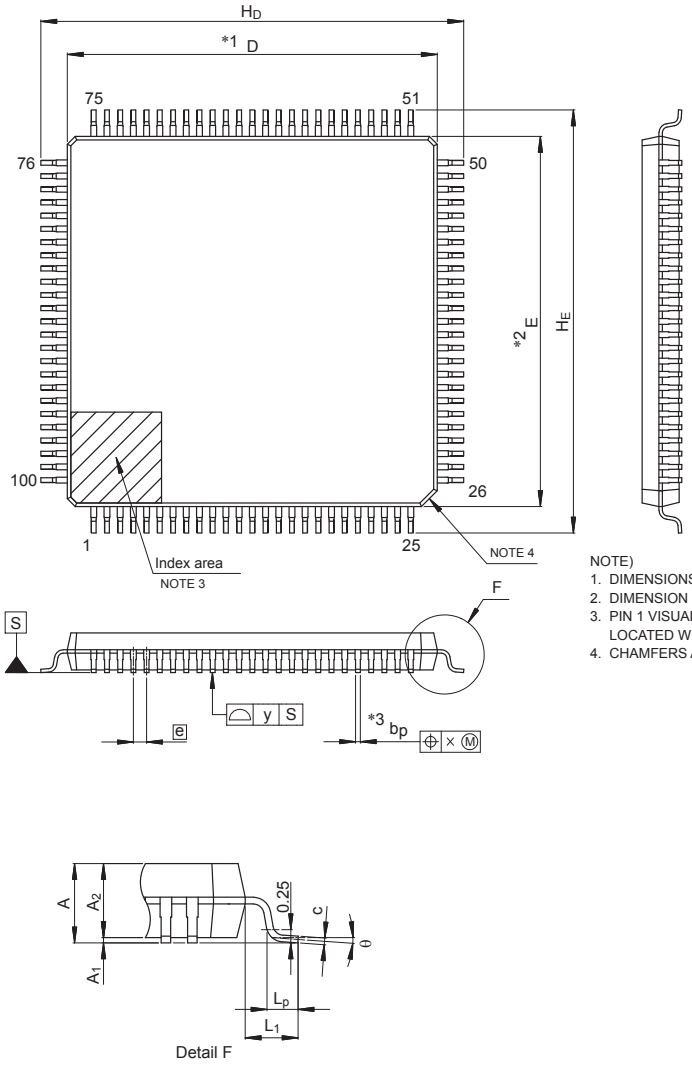
**Figure 2.1 LQFP 144-pin**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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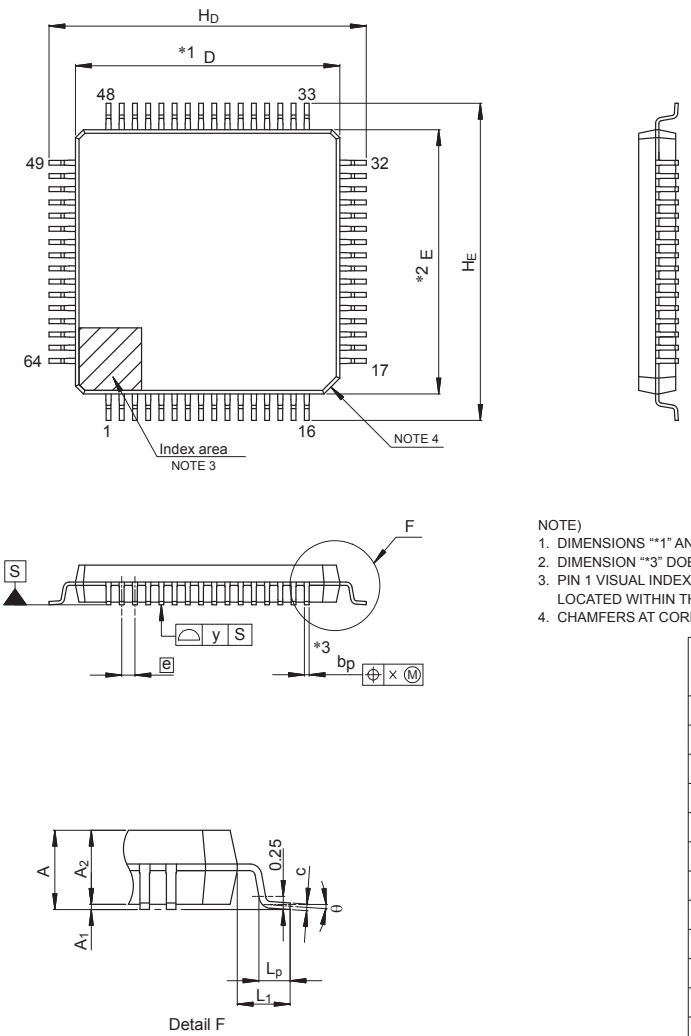
**Figure 2.2 LQFP 100-pin**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | — | 0.3 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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**Figure 2.3 LQFP 64-pin**

# Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

## 3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

**Table 3.1 Peripheral base address (1 of 3)**

| Name | Description | Base address |
|---|---|---|
| RMPU | Renesas Memory Protection Unit | 0x4000_0000 |
| TZF | TrustZone Filter | 0x4000_0E00 |
| SRAM | SRAM Control | 0x4000_2000 |
| BUS | BUS Control | 0x4000_3000 |
| DMAC0 | Direct memory access controller 0 | 0x4000_5000 |
| DMAC1 | Direct memory access controller 1 | 0x4000_5040 |
| DMAC2 | Direct memory access controller 2 | 0x4000_5080 |
| DMAC3 | Direct memory access controller 3 | 0x4000_50C0 |
| DMAC4 | Direct memory access controller 4 | 0x4000_5100 |
| DMAC5 | Direct memory access controller 5 | 0x4000_5140 |
| DMAC6 | Direct memory access controller 6 | 0x4000_5180 |
| DMAC7 | Direct memory access controller 7 | 0x4000_51C0 |
| DMA | DMAC Module Activation | 0x4000_5200 |
| DTC | Data Transfer Controller | 0x4000_5400 |
| ICU | Interrupt Controller | 0x4000_6000 |
| CACHE | CACHE | 0x4000_7000 |
| CPSCU | CPU System Security Control Unit | 0x4000_8000 |
| DBG | Debug Function | 0x400_1B000 |
| FCACHE | Flash Cache | 0x400_1C100 |
| SYSC | System Control | 0x4001_E000 |
| PORT0 | Port 0 Control Registers | 0x4008_0000 |
| PORT1 | Port 1 Control Registers | 0x4008_0020 |
| PORT2 | Port 2 Control Registers | 0x4008_0040 |
| PORT3 | Port 3 Control Registers | 0x4008_0060 |
| PORT4 | Port 4 Control Registers | 0x4008_0080 |
| PORT5 | Port 5 Control Registers | 0x4008_00A0 |
| PORT6 | Port 6 Control Registers | 0x4008_00C0 |
| PORT7 | Port 7 Control Registers | 0x4008_00E0 |
| PORT8 | Port 8 Control Registers | 0x4008_0100 |
| PFS | Pmn Pin Function Control Register | 0x4008_0800 |
| ELC | Event Link Controller | 0x4008_2000 |
| RTC | Realtime Clock | 0x4008_3000 |
| IWDT | Independent Watchdog Timer | 0x4008_3200 |
| WDT | Watchdog Timer | 0x4008_3400 |
| CAC | Clock Frequency Accuracy Measurement Circuit | 0x4008_3600 |

**Table 3.1 Peripheral base address (2 of 3)**

| Name | Description | Base address |
|---|---|---|
| MSTP | Module Stop Control A, B, C, D | 0x4008_4000 |
| POEG | Port Output Enable Module for GPT | 0x4008_A000 |
| USBFS | USB 2.0 FS Module | 0x4009_0000 |
| SDHI0 | SD Host Interface 0 | 0x4009_2000 |
| SSIE0 | Serial Sound Interface Enhanced (SSIE) | 0x4009_D000 |
| IIC0 | Inter-Integrated Circuit 0 | 0x4009_F000 |
| IIC0WU | Inter-Integrated Circuit 0 Wake-up Unit | 0x4009_F014 |
| IIC1 | Inter-Integrated Circuit 1 | 0x4009_F100 |
| OSPI | Octa Serial Peripheral Interface | 0x400A_6000 |
| CAN0 | CAN0 Module | 0x400A_8000 |
| CAN1 | CAN1 Module | 0x400A_9000 |
| CTSU | Capacitive Touch Sensing Unit | 0x400D_0000 |
| PSCU | Peripheral Security Control Unit | 0x400E_0000 |
| AGT0 | Low Power Asynchronous General purpose Timer 0 | 0x400E_8000 |
| AGT1 | Low Power Asynchronous General purpose Timer 1 | 0x400E_8100 |
| AGT2 | Low Power Asynchronous General purpose Timer 2 | 0x400E_8200 |
| AGT3 | Low Power Asynchronous General purpose Timer 3 | 0x400E_8300 |
| AGT4 | Low Power Asynchronous General purpose Timer 4 | 0x400E_8400 |
| AGT5 | Low Power Asynchronous General purpose Timer 5 | 0x400E_8500 |
| TSN | Temperature Sensor | 0x400F_3000 |
| CRC | CRC Calculator | 0x4010_8000 |
| DOC | Data Operation Circuit | 0x4010_9000 |
| EDMAC0 | DMA Controller for the Ethernet Controller Channel 0 | 0x4011_4000 |
| ETHERC0 | Ethernet Controller Channel 0 | 0x4011_4100 |
| SCI0 | Serial Communication Interface 0 | 0x4011_8000 |
| SCI1 | Serial Communication Interface 1 | 0x4011_8100 |
| SCI2 | Serial Communication Interface 2 | 0x4011_8200 |
| SCI3 | Serial Communication Interface 3 | 0x4011_8300 |
| SCI4 | Serial Communication Interface 4 | 0x4011_8400 |
| SCI5 | Serial Communication Interface 5 | 0x4011_8500 |
| SCI6 | Serial Communication Interface 6 | 0x4011_8600 |
| SCI7 | Serial Communication Interface 7 | 0x4011_8700 |
| SCI8 | Serial Communication Interface 8 | 0x4011_8800 |
| SCI9 | Serial Communication Interface 9 | 0x4011_8900 |
| SPI0 | Serial Peripheral Interface 0 | 0x4011_A000 |
| SPI1 | Serial Peripheral Interface 1 | 0x4011_A100 |
| SCE9 | Secure Cryptographic Engine | 0x4016_1000 |
| GPT320 | General PWM 32-Bit Timer 0 | 0x4016_9000 |
| GPT321 | General PWM 32-Bit Timer 1 | 0x4016_9100 |
| GPT322 | General PWM 32-Bit Timer 2 | 0x4016_9200 |
| GPT323 | General PWM 32-Bit Timer 3 | 0x4016_9300 |

**Table 3.1 Peripheral base address (3 of 3)**

| Name | Description | Base address |
|---|---|---|
| GPT164 | General PWM 16-Bit Timer 4 | 0x4016_9400 |
| GPT165 | General PWM 16-Bit Timer 5 | 0x4016_9500 |
| GPT166 | General PWM 16-Bit Timer 6 | 0x4016_9600 |
| GPT167 | General PWM 16-Bit Timer 7 | 0x4016_9700 |
| GPT168 | General PWM 16-Bit Timer 8 | 0x4016_9800 |
| GPT169 | General PWM 16-Bit Timer 9 | 0x4016_9900 |
| GPT_OPS | Output Phase Switching Controller | 0x4016_9A00 |
| ADC120 | 12bit A/D Converter 0 | 0x4017_0000 |
| ADC121 | 12bit A/D Converter 1 | 0x4017_0200 |
| DAC12 | 12-bit D/A converter | 0x4017_1000 |
| FLAD | Data Flash | 0x407F_C000 |
| FACI | Flash Application Command Interface | 0x407F_E000 |
| QSPI | Quad-SPI | 0x6400_0000 |

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

## 3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

**Table 3.2 Access cycles (1 of 4)**

| Peripherals | Address | | Number of access cycles | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | ICLK = PCLK | | ICLK > PCLK*1 | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 4 | 3 | 4 | 3 | ICLK | Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller |

**Table 3.2 Access cycles (2 of 4)**

| Peripherals | Address | | Number of access cycles | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | ICLK = PCLK | | ICLK > PCLK*1 | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| CACHE | 0x4000_7000 | 0x4000_7FFF | 3 | 5 | 3 | 5 | ICLK | CACHE |
| CPSCU, DBG, FCACHE | 0x4000_8000 | 0x4001_CFFF | 4 | 3 | 4 | 3 | ICLK | CPU System Security Control Unit, Debug Function, Flash Cache |
| SYSC | 0x4001_E000 | 0x4001_E3FF | 5 | 4 | 5 | 4 | ICLK | System Control |
| SYSC | 0x4001_E400 | 0x4001_E5FF | 9 | 8 | 5 to 8 | 5 to 8 | PCLKB | System Control |
| PORTn, PFS | 0x4008_0000 | 0x4008_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Port n Control Registers, Pmn Pin Function Control Register |
| ELC, RTC, IWDT, WDT, CAC | 0x4008_2000 | 0x4008_3FFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit |
| MSTP | 0x4008_4000 | 0x4008_4FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Module Stop Control |
| POEG | 0x4008_A000 | 0x4008_AFFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Port Output Enable Module for GPT |
| USBFS | 0x4009_0000 | 0x4009_3FFF | 6 | 5 | 3 to 6 | 3 to 5 | PCLKB | USB 2.0 FS Module |
| USBFS | 0x4009_4000 | 0x4009_4FFF | 4 | 3 | 1 to 4 | 1 to 3 | PCLKB | USB 2.0 FS Module |
| SDHI0, SSIE0, IICn, IIC0WU | 0x4009_2000 | 0x4009_FFFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | SD Host Interface 0, Serial Sound Interface Enhanced, Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit |
| OSPI | 0x400A_6000 | 0x400A_6FFF | 15 | 17 | 12 to 15 | 15 to 17 | PCLKB | Octa Serial Peripheral Interface |
| CANn | 0x400A_8000 | 0x400A_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | CANn Module |
| CTSU | 0x400D_0000 | 0x400D_FFFF | 4 | 3 | 1 to 4 | 1 to 3 | PCLKB | Capacitive Touch Sensing Unit |
| PSCU | 0x400E_0000 | 0x400E_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Peripheral Security Control Unit |
| AGTn | 0x400E_8000 | 0x400E_8FFF | 7 | 4 | 5 to 7 | 2 to 4 | PCLKB | Low Power Asynchronous General purpose Timer n |
| TSN | 0x400F_3000 | 0x400F_3FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Temperature Sensor |
| CRC, DOC | 0x4010_8000 | 0x4010_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | CRC Calculator, Data Operation Circuit |
| EDMAC0 | 0x4011_4000 | 0x4011_40FF | 6 | 5 | 3 to 6 | 3 to 5 | PCLKA | DMA Controller for the Ethernet Controller Channel 0 |
| ETHERC0 | 0x4011_4100 | 0x4011_4FFF | 15 | 14 | 12 to 15 | 12 to 14 | PCLKA | Ethernet Controller Channel 0 |
| SCIn | 0x4011_8000 | 0x4011_8FFF | 5*2 | 4*2 | 2 to 5*2 | 2 to 4*2 | PCLKA | Serial Communication Interface n |
| SPIn | 0x4011_A000 | 0x4011_AFFF | 5*3 | 4*3 | 2 to 5*3 | 2 to 4*3 | PCLKA | Serial Peripheral Interface n |
| SCE9 | 0x4016_1000 | 0x4016_1FFF | 6 | 4 | 3 to 6 | 2 to 4 | PCLKA | Secure Cryptographic Engine |

**Table 3.2 Access cycles (3 of 4)**

| Peripherals | Address | | Number of access cycles | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | ICLK = PCLK | | ICLK > PCLK*1 | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| GPT32n, GPT16n, GPT_OPS | 0x4016_9000 | 0x4016_9FFF | 7 | 4 | 4 to 7 | 2 to 4 | PCLKA | General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller |
| ADC12n, DAC12 | 0x4017_0000 | 0x4017_2FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | 12bit A/D Converter n, 12-bit D/A converter |
| QSPI | 0x6400_0000 | 0x6400_000F | 5 | 14 to *4 | 2 to 5 | 14 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0010 | 0x6400_0013 | 25 to *4 | 6 to *4 | 25 to *4 | 5 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0014 | 0x6400_0037 | 5 | 14 to *4 | 2 to 5 | 14 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0804 | 0x6400_0807 | 4 | 3 | 1 to 4 | 1 to 3 | PCLKA | Quad-SPI |

**Table 3.2 Access cycles (4 of 4)**

| Peripherals | Address | | Number of access cycles | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | ICLK = FCLK | | ICLK > FCLK*1 | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| FLAD, FACI | 0x407F_C000 | 0x407F_EFFF | 5 | 4 | 2 to 5 | 2 to 4 | FCLK | Data Flash, Flash Application Command Interface |

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Note 4. The access cycles depend on the QSPI bus cycles.

# Revision History

**Revision 1.00 — April 09, 2020**

First edition, issued

**Revision 1.10 — September 29, 2020**

**1. Overview:**
- Added note to Figure 1.1 Block diagram.

**2. Electrical Characteristics:**
- Added description that Supported peripheral functions and pins differ from one product name to another.

**Appendix:**
- Removed NOTE about USB host operation in Appendix 1.
- Added Access cycles for FLAD and FACI to Tables 3.2 in Appendix 3.
- Removed NOTE2 about BWAIT in Table 3.2, and along with that,changed the NOTE number in this table in Appendix 3.

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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