Data Sheet | December 28, 2004 | FN9106.3

Multi-Phase PWM Controller

The ISL6244 provides core-voltage regulation by driving 2 to 4 interleaved synchronous-rectified buck-converter channels in parallel. Interleaving the channel timing results in increased ripple frequency which reduces input and output ripple currents. The reduction in ripple results in lower component cost, reduced dissipation, and a smaller implementation area.

The ISL6244 uses cost and space-saving $r_{DS(ON)}$ sensing for channel current balance, active voltage positioning, and over-current protection. Output voltage is monitored by an internal differential remote sense amplifier. A high-bandwidth error amplifier drives the output voltage to match the programmed 5-bit DAC reference voltage. The resulting compensation signal guides the creation of pulse width modulated (PWM) signals to control companion Intersil MOSFET drivers. The OFS pin allows direct offset of the DAC voltage from 0V to 100mV using a single external resistor. The entire system is trimmed to ensure a system accuracy of ±1%.

Outstanding features of this controller IC include Dynamic VID™ technology allowing seamless on-the-fly VID changing without the need of any external components. Battery “feed-forward” is provided to allow for traditional control schemes over total input voltage variation. Output voltage “droop” or active voltage positioning is optional. When employed, it allows the reduction in size and cost of the output capacitors required to support load transients. A threshold-sensitive enable input allows the use of an external resistor divider for start-up coordination with Intersil MOSFET drivers or any other devices powered from a separate supply.

Superior over-voltage protection is achieved by gating on the lower MOSFET of all phases to reduce the output voltage. Under-voltage conditions are detected, but PWM operation is not disrupted. Over-current conditions cause a hiccup-mode response as the controller repeatedly tries to restart. After a set number of failed startup attempts, the controller latches off. A power good logic signal indicates when the converter output is between the UV and OV thresholds.

Features

- Multi-Phase Power Conversion
  - 2, 3 or 4 Phase Operation
- Active Channel Current Balancing
- Precision $r_{DS(ON)}$ Current Sharing
  - Lossless
  - Low Cost
- Precision CORE Voltage Regulation
  - Differential Remote Output Voltage Sensing
  - Programmable Reference Offset
  - ±1% System Accuracy
- Microprocessor Voltage Identification Input
  - 5-Bit VID Input
  - 0.800V to 1.550V in 25mV Steps
  - Dynamic VID Technology
- Programmable Droop Voltage
- Excellent Dynamic Response
  - Combined Input Voltage Feed-Forward and Pulse-by-Pulse Average Current Mode
- Over Current Protection
- Digital Soft Start
- Threshold Sensitive Enable Input
- High Ripple Frequency (160kHz to 4MHz)
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Available (RoHS Compliant)

Applications

- AMD Hammer Family Processor Voltage Regulator
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
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Ordering Information

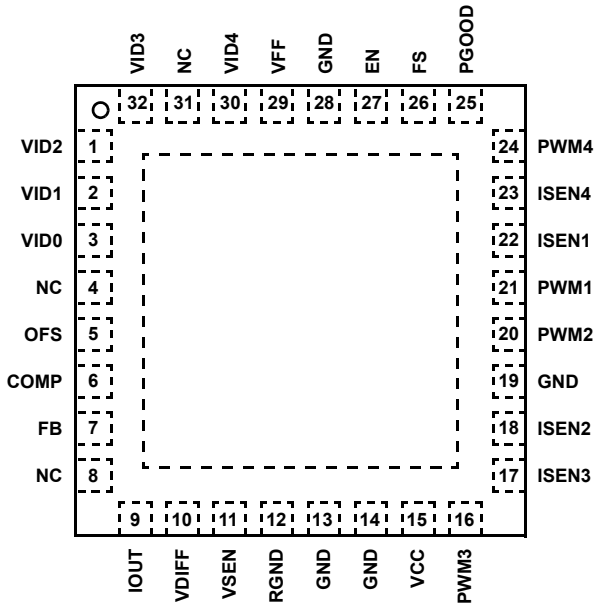
PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6244CR	0 to 70	32 Ld 5x5 QFN	L32.5x5
ISL6244CRZ (Note 1)	0 to 70	32 Ld 5x5 QFN (Pb-Free)	L32.5x5
ISL6244HR	-10 to 100	32 Ld 5x5 QFN	L32.5x5
ISL6244HRZ (Note 1)	-10 to 100	32 Ld 5x5 QFN (Pb-Free)	L32.5x5

NOTES:

1. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-T” suffix for 32 QFN 5x5 Tape and Reel packages.

Pinout

ISL6244CR
(32 LEAD QFN 5x5)
TOP VIEW



NC = NO CONNECT

Absolute Maximum Ratings

Supply Voltage, VCC (Note 3) . . . . . .+7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class II

Operating Conditions

Supply Voltage, VCC . . . . . +5V ±5%
Ambient Temperature. . . . . .-10°C to 100°C
Maximum Junction Temperature . . . . . .125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 6).	32	4

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

3. For VCC > 5.5V, current must be limited to 25mA.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. Tolerance does not include the VID offset error or any external component tolerances.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, T_A = -10°C to 100°C. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R_T = 100kΩ ±1%	8.0	10.8	14.0	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R_T = 100kΩ ±1%	8.0	10.3	13.0	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC Rising	4.25	4.35	4.60	V
	VCC Falling	3.75	3.85	4.00	V
ENABLE Threshold	EN Rising	1.215	1.240	1.265	V
	Hysteresis	82	92	102	mV
REFERENCE VOLTAGE AND DAC					
System Accuracy (Note 5)		-1.2	-	1.2	%VID
	0 to 70°C	-1	-	1	%VID
VID on Fly Step Size	R_T = 100kΩ	-	25	-	mV
VID Pull Up		-30	-20	-10	µA
VID Input Low Level		-	-	0.8	V
VID Input High Level		2.0	-	-	V
PIN-ADJUSTABLE OFFSET					
OFS Current		-	100	-	µA
Offset Accuracy	ROFS = 5kΩ ±1%	92.0	100.0	108.0	mV
	ROFS = 5kΩ ±1% , 0 to 70°C	94.0	100.0	106.0	
Maximum Offset		-	-	100.0	mV
OSCILLATOR					
Accuracy		-12.5	-	12.5	%
	RT = 100K	245	280	315	kHz
Adjustment Range		0.08	-	1.0	MHz
VFF Range		0.5	-	2.5	V
Max Duty Cycle		-	75	-	%

Electrical Specifications Operating Conditions: VCC = 5V, T_A = -10°C to 100°C. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	-	72	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, Load = ±400mA	3	7.1	11	V/µs
Maximum Output Voltage	R_L = 10kΩ to ground	3.6	4.5	-	V
Source Current		3.0	7.0	11.5	mA
Sink Current		1.6	3.0	5.4	mA
REMOTE-SENSE AMPLIFIER					
Input Impedance		-	80	-	kΩ
Bandwidth		-	20	-	MHz
Slew Rate		-	6	-	V/µs
SENSE CURRENT					
IOUT Accuracy	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 50µA	-5	-	5	%
ISEN Offset Voltage		-	6	-	mV
Over-Current Trip Level		68	85	102	µA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
Under-Voltage Offset From VID	VSEN Falling	320	370	420	mV
Over-Voltage Threshold	VSEN Rising	2.08	2.13	2.20	V

Typical Operating Performance

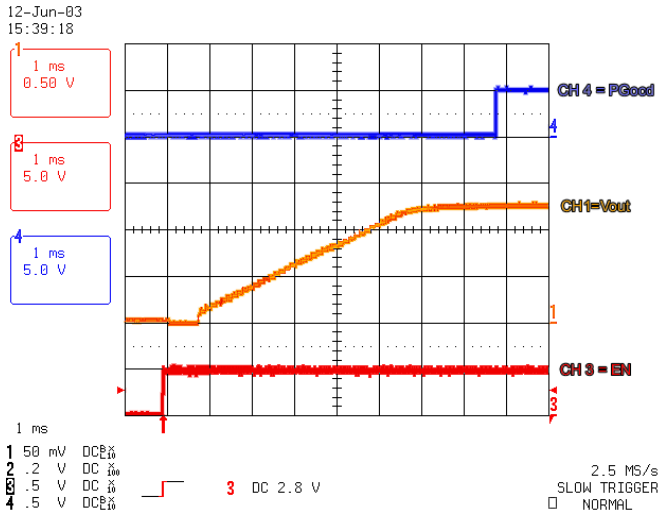


FIGURE 1. SOFT-START WAVEFORM

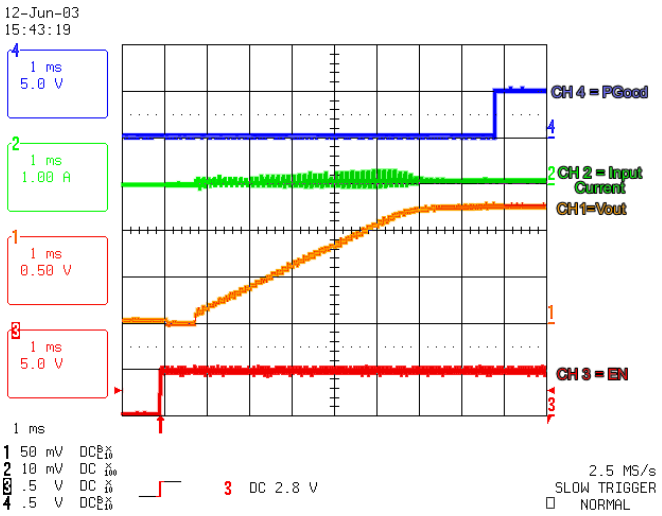


FIGURE 2. INRUSH CURRENT AT VIN 19V @ 52A

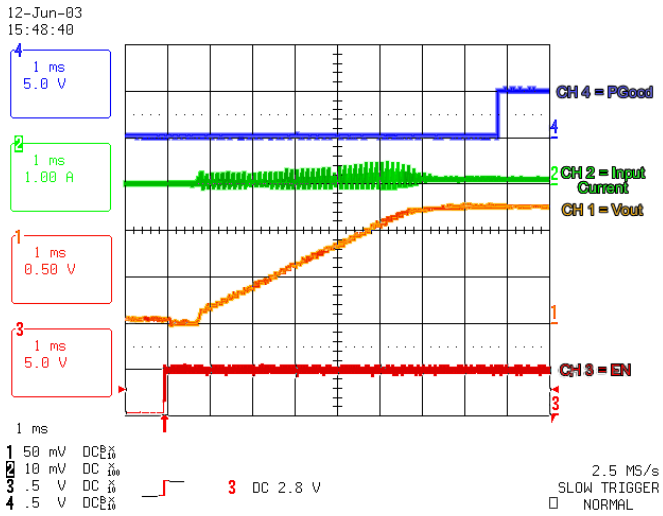


FIGURE 3. INRUSH CURRENT AT VIN 10.8V @ 52A

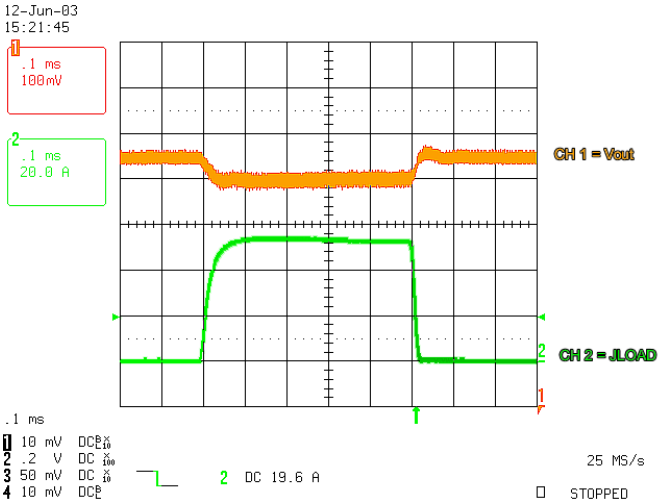


FIGURE 4. TRANSIENT WAVEFORM FROM 0A TO 52A

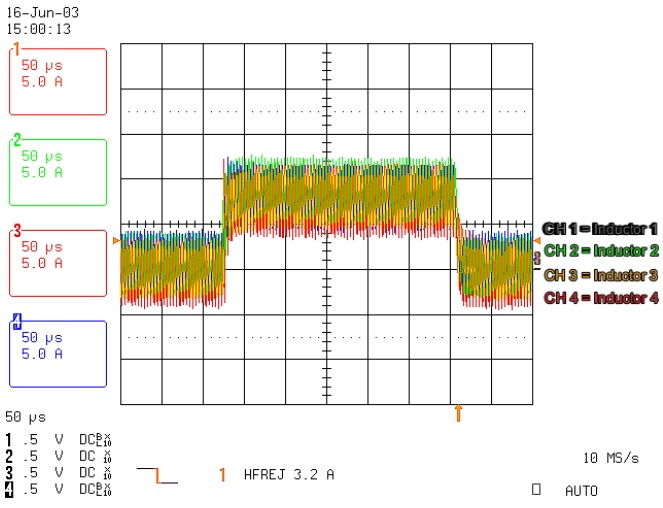


FIGURE 5. INDUCTOR CURRENT TRANSIENT

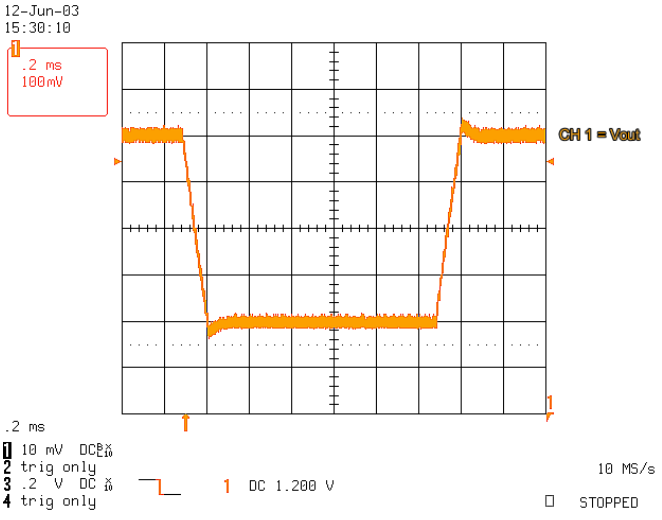


FIGURE 6. VID CHANGES FROM 1.60V TO 1.20V

Typical Operating Performance

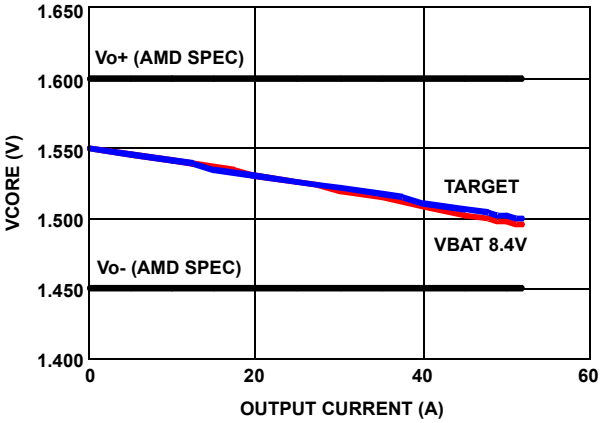


FIGURE 7. ISL6244 DROOP: V_{BAT} = 8.4V

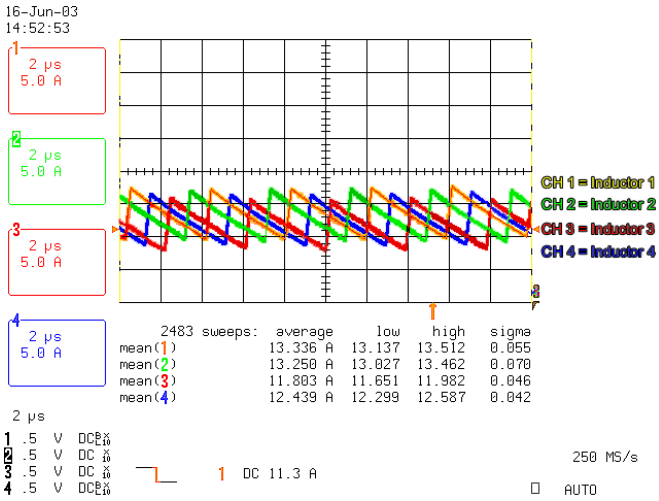


FIGURE 8. FOUR PHASE CURRENT BALANCE @ 52A

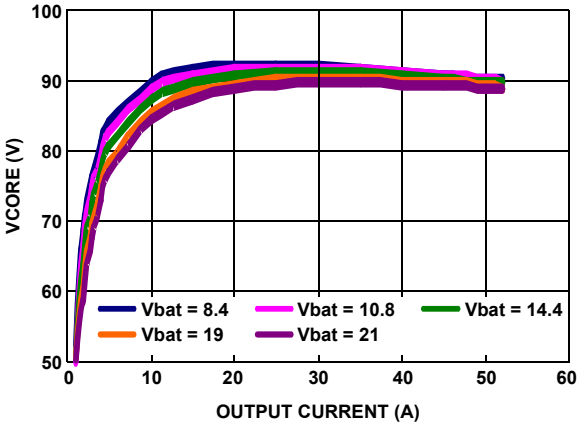


FIGURE 9. ISL6244 EFFICIENCY vs LOAD

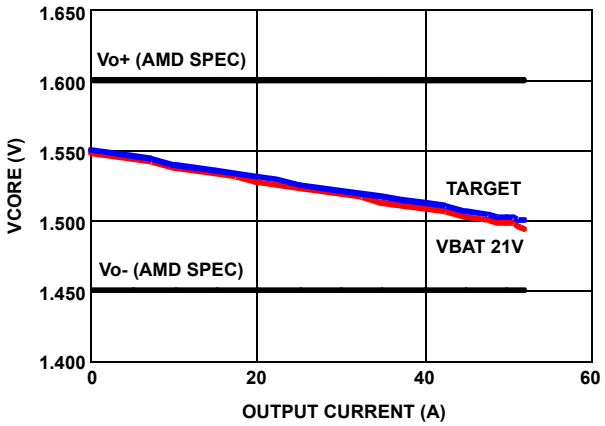
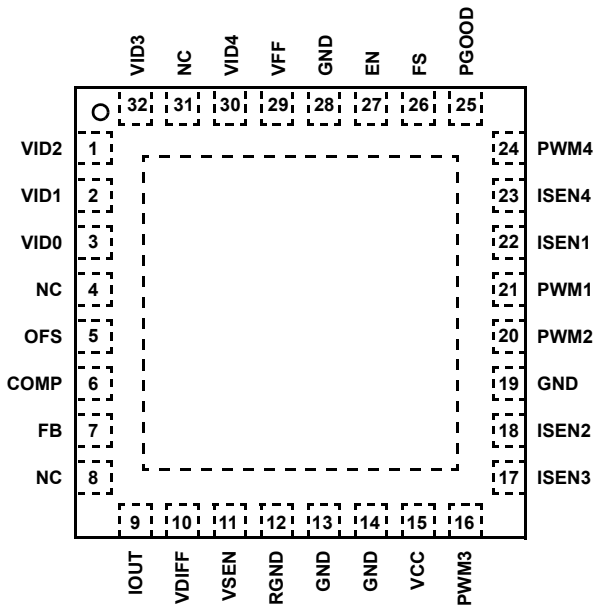


FIGURE 10. ISL6244 DROOP: V_{BAT} = 21V

Functional Pin Description

ISL6244CR
(32 LEAD QFN 5x5)
TOP VIEW



NC = NO CONNECT

GND

Bias and reference ground for the IC.

VFF

This pin is connected to VIN through a 10:1 voltage divider to allow for battery “feed-forward,” which improves stability over varying input line.

VID4, VID3, VID2, VID1, VID0

The state of these five inputs program the internal DAC, which provides the reference voltage for output regulation. Connect these pins to either open-drain or active pull-up type outputs. Pulling these pins above 2.9V can cause a reference offset inaccuracy.

OFS

Connecting a resistor between this pin and ground creates a positive offset voltage which is added to the DAC voltage, allowing easy implementation of load-line regulation. For no offset, simply tie this pin to ground.

FB and COMP

The internal error amplifier inverting input and output respectively. Connect the external R-C feedback compensation network of the regulator to these pins.

IOUT

The current carried out of this pin is proportional to output current and can be used to incorporate output voltage droop and/or load sharing. The scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$. If droop is desired, connect this pin to FB. When not used for droop or load sharing, simply leave this pin open.

VSEN, RGND, VDIFF

VSEN and RGND are the inputs to the differential remote-sense amplifier. Connect these pins to the sense points of the remote load. Connect an appropriately sized feedback resistor, R_{FB}, between VDIFF and FB.

VCC

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply.

ISEN1, ISEN2, ISEN3, ISEN4

Current sense inputs. A resistor connected between these pins and their respective phase node sets a current proportional to the current in the lower MOSFET during it’s conduction interval. This current is used as a reference for channel balancing, load sharing, protection, and load-line regulation. Inactive channels should have their respective sense inputs left open.

PWM1, PWM2, PWM3, PWM4

Pulse-width modulating outputs. Connect these pins to the individual ISL620X driver PWM input pins. These logic outputs command the driver IC(s) in switching the half-bridge configuration of MOSFETs. The number of active channels is determined by the state of PWM3 and PWM4. If PWM3 is tied to VCC, this indicates to the controller that two channel operation is desired. In this case, PWM 4 should be left open or tied to VCC. Shorting PWM4 to VCC indicates that three channel operation is desired.

PGOOD

Power good is an open-drain logic output that changes to a logic low when the voltage at VDIFF is 350mV below the VID setting (under-voltage) or above 2.2V (over-voltage).

FS

A pin for setting the switching frequency of the regulator. Place a resistor from this pin to ground to set the switching frequency between 80kHz and 1MHz.

EN

This pin enables the ISL6244 regulator.

Typical Application: 3-Phase Buck Converter with $r_{DS(ON)}$ Current Sensing

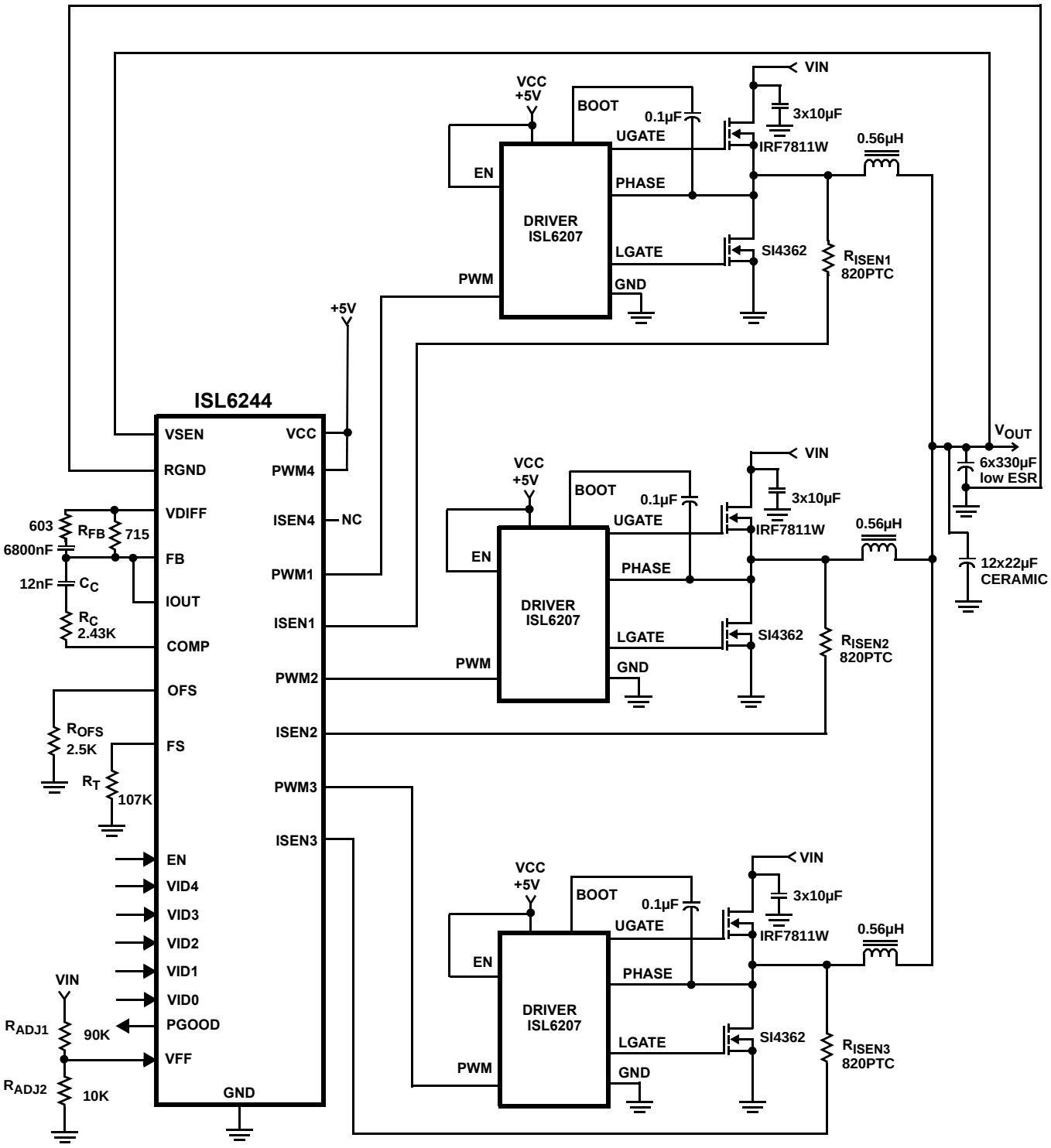


FIGURE 11. TYPICAL APPLICATION

Theory of Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point where the multi-phase power conversion advantage is pronounced. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6244 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram in Figure 12 provides a top level view of multi-phase power conversion using the ISL6244 controller.

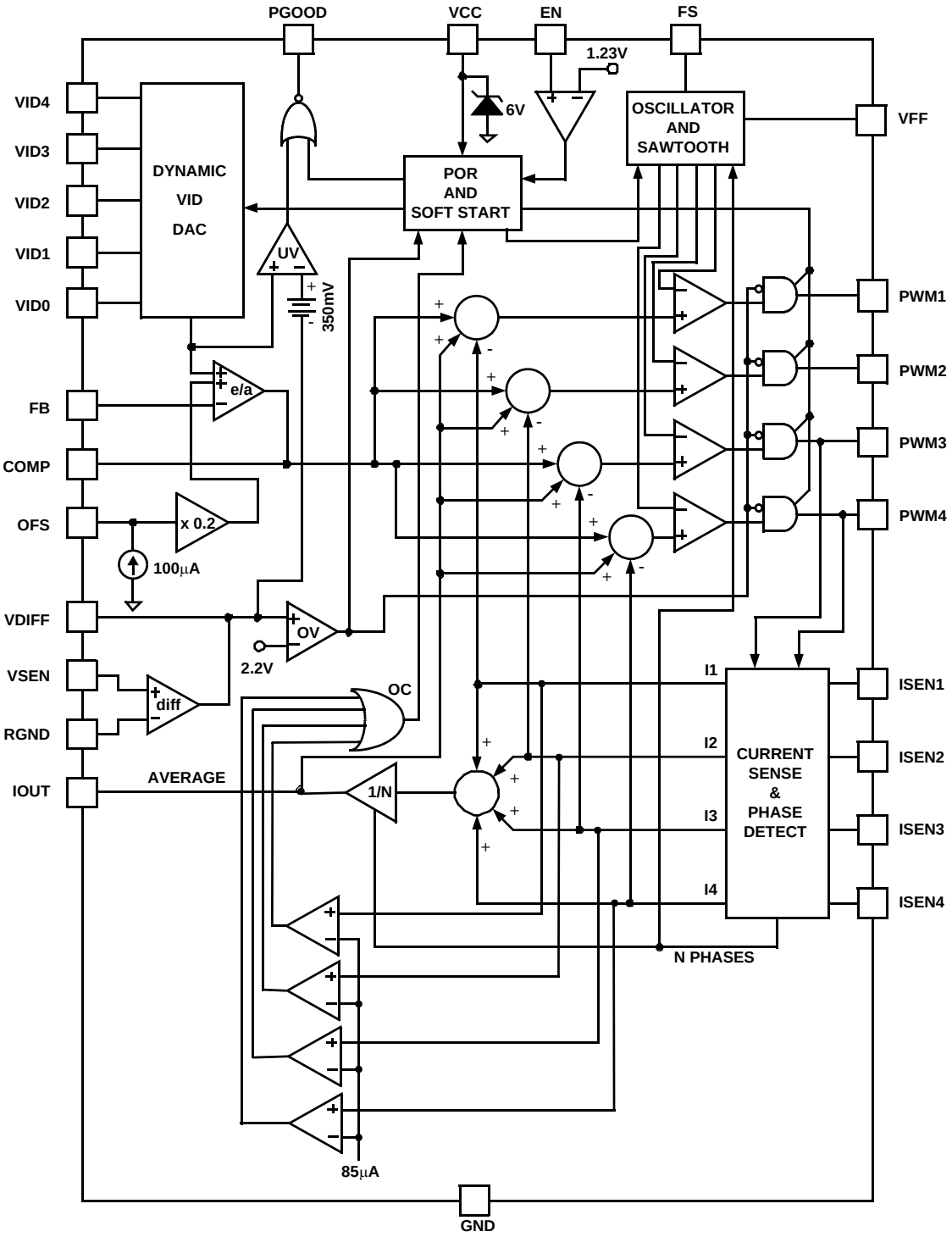


FIGURE 12. BLOCK DIAGRAM

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

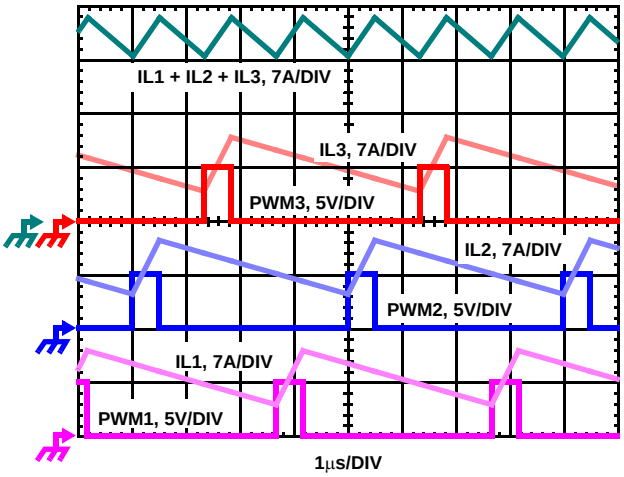


FIGURE 13. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Figure 13 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3), combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle, or 1.33µs for f_S = 250kHz, after the PWM pulse of the previous phase. The peak-to-peak current waveforms for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 14 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

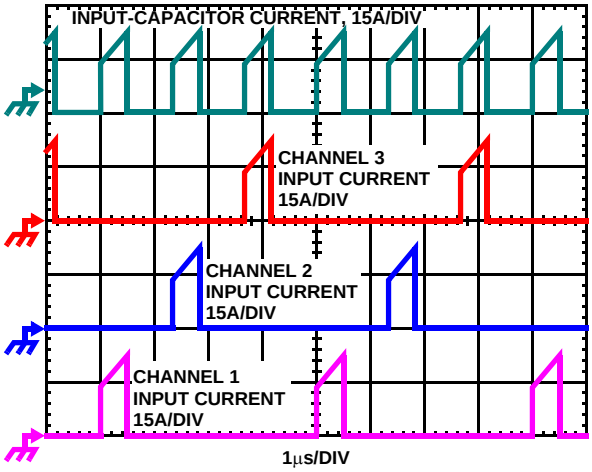


FIGURE 14. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 14 delivers 52A to a 1.20V load from a 19V input. The RMS input capacitor current is 6.5A. Compare this to a single-phase converter also stepping down 19V to 1.20V at 52A. The single-phase converter has 11.96A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 28, 29 and 30 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 31 shows the single phase input-capacitor RMS current for comparison.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6244 is four. One switching cycle is defined as the time between PWM1 pulse termination signals. The pulse termination signal is an internally generated clock signal which triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands the channel-1 PWM output to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/4 of a cycle after PWM1. The PWM 3 output follows another 1/4 of a cycle after PWM2. PWM4 terminates another 1/4 of a cycle after PWM3.

If PWM3 is connected to VCC, then two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle later. Connecting PWM4 to VCC selects three channel operation and the pulse-termination times are spaced in 1/3 cycle increments.

Once a PWM signal transitions low, it is held low for a minimum of 1/4 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 1. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sensing

During the forced off time following a PWM transition low, the controller senses channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, see Figure 15. A ground-referenced amplifier, internal to the ISL6244, connects to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $R_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is then sampled and held after sufficient settling time every switching cycle. The sampled current, I_n, is used for channel-current balance, load-line regulation and overcurrent protection. From Figure 15, the following equation for I_n is derived

$$I_n = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 3)}$$

where I_L is the channel current.

If $R_{DS(ON)}$ sensing is not desired, an independent current-sense resistor in series with the lower MOSFET source can serve as a sense element. The circuitry shown in Figure 15 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending upon the status of the PWM3 and PWM4 pins as described in the previous section.

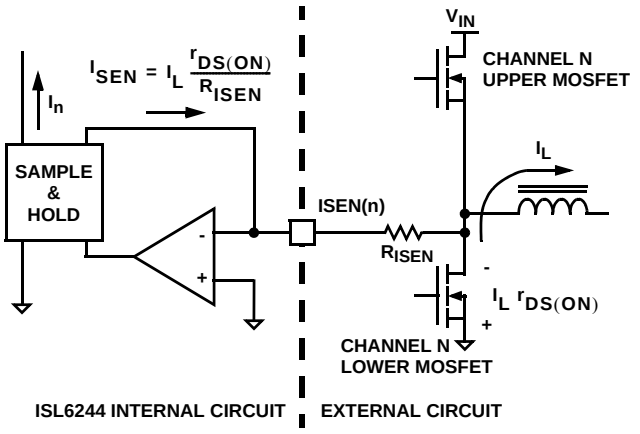


FIGURE 15. INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

Channel-Current Balance

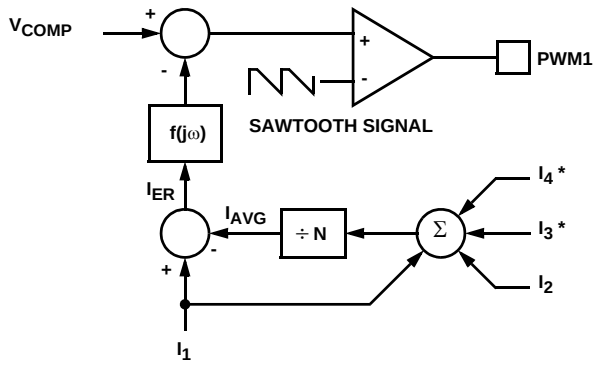
The sampled current, I_n, from each active channel is used to gauge both overall load current and the relative channel current carried in each leg of the converter. The individual sample currents are summed and divided by the number of active channels. The resulting average current, I_{AVG}, provides a measure of the total load current demand on the converter and the appropriate level of channel current. Using Figures 15 and 16, the average current is defined as:

$$I_{AVG} = \frac{I_1 + I_2 + \ldots I_N}{N} \quad \text{(EQ. 4)}$$

$$I_{AVG} = \frac{I_{OUT}}{N} \frac{r_{DS(ON)}}{R_{ISEN}}$$

where N is the number of active channels and I_{OUT} is the total load current.

The average current is then subtracted from the individual channel sample currents. The resulting error current, I_{ER}, is then filtered before it adjusts V_{COMP}. The modified V_{COMP} signal is compared to a sawtooth ramp signal and produces a pulse width which corrects for any imbalance and drives the error current toward zero. Figure 16 illustrates Intersil's patented current-balance method as implemented on channel-1 of a multi-phase converter.



NOTE: *Channels 3 and 4 are optional.

FIGURE 16. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Two considerations designers face are MOSFET selection and inductor design. Both are significantly improved when channel currents track at any load level. The need for complex drive schemes for multiple MOSFETs, exotic magnetic materials, and expensive heat sinks is avoided, resulting in a cost-effective and easy to implement solution relative to single-phase conversion. Channel-current balance insures the thermal advantage of multi-phase conversion is realized. Heat dissipation is spread over multiple channels and a greater area than single phase approaches.

Voltage Regulation

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to modulate the pulse width of the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. Three distinct inputs to the error amplifier determine the voltage level of V_{COMP}. The internal and external circuitry which control voltage regulation is illustrated in Figure 17.

Most multi-phase controllers simply have the output voltage fed back to the inverting input of the error amplifier through a resistor. The ISL6244 features an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense amplifier output, V_{DIFF}, is then tied through an external resistor to the inverting input of the error amplifier.

A digital to analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID4 through VID0. The DAC decodes a 5-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 20μA pull-up to an internal 2.5V source for use with open-drain outputs. External pull-up resistors or active-high output stages can augment the pull-up current sources, but a slight accuracy error can occur if they are pulled above 2.9V. The DAC-selected reference voltage is connected to the non-inverting input of the error amplifier.

The ISL6244 features a second non-inverting input to the error amplifier which allows the user to directly offset the DAC reference voltage in the positive direction only. The offset voltage is created by an internal current source which feeds out the OFS pin into a user selected external resistor to ground.

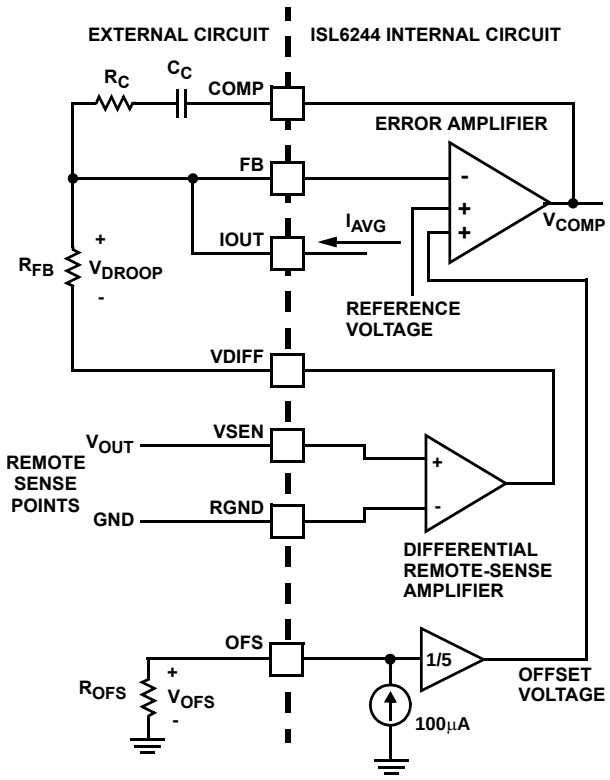


FIGURE 17. OUTPUT-VOLTAGE AND LOAD-LINE REGULATION

The resulting voltage across the resistor, V_{OFS}, is internally divided down by five to create the offset voltage. This method of offsetting the DAC voltage is more accurate than external methods of level-shifting the FB pin.

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

The integrating compensation network shown in Figure 17 assures that the steady-state error in the output voltage is limited to the error in the reference voltage (output of the DAC) plus offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6244 to include all variations in current sources, amplifiers and the reference so that the output voltage remains within the specified system tolerance of ±1%. The 1% does not include the VID offset tolerance or any external component tolerances.

FEED-FORWARD RAMP COMPENSATION

The ISL6244 features a V_{FF} pin for setting the pulse width modulator gain. The V_{FF} voltage is set by a resistor divider network from the battery voltage, as illustrated in Figure 18. The V_{FF} voltage sets the peak-to-peak voltage of the ramp oscillator relative to the battery voltage. By feeding the battery voltage forward, the pulse width modulation gain, G_{mod}, is independent of battery voltage, see Equation 5.

$$G_{mod} = \frac{d_{MAX} \cdot V_{BATTERY}}{\frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \cdot V_{BATTERY}} = 0.75x10 = 7.5 \quad \text{(EQ. 5)}$$

The ramp modulator gain is then set by the ratio of the maximum duty cycle, d_{MAX}, to the amount of attenuation programmed by the resistor network on the V_{FF} pin. For typical applications, select R_{ADJ1} to be 9 times the value of R_{ADJ2} for a 1/10 attenuation of the battery voltage, resulting in a constant pulse width modulator gain of 7.5 over the entire range of battery voltage (see note below).

NOTE: the V_{FF} voltage must be bounded between 0.5V and 2.5V.

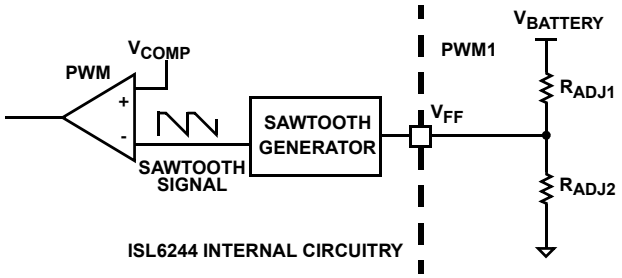


FIGURE 18. BATTERY VOLTAGE FEED-FORWARD COMPENSATION

LOAD-LINE REGULATION

Microprocessor load current demands change from near no-load to full load often during operation. The resulting sizable transient current slew rate causes an output voltage spike since the converter is not able to respond fast enough to the rapidly changing current demands. The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. In order to drive the cost of the output capacitor solution down, one commonly accepted approach is active voltage positioning. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works against the voltage spike.

The average current of all the active channels, I_{AVG}, flows out IOUT, see Figure 17. IOUT is connected to FB through a load-line regulation resistor, R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as

$$V_{DROOP} = I_{AVG} R_{FB} \quad \text{(EQ. 6)}$$

In most cases, each channel uses the same R_{ISEN} value to sense current. A more complete expression for V_{DROOP} is derived by combining equations 15 and 16.

$$V_{DROOP} = \frac{I_{OUT}}{N}\frac{r_{DS(ON)}}{R_{ISEN}}R_{FB} \quad \text{(EQ. 7)}$$

Droop is an optional feature of the ISL6244. If active voltage positioning is not required, simply leave the IOUT pin open.

REFERENCE OFFSET

Typical microprocessor tolerance windows are centered around a nominal DAC set point. Implementing a load-line would require offsetting the output voltage above this nominal DAC set point, centering the load-line within the static specification window. The ISL6244 features an internal 100µA current source which feeds out the OFS pin. Placing a resistor from OFS and ground allows the user to set the amount of positive offset desired directly to the reference voltage. The voltage developed across the OFS resistor, R_{OFS}, is divided down internally by a factor of 5 and directly counters the DAC voltage at the error amplifier non-inverting input. Select the resistor value based on the voltage offset desired, V_{OFS}, using Equation 19.

$$R_{OFS} = \frac{5 \cdot V_{OFS}}{100\mu A} \quad \text{(EQ. 8)}$$

DYNAMIC VID

Next generation microprocessors can change VID inputs at any time while the regulator is in operation. The power management solution is required to monitor the DAC inputs and respond to VID voltage transitions or 'on-the-fly' VID changes, in a controlled manner, supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption.

The ISL6244 will register a VID change within 1 to 2 clock cycles. If the VID change is stable for an additional 1 to 2 clock cycles, the controller will begin executing the output voltage change. The controller begins incrementing the reference voltage by making 25mV steps every two switching cycles until it reaches the new VID code.

The total time required for a VID change, t_{DV}, is dependent on the switching frequency (f_S), the size of the change (ΔVID), and the time before the next switching cycle begins. Since the ISL6244 recognizes VID-code changes only at the beginning of switching cycles, up to one full cycle may pass before a VID change registers. This is followed by a one-cycle wait before the output voltage begins to change. The uncertainty in Equation 9 is due to the possibility that the VID code change may occur between two and four full cycles before being recognized.

$$\frac{2}{f_S}\left(\frac{\Delta VID}{0.025}+1\right) < t_{DV} \leq \frac{2}{f_S}\left(\frac{\Delta VID}{0.025}+2\right) \quad \text{(EQ. 9)}$$

The time required for a converter running with f_S = 250kHz to make a 1.2V to 1.4V reference-voltage change is between 72µs and 80µs as calculated using Equation 9. This example is also illustrated in Figure 7.

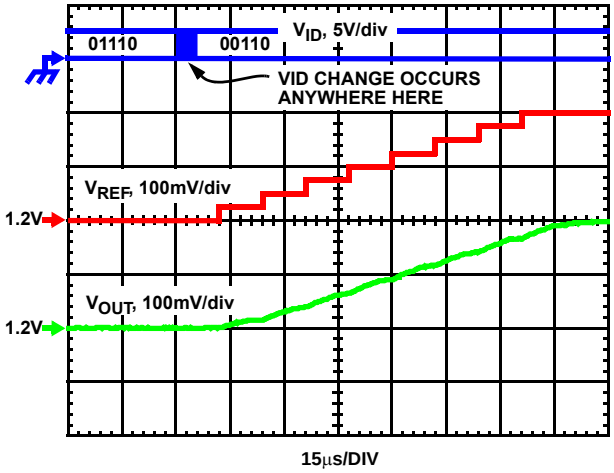


FIGURE 19. DYNAMIC-VID WAVEFORMS FOR 250kHz ISL6244 BASED MULTI-PHASE BUCK CONVERTER

Operation Initialization

Before converter operation is initialized, proper conditions must exist on the enable and disable inputs. Once these conditions are met, the controller begins a soft-start interval. Once the output voltage is within the proper window of operation, the PGOOD output changes state to update an external system monitor.

Enable and Disable

The PWM outputs are held in a high-impedance state to assure the drivers remain off while in shutdown mode. Three separate input conditions must be met before the ISL6244 is released from shutdown mode.

First, the bias voltage applied at VCC must reach the internal power-on reset (POR) circuit rising threshold. Once this threshold is met, proper operation of all aspects of the ISL6244 is guaranteed. Hysteresis between the rising and falling thresholds insures that once enabled, the ISL6244 will not inadvertently turn off unless the bias voltage drops substantially. See the *Electrical Specifications* for specifics on POR rising and falling thresholds.

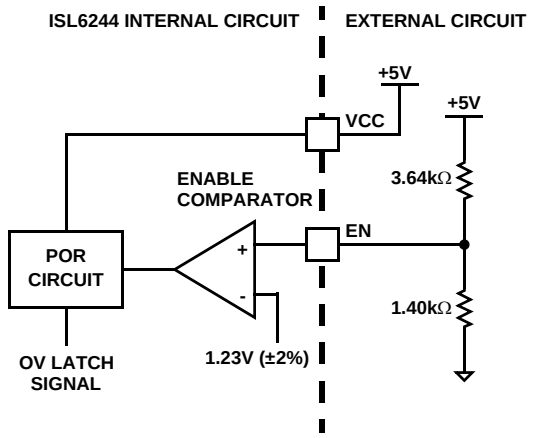


FIGURE 20. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

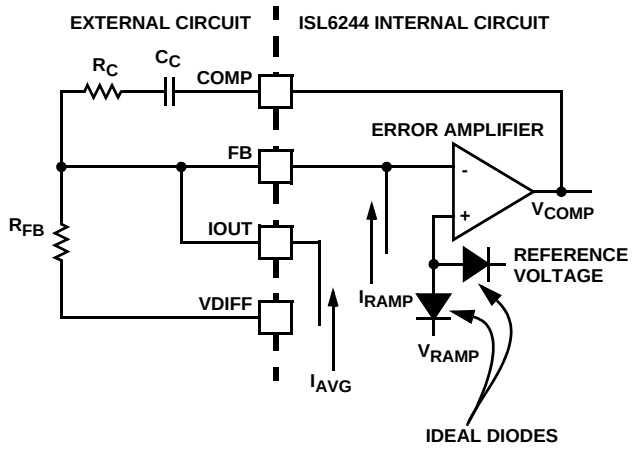


FIGURE 21. RAMP CURRENT AND VOLTAGE FOR REGULATING SOFT-START SLOPE AND DURATION

Second, the ISL6244 features an enable input (EN) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6244 in shutdown until the voltage at EN rises above 1.23V. The enable comparator has about 90mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the ISL6244 becomes enabled. The schematic in Figure 20 demonstrates sequencing the ISL6244 with the ISL620X family of Intersil MOSFET drivers which require 5V bias.

The 11111 VID code is reserved as a signal to the controller that no load is present. The controller will enter shutdown mode after receiving this code and will start up upon receiving any other code. This code is not intended as a means of enabling the controller when a load is present.

To enable the controller, VCC must be greater than the POR threshold; the voltage on EN must be greater than 1.23V; and VID cannot be equal to 11111. Once these conditions are true, the controller immediately initiates a soft-start sequence.

Soft-Start

The soft-start time, t_{SS}, is determined by an 11-bit counter that increments with every pulse of the phase clock. For example, a converter switching at 250kHz per phase has a soft-start time of

$$T_{SS} = \frac{2048}{f_{SW}} = 8.3ms \quad \text{(EQ. 10)}$$

During the soft-start interval, the soft-start voltage, V_{RAMP}, increases linearly from zero to 140% of the programmed DAC voltage. At the same time a current source, I_{RAMP}, is decreasing from 160µA down to zero. These signals are connected as shown in Figure 21 (I_{OUT} may or may not be connected to FB depending on the particular application).

The ideal diodes in Figure 21 assure that the controller tries to regulate its output to the lower of either the reference voltage or V_{RAMP}. Since I_{RAMP} creates an initial offset across R_{FB} of (R_{FB} x 160µA), the first PWM pulse will not be seen until V_{RAMP} is greater than the $R_{FB}I_{RAMP}$ offset. This produces a delay after the ISL6244 enables before the output voltage starts moving. For example, if VID = 1.5V, R_{FB} = 1kΩ and T_{SS} = 8.3ms, the delay time can be expressed using Equation 11.

$$t_{DELAY} = \frac{T_{SS}}{1 + \frac{1.4(VID)}{R_{FB}160 \times 10^{-6}}} = 560\mu s \quad \text{(EQ. 11)}$$

Following the delay, the soft start ramps linearly until V_{RAMP} reaches VID. For the system described above, this first linear ramp will continue for approximately

$$t_{RAMP1} = \frac{T_{SS}}{1.4} - t_{DELAY} = 5.27ms \quad \text{(EQ. 12)}$$

The final portion of the soft-start sequence is the time remaining after V_{RAMP} reaches VID and before I_{RAMP} gets to zero. This is also characterized by a slight change in the slope of the output voltage ramp which, for the current example, exists for a time of

$$t_{RAMP2} = T_{SS} - t_{RAMP1} - t_{DELAY} = 2.34ms \quad \text{(EQ. 13)}$$

This behavior is seen in the example in Figure 22 of a converter switching at 500kHz. For this converter, R_{FB} is set to 2.67kΩ leading to T_{SS} = 4.0ms, t_{DELAY} = 700ns, t_{RAMP1} = 2.23ms, and t_{RAMP2} = 1.17ms.

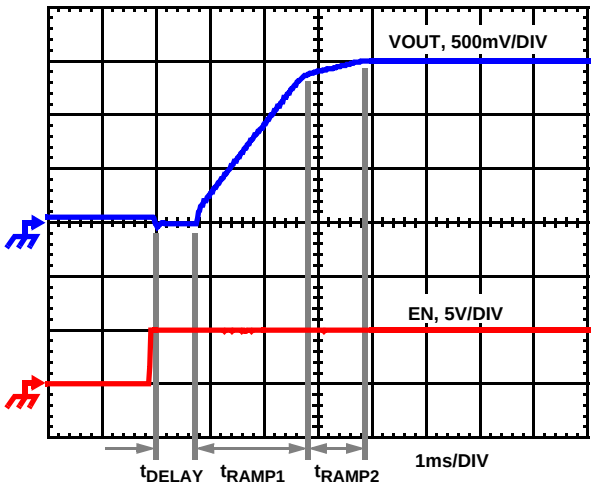


FIGURE 22. SOFT-START WAVEFORMS FOR ISL6244 BASED MULTI-PHASE BUCK CONVERTER

NOTE: Switching frequency 500kHz and R_{FB} = 2.67kΩ.

Fault Monitoring and Protection

The ISL6244 actively monitors voltage and current feedback to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indication signal is provided for linking to external system monitors. The schematic in Figure 23 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output which indicates that the converter is operating properly and the output voltage is within a set window. The under-voltage (UV) and over-voltage (OV) comparators create the output voltage window. The controller also takes advantage of current feedback to detect output over-current (OC) conditions. PGOOD pulls low during shutdown and releases high during soft-start once the output voltage reaches the DAC level. Once high, PGOOD will only transition low when the controller is disabled or a fault condition is detected. It will return high under certain circumstances once a fault clears.

Under-Voltage Protection

The voltage on V_{DIFF} is internally offset by 350mV before it is compared with the DAC reference voltage. By positively offsetting the output voltage, an UV threshold is created which moves relative to the VID code. During soft-start, the slow rising output voltage eventually exceeds the UV threshold. If a fault condition arises during operation and the output voltage drops below the UV threshold, PGOOD will immediately pull low, but converter operation will continue. PGOOD will return high once the output voltage again reaches regulation.

If the ISL6244 is disabled during operation, the PGOOD signal will not pull low until the output voltage decays below the UV threshold.

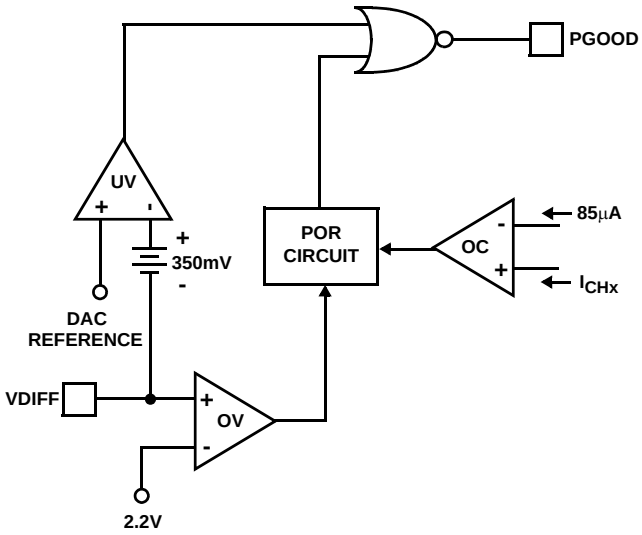


FIGURE 23. POWER GOOD AND PROTECTION CIRCUITRY

Over-Voltage Protection

When the output of the differential amplifier (VDIFF) reaches 2.2V, PGOOD immediately goes low indicating a fault. Two protective actions are taken by the ISL6244 to protect the microprocessor load.

All PWM outputs are commanded low, directing the Intersil drivers to turn on the lower MOSFETs. This shunts the output to ground preventing any further increase in output voltage. The PWM outputs remain low until VDIFF falls to the programmed DAC level at which time they go into a high-impedance state. The Intersil drivers respond by turning off both upper and lower MOSFETs. If the over-voltage condition recurs, the ISL6244 will again command the lower MOSFETs to turn on. The ISL6244 will continue to protect the load in this fashion as long as the over-voltage repeats.

Once an over-voltage condition is detected, normal PWM operation ceases and PGOOD remains low until the ISL6244 is reset. Cycling the voltage on EN below 1.23V or the bias to VCC below the POR-falling threshold will reset the controller.

Over-Current Protection

The ISL6244 monitors individual channel current to detect an over-current condition. Each channel current is continually compared with a constant 85µA reference current. Once any of the currents exceeds the reference current, the comparator triggers the converter to shutdown. The POR circuit places all PWM signals in a high-impedance state which commands the drivers to turn off both upper and lower MOSFETs. PGOOD pulls low and the system remains in this state while the controller counts 2048 phase clock cycles. This is followed by a soft-start attempt (see *Soft-Start*).

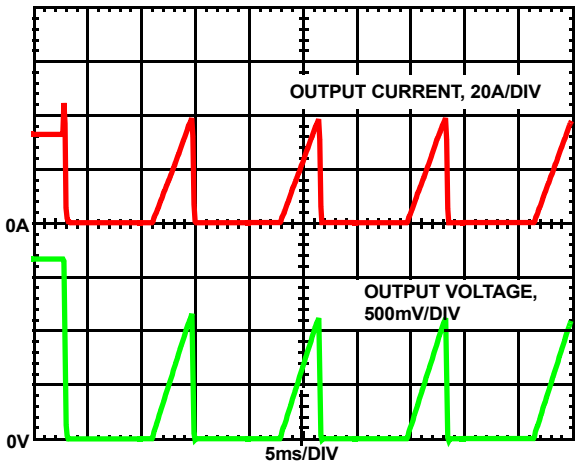


FIGURE 24. OVERCURRENT BEHAVIOR IN HICCUP MODE

During the soft-start interval, the over-current protection circuitry remains active. As the output voltage ramps up, if an over-current condition is detected, the ISL6244 immediately places all PWM signals in a high-impedance state. The ISL6244 repeats the 2048-cycle wait period and follows with another soft-start attempt, as shown in Figure 24. This hiccup mode of operation repeats up to seven times. On the eighth soft-start attempt, the part latches off. Once latched off, the ISL6244 can only be reset when the voltage on EN is brought below 1.23V or VCC is brought below the POR falling threshold. Upon completion of a successful soft-start attempt, operation will continue as normal, PGOOD will return high, and the OC latch counter is reset.

During VID-on-the-fly transitions, the OC comparator output is blanked. The quality and mix of output capacitors used in different applications leads to a wide output capacitance range. Depending upon the magnitude and direction of the VID change, the change in voltage across the output capacitors could result in significant current flow. Summing this instantaneous current with the load current already present could drive the average current above the reference current level and cause an OC trip during the transition. By blanking the OC comparator during the VID-on-the-fly transition, nuisance tripping is avoided.

Application Information

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board and the total board space available for power-supply circuitry. Generally speaking, the most economical solutions are those where each phase handles between 15 and 20A. In cases where board space is the limiting constraint, current can be pushed as high as 30A per phase, but these designs require heat sinks and forced air to cool the MOSFETs.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 14, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_L = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2(1-d) + \frac{I_{L,PP}^2(1-d)}{12}\right] \quad \text{(EQ. 14)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_S; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_D = V_{D(ON)} f_S\left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) t_{d2}\right] \quad \text{(EQ. 15)}$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of P_L and P_D.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 16, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right) f_S \quad \text{(EQ. 16)}$$

The upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 17, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right) f_S \quad \text{(EQ. 17)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$ and is approximately

$$P_{UP,3} = V_{IN} Q_{rr} f_S \quad \text{(EQ. 18)}$$

Finally, the resistive part of the upper MOSFET's is given in Equation 19 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 19)}$$

In this case, of course, $r_{DS(ON)}$ is the on resistance of the upper MOSFET.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 16, 17, 18 and 19. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process that involves repetitively solving the loss equations for different MOSFETs and different switching frequencies until converging upon the best solution.

Current Sensing

The ISEN pins are denoted ISEN1, ISEN2, ISEN3 and ISEN4. The resistors connected between these pins and their respective phase nodes determine the gains in the load-line regulation loop and the channel-current balance loop. Select the values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full-load operating current, I_{FL}; and the number of phases, N according to Equation 20 (see also Figure 15).

$$R_{ISEN} = \frac{r_{DS(ON)}}{50 \times 10^{-6}} \frac{I_{FL}}{N} \quad \text{(EQ. 20)}$$

In certain circumstances, it may be necessary to adjust the value of one or more of the ISEN resistors. This can arise when the components of one or more channels are inhibited from dissipating their heat so that the affected channels run hotter than desired (see the section entitled *Channel-Current Balance*). In these cases, chose new, smaller values of R_{ISEN} for the affected phases. Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 21)}$$

In Equation 21, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 21 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve perfect thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 17. Its value depends on the desired full-load droop voltage (V_{DROOP} in Figure 17). If Equation 20 is used to select each ISEN resistor, the load-line regulation resistor is as shown in Equation 22.

$$R_{FB} = \frac{V_{DROOP}}{50 \times 10^{-6}} \quad \text{(EQ. 22)}$$

If one or more of the ISEN resistors was adjusted for thermal balance, as in Equation 21, the load-line regulation resistor should be selected according to Equation 23. Where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the n^{th} ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL}\, r_{DS(ON)}} \sum_n R_{ISEN(n)} \quad \text{(EQ. 23)}$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in Load-Line Regulation, there are two distinct methods for achieving these goals.

COMPENSATING LOAD-LINE REGULATED CONVERTER

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

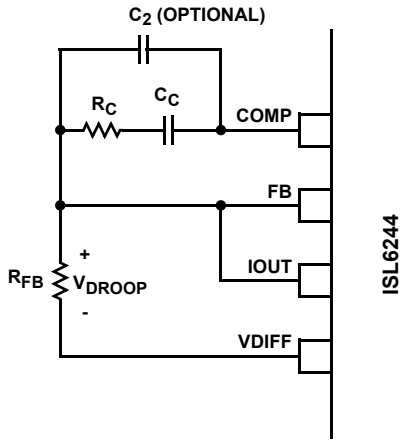


FIGURE 25. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6244 CIRCUIT

Since the system poles and zero are effected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator by compensating the L-C poles and the ESR zero of the voltage-mode approximation yields a solution that is always stable with very close to ideal transient performance.

The feedback resistor, R_{FB}, has already been chosen as outlined in *Load-Line Regulation Resistor*. Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the three cases which follow, there is a separate set of equations for the compensation components.

Case 1: $\frac{1}{2\pi\sqrt{LC}} > f_0$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}\sqrt{LC}}{0.75V_{IN}}$$

$$C_C = \frac{0.75V_{IN}}{2\pi V_{PP} R_{FB} f_0}$$

Case 2: $\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB}\frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.75\,V_{IN}} \qquad \text{(EQ. 24)}$$

$$C_C = \frac{0.75V_{IN}}{(2\pi)^2 f_0^2 V_{PP} R_{FB}\sqrt{LC}}$$

Case 3: $f_0 > \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp} L}{0.75\,V_{IN}(ESR)}$$

$$C_C = \frac{0.75V_{IN}(ESR)\sqrt{C}}{2\pi V_{PP} R_{FB} f_0\sqrt{L}}$$

In Equations 24, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 16 and *Electrical Specifications*.

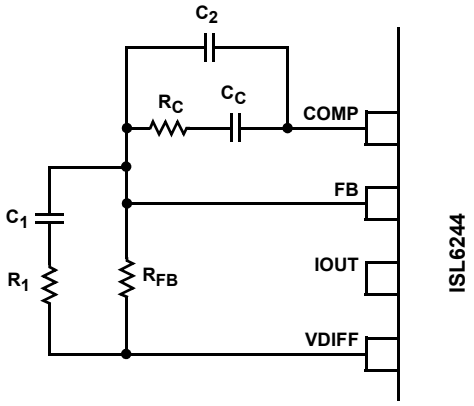


FIGURE 26. COMPENSATION CIRCUIT FOR ISL6244 BASED CONVERTER WITHOUT LOAD-LINE REGULATION

Once selected, the compensation values in Equations 24 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equations 24 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 25). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

COMPENSATION WITHOUT LOAD-LINE REGULATION

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 26, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to chose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equations 25, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equations 25.

$$R_1 = R_{FB}\frac{C(ESR)}{\sqrt{LC} - C(ESR)}$$

$$C_1 = \frac{\sqrt{LC} - C(ESR)}{R_{FB}}$$

$$C_2 = \frac{0.75V_{IN}}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}}$$

$$R_C = \frac{V_{PP}(2\pi)^2 f_0 f_{HF} LCR_{FB}}{0.75V_{IN}\left[\left(2\pi f_{HF}\sqrt{LC} - 1\right)\right]}$$

$$C_C = \frac{0.75V_{IN}\left(2\pi f_{HF}\sqrt{LC} - 1\right)}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}} \quad \text{(EQ. 25)}$$

In Equations 25, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 16 and *Electrical Specifications*.

Output Filter Design

The output inductors and the output capacitor bank together form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy during the interval of time after the beginning of the transient until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response leaving the output capacitor bank to supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 26)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR)\frac{\left(V_{IN} - NV_{OUT}\right)V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \quad \text{(EQ. 27)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limits on inductance.

$$L \leq \frac{2NCV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \quad \text{(EQ. 28)}$$

$$L \leq \frac{(N \cdot \Delta V_{MAX} \cdot C)(1.5V_{IN} - 2V_O)}{(\Delta I)^2} \quad \text{(EQ. 29)}$$

Equation 29 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 28 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

Input Supply Voltage Selection

The VCC input of the ISL6244 can be connected to either a +5V supply directly or through a current limiting resistor to a +12V supply. An integrated 5.8V shunt regulator maintains the voltage on the VCC pin when a +12V supply is used. A 300Ω resistor is suggested for limiting the current into the VCC pin to approximately 20mA.

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T (see Figure 11). Figure 27 and Equation 30 are provided to assist in the selecting the correct value for R_T.

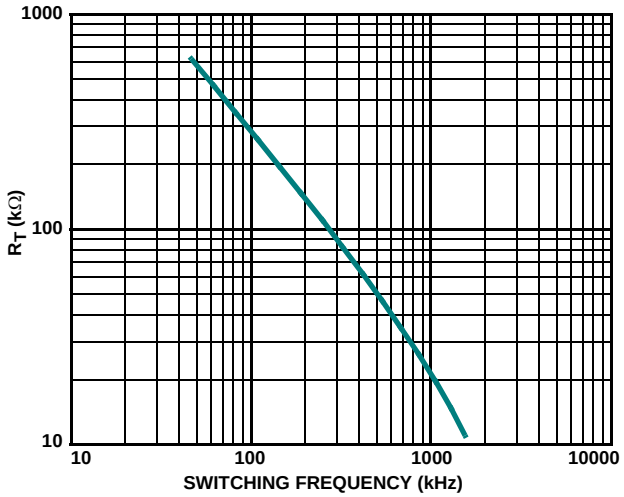


FIGURE 27. R_T vs SWITCHING FREQUENCY

$$R_T = 10^{[11.09 - 1.13\log(f_S)]} \quad \text{(EQ. 30)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

For a two phase design, use Figure 28 to determine the input-capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the combined peak-to-peak inductor current ($I_{C,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

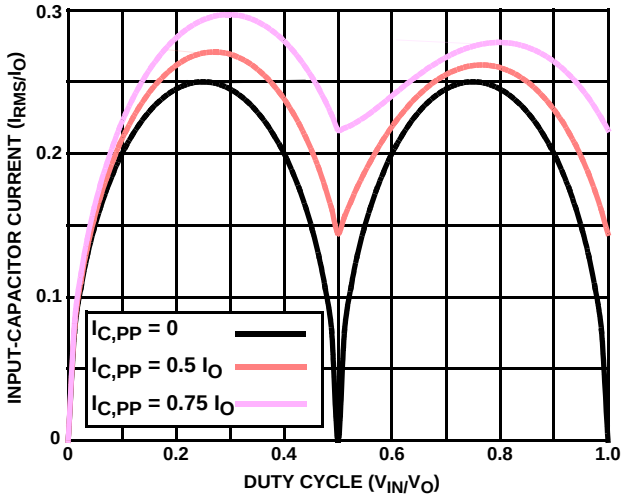


FIGURE 28. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

Figures 29 and 30 provide the same input RMS current information for three and four phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as described above.

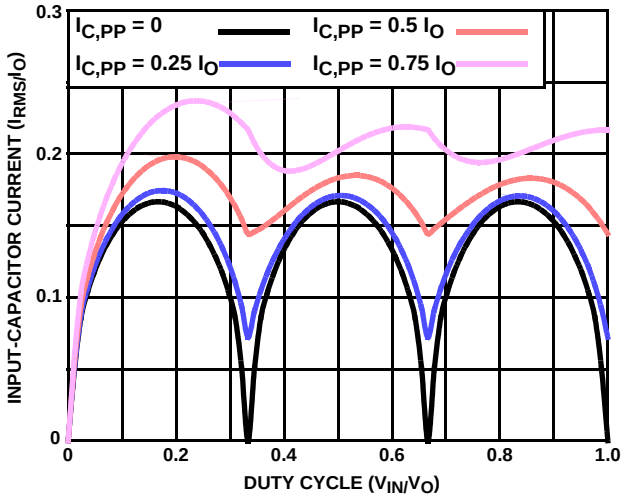


FIGURE 29. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

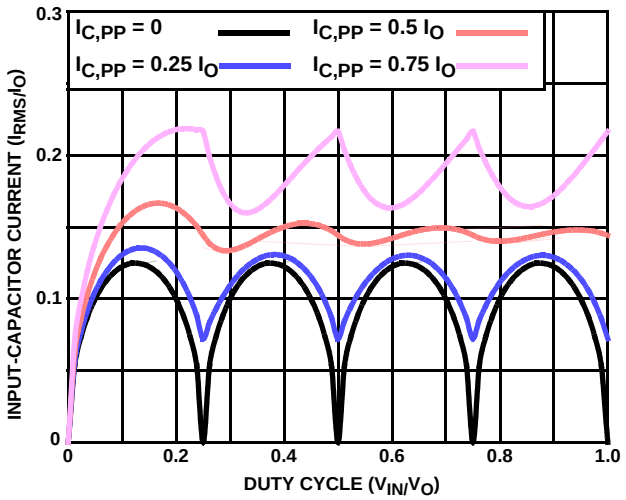


FIGURE 30. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

MULTIPHASE RMS IMPROVEMENT

Figure 31 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology.

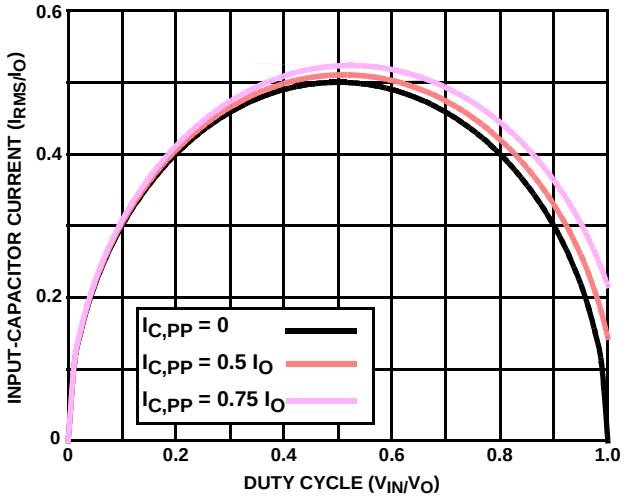


FIGURE 31. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

For example, compare the input rms current requirements of a two-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{C,PP}$ to I_O of 0.5. The single phase converter would require 17.3 Arms current capacity while the two-phase converter would only require 10.9 Arms. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout Considerations

Printed circuit board (PCB) layout is very important in high frequency switching converter design. With components switching at greater than 200kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, lead to device over-voltage stress, radiate noise into sensitive nodes, and increase thermal stress on critical components. Careful component placement and PCB layout minimizes the voltage spikes in the converter.

The following multi-layer printed circuit board layout strategies minimize the impact of board parasitics on converter performance and optimize the heat-dissipating capabilities of the printed-circuit board. This section highlights some important practices which should not be overlooked during the layout process.

Component Placement

Determine the total implementation area and orient the critical switching components first. Symmetry is very important in multiphase converter placement and the switching components dictate how the available space is filled. The switching components carry large amounts of energy and tend to generate high levels of noise. A tight layout of the output inductors and MOSFETs with short, wide

traces, such that space between the components is reduced while creating the PHASE plane, is recommended. Stray Inductance in the switch path adds to the voltage spikes generated during the switching interval. By keeping the phase plane small, the magnitude of the potential spikes is minimized. If possible, duplicate the same placement and layout of these components for each phase. Figure 32 illustrates the connection of critical components for one output channel of a converter.

Place the ISL6207 drivers as close as possible to the MOSFETs they control to reduce the parasitics due to trace length between critical driver input and output signals. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFETs drains results in too much trace inductance and a reduction in capacitor performance. In Figure 32, C_{IN} and C_{OUT} represent numerous physical capacitors.

Locate the output capacitors between the inductors and the load, while keeping them in close proximity around the microprocessor socket. Care should be taken not to add inductance in the circuit board traces that could cancel the usefulness of the low inductance components.

The ISL6244 can be placed off to one side or centered relative to the individual phase switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the feedback resistor R_{FB}, frequency select resistor R_{FS}, offset resistor R_{OFS}, feedforward ramp adjustment resistors R_{ADJ1} and R_{ADJ2}, and compensation components R_C and C_C. Because the remote sense traces for VSEN and VRTN may be long and routed close to switching nodes, a 1.0µF ceramic decoupling capacitor can be placed between VSEN and RTN of the package. This value may vary depending on the impact of the converter response.

Bypass capacitors, C_{BP}, supply critical bypassing current for the ISL6244 and ISL6207 drivers bias supplies and must be placed next to their respective pins. Stray trace parasitics will reduce their effectiveness, so keep the traces to these components as short and wide as possible.

Plane Allocation and Routing

Dedicate at least one solid layer, usually a middle layer of the PCB, for a ground plane and make all critical component ground connections with vias to this layer. If two ground layers can be used, it is beneficial to run all signal lines in between these to shield them from radiative coupling. These include the current sense lines from PHASE, PWM, VID and Enable lines. Dedicate one additional solid layer as a power plane and break this plane into smaller islands of common voltage. Keep the metal runs from the PHASE terminal to the output inductor short. The power planes should support the input power and output power nodes. Use copper filled areas on the top and bottom circuit layers for the phase nodes. Use the remaining PCB layers for small signal routing. Size the traces from the ISL6207 driver to the power MOSFET gates and sources to carry at least 1A of continuous current. When routing components in the switching path, use short wide traces to reduce the associated parasitics.

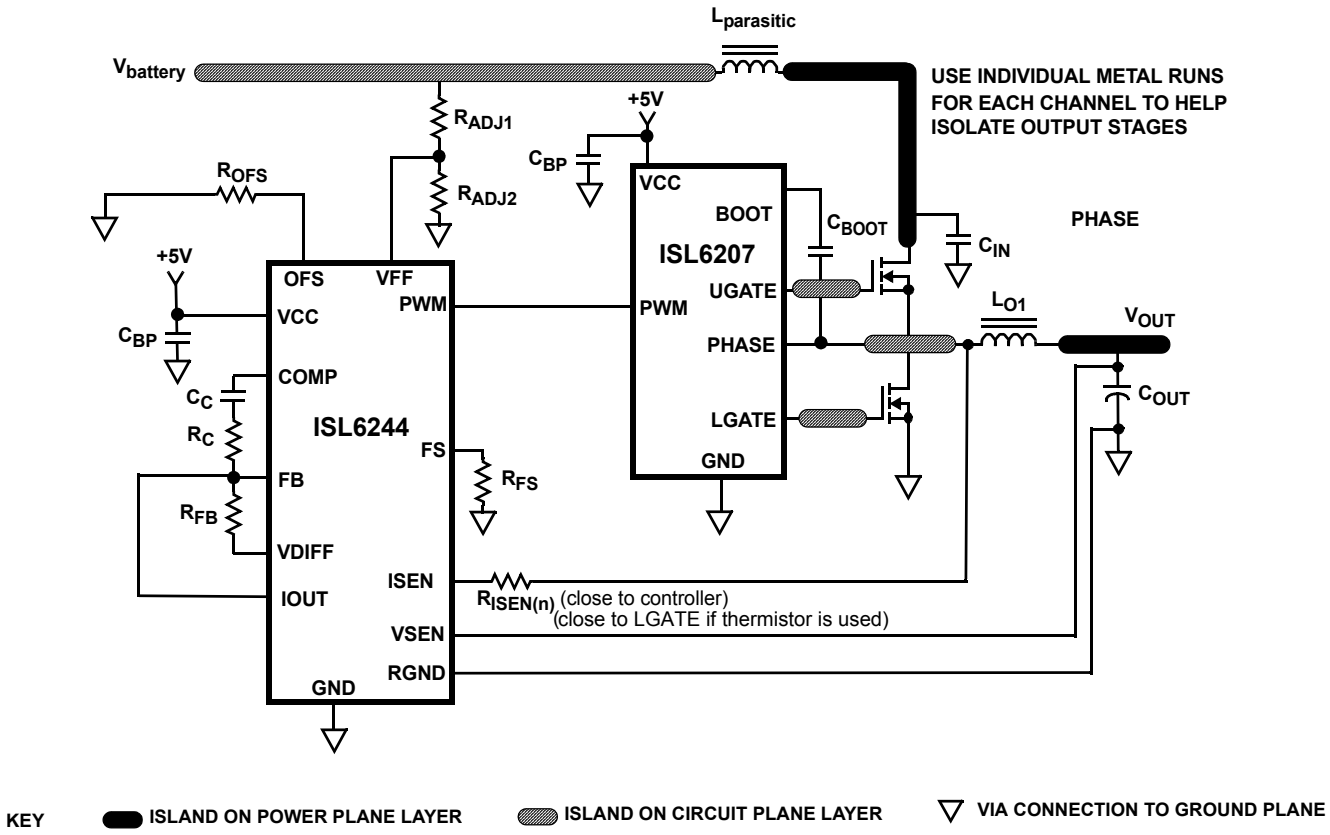
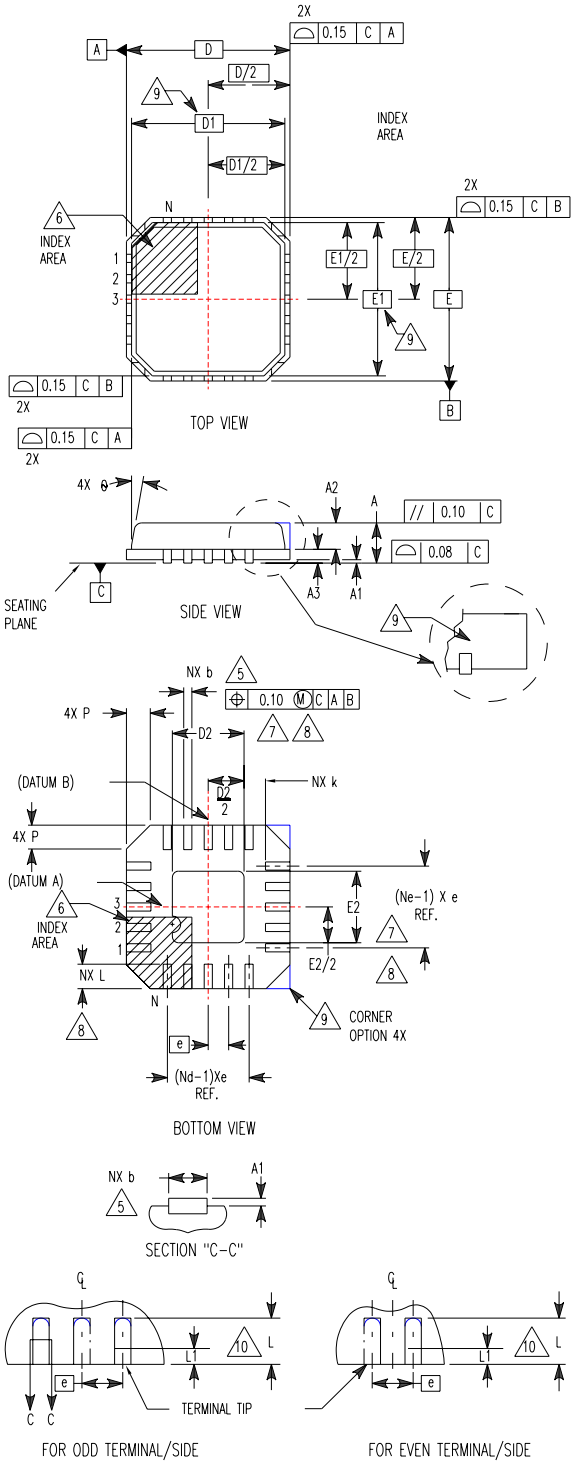


FIGURE 32. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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