Integrated Circuit Systems, Inc.

ICS94228

Programmable System Clock Chip for AMD - K7™ processor

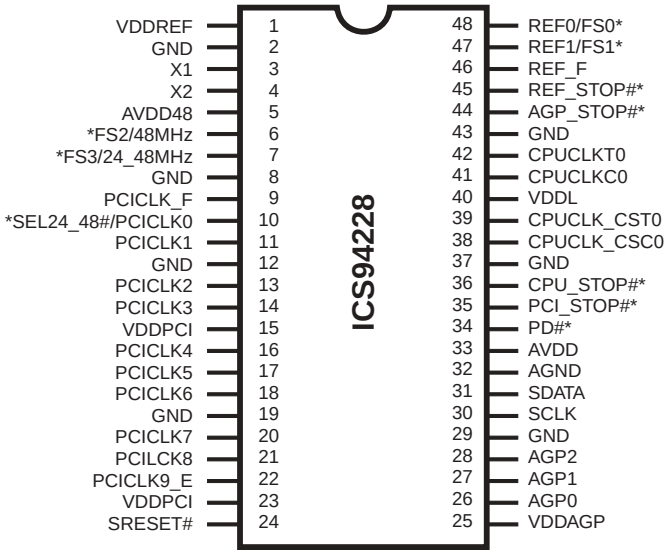
Recommended Application:
VIA KT266 style chipset

Output Features:
- 1 - Differential pair open drain CPU clocks @ 2.7V
- 1 - Differential pair push-pull CPU clocks @ 2.5V
- 11 - PCI including 1 free running and 1 early @ 3.3V
- 1 - 48MHz, @ 3.3V fixed
- 1 - 24/48MHz @ 3.3V
- 3 - REF @ 3.3V, 14.318MHz.

Features:
- Programmable output frequency.
- Programmable output rise/fall time.
- Programmable slew and skew control for CPUCLK, PCICLK, AGP, REF, 48MHz and 24_48MHz.
- Real time system reset output.
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage.
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Uses external 14.318MHz crystal.

Skew Specifications:
- CPU - CPU: <200ps
- PCI - PCI: <500ps
- CPU (early - PCI: min=1.0ns, max=2.6ns
- CPU cycle to cycle jitter: <250ps

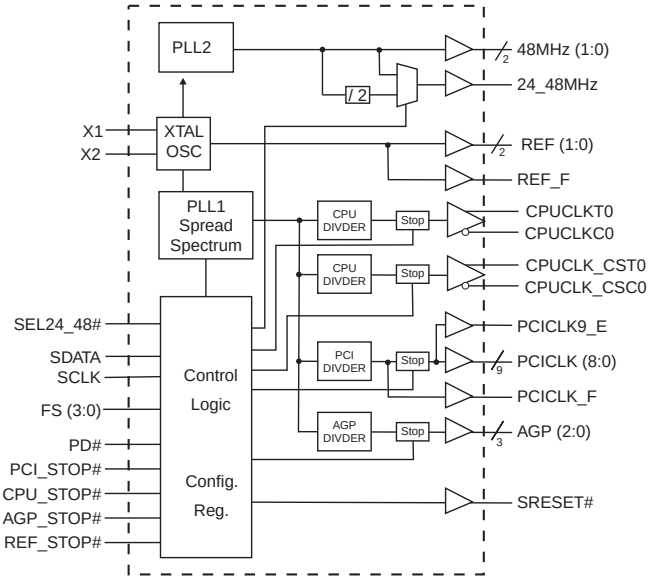
Pin Configuration



48-Pin 300mil SSOP

* Internal Pull-up Resistor of 120K to VDD

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	AGP (MHz)	PCICLK (MHz)
0	0	0	0	233.33	77.78	38.88
0	0	0	1	220.00	73.33	36.67
0	0	1	0	210.00	70.00	35.00
0	0	1	1	200.00	66.67	33.33
0	1	0	0	190.00	76.00	38.00
0	1	0	1	180.00	72.00	36.00
0	1	1	0	170.00	68.00	34.00
0	1	1	1	150.00	75.00	37.50
1	0	0	0	140.00	70.00	35.00
1	0	0	1	120.00	60.00	30.00
1	0	1	0	110.00	66.00	33.00
1	0	1	1	66.67	66.67	33.33
1	1	0	0	200.00	66.67	33.33
1	1	0	1	166.67	66.67	33.33
1	1	1	0	100.00	66.67	33.33
1	1	1	1	133.33	66.67	33.33

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 15, 23, 25,	VDD	PWR	Power supply, nominal 3.3V
2, 8, 12, 19, 29, 37, 43	GND	PWR	Ground
3	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF)
5	AVDD48	PWR	Power supply, nominal 3.3V
6	FS2[1, 2]	IN	Frequency select pin. Latched Input
	48MHz	OUT	48MHz output clock, stoppable by REF_Stop
7	FS3[1, 2]	IN	Frequency select pin. Latched Input
	24_48MHz	OUT	24 or 48MHz clock output, stoppable by REF_Stop
9	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
10	SEL24_48#[1, 2]	IN	Logic input to select 24 or 48MHz for pin 7 output
	PCICLK0	OUT	PCI clock output
21, 20, 18, 17, 16, 14, 13, 11	PCICLK (8:1)	OUT	PCI clock outputs.
22	PCICLK9_E	OUT	Early PCI clock. Leads general PCI clocks by 2ns. Can be stopped by PCI_STOP#.
24	SRESET#[1]	OUT	Real time system reset signal for watchdog tmer timeout. This signal is active low.
28, 27, 26	AGP (2:0)	OUT	AGP clock outputs
30	SCLK	IN	Clock input of I^2C input, 5V tolerant input
31	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
32	AGND	PWR	Analog ground
33	AVDD	PWR	Power supply, nominal 3.3V
34	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
35	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
36	CPU_STOP#[1, 2]	IN	This asynchronous input halts CPUCLKT, CPUCLKC & CUCLKC_CS clocks at logic "0" level when driven low.
38	CPUCLK_CSC0	OUT	"Complementary" clock of differential pair output chipset (push-pull).
39	CPUCLK_CST0	OUT	"True" clock of differential pair CPU output chipset (push-pull).
40	VDDL	PWR	Power supply for CPUCLKs, nominal 2.5V
42	CPUCLKT0	OUT	"True" clock of differential pair CPU output. These open drain outputs need an external 1.5V pull-up (open drain).
41	CPUCLKC0	OUT	"Complementary" clock of differential pair CPU output. These open drain outputs need an external 1.5V pull-up (open drain).
44	AGP_STOP#	IN	Stops all AGP clocks at logic 0 level, when input low
45	REF_STOP#	IN	Stops REF, 48MHz and 24/48MHz clocks at logic 0 level, when input low.
46	REF_F	OUT	14.318 MHz free running reference clock., not afftected by REF_STOP#
47	FS1[1, 2]	IN	Frequency select pin. Latched Input
	REF1	OUT	14.318 MHz reference clock.
48	FS0[1, 2]	IN	Frequency select pin. Latched Input
	REF0	OUT	14.318 MHz reference clock.

Notes:
1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS94228** is a main clock synthesizer chip for AMD-K7 based systems with VIA style chipset. This provides all clocks required for such a system.

The **ICS94228** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

SRESET# Signal Description

The SRESET# signal from ICS94228 system clock generator is a real time active low pulse that can be used to reset the system.

The Open-Drain Nch output Reset# pin needs to be tied to the system reset line which has a pull-up resistor. When activated, the SRESET# output will be driven to a low with a 32ms pulse width.

General I^2C serial interface information for the ICS94228

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 16*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 6 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 6).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 14	
	ACK
Byte 15	
	ACK
Byte 16	
	ACK
Stop Bit	

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B6	***Byte 7***
ACK	
○	○
○	○
○	○
If $1A_H$ has been written to B6	***Byte 14***
ACK	
If $1B_H$ has been written to B6	***Byte 15***
ACK	
If $1C_H$ has been written to B6	***Byte 16***
ACK	
Stop Bit	

*See notes on the following page.

Brief I²C registers description for ICS94228 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1, 2, 3	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	5, 6, 7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Enable Register	4	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers		Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	4, 5	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	9, 10	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	11, 12	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	13, 14	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	15, 16	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPUCLK	AGPCLK	PCICLK	Spread Percentage
SSB1	SSB0	FS3	FS2	FS1	FS0				
0	0	0	0	0	0	233.33	77.78	38.88	+/- 0.25% Center Spread
0	0	0	0	0	1	220.00	73.33	36.67	+/- 0.25% Center Spread
0	0	0	0	1	0	210.00	70.00	35.00	+/- 0.25% Center Spread
0	0	0	0	1	1	200.00	66.67	33.33	+/- 0.25% Center Spread
0	0	0	1	0	0	190.00	76.00	38.00	+/- 0.25% Center Spread
0	0	0	1	0	1	180.00	72.00	36.00	+/- 0.25% Center Spread
0	0	0	1	1	0	170.00	68.00	34.00	+/- 0.25% Center Spread
0	0	0	1	1	1	150.00	75.00	37.50	+/- 0.25% Center Spread
0	0	1	0	0	0	140.00	70.00	35.00	+/- 0.25% Center Spread
0	0	1	0	0	1	120.00	60.00	30.00	+/- 0.25% Center Spread
0	0	1	0	1	0	110.00	66.00	33.00	+/- 0.25% Center Spread
0	0	1	0	1	1	66.67	66.67	33.33	+/- 0.25% Center Spread
0	0	1	1	0	0	200.00	66.67	33.33	+/- 0.25% Center Spread
0	0	1	1	0	1	166.67	66.67	33.33	+/- 0.25% Center Spread
0	0	1	1	1	0	100.00	66.67	33.33	+/- 0.25% Center Spread
0	0	1	1	1	1	133.33	66.67	33.33	+/- 0.25% Center Spread
0	1	0	0	0	0	200.00	66.67	33.33	0 to -0.5% Down Spread
0	1	0	0	0	1	166.67	66.67	33.33	0 to -0.5% Down Spread
0	1	0	0	1	0	100.00	66.67	33.33	0 to -0.5% Down Spread
0	1	0	0	1	1	133.33	66.67	33.33	0 to -0.5% Down Spread
1	0	0	1	0	0	200.00	66.67	33.33	+/- 0.50% Center Spread
1	0	0	1	0	1	166.67	66.67	33.33	+/- 0.50% Center Spread
1	0	0	1	1	0	100.00	66.67	33.33	+/- 0.50% Center Spread
1	0	0	1	1	1	133.33	66.67	33.33	+/- 0.50% Center Spread
1	1	1	0	0	0	200.00	66.67	33.33	+/- 0.75% Center Spread
1	1	1	0	0	1	166.67	66.67	33.33	+/- 0.75% Center Spread
1	1	1	0	1	0	100.00	66.67	33.33	+/- 0.75% Center Spread
1	1	1	0	1	1	133.33	66.67	33.33	+/- 0.75% Center Spread
1	0	1	1	0	0	200.00	66.67	33.33	0 to +0.5% Up Spread
1	0	1	1	0	1	166.67	66.67	33.33	0 to +0.5% Up Spread
1	0	1	1	1	0	100.00	66.67	33.33	0 to +0.5% Up Spread
1	0	1	1	1	1	133.33	66.67	33.33	0 to +0.5% Up Spread

Bit 6: 0 = Hardware select; 1 = I^2C select. Default is OFF.

Bit 7: 0 = Spread off; 1 = Spread spectrum enable. Default is OFF

Byte 1: CPU, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	42, 41	1	CPUCLKT0, CPUCLKC0
Bit 6	39, 38	1	CPUCLK_CST0, CPUCLK_CSC0
Bit 5	6	1	48MHz
Bit 4	7	1	24_48MHz
Bit 3	-	1	FS0 (readback)
Bit 2	28	1	AGP2
Bit 1	27	1	AGP1
Bit 0	26	1	AGP0

Byte 2: PCI, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	20	1	PCICLK7
Bit 6	18	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	14	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	11	1	PCICLK1
Bit 0	10	1	PCICLK0

Byte 3: PCI, REF, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	9	1	PCICLK_F
Bit 6	22	1	PCICLK9_E
Bit 5	-	1	FS1 (readback)
Bit 4	21	1	PCICLK8
Bit 3	46	1	REF_F
Bit 2	-	1	FS2 (readback)
Bit 1	47	1	REF1
Bit 0	48	1	REF0

Byte 4: Watch Dog Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Watch dog enable 0: stop 1: start
Bit 6	-	0	M/N program enable
Bit 5	-	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 8X 580ms = 4.6 seconds.
Bit 4	-	0	
Bit 3	-	1	
Bit 2	-	0	
Bit 1	-	0	
Bit 0	-	0	

Byte 5: Vendor Specific Feature, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	SEL24_48# (readback)
Bit 6	-	0	FS3 (readback)
Bit 5	-	0	Watchdog status: 0=Normal 1=Alarm
Bit 4	-	1	SSB1
Bit 3	-	1	FS3
Bit 2	-	1	FS2
Bit 1	-	1	FS1
Bit 0	-	1	FS0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 6: Vendor ID1 , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Device ID
Bit6	-	0	
Bit5	-	0	
Bit4	-	1	
Bit3	-	0	Vendor ID
Bit2	-	0	
Bit1	-	0	
Bit0	-	1	

Note: Don't write into this register, writing into this register can cause malfunction

Byte 7: Vendor ID2, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Revision ID
Bit 6	-	0	Revision ID
Bit 5	-	0	Revision ID
Bit 4	-	0	Revision ID
Bit 3	-	1	Revision ID
Bit 2	-	1	Revision ID
Bit 1	-	0	Revision ID
Bit 0	-	0	Revision ID

Byte 8: Byte Count Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	1	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Byte 9: VCO Frequency Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	VCO Divder Bit 0
Bit 6	-	X	REF Divder Bit 6
Bit 5	-	X	REF Divder Bit 5
Bit 4	-	X	REF Divder Bit 4
Bit 3	-	X	REF Divder Bit 3
Bit 2	-	X	REF Divder Bit 2
Bit 1	-	X	REF Divder Bit 1
Bit 0	-	X	REF Divder Bit 0

Byte 10: VCO Frequency Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	VCO Divider Bit 8
Bit 6	-	X	VCO Divider Bit 7
Bit 5	-	X	VCO Divider Bit 6
Bit 4	-	X	VCO Divider Bit 5
Bit 3	-	X	VCO Divider Bit 4
Bit 2	-	X	VCO Divider Bit 3
Bit 1	-	X	VCO Divider Bit 2
Bit 0	-	X	VCO Divider Bit 1

Byte 11: VCO Spread Spectrum Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Spread Spectrum Bit 7
Bit 6	-	X	Spread Spectrum Bit 6
Bit 5	-	X	Spread Spectrum Bit 5
Bit 4	-	X	Spread Spectrum Bit 4
Bit 3	-	X	Spread Spectrum Bit 3
Bit 2	-	X	Spread Spectrum Bit 2
Bit 1	-	X	Spread Spectrum Bit 1
Bit 0	-	X	Spread Spectrum Bit 0

Byte 12: VCO Spread Spectrum Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Spread Spectrum Bit 12
Bit 3	-	X	Spread Spectrum Bit 11
Bit 2	-	X	Spread Spectrum Bit 10
Bit 1	-	X	Spread Spectrum Bit 9
Bit 0	-	X	Spread Spectrum Bit 8

Byte 13: Output Skew Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	CPUCLKC0/T0 Skew Control
Bit 6	-	0	
Bit 5	-	0	
Bit 4	-	0	
Bit 3	-	0	CPUCLKC_CST/C Skew Control
Bit 2	-	0	
Bit 1	-	0	
Bit 0	-	0	

Byte 14: Output Skew Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	PCICLK(8:0) Skew Control
Bit 6	-	0	
Bit 5	-	1	
Bit 4	-	0	
Bit 3	-	0	AGP(2:0) Skew Control
Bit 2	-	0	
Bit 1	-	0	PCICLK9_E: Slew Rate Control
Bit 0	-	0	

Byte 15: Output Rise/Fall Time Select Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	CPUCLKT0
Bit 6	-	0	CPUCLKC0
Bit 5	-	0	CPUCLKT_CST
Bit 4	-	0	CPUCLKC_CSC
Bit 3	-	1	AGP(2:0): Slew Rate Control
Bit 2	-	0	
Bit 1	-	0	REF(2:0): Slew Rate Control
Bit 0	-	0	

Byte 16: Output Rise/Fall Time Select Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	PCICLK(3:0): Slew Rate Control
Bit 6	-	0	
Bit 5	-	1	PCICLK(8:4): Slew Rate Control
Bit 4	-	0	
Bit 3	-	0	48MHz: Slew Rate Control
Bit 2	-	0	
Bit 1	-	0	24_48MHz: Slew Rate Control
Bit 0	-	0	

Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz				
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz				
Power Down	PD				600	mA
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew Window	$t_{CPU-PCI}$			2.3	2.6	ns
	$t_{CPU-AGP}$			300	550	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.3	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5V	45	54	57	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK (Open Drain)

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; V_{DDL}=2.5V+/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$				W
Output High Voltage	V_{OH2B}	Termination to Vpull-up(external)	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to Vpull-up(external)			0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3V	18			mA
Rise Time[1], CPUCLK	t_{r2B}	V_{OL} = 20%, V_{OH} = 80%		2.2	2.5	ns
Fall Time[1], CPUCLK	t_{f2B}	V_{OH} = 80%, V_{OL}=20%		1.3	2.0	ns
Differential voltage-AC[1]	V_{DIF}	Note 2	0.4		Vpullup(external) + 0.6	V
Differential voltage-DC[1]	V_{DIF}	Note 2	0.2		Vpullup(external) + 0.6	V
Differential Crossover Voltage[1] CPUCLK(Open Drain)	V_X	Note 3	1.2	1.4	1.7	V
Duty Cycle[1]	d_{t2B}	V_T = 50%	45	50	55	%
Skew[1]	t_{sk2B}	V_T = 50%		140	200	
Jitter, Cycle-to-cycle[1], CPUCLK	$t_{jcyc-cyc2B}$	$V_T = V_X$		150	250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - VDIF specifies the minimum input differential voltages (VTR-VCP) required for switching, where VTR is the "tr

3 - Vpullup(external) = 2.7V, Min = Vpullup(external)/2-150mV; Max=(Vpullup(external)/2)+150mV

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4V		2.0	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4V, V_{OL} = 0.4V		1.8	2.5	ns
Duty Cycle[1]	dt1	V_T = 1.5 V	45	51	55	%
Jitter Cycle-to-Cycle[1]	$tj_{cyc-cyc1}$	V_T = 1.5V		130	500	ps
Skew1(window)	Tsk1	V_T = 1.5V		330	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_E

T_A = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4V		1.7	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4V, V_{OL} = 0.4V		2.0	2.5	ns
Duty Cycle[1]	dt1	V_T = 1.5 V	45	52	55	%
Jitter Cycle-to-Cycle[1]	$tj_{cyc-cyc1}$	V_T = 1.5V		100	500	ps
PCI_E to PCI Skew1	Tsk1	V_T = 1.5V		2.3	2.7	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz

T_A = 0 - 70°C; VDD = 3.3 V +/-5%, VDDL = 2.5 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	tr_5	V_{OL} = 0.4 V, V_{OH} = 2.4V		1.3	4	ns
Fall Time[1]	tf_5	V_{OH} = 2.4 V, V_{OL} = 0.4V		1.3	4	ns
Duty Cycle[1]	dt_5	VT = 1.5 V	45	52	55	%
Jitter, Cycle-to-Cycle [1]	tjcyc-cyc1	V_T = 1.5 V		190	500	ps
Jitter, Absolute[1]	tjabs5	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS94228 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

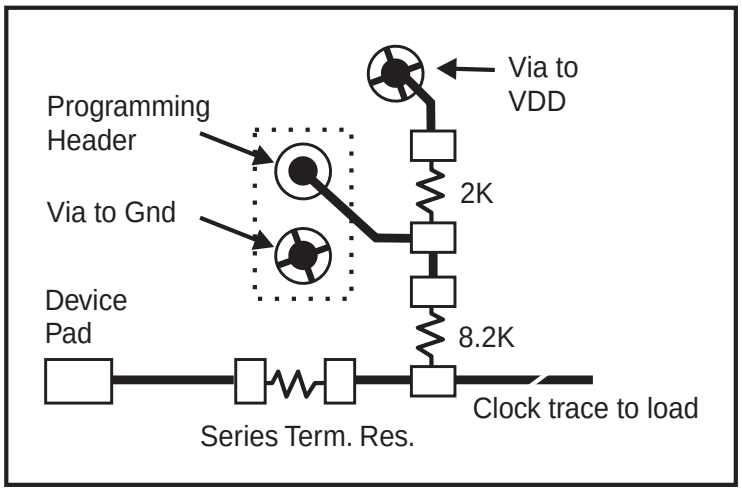
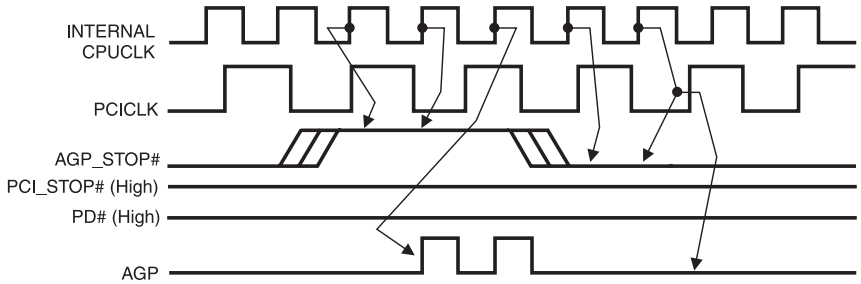


Fig. 1

AGP_STOP# Timing Diagram

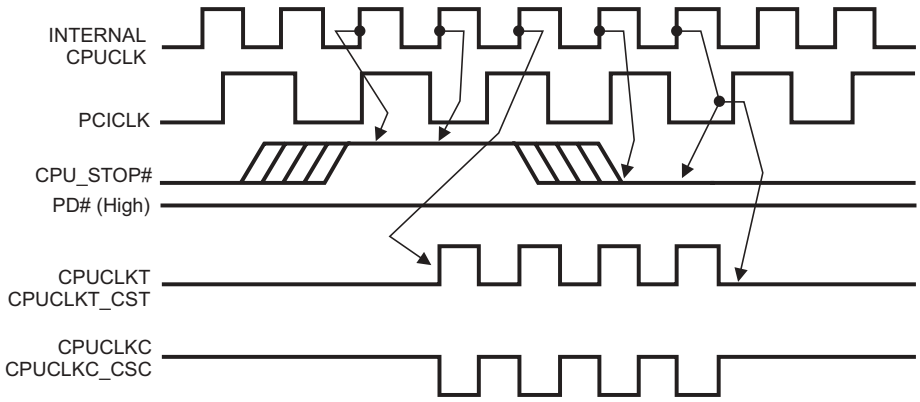
AGP_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the AGP clocks. for low power operation. AGP_STOP# is synchronized by the **ICS94228**. The AGPCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. AGPCLK on latency is less than AGPCLK and AGPCLK off latency is less than 3 AGPCLKs. This function is available only with MODE pin latched low.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. AGP_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS4228**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.
5. Only applies if MODE pin latched 0 at power up.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS94228**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

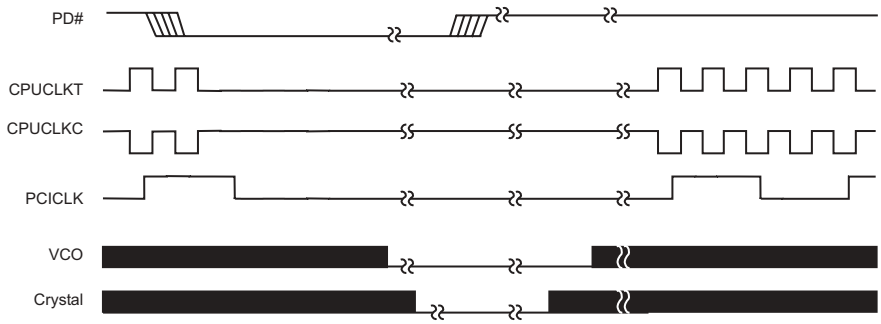


Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS94228**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

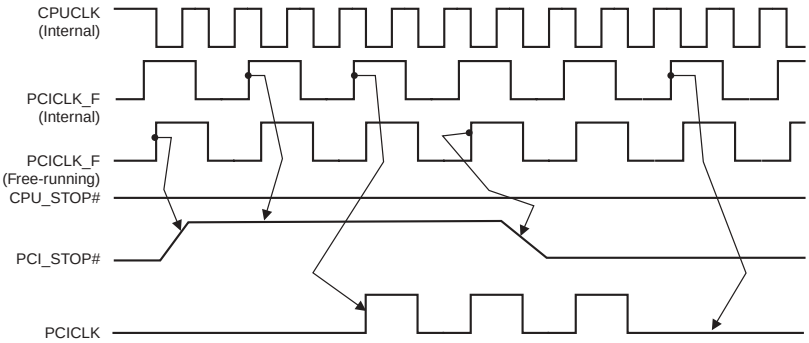
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94228 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

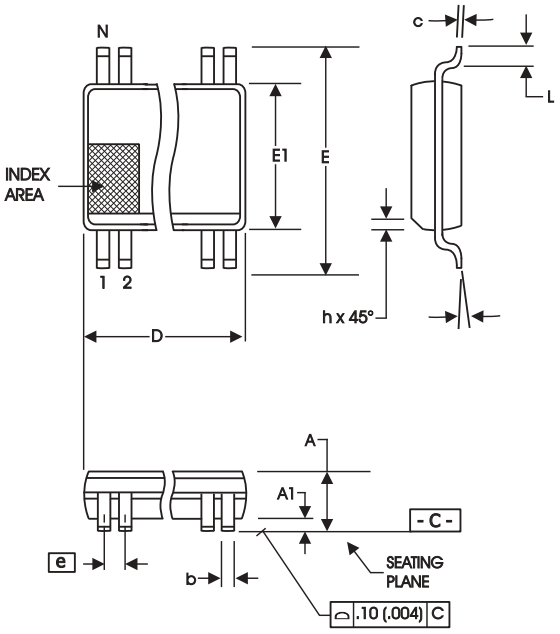
PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94228**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94228** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94228 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94228.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

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300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS94228yFLF-T

Example:

ICS XXXX y **F LF- T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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