NCP5378

Single Phase Synchronous Buck Controller with Integrated Gate Drivers and Programmable DAC

The NCP5378 is a single chip solution which combines differential voltage sensing, differential phase current sensing, adaptive voltage positioning, and on board gate drivers to provide accurately regulated power for Intel processors. This controller IC maintains the same features as the multi−phase product family, but reduces the output to a single−phase, for lower current systems. Low power mode operation combined with inductor current sensing reduces system cost by providing the fastest initial response to dynamic load events.

The gate drive adaptive non overlap and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook and desktop systems. A high performance operational error amplifier is provided to simplify compensation of the system. Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance.

Features

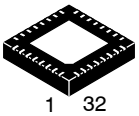
- Meets Intel's VR11.1 Specifications
- High Performance Operational Error Amplifier
- Internal Soft Start
- Dynamic Reference Injection (Patent #US07057381)
- DAC Range from 0.5 V to 1.6 V
- ±0.5% DAC Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- "Lossless" Differential Inductor Current Sensing
- Adaptive Voltage Positioning (AVP)
- Latched Over Voltage Protection (OVP)
- Guaranteed Startup into Pre−Charged Loads
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Thermally Compensated Current Monitoring
- Thermal Shutdown Protection
- Adaptive−Non−Overlap Gate Drive Circuit
- Integrated MOSFET Drivers
- Automatic Power−saving Modes Maximize Efficiency during Light Load Operation
- 32−lead QFN
- This is a Pb−Free Device

Applications

- Desktop Power Supplies for Next−generation Intel Chipsets

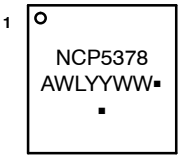
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QFN32
CASE 488AM

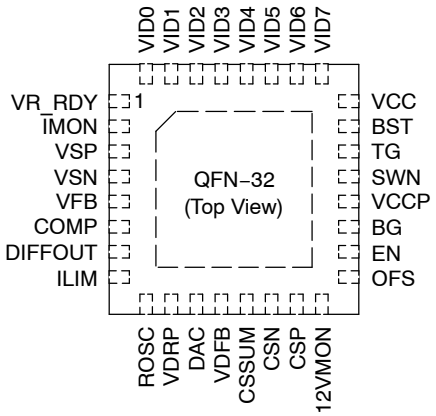
MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP5378MNR2G	QFN32 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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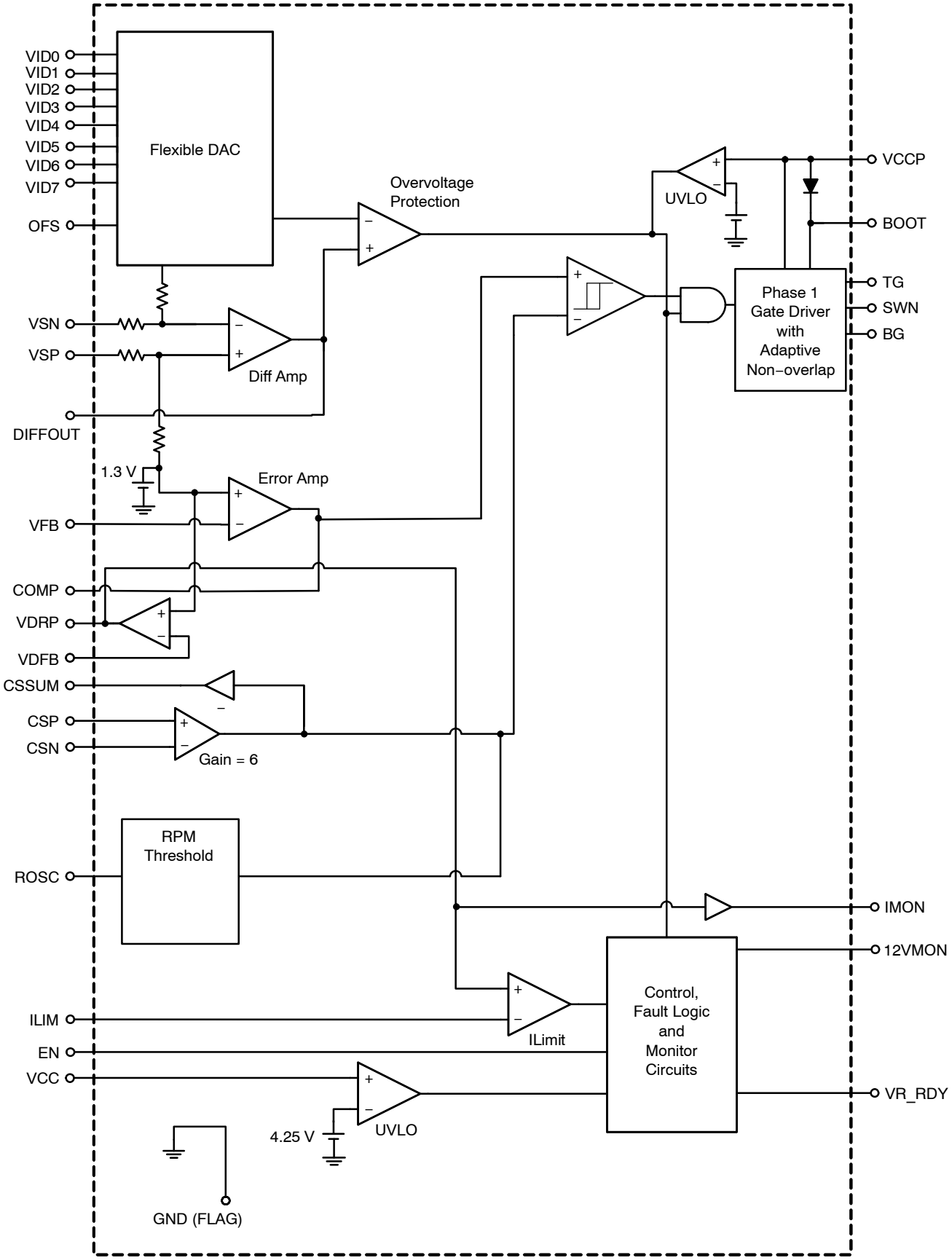


Figure 1. Functional Block Diagram

Table 1. PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	VR_RDY	Open collector output. High indicates that the output is regulating
2	IMON	0 to 1 Volt analog signal proportional to the output load current. VSN referenced Clamped to 1.1 Vmax
3	VSP	Non−inverting input to the internal differential remote sense amplifier
4	VSN	Inverting input to the internal differential remote sense amplifier
5	VFB	Compensation amplifier voltage feedback
6	COMP	Output of the compensation amplifier
7	DIFFOUT	Output of the differential remote sense amplifier
8	ILIM	Over current shutdown threshold setting. ILIM = VDRP − 1.3 V. Resistor divide ROSC to set threshold
9	ROSC	A resistance from this pin to ground programs the oscillator frequency according to f SW = 1 / (ROSC • 100 pF). This pin supplies a trimmed output voltage of 2.00 V.
10	VDRP	Voltage output signal proportional to current used for current limit and output voltage droop
11	DAC	DAC output used to provide feed forward for dynamic VID
12	VDFB	Droop Amplifier Voltage Feedback
13	CSSUM	Inverted Sum of the Differential Current Sense inputs.
14	CSN	Inverting input to current sense amplifier
15	CSP	Non−inverting input to current sense amplifier
16	12VMON	Monitor a 12 V input through a resistor divider
17	OFS	External Offset
18	EN	Threshold sensitive input. High = startup, Low = shutdown.
19	BG	Low side gate drive
20	VCCP	Power VCC for gate drivers with UVLO monitor
21	SWN	Switch Node
22	TG	High side gate drive
23	BST	Upper MOSFET floating BSTstrap supply for driver
24	VCC	Power for the internal control circuits with UVLO monitor
25	VID7	Voltage ID DAC input
26	VID6	Voltage ID DAC input
27	VID5	Voltage ID DAC input
28	VID4	Voltage ID DAC input
29	VID3	Voltage ID DAC input
30	VID2	Voltage ID DAC input
31	VID1	Voltage ID DAC input
32	VID0	Voltage ID DAC input
33/ FLAG	GND	Power supply return (QFN Flag)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
ELECTRICAL INFORMATION			
Controller Power Supply Voltages to GND	V_{CC}	−0.3, 7	V
Driver Power Supply Voltages to GND	V_{CCP}	−0.3, 15	V
High−Side Gate Driver Supplies: BST to SWN	$V_{BST} - V_{SWN}$	40 V wrt/GND 40 V ≤ 50 ns wrt/GND −0.3, 15 wrt/SWN	V
High−Side FET Gate Driver Voltages: TG to SWN	$V_{TG} - V_{SWN}$	BOOT + 0.3 V 35 V ≤ 50 ns wrt/GND −0.3, 15 wrt/SWN −5 V (200 ns)	V
Switch Node: SWN	V_{SWN}	35 40 V ≤ 50 ns wrt/GND −5 VDC −10 V (200 ns)	V
Low−Side Gate Drive: BG	V_{BG} − AGND	V_{CC} + 0.3 V −5 V (200 ns)	V
Logic Inputs	V_{LOGIC}	−0.3, 6	V
GND	V_{GND}	0	V
V−		GND ±300	mV
Imon Out	V_{IMON}	1.1	V
All Other Pins		−0.3, 5.5	V
THERMAL INFORMATION			
Thermal Characteristic QFN Package (Note 1)	$R_{\theta JA}$	32.6	°C/W
Operating Junction Temperature Range (Note 2)	T_J	0 to 125	°C
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*All signals referenced to GND unless noted otherwise.

*The maximum package power dissipation must be observed.

1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. Operation at −40°C to 0°C guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; C_{VCC} = 0.1 μF unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current		−200	–	200	nA
Open Loop DC Gain	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	100	–	dB
Open Loop Unity Gain Bandwidth	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	18	–	MHz
Open Loop Phase Margin	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	70	–	°
Slew Rate	ΔV_{in} = 100 mV, G = −10V/V, ΔV_{out} = 1.5 V − 2.5 V, C_L = 60 pF to GND, DC Load = ±125 μA to GND	–	10	–	V/μs
Maximum Output Voltage	10 mV of Overdrive, I_{SOURCE} = 2.0 mA	3.0	–	–	V
Minimum Output Voltage	10 mV of Overdrive, I_{SINK} = 500 μA	–	–	75	mV
Output Source Current	10 mV of Overdrive, V_{out} = 3.5 V	1.5	2.0	–	mA
Output Sink Current	10 mV of Overdrive, V_{out} = 0.1 V	0.65	1.0	–	mA
DIFFERENTIAL SUMMING AMPLIFIER					
V+ Input Pull down Resistance	DRVON = low DRVON = high	– –	0.6 6.0	– –	kΩ
V+ Input Bias Voltage	DRVON = low DRVON = high	– 0.8	0.05 0.88	0.1 0.95	V
Input Voltage Range (Note 3)		−0.3	–	3.0	V
−3 dB Bandwidth	C_L = 80 pF to GND, R_L = 10 kΩ to GND	–	15	–	MHz
Closed Loop DC gain VS to Diffout (Note 3)	VS+ to VS− = 0.5 V to 1.6 V	0.98	1.0	1.02	V/V
Maximum Output Voltage	10 mV of Overdrive, I_{SOURCE} = 2 mA	3.0	–	–	V
Minimum Output Voltage	10 mV of Overdrive, I_{SINK} = 1 mA	–	–	0.5	V
Output Source Current	10 mV of Overdrive, V_{out} = 3 V	1.5	2.0	–	mA
Output Sink Current	10 mV of Overdrive, V_{out} = 0.2 V	1.0	1.5	–	mA
INTERNAL OFFSET VOLTAGE					
Offset Voltage to the (+) Pin of the Error Amp & the VDRP Pin		−2	0	+2	mV
VDROOP AMPLIFIER					
Input Bias Current		−200	–	200	nA
Inverting Voltage Range		0	1.3	3.0	V
Open Loop DC Gain	C_L = 20 pF to GND including ESD R_L = 1 kΩ to GND	–	100	–	dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND including ESD R_L = 1 kΩ to GND	–	18	–	MHz

3. Guaranteed by design.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.

ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; C_{VCC} = 0.1 μF unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
VDROOP AMPLIFIER					
Open Loop Phase Margin	C_L = 20 pF to GND including ESD R_L = 1 kΩ to GND	–	70	–	°
Slew Rate	C_L = 20 pF to GND including ESD R_L = 1 kΩ to GND	–	10	–	V/μs
Maximum Output Voltage	10 mV of Overdrive, I_{SOURCE} = 4.0 mA	3.0	–	–	V
Minimum Output Voltage	10 mV of Overdrive, I_{SINK} = 1.0 mA	–	–	1.0	V
Output Source Current	10 mV of Overdrive, V_{out} = 3.0 V	4.0	–	–	mA
Output Sink Current	10 mV of Overdrive, V_{out} = 1.0 V	1.0	–	–	mA
CSSUM AMPLIFIER					
Current Sense Input to V_{DRP} −3 dB Bandwidth	C_L = 10 pF to GND, R_L = 10 kΩ to GND	–	12	–	MHz
Current Summing Amp Output Offset Voltage	CSP − CSN = 0, CSP = 1.1 V	−16	–	+5	mV
Maximum CSSUM Output Voltage	CSP − CSN = −0.2 V (all phases) I_{SOURCE} = 1 mA	3.0	–	–	V
Minimum CSSUM Output Voltage	CSP − CSN = 0.7 V (all phases) I_{SINK} = 1 mA	–	–	0.3	V
Output Source Current	V_{out} = 3.0 V	1.0	–	–	mA
Output Sink Current	V_{out} = 0.3 V	4.0	–	–	mA
CURRENT SENSE AMPLIFIERS					
Input Bias Current	CSP = CSN = 1.4 V	−50	–	50	nA
Common Mode Input Voltage Range		−0.3	–	2.0	V
Differential Mode Input Voltage Range		−120	–	120	mV
Current Sharing Offset CSP to CSN (Note 3)	all VIOS	−2	–	2	mV
Current Sense Input to CSSUM Gain	0 V < CSP − CSN < 0.1 V	−3.834	−3.7	−3.574	V/V
IMON					
V_{DRP} to IMON Gain	1.325 V > V_{DRP} > 1.75 V	1.965	–	2.02	V/V
Current Sense Input to V_{DRP} −3 dB Bandwidth	C_L = 30 pF to GND, R_L = 100 kΩ to GND	–	4.0	–	MHz
Output Referred Offset Voltage	V_{DRP} = 1.5 V, I_{SOURCE} = 0 mA	0	23	50	mV
Minimum Output Voltage	V_{DRP} = 1.3 V, I_{SINK} = 25 μA	–	–	0.1	V
Maximum Output Voltage	I_{out} = 300 μA	1.0	–	–	V
Output Sink Current	V_{out} = 0.3 V	175	–	–	μA
Maximum Clamp Voltage	IMON − VSN V_{DRP} = HIGH R_{LOAD} = Open	1.1	–	1.2	V
RPM THRESHOLD					
Ramp Slope (Note 3)	R_{OSC} = 69.8 kΩ, DAC = 1.1 V		0.175		V/μs
R_{OSC} Output		1.93	2.00	2.05	V
VR_RDY (Power Good) OUTPUT					
VR_RDY Output Saturation Voltage	I_{PGD} = 5 mA	–	–	0.4	V
VR_RDY Rise Time	External pull−up of 1 KΩ to 1.25 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%	–	100	250	ns

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ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; C_{VCC} = 0.1 μF unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_RDY (Power Good) OUTPUT					
VR_RDY Output Voltage at Power−up	VR_RDY pulled up to 5 V via 2 kΩ, $t_{R(VCC)} \le 3 \times t_{R(5V)}$ 100 μs ≤ $t_{R(VCC)}$ ≤ 20 ms	–	–	1.0	V
VR_RDY High − Output Leakage Current	VR_RDY = 5.5 V via 1 K	–	–	0.1	μA
VR_RDY Upper Threshold Voltage (INTEL)	VCore Increasing, DAC = 1.3 V	–	300	250	mV (below DAC)
VR_RDY Lower Threshold Voltage (INTEL)	VCore Decreasing, DAC = 1.3 V	390	350	300	mV (below DAC)
VR_RDY Rising Delay	VCore Increasing	–	250	–	ns
VR_RDY Falling Delay	VCore Decreasing	–	5.0	–	ns
DIGITAL SOFT−START					
Soft−Start Ramp Time	DAC = 0 to DAC = 1.1 V	1.0	–	1.3	ms
VR11 V_{boot} time	Not used in Legacy Startup	400	500	600	μs
VR11					
VID Threshold		450	600	770	mV
VR11 Input Bias Current		−100	–	100	nA
Delay Before Latching VID Change (VID Deskewing) (Note 3)	Measured from the Edge of the 1st VID Change	200	–	300	ns
ENABLE INPUT					
Enable High Input Leakage Current	Pull−up to 1.3 V	–	–	200	nA
VR11.1 Threshold		450	600	770	mV
Enable Delay Time	Measure time from Enable transitioning HI to when SS begins	–	3.5	–	ms
CURRENT LIMIT					
ILIM to VDRP Gain		0.97	1.00	1.03	V/V
ILIM Pin Input Bias Current		–	0.1	1.0	μA
ILIM Pin Working Voltage Range		0.1	–	2.0	V
ILIM Accuracy	Measured with respect to the ILIM setting	−25	–	25	mV
Delay		–	–	120	ns
OVERVOLTAGE PROTECTION					
VR11 Over Voltage Threshold		VID+ 180	VID+ 205	VID+ 230	mV
Delay		–	–	100	ns
UNDERVOLTAGE PROTECTION					
V_{CC} UVLO Start Threshold		4.0	4.25	4.5	V
V_{CC} UVLO Stop Threshold		3.8	4.05	4.3	V
V_{CC} UVLO Hysteresis		150	200	–	mV
12VMON UVLO					
12VMON (High Threshold)	V_{CC} Valid	–	0.77	0.8	V
12VMON (Low Threshold)	V_{CC} Valid	0.4	0.68	–	V

3. Guaranteed by design.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.

ELECTRICAL CHARACTERISTICS

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Parameter	Test Conditions	Min	Typ	Max	Unit
DAC OUTPUT					
Output Source Current	V_{out} = 1.6 V	0	–	5.0	mA
Output Sink Current	V_{out} = 0.3 V	5.0	–	16	mA
VID INPUTS					
Threshold		450	600	770	mV
VR11 Mode Leakage		−100	–	100	nA
Delay before Latching VID Change (VID Deskewing) (Note 3)	Measured from the edge of the 1st VID change	200	–	300	ns
DIGITAL DAC SLEW RATE LIMITER					
Slew Rate Limit		12.5	–	16	mV/μs
Soft−Start Slew Rate		–	0.84	–	mV/μs
INPUT SUPPLY CURRENT					
V_{CC} Quiescent Current	EN Low, No PWM	10	–	30	mA
V_{CCP} SUPPLY VOLTAGE					
V_{CCP} UVLO Start Threshold		8.2	9.0	9.5	V
V_{CCP} UVLO Stop Threshold		7.2	8.0	8.5	V
V_{CCP} UVLO Hysteresis		1.0	–	–	V
V_{CCP} POR	Voltage at which the Driver OVP becomes active	3.0	3.2	–	
BOOST PIN UVLO					
BOOST UVLO Start Threshold (Note 3)		3.15		4.15	V
BOOST UVLO Stop Threshold (Note 3)		3.0		3.85	V
BOOST UVLO Hysteresis (Note 3)		50	200	–	mV
STARTUP HIGH SIDE SHORT TRIP (Active only during 1st power on)					
V_{swx} Output Overvoltage Trip Threshold at Startup	Power Startup time, V_{CC} > 9 V	1.7	–	2.03	V
HIGH SIDE DRIVER					
R_{H_TG} Output Resistance, Sourcing	$V_{BST} - V_{SW}$ = 12 V	–	1.8	–	Ω
R_{H_TG} Output Resistance, Sinking	$V_{BST} - V_{SW}$ = 12 V	–	1.0	–	
Tr_{DRVH} Transition Time	C_{LOAD} = 3 nF, $V_{BST} - V_{SW}$ = 12 V	–	25	–	ns
Tf_{DRVH} Transition Time	C_{LOAD} = 3 nF, $V_{BST} - V_{SW}$ = 12 V	–	20	–	ns
$Tpdh_{DRVH}$ Propagation Delay (Note 4)	Driving High, C_{LOAD} = 3.3 nF, V_{CCP} = 12 V	–	15	–	ns
LOW SIDE DRIVER					
R_{H_BG} Output Resistance, Sourcing	SW = GND	–	1.6	–	Ω
R_{L_BG} Output Resistance, Sinking	SW = V_{CC}	–	1.0	–	Ω
Tr_{DRVL} Transition Time	C_{LOAD} = 3 nF	–	20	–	ns
Tf_{DRVL} Transition Time	C_{LOAD} = 3 nF	–	20	–	ns
$Tpdh_{DRVL}$ Propagation Delay (Note 4)	Driving High, C_{LOAD} = 3.3 nF, V_{CCP} = 12 V	–	20	–	ns
V_{NCDT} Negative Current Detector Threshold (Note 3)		–	−4.0	–	mV

3. Guaranteed by design.
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ELECTRICAL CHARACTERISTICS

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Parameter	Test Conditions	Min	Typ	Max	Unit
THERMAL SHUTDOWN					
Tsd Thermal Shutdown (Note 3)		150	170	–	°C
Tsdhys Thermal Shutdown Hysteresis (Note 3)		–	20	–	°C
VRM 11 DAC					
System Voltage Accuracy	1.0 V < DAC < 1.6 V 0.8 V < DAC < 1.0 V 0.5 V < DAC < 0.8 V	– – –	– – –	±0.5 ±5.0 ±8.0	% mV mV

3. Guaranteed by design.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.

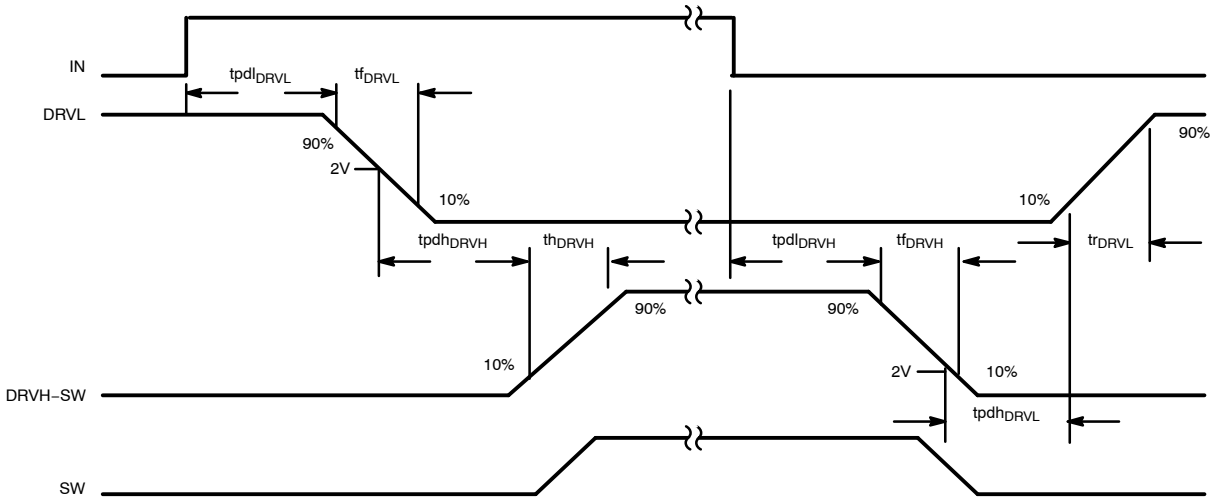


Figure 2. Timing Diagram

FUNCTIONAL DESCRIPTIONS

General

The NCP5378 is a ramp−pulse−modulated (RPM) controller designed with necessary features for CPU applications. The IC consists of the following blocks: Precision Flexible DAC, Differential Remote Voltage Sense Amplifier, High Performance Voltage Error Amplifier, Differential Current Feedback Amplifier, precision programmable DAC and PWM Comparator with Hysteresis. The controller also supports power saving operation at light load. Protection features include: Undervoltage Lockout, Soft Start, Over Current Protection, Over Voltage Protection, and Power Good Monitor.

VID Inputs

VID0−VID7 control the target regulation voltage during normal operation. In VR11 mode the VID capture is enabled at the end of the V_{BST} waiting period. If the VID is valid the DAC counter will track to it. If an invalid VID occurs it will be ignored for 10 μs before the controller shuts down.

Remote Sense Amplifier

A high performance differential amplifier is provided to accurately sense the output voltage of the regulator. The noninverting input should be connected to the regulator's output voltage. The inverting input should be connected to the return line of the regulator. Both connection points are intended to be at a remote point so that the most accurate reading of the output voltage can be obtained. The amplifier is configured in a very unique way. First, the gain of the amplifier is internally set to unity. Second, both the inverting and noninverting inputs of the amplifier are summing nodes. The inverting input sums the output voltage return voltage with the DAC voltage. The noninverting input sums the remote output voltage with a 1.3 V reference. The resulting voltage at the output of the remote sense amplifier is:

$$V_{Diffout} = V_{out} + 1.3\ V - V_{dac} - V_{outreturn}$$

This signal then goes through a standard compensation circuit and into the inverting input of the error amplifier. The noninverting input of the error amplifier is also connected to the 1.3 V reference. The 1.3 V reference then is subtracted out and the error signal at the comp pin of the error amplifier is as normally expected:

$$V_{comp} = V_{dac} - V_{out}$$

The noninverting input of the remote sense amplifier is pulled low through a small current sink during a fault condition to prevent accidental charging of the regulator output.

High Performance Voltage Error Amplifier

A high performance voltage error amplifier is provided. The error amplifier's inverting input and its output (the compensation pin) are both pinned out. A standard type 3 compensation circuit is used to compensate the system. This involves a 3 pole, 2 zero compensation network. The system output current during a transient can slew as fast as 500 A/μs. The high frequency output impedance of the system may be as low as 0.5 milli−ohm. The PWM will need to go from a low duty cycle to full duty cycle within 100 ns. In order to respond to this magnitude of change, the output of the error amplifier must slew at a rate of at least 5 V/μs. The error amplifier output voltage needs to be able to slew from steady state to below 1.0 V or above 2.5 V. The error amplifier also needs to be very fast. The output of the error amplifier needs to respond within 50 ns to any perturbation on the input.

The comp pin will be pulled to ground in a fault condition and should not jump up when the fault cleared.

Differential Current Feedback Amplifier

A differential amplifier are provided to sense the output current of each phase.

The current sense amplifier senses the current through its corresponding phase. A voltage is generated across a current sense element such as an inductor or sense resistor. The sense voltage will be very low. The sense element will normally be between 0.5 mΩ and 1.5 mΩ. It is possible to sense both negative and positive going current. It is further possible that the differential sense signal is below 0 V. The output of these amplifiers shall not invert if the common mode range is exceeded.

The gain of this amplifier is fixed and is noninverting. The output of the amplifier is used to control 3 functions. First, the output controls the adaptive voltage positioning, where the output voltage is actively controlled according to the output current. Second, the output signal is fed to the current limit circuit. Finally, the phase current is connected to the PWM comparator. The offset voltage difference from amplifier to amplifier and the error in bias current from amplifier to amplifier need to be minimized. The offset and bias current design needs to be able to eliminate differences from amplifier to amplifier.

Switching Frequency in RPM Mode

When the NCP5378 operates in RPM mode, its switching frequency is controlled by the ripple voltage on the COMP pin. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and ground, an internal ramp signal is started and TG is driven high. The slew rate of the internal ramp is programmed by the current entering the ROSC pin. When the internal ramp signal intercepts the COMP voltage, the TG pin is reset low. In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table.

The VR11 mode ramps DAC to 1.1 V, pauses for 500 μs, reads the DAC setting, then ramps to the final DAC setting.

Digital Slew Rate Limiter / Soft Start Block

The slew rate limiter and the soft−start block are to be implemented with a digital up/down counter controlled by an oscillator that can be synchronized to VID line changes. During soft start the DAC will ramp at the softstart rate, after soft start is complete the ramp rate will follow the Intel rate depending on the mode. In normal operation the design must keep up with the Intel spec of 1 DAC step every 1.25 μs.

The DAC must be implemented down as close to zero as possible (less than 20 mV out the DAC Buffer) in order to avoid the output voltage jumping up at the beginning of the ramp.

Preferably when DAC = 0 the buffer to the RS amp should deliver less than 20 mV. The digital DAC offset should be introduced prior to the digital compare.

Protection Features

Undervoltage Lockouts

An undervoltage circuit senses the input V_{CC} and V_{CCP} of the controller and driver voltage rail. During power up the input voltage to the controller is monitored. The PWM outputs and the soft start circuit are disabled until the input voltage exceeds the threshold voltage of the comparator. Hysteresis is incorporated within the comparator.

The PWM signals will control the gate status when V_{CC} threshold is exceeded. If V_{CC} decreases below the stop threshold, the output gate will be forced low unit input voltage V_{CC} rises above the startup threshold.

Overcurrent Latch

A programmable overcurrent latch is incorporated within the IC. The oscillator pin provides the reference voltage for this pin. A resistor divider from this pin generates the reference voltage. The latch is set when the current information exceeds the programmed voltage. To recover the part must be reset by the EN pin or by cycling V_{CC}.

The outputs will remain disabled until the V_{CC} voltage or EN is removed and reapplied.

UVLO Monitor

If the output voltage falls greater than 300 mV below the DAC voltage the UVLO comparator will trip sending the VR_RDY signal low.

Overvoltage Protection

The output voltage is monitored at the input of the differential amplifier. During normal operation, if the output voltage exceeds the DAC voltage by 180 mV (OR 350 mV if OFS is active), the VR_RDY flag goes low, the high side gate drivers are all brought low, and the low side gate drivers are all brought high until the voltage falls below the OVP threshold. If the over voltage trip 8 times the output voltage will shut down. The OVP will not shut down the controller if it occurs during soft−start. This is to allow the controller to pull the output down to the DAC voltage and start up into a pre−charged output.

V_{CCP} Power ON Reset OVP

The V_{CCP} power on reset OVP feature is used to protect the CPU during startup. When V_{CCP} is higher than 3.2 V, the gate driver will monitor the switching node SW pin. If SWN pin higher than 1.9 V, the bottom gate will be forced to high for discharge of the output capacitor. This works best if the 5 V standby is diode OR'ed into V_{CCP} with the 12 V rail. The

fault mode will be latched unless V_{CCP} is reduced below the UVLO threshold.

Power Saving Mode

The device maintains a RPM operation in power saving mode. The 12VMON input will be used for two purposes: feedforward input supply information for RPM mode and secondary power input voltage UVLO.

Adaptive Non−overlap

The non−overlap dead time control is used to avoid shoot through damage to the power MOSFETs. When the PWM signal pull high, BG will go low after a propagation delay, the controller monitors the switching node (SWN) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high−side MOSFET. When the PWM pull low, gate TG will go low after the propagation delay (tpdlDRVH). The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

Externally Programmable Offset

The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor, R_{FB} between FB and V_{DIFF}. The offset current is generated via an external resistor and precision internal voltage references. For positive offset connect a resistor to GND. For negative offset connect a resistor to V_{CC}. The nominal no-load offset on NCP5378 is −19 mV.

To set the no−load offset please use the equations below:

For Negative Offset connect R_{OFS} to V_{CC}

$$R_{OFS} = \frac{\left(V_{CC} - 2.0\right) \cdot R_{FB}}{V_{OFFSET}}$$

For Positive Offset connect R_{OFS} to GND

$$R_{OFS} = \frac{0.3 \times R_{FB}}{V_{OFFSET}}$$

For example to get 0 mV no-load offset; (since the part has a nominal of -19mV)

$$R_{OFS} = \frac{0.3 \times R_{FB}}{19\ mV}$$

Layout Guidlines

Layout is very important thing for design a DC−DC converter. The strap capacitor and Vin capacitor are most critical items, it should be placed as close as to the controller IC. Another item is using a GND plane. Ground plane can provide a good return path for gate drives for reducing the ground noise. Therefore GND pin should be directly connected to the ground plane and close to the low−side MOSFET source pin. Also, the gate drive trace should be considered. The gate drives has a high di/dt when switching, therefore a minimized gate drives trace can reduce the di/dv, raise and fall time for reduce the switching loss.

Table 2. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	0	0	0	0	0	0		00
0	0	0	0	0	0	0	1		01
0	0	0	0	0	0	1	0	1.60000	02
0	0	0	0	0	0	1	1	1.59375	03
0	0	0	0	0	1	0	0	1.58750	04
0	0	0	0	0	1	0	1	1.58125	05
0	0	0	0	0	1	1	0	1.57500	06
0	0	0	0	0	1	1	1	1.56875	07
0	0	0	0	1	0	0	0	1.56250	08
0	0	0	0	1	0	0	1	1.55625	09
0	0	0	0	1	0	1	0	1.55000	0A
0	0	0	0	1	0	1	1	1.54375	0B
0	0	0	0	1	1	0	0	1.53750	0C
0	0	0	0	1	1	0	1	1.53125	0D
0	0	0	0	1	1	1	0	1.52500	0E
0	0	0	0	1	1	1	1	1.51875	0F
0	0	0	1	0	0	0	0	1.51250	10
0	0	0	1	0	0	0	1	1.50625	11
0	0	0	1	0	0	1	0	1.50000	12
0	0	0	1	0	0	1	1	1.49375	13
0	0	0	1	0	1	0	0	1.48750	14
0	0	0	1	0	1	0	1	1.48125	15
0	0	0	1	0	1	1	0	1.47500	16
0	0	0	1	0	1	1	1	1.46875	17
0	0	0	1	1	0	0	0	1.46250	18
0	0	0	1	1	0	0	1	1.45625	19
0	0	0	1	1	0	1	0	1.45000	1A
0	0	0	1	1	0	1	1	1.44375	1B
0	0	0	1	1	1	0	0	1.43750	1C
0	0	0	1	1	1	0	1	1.43125	1D
0	0	0	1	1	1	1	0	1.42500	1E
0	0	0	1	1	1	1	1	1.41875	1F
0	0	1	0	0	0	0	0	1.41250	20
0	0	1	0	0	0	0	1	1.40625	21
0	0	1	0	0	0	1	0	1.40000	22
0	0	1	0	0	0	1	1	1.39375	23
0	0	1	0	0	1	0	0	1.38750	24
0	0	1	0	0	1	0	1	1.38125	25
0	0	1	0	0	1	1	0	1.37500	26
0	0	1	0	0	1	1	1	1.36875	27
0	0	1	0	1	0	0	0	1.36250	28
0	0	1	0	1	0	0	1	1.35625	29
0	0	1	0	1	0	1	0	1.35000	2A

Table 2. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	1	0	1	0	1	1	1.34375	2B
0	0	1	0	1	1	0	0	1.33750	2C
0	0	1	0	1	1	0	1	1.33125	2D
0	0	1	0	1	1	1	0	1.32500	2E
0	0	1	0	1	1	1	1	1.31875	2F
0	0	1	1	0	0	0	0	1.31250	30
0	0	1	1	0	0	0	1	1.30625	31
0	0	1	1	0	0	1	0	1.30000	32
0	0	1	1	0	0	1	1	1.29375	33
0	0	1	1	0	1	0	0	1.28750	34
0	0	1	1	0	1	0	1	1.28125	35
0	0	1	1	0	1	1	0	1.27500	36
0	0	1	1	0	1	1	1	1.26875	37
0	0	1	1	1	0	0	0	1.26250	38
0	0	1	1	1	0	0	1	1.25625	39
0	0	1	1	1	0	1	0	1.25000	3A
0	0	1	1	1	0	1	1	1.24375	3B
0	0	1	1	1	1	0	0	1.23750	3C
0	0	1	1	1	1	0	1	1.23125	3D
0	0	1	1	1	1	1	0	1.22500	3E
0	0	1	1	1	1	1	1	1.21875	3F
0	1	0	0	0	0	0	0	1.21250	40
0	1	0	0	0	0	0	1	1.20625	41
0	1	0	0	0	0	1	0	1.20000	42
0	1	0	0	0	0	1	1	1.19375	43
0	1	0	0	0	1	0	0	1.18750	44
0	1	0	0	0	1	0	1	1.18125	45
0	1	0	0	0	1	1	0	1.17500	46
0	1	0	0	0	1	1	1	1.16875	47
0	1	0	0	1	0	0	0	1.16250	48
0	1	0	0	1	0	0	1	1.15625	49
0	1	0	0	1	0	1	0	1.15000	4A
0	1	0	0	1	0	1	1	1.14375	4B
0	1	0	0	1	1	0	0	1.13750	4C
0	1	0	0	1	1	0	1	1.13125	4D
0	1	0	0	1	1	1	0	1.12500	4E
0	1	0	0	1	1	1	1	1.11875	4F
0	1	0	1	0	0	0	0	1.11250	50
0	1	0	1	0	0	0	1	1.10625	51
0	1	0	1	0	0	1	0	1.10000	52
0	1	0	1	0	0	1	1	1.09375	53
0	1	0	1	0	1	0	0	1.08750	54
0	1	0	1	0	1	0	1	1.08125	55

Table 2. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	1	0	1	0	1	1	0	1.07500	56
0	1	0	1	0	1	1	1	1.06875	57
0	1	0	1	1	0	0	0	1.06250	58
0	1	0	1	1	0	0	1	1.05625	59
0	1	0	1	1	0	1	0	1.05000	5A
0	1	0	1	1	0	1	1	1.04375	5B
0	1	0	1	1	1	0	0	1.03750	5C
0	1	0	1	1	1	0	1	1.03125	5D
0	1	0	1	1	1	1	0	1.02500	5E
0	1	0	1	1	1	1	1	1.01875	5F
0	1	1	0	0	0	0	0	1.01250	60
0	1	1	0	0	0	0	1	1.00625	61
0	1	1	0	0	0	1	0	1.00000	62
0	1	1	0	0	0	1	1	0.99375	63
0	1	1	0	0	1	0	0	0.98750	64
0	1	1	0	0	1	0	1	0.98125	65
0	1	1	0	0	1	1	0	0.97500	66
0	1	1	0	0	1	1	1	0.96875	67
0	1	1	0	1	0	0	0	0.96250	68
0	1	1	0	1	0	0	1	0.95625	69
0	1	1	0	1	0	1	0	0.95000	6A
0	1	1	0	1	0	1	1	0.94375	6B
0	1	1	0	1	1	0	0	0.93750	6C
0	1	1	0	1	1	0	1	0.93125	6D
0	1	1	0	1	1	1	0	0.92500	6E
0	1	1	0	1	1	1	1	0.91875	6F
0	1	1	1	0	0	0	0	0.91250	70
0	1	1	1	0	0	0	1	0.90625	71
0	1	1	1	0	0	1	0	0.90000	72
0	1	1	1	0	0	1	1	0.89375	73
0	1	1	1	0	1	0	0	0.88750	74
0	1	1	1	0	1	0	1	0.88125	75
0	1	1	1	0	1	1	0	0.87500	76
0	1	1	1	0	1	1	1	0.86875	77
0	1	1	1	1	0	0	0	0.86250	78
0	1	1	1	1	0	0	1	0.85625	79
0	1	1	1	1	0	1	0	0.85000	7A
0	1	1	1	1	0	1	1	0.84375	7B
0	1	1	1	1	1	0	0	0.83750	7C
0	1	1	1	1	1	0	1	0.83125	7D
0	1	1	1	1	1	1	0	0.82500	7E
0	1	1	1	1	1	1	1	0.81875	7F
1	0	0	0	0	0	0	0	0.81250	80

Table 2. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	0	0	0	0	0	1	0.80625	81
1	0	0	0	0	0	1	0	0.80000	82
1	0	0	0	0	0	1	1	0.79375	83
1	0	0	0	0	1	0	0	0.78750	84
1	0	0	0	0	1	0	1	0.78125	85
1	0	0	0	0	1	1	0	0.77500	86
1	0	0	0	0	1	1	1	0.76875	87
1	0	0	0	1	0	0	0	0.76250	88
1	0	0	0	1	0	0	1	0.75625	89
1	0	0	0	1	0	1	0	0.75000	8A
1	0	0	0	1	0	1	1	0.74375	8B
1	0	0	0	1	1	0	0	0.73750	8C
1	0	0	0	1	1	0	1	0.73125	8D
1	0	0	0	1	1	1	0	0.72500	8E
1	0	0	0	1	1	1	1	0.71875	8F
1	0	0	1	0	0	0	0	0.71250	90
1	0	0	1	0	0	0	1	0.70625	91
1	0	0	1	0	0	1	0	0.70000	92
1	0	0	1	0	0	1	1	0.69375	93
1	0	0	1	0	1	0	0	0.68750	94
1	0	0	1	0	1	0	1	0.68125	95
1	0	0	1	0	1	1	0	0.67500	96
1	0	0	1	0	1	1	1	0.66875	97
1	0	0	1	1	0	0	0	0.66250	98
1	0	0	1	1	0	0	1	0.65625	99
1	0	0	1	1	0	1	0	0.65000	9A
1	0	0	1	1	0	1	1	0.64375	9B
1	0	0	1	1	1	0	0	0.63750	9C
1	0	0	1	1	1	0	1	0.63125	9D
1	0	0	1	1	1	1	0	0.62500	9E
1	0	0	1	1	1	1	1	0.61875	9F
1	0	1	0	0	0	0	0	0.61250	A0
1	0	1	0	0	0	0	1	0.60625	A1
1	0	1	0	0	0	1	0	0.60000	A2
1	0	1	0	0	0	1	1	0.59375	A3
1	0	1	0	0	1	0	0	0.58750	A4
1	0	1	0	0	1	0	1	0.58125	A5
1	0	1	0	0	1	1	0	0.57500	A6
1	0	1	0	0	1	1	1	0.56875	A7
1	0	1	0	1	0	0	0	0.56250	A8
1	0	1	0	1	0	0	1	0.55625	A9
1	0	1	0	1	0	1	0	0.55000	AA
1	0	1	0	1	0	1	1	0.54375	AB

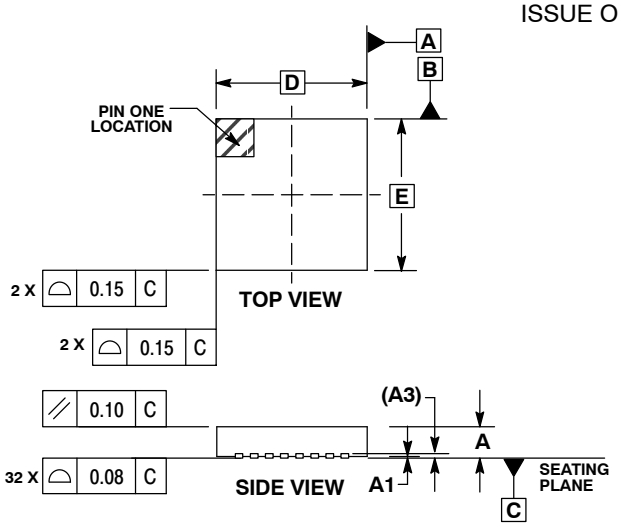
Table 2. VRM11 VID Codes

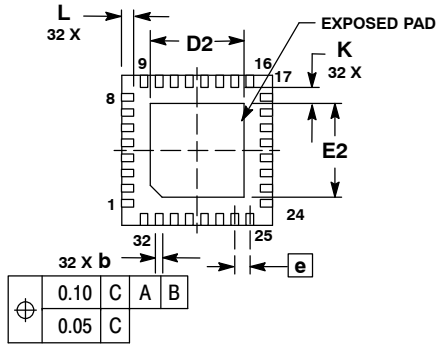
VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	1	0	1	1	0	0	0.53750	AC
1	0	1	0	1	1	0	1	0.53125	AD
1	0	1	0	1	1	1	0	0.52500	AE
1	0	1	0	1	1	1	1	0.51875	AF
1	0	1	1	0	0	0	0	0.51250	B0
1	0	1	1	0	0	0	1	0.50625	B1
1	0	1	1	0	0	1	0	0.50000	B2
1	1	1	1	1	1	1	0	OFF	FE
1	1	1	1	1	1	1	1	OFF	FF

5. NOTE: Internal DAC voltage is centered 19 mV below the listed voltage for VR11.1.

PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM−01
ISSUE O



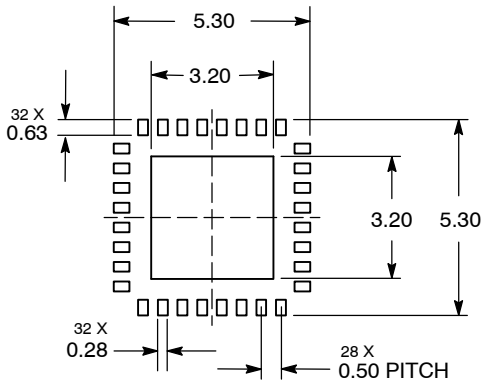


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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