MAX17552

60V, 100mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter with 22µA No-Load Supply Current

General Description

The MAX17552 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4V to 60V input voltage range. The converter can deliver output current up to 100mA at output voltages of 0.8V to 0.9 x V_{IN}. The output voltage is accurate to within ±1.75% over the -40°C to +125°C temperature range.

The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. The converter consumes only 22µA of no-load supply current in PFM mode. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify PCB layout.

The device offers programmable switching frequency to optimize solution size and efficiency. Programmable soft-start allows the user to reduce the inrush currents. An EN/UVLO pin allows the user to turn on/off the device at the desired input-voltage level. An open-drain $\overline{\text{RESET}}$ pin allows output-voltage monitoring. The device operates over the -40°C to +125°C industrial temperature range and is available in a compact 10-pin (3mm x 2mm) TDFN and 10-pin (3mm x 3mm) µMAX® packages. Simulation models are available.

Applications

- Industrial Sensors and Process Control
- 4mA–20mA Current-Loop Powered Sensors
- High-Voltage LDO Replacement
- Battery-Powered Equipment
- HVAC and Building Control
- General-Purpose Point-of-Load

Benefits and Features

- Eliminates External Components and Reduces Total Cost
  - No Schottky—Synchronous Operation for High Efficiency and Reduced Cost
  - Internal Compensation
  - Fixed Internal 5.1ms or Programmable Soft-Start
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4V to 60V Input Voltage Range
  - Adjustable 0.8V to 0.9 x V_{IN} Output Voltages
  - Delivers Up to 100mA Load Current
  - 100kHz to 2.2MHz Adjustable Switching Frequency Range with External Synchronization
  - Configurable Between PFM and Forced-PWM Modes
- Reduces Power Dissipation
  - 22µA No Load Supply Current
  - Peak Efficiency > 90%
  - PFM Feature for High Light-Load Efficiency
  - 1.2µA (typ) Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Peak Current-Limit Protection
  - Built-In Output-Voltage Monitoring with Open-Drain $\overline{\text{RESET}}$ Pin
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output
  - Overtemperature Protection
  - -40°C to +125°C Industrial/Automotive Temperature Range

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX17552.related.

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19-6903; Rev 1; 6/14

Absolute Maximum Ratings

IN, EN/UVLO, V_{OUT}, $\overline{RESET}$ to GND ..... -0.3V to 70V
LX to GND ..... -0.3V to IN + 0.3V
RT/SYNC, SS, FB, MODE to GND ..... -0.3V to 6V
LX Total RMS Current ..... ±1.6A
Output Short-Circuit Duration ..... Continuous

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Continuous Power Dissipation (T_A = +70°C)
(derate 14.9mW/°C above +70°C) 1188.7mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 67.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 18.2°C/W

µMAX
Continuous Power Dissipation (T_A = +70°C)
(derate 8.8mW/°C above +70°C) 707.3mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 113.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, V_{GND} = 0V, V_{VOUT} = 3.3V, V_{FB} = 0.85V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, LX = SS = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input Voltage Range	V_{IN}		4		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	0.67	1.2	2.25	µA
Input Supply Current	I_{Q-PFM}	V_{MODE} = unconnected (Note 2)		18	32	µA
	I_{Q-PWM}	Normal switching mode, V_{IN} = 24V	245	525	760	µA
EXTERNAL BIAS (V_{OUT})						
V_{OUT} Switchover Threshold			2.96	3.05	3.12	V
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.2	1.25	1.3	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.1	1.15	1.2	V
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown		0.7		V
EN/UVLO Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 1.3V, T_A = +25°C	-100		+100	nA
POWER MOSFETs						
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.1A (sourcing)	1.5	2.7	5.1	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.1A (sinking)	0.8	1.4	2.6	Ω
LX Leakage Current	I_{LX-LKG}	V_{EN} = 0V, T_A = +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V)	-1		+1	µA

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, V_{VOUT} = 3.3V, V_{FB} = 0.85V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, LX = SS = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START (SS)						
Soft-Start Time	t_{SS}	SS = unconnected	4.4	5.1	5.8	ms
SS Charging Current	I_{SS}		4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	MODE = GND	0.786	0.8	0.814	V
		MODE = unconnected	0.786	0.812	0.826	
FB Input Leakage Current	I_{FB}	V_{FB} = 1V, T_A = 25°C	-100		+100	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		185	210	235	mA
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	V_{MODE} = GND	79	105	130	mA
		V_{MODE} = unconnected		0.01		
PFM Current Level	I_{PFM}	V_{MODE} = unconnected	50	72	90	mA
OSCILLATOR (RT/SYNC)						
Switching Frequency	f_{SW}	R_{RT} = 422kΩ	90	100	111	kHz
		R_{RT} = 191kΩ	205	220	235	
		R_{RT} = 130kΩ	295	319	340	
		R_{RT} = 69.8kΩ	540	592	638	
		R_{RT} = 45.3kΩ	813	900	973	
		R_{RT} = 19.1kΩ	1.86	2.08	2.3	MHz
Switching Frequency Adjustable Range		See the Switching Frequency (RT/SYNC) section for details	100		2200	kHz
SYNC Input Frequency			1.1 x f_{SW}		2200	kHz
SYNC Pulse Minimum Off-Time			40			ns
SYNC Rising Threshold	V_{SYNC-H}		1	1.22	1.44	V
Hysteresis	$V_{SYNC-HYS}$		0.115	0.18	0.265	
No of SYNC Pulses to Enable Synchronization				1		Cycles
TIMING						
Minimum On-Time	t_{ON-MIN}		46	82	128	ns
Maximum Duty Cycle	D_{MAX}	f_{SW} ≤ 600kHz, V_{FB} = 0.98 x V_{FB-REG}	90	94	98	%
		f_{SW} > 600kHz, V_{FB} = 0.98 x V_{FB-REG}	87	92		

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, V_{VOUT} = 3.3V, V_{FB} = 0.85V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, LX = SS = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted) (Note 2)

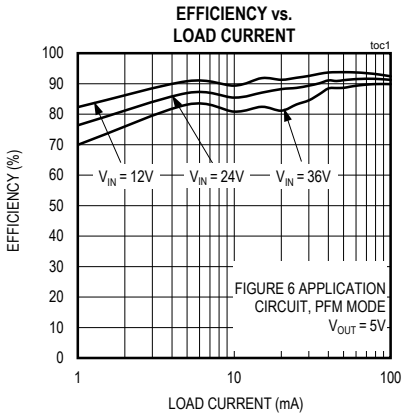
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$						
FB Threshold for $\overline{RESET}$ Rising	V_{FB-OKR}	V_{FB} rising	93	95	97	%
FB Threshold for $\overline{RESET}$ Falling	V_{FB-OKF}	V_{FB} falling	90	92	94	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				2.1		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 1mA		0.23		V
$\overline{RESET}$ Output Leakage Current		V_{FB} = 1.01 x V_{FB-REG}, T_A = +25°C			1	µA
MODE						
MODE PFM Threshold	$V_{MODE-PFM}$		1	1.22	1.44	V
MODE Hysteresis	$V_{MODE-HYS}$			0.19		V
MODE Internal Pullup Resistor		V_{MODE} = unconnected		235		kΩ
		V_{MODE} = GND		1390		
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		160		°C
Thermal-Shutdown Hysteresis				20		°C

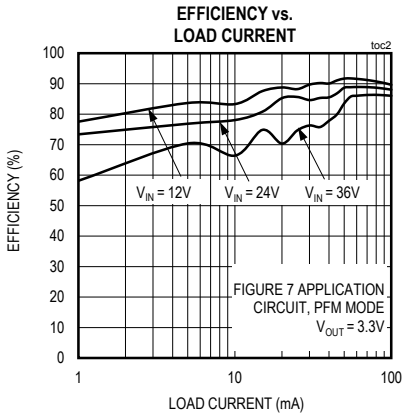
Note 2: Actual I_{Q-PFM} in the application circuit is higher due to additional current in the output voltage feedback resistor divider. For example, I_{Q-PFM} (MODE = unconnected) = 26µA for Figure 6, 22µA for Figure 7, and 78µA for Figure 11.

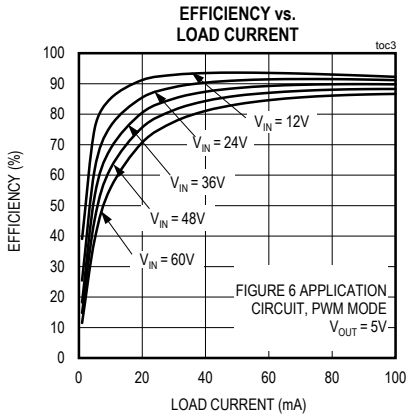
Note 3: All limits are 100% tested at +25°C. Limits over temperature are guaranteed by design.

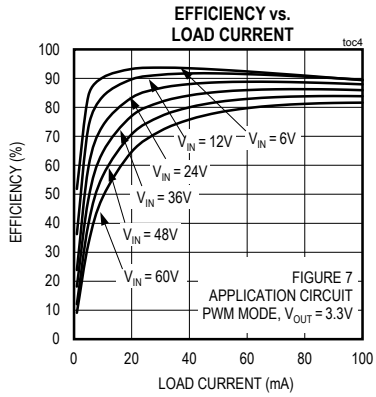
Typical Operating Characteristics

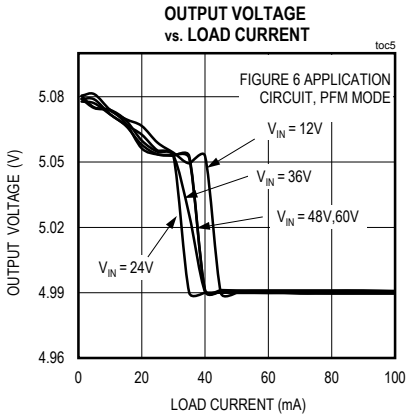
(V_{IN} = 24V, V_{GND} = 0V, V_{OUT} = 3.3V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, C_{IN} = 1µF, T_A = +25°C unless otherwise noted)

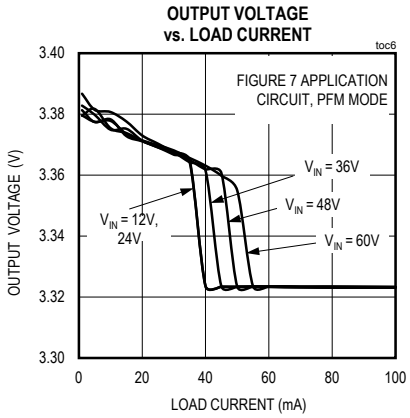


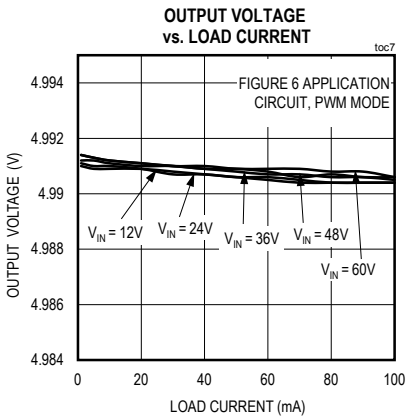


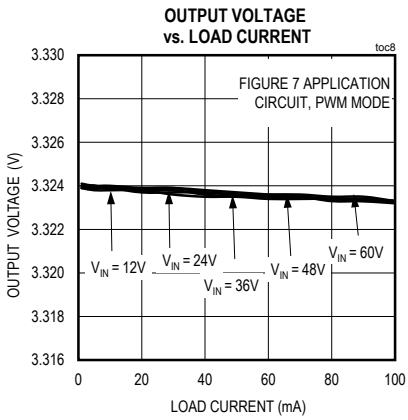


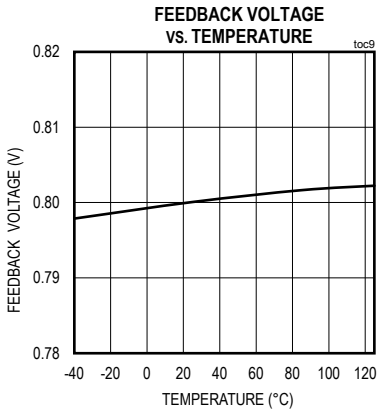






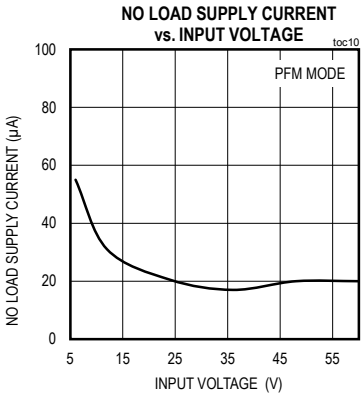


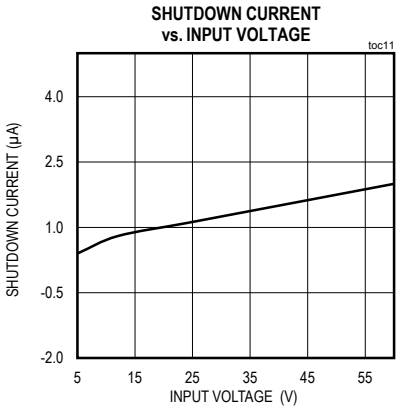


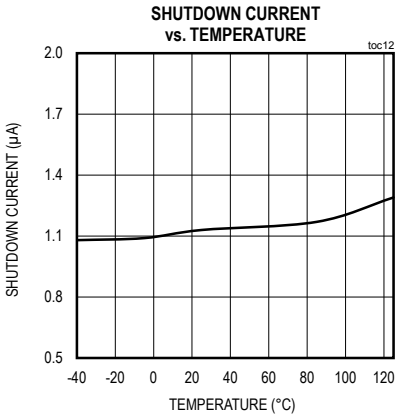


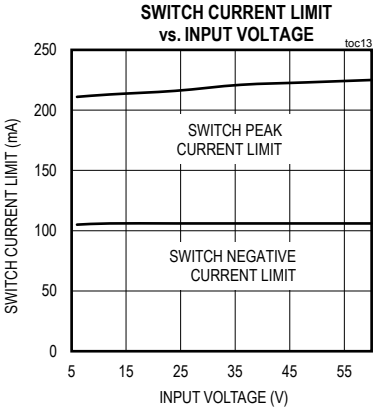
Typical Operating Characteristics (continued)

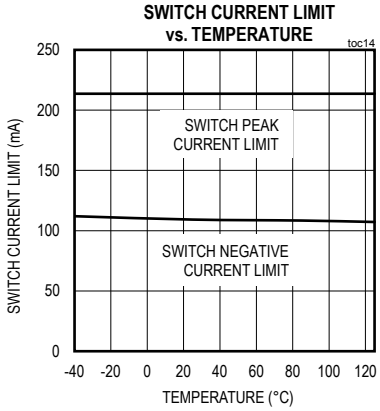
(V_{IN} = 24V, V_{GND} = 0V, V_{OUT} = 3.3V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, C_{IN} = 1µF, T_A = +25°C unless otherwise noted)

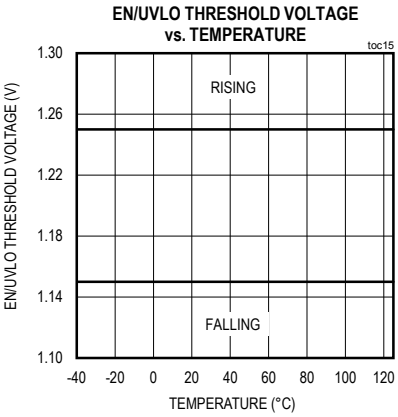


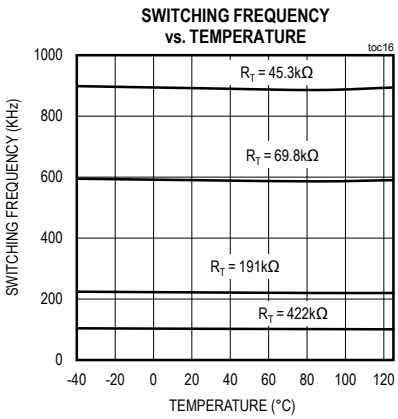


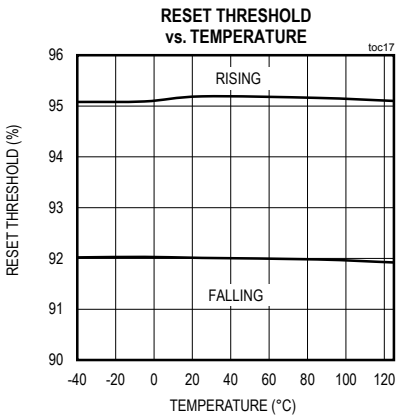


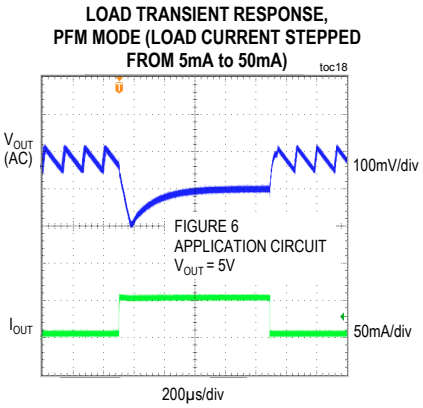








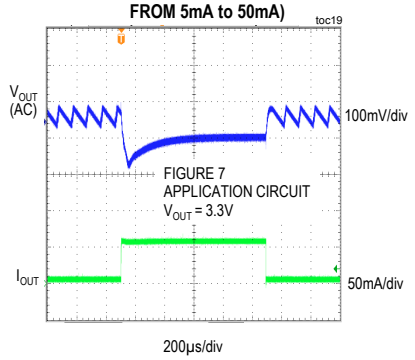




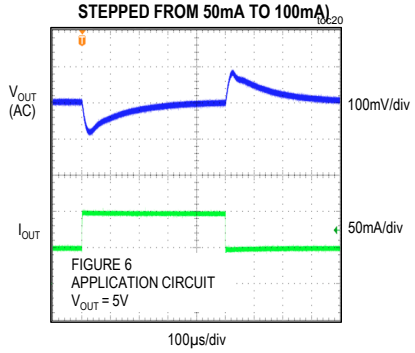
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, V_{OUT} = 3.3V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, C_{IN} = 1µF, T_A = +25°C unless otherwise noted)

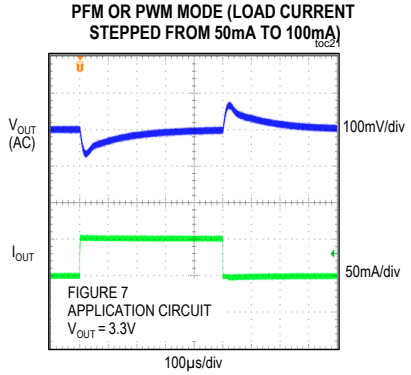
LOAD TRANSIENT RESPONSE PFM MODE (LOAD CURRENT STEPPED FROM 5mA to 50mA)



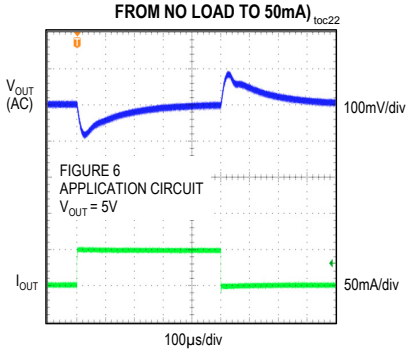
LOAD TRANSIENT RESPONSE PFM OR PWM MODE (LOAD CURRENT STEPPED FROM 50mA TO 100mA)



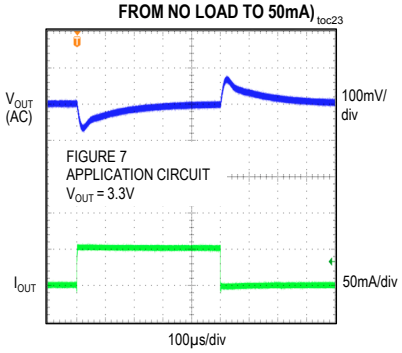
LOAD TRANSIENT RESPONSE PFM OR PWM MODE (LOAD CURRENT STEPPED FROM 50mA TO 100mA)



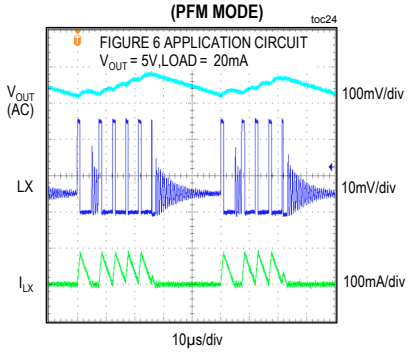
LOAD TRANSIENT RESPONSE PWM MODE (LOAD CURRENT STEPPED FROM NO LOAD TO 50mA)



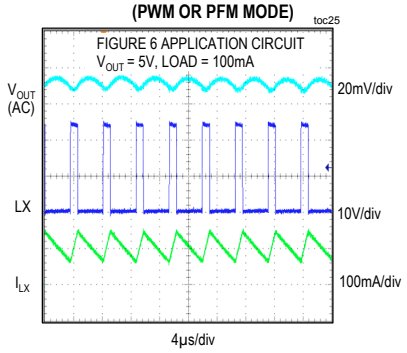
LOAD TRANSIENT RESPONSE PWM MODE (LOAD CURRENT STEPPED FROM NO LOAD TO 50mA)



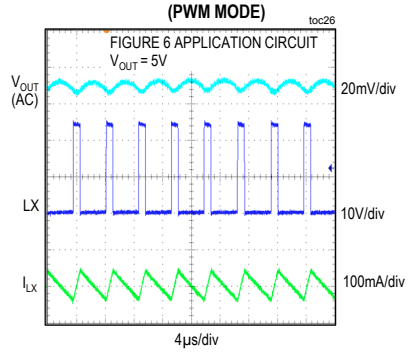
SWITCHING WAVEFORMS (PFM MODE)



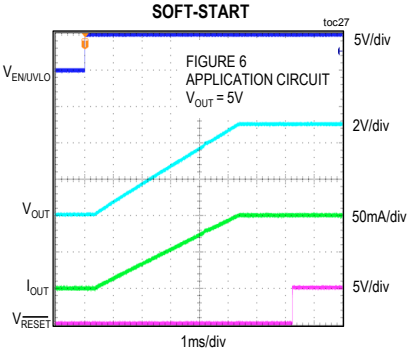
FULL LOAD SWITCHING WAVEFORMS (PWM OR PFM MODE)



NO LOAD SWITCHING WAVEFORMS (PWM MODE)

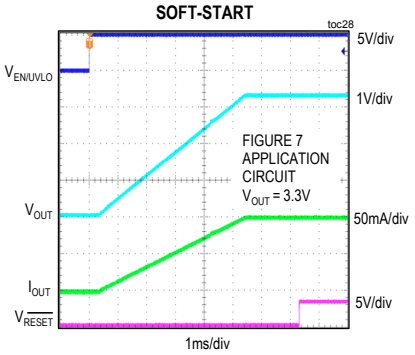


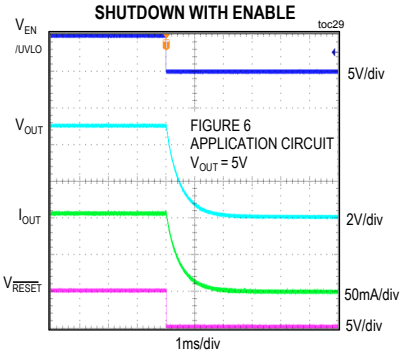
SOFT-START

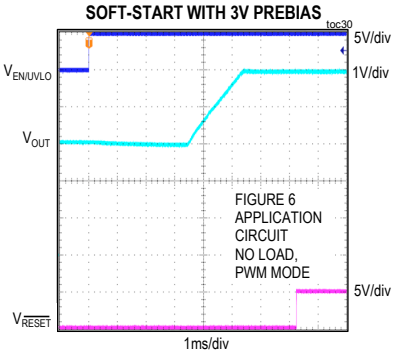


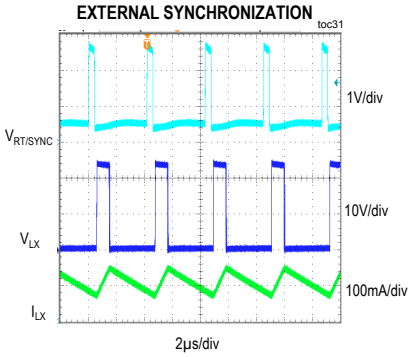
Typical Operating Characteristics (continued)

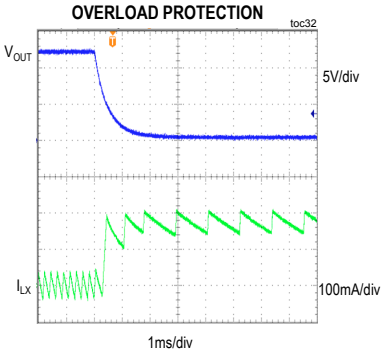
(V_{IN} = 24V, V_{GND} = 0V, V_{OUT} = 3.3V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 191kΩ, C_{IN} = 1µF, T_A = +25°C unless otherwise noted)

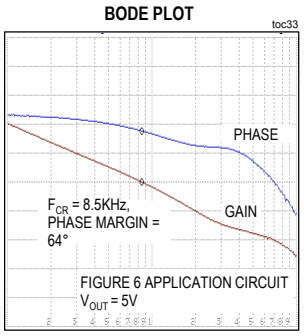


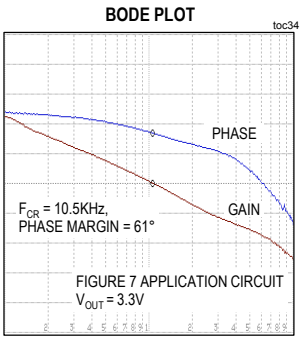




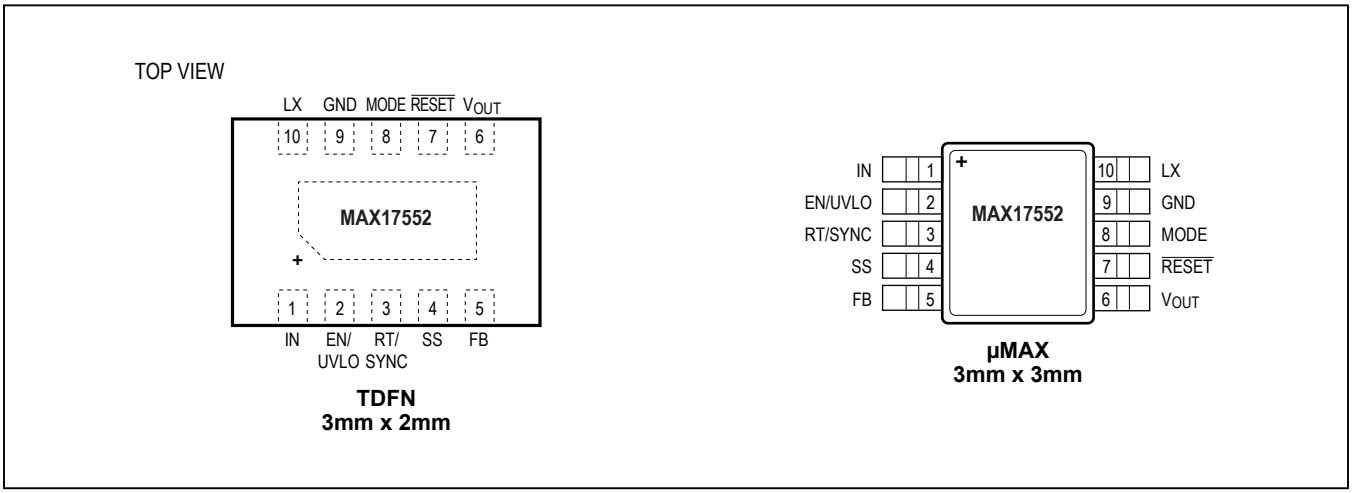








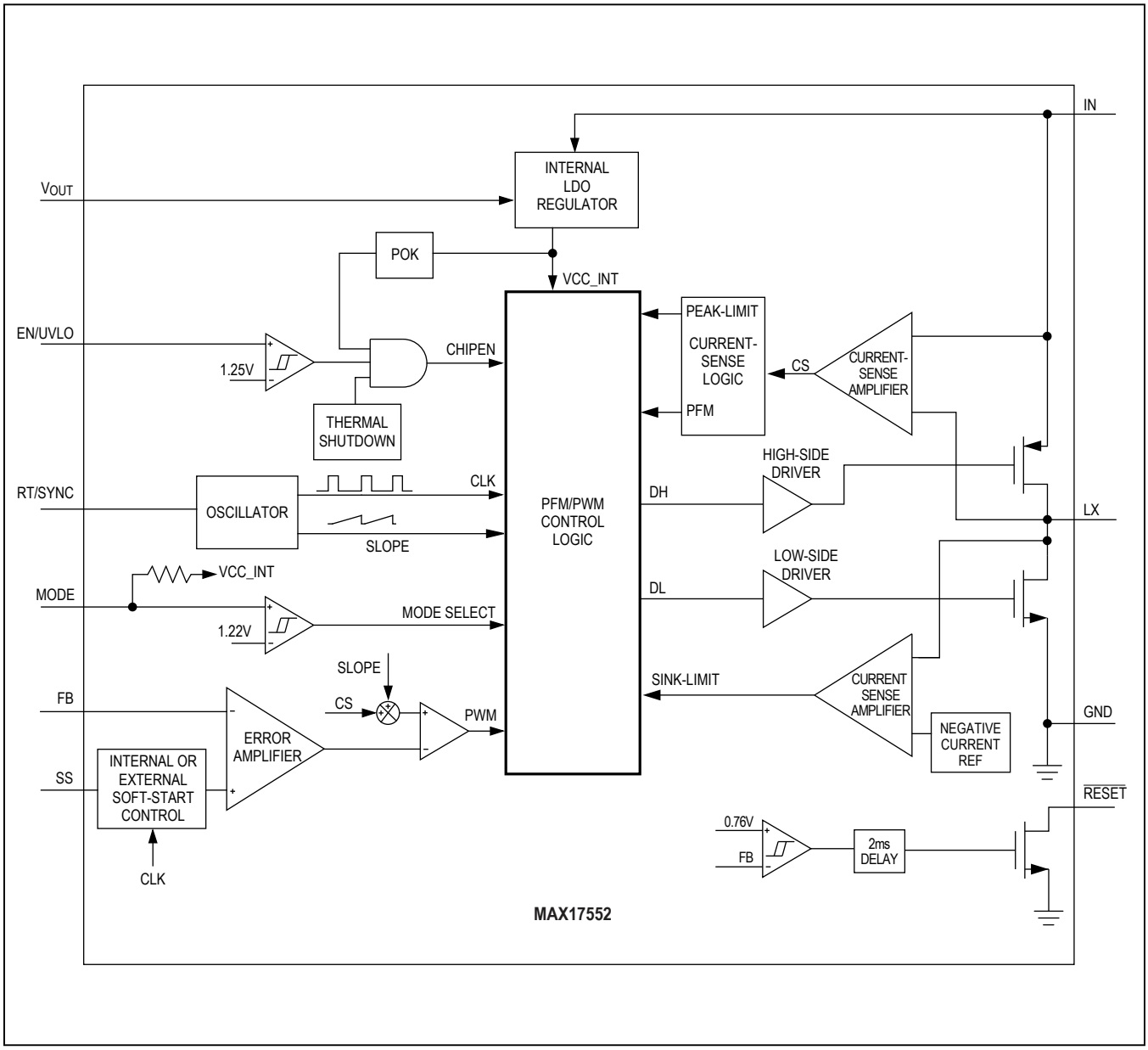
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	IN	Switching Regulator Input. Connect a X7R 1µF ceramic capacitor from IN to GND for bypassing.
2	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to IN for always-on operation. Connect a resistor-divider between IN, EN/UVLO, and GND to program the input voltage at which the device is enabled and turns on.
3	RT/SYNC	Oscillator Timing Resistor Input. Connect a resistor from RT/SYNC to GND to program the switching frequency from 100kHz to 2.2MHz. See the *Switching Frequency (RT/SYNC)* section for details. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. See the *External Synchronization* section for details.
4	SS	Soft-Start Capacitor Input. Connect a capacitor from SS to GND to set the soft-start time. Leave SS unconnected for default 5.1ms internal soft-start.
5	FB	Output Feedback Connection. Connect FB to a resistor-divider between V_{OUT} and GND to set the output voltage. See the *Adjusting the Output Voltage* section for details.
6	VOUT	External Bias Input for Internal Control Circuitry. Decouple to GND with a 0.22µF capacitor and connect to output capacitor positive terminal with a 22.1Ω resistor for applications with an output voltage from 3.3V to 5V. Connect to GND for output voltages < 3.3V and > 5V. See the *External Bias* section for details.
7	RESET	Open-Drain Reset Output. Pull up $\overline{RESET}$ to an external power supply with an external resistor. $\overline{RESET}$ pulls low if FB voltage drops below 92% of its set value. $\overline{RESET}$ goes high impedance 2ms after FB voltage rises above 95% of its set value.
8	MODE	PFM/PWM Mode-Selection Input. Connect MODE to GND to enable the fixed-frequency PWM operation. Leave MODE unconnected for light-load PFM operation.
9	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
10	LX	Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown.
—	EP	Exposed Pad (TDFN Only). Connect to the GND pin to the IC.

Block Diagram



Detailed Description

The MAX17552 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4V to 60V input voltage range. The converter can deliver output current up to 100mA at output voltages of 0.8V to 0.9 x V_{IN}. The output voltage is accurate to within ±1.75% over -40°C to +125°C. The converter consumes only 22µA of supply current in PFM mode while regulating the output voltage at no load.

The device uses an internally compensated, peak-current-mode control architecture (see the *Block Diagram*). On the rising edge of the internal clock, the high-side p-MOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the "on-time." During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, cycle-by-cycle current-limit feature limits inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Mode Selection (MODE)

The device features a MODE pin for selecting either forced-PWM or PFM mode of operation. If the MODE pin is left unconnected, the device operates in PFM mode at light loads. If the MODE pin is grounded, the device operates in a constant-frequency forced-PWM mode at all loads. Mode of operation can be changed on-the-fly during normal operation of the device.

In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency-sensitive applications and provides fixed switching frequency at all loads. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation.

PFM mode disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 72mA (typ) (I_{PFM}) every clock cycle until the output rises to 102% (typ) of the nominal voltage. Once the output reaches 102% (typ) of the nominal voltage, both high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% (typ) of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% (typ) of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102% (typ) of the nominal output voltage. The device naturally exits PFM mode when the load current increases to a magnitude of approximately:

$$I_{PFM} - (\Delta I/2)$$

where ΔI is the peak-peak ripple current in the output inductor. The part enters PFM mode again if the load current reduces to approximately (ΔI/2). See the *Inductor Selection* section for details. The advantage of the PFM mode is higher efficiency at light loads because of lower current drawn from the supply.

Enable Input (EN/UVLO) and Soft-Start (SS)

When EN/UVLO voltage increases above 1.25V (typ), the device initiates a soft-start sequence and the duration of the soft-start depends on the status of the SS pin voltage at the time of power-up. If the SS pin is not connected, the device uses a fixed 5ms internal soft-start to ramp up the internal error-amplifier reference. If a capacitor is connected from SS to GND, a 5µA current source charges the capacitor and ramps up the SS pin voltage. The SS pin voltage is used as reference for the internal error amplifier. Such a reference ramp up allows the output voltage to increase monotonically from zero to the final set value independent of the load current.

EN/UVLO can be used as an input voltage UVLO-adjustment input. An external voltage-divider between IN and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. See the *Setting the Input Undervoltage-Lockout Level* section for details. If input UVLO programming is not desired, connect EN/UVLO to IN (see the *Electrical Characteristics* table for EN/UVLO rising and falling-threshold voltages). Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces IN quiescent current to below 1.2µA. The SS capacitor is discharged with an internal pulldown resistor when EN/UVLO is low. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

Switching Frequency (RT/SYNC)

Switching frequency of the device can be programmed from 100kHz to 2.2MHz by using a resistor connected from RT/SYNC to GND. The switching frequency (f_{SW}) is related to the resistor connected at the RT/SYNC pin (R_T) by the following equation, where R_T is in kΩ and f_{SW} is in kHz:

$$R_T = \frac{42000}{f_{SW}}$$

The switching frequency in ranges of 130kHz to 160kHz and 230kHz to 280kHz are not allowed for user programming to ensure proper configuration of the internal adaptive-loop compensation scheme.

External Synchronization

The RT/SYNC pin can be used to synchronize the device's internal oscillator to an external system clock. The external clock should be coupled to the RT/SYNC pin through a 47pF capacitor, as shown in Figure 1. The external clock logic high level should be higher than 3V, logic low level lower than 0.5V and the duty cycle of the external clock should be in the range of 10% to 70%. External clock synchronization is allowed only in PWM mode of operation (MODE pin connected to GND). The RT resistor should be selected to set the switching frequency 10% lower than the external clock frequency. The external clock should be applied at least 500µs after enabling the device, for proper configuration of the internal loop compensation.

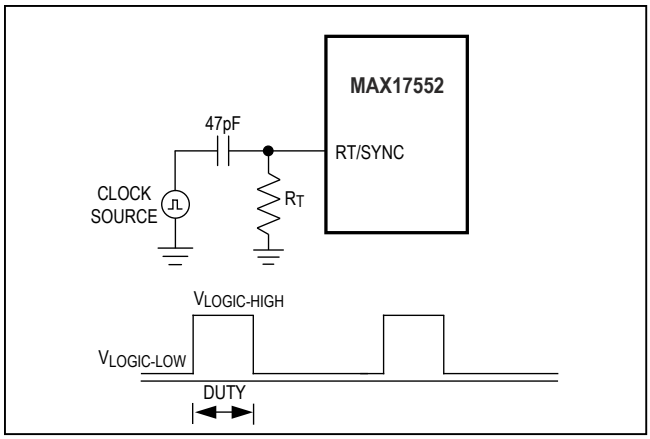


Figure 1. Synchronization to an External Clock

External Bias (V_{OUT})

The device provides a V_{OUT} pin to power the internal blocks from a low-voltage supply. When the V_{OUT} pin voltage exceeds 3.1V, the device draws switching and quiescent current from this pin to improve the converter's efficiency. In applications with an output voltage setting from 3.3V to 5V, V_{OUT} should be decoupled to GND with a ceramic capacitor, and should be connected to the positive terminal of the output capacitor with a resistor (R4, C1) as shown in the typical application circuits. In the absence of R4 and C1, the absolute maximum rating of V_{OUT} (-0.3V) can be exceeded under short-circuit conditions, due to oscillations between the ceramic output capacitor and the inductance of the short-circuit path. In general, parasitic board or wiring inductance should be minimized and the output voltage waveform under short circuit operation should be verified to ensure that the absolute maximum rating of V_{OUT} is not exceeded. For applications with an output voltage setting less than 3.3V or greater than 5V, V_{OUT} should be connected to GND.

Reset Output ($\overline{RESET}$)

The device includes an open-drain $\overline{RESET}$ output to monitor output voltage. $\overline{RESET}$ should be pulled up with an external resistor to the desired external power supply. $\overline{RESET}$ goes high impedance 2ms after the output rises above 95% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal output voltage.

Startup Into a Prebiased Output

The device supports monotonic startup into a prebiased output. When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time, and the minimum operating input voltage is determined by the maximum

duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{INMIN} = \frac{V_{OUT} + (I_{OUT} \times (R_{DCR} + 2.6))}{D_{MAX}} + (I_{OUT} \times 2.5)$$

$$V_{INMAX} = \frac{V_{OUT}}{t_{ONMIN} \times f_{SW}}$$

where V_{OUT} is the steady-state output voltage, I_{OUT} is the maximum load current, R_{DCR} is the DC resistance of the inductor, f_{SW} is the switching frequency (max), D_{MAX} is the maximum duty cycle (0.9), and t_{ONMIN} is the worst-case minimum controllable switch on-time (128ns)

Overcurrent Protection

The device implements a hysteretic cycle-by-cycle peak-current limit protection scheme to protect the inductor and internal FETs under output short circuit conditions. When the inductor peak current exceeds 0.21A (typ), high side switch is turned off and low side switch is turned on to discharge the inductor current. Subsequent clock pulses do not turn on the high-side switch until inductor current discharges to 0.15A (typ). This operation continues until overload/short circuit is removed on the output. Since the inductor current is bounded between two limits, inductor current runaway never happens in this scheme. Additionally, hysteretic negative peak current limit controls the low-side switch negative current when it exceeds 0.1A (typ).

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the IC. When the junction temperature exceeds +160°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The device turns on after the junction temperature cools by 20°C.

Applications Information

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. Calculate the required inductance from the equation:

$$L = \frac{10000 \times V_{OUT}}{f_{SW}}$$

where L is inductance in µH, V_{OUT} is output voltage and f_{SW} is the switching frequency in kHz. Calculate the peak-peak ripple current (ΔI) in the output inductor from the equation:

$$\Delta I = \frac{1000 \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times L}$$

where L is inductance in µH, V_{OUT} is output voltage, V_{IN} is input voltage and f_{SW} is the switching frequency in kHz.

The saturation current rating of the inductor must exceed the maximum current-limit value ($I_{PEAK-LIMIT}$). The saturation current rating should be the maximum of either 0.235A or the value from the equation:

$$I_{SAT} = 0.15 + \frac{V_{INMAX} \times t_{ON-MIN}}{L}$$

where L is inductance in H, V_{INMAX} is maximum input voltage and t_{ON-MIN} is worst case minimum on time (128ns).

Once the L value is known, the next step is to select the right core material. Ferrite and powdered iron are commonly available core materials. Ferrite cores have low core losses and are preferred for high-efficiency designs. Powdered iron cores have more core losses and are relatively cheaper than ferrite cores.

Input Capacitor Selection

Small ceramic input capacitors are recommended for the IC. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. A minimum of 1µF, X7R-grade capacitor in a package larger than 0805 is recommended for the input capacitor of the IC to keep the input-voltage ripple under 2% of the minimum input voltage, and to meet the maximum ripple-current requirements.

Output Capacitor Selection

Small ceramic X7R-grade output capacitors are recommended for the device. The output capacitor has two functions. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. Usually the output capacitor is sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is less than 3%. Calculate the minimum required output capacitance from the following equations:

Frequency Range (kHz)	Minimum Output Capacitance (µF)
100 to 130	$\frac{50}{V_{OUT}}$
160 to 230	$\frac{25}{V_{OUT}}$
280 to 2200	$\frac{17}{V_{OUT}}$

It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

Soft-Start Capacitor Selection

The device offers a 5.1ms internal soft-start when the SS pin is left unconnected. When adjustable soft-start time is required, connect a capacitor from SS to GND to program the soft-start time. Soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$C_{SS} = 6.25 \times t_{SS}$$

where t_{SS} is in milliseconds and C_{SS} is in nanofarads.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to GND (see *Figure 2*). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ max and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.25}{(V_{INU} - 1.25)}$$

where V_{INU} is the voltage at which the device is required to turn on.

Adjusting the Output Voltage

The output voltage can be programmed from 0.8V to 0.9 x V_{IN}. Set the output voltage by connecting a resistor-divider from output to FB to GND (see Figure 3). Choose R2 in the range of 25kΩ to 100kΩ and calculate R1 with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{0.8} - 1\right]$$

Transient Protection

In applications where fast line transients or oscillations with a slew rate in exces of 15V/µs are expected during power-up or steady-state operation, the MAX17552 should be protected with a series resistor that forms a lowpass filter with the input ceramic capacitor (Figure 4). These transients can occur in conditions such as hot-plugging from a low-impedance source or due to inductive load switching and surges on the supply lines.

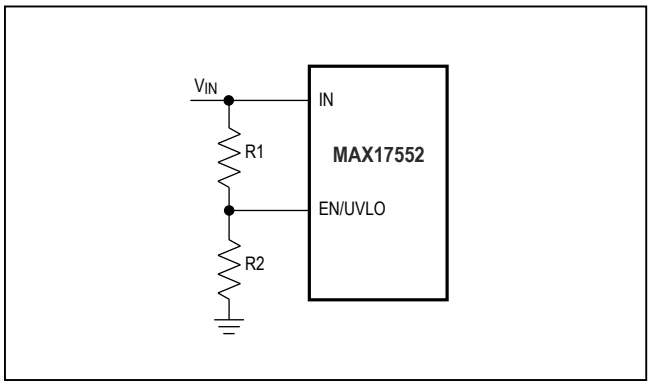


Figure 2. Adjustable EN/UVLO Network

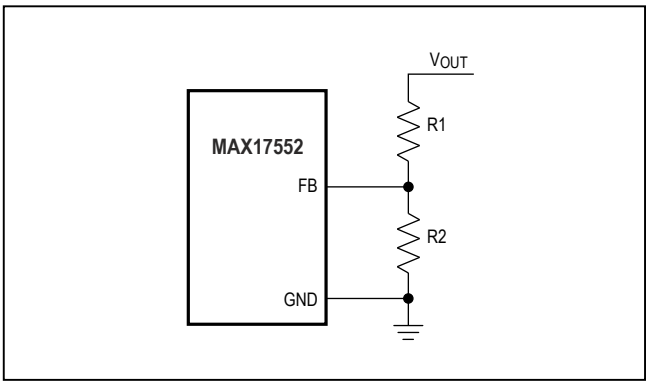


Figure 3. Setting the Output Voltage

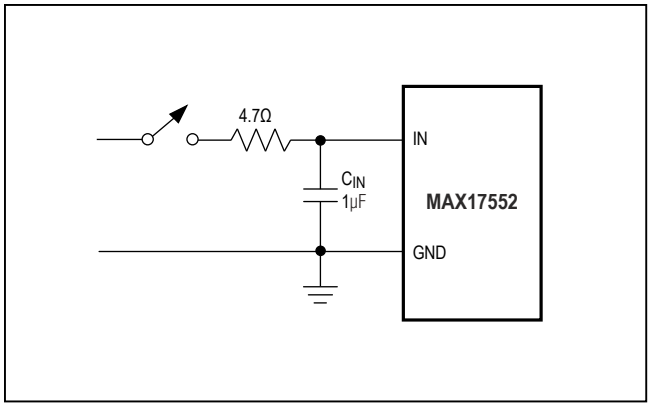


Figure 4. Transient Protection

Power Dissipation

Ensure that the junction temperature of the device does not exceed 125°C under the operating conditions specified for the power supply. At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - (I_{OUT}{}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is the efficiency of power conversion, and R_{DCR} is the DC resistance of the output inductor. See the *Typical Operating Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation.

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

where θ_{JA} is the junction-to-ambient thermal impedance of the package.

PCB Layout Guidelines

Careful PCB layout (Figure 5) is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

- Place the input ceramic capacitor as close as possible to V_{IN} and GND pins
- Minimize the area formed by the LX pin and inductor connection to reduce the radiated EMI
- Ensure that all feedback connections are short and direct
- Route high-speed switching node (LX) away from the signal pins

For a sample PCB layout that ensures the first-pass success, refer to the MAX17552 evaluation kit data sheet.

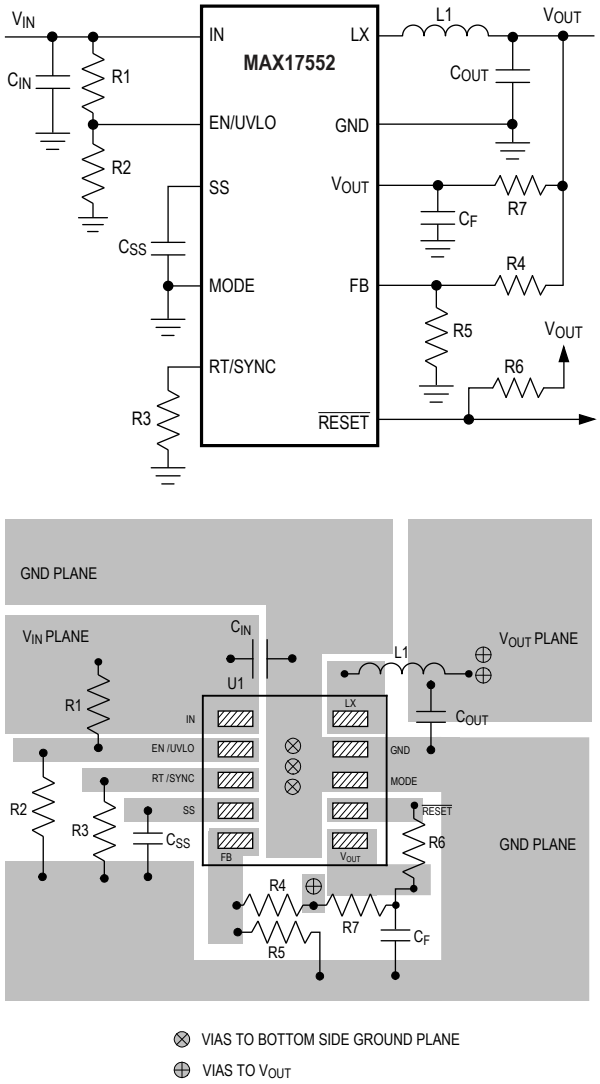


Figure 5. Layout Guidelines

Typical Application Circuits

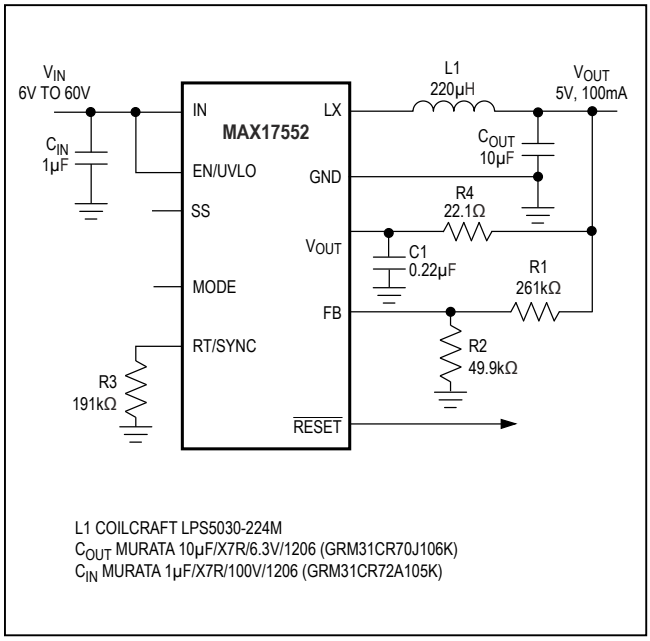


Figure 6. High-Efficiency 5V, 100mA Regulator

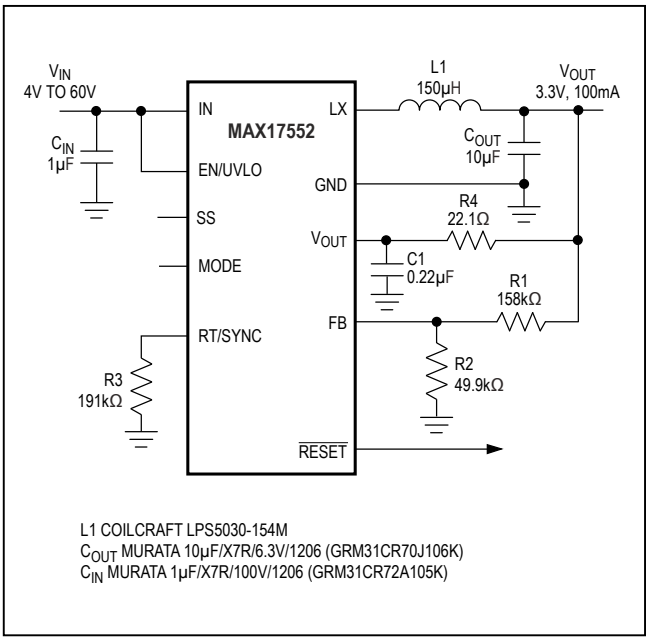


Figure 7. High-Efficiency 3.3V, 100mA Regulator

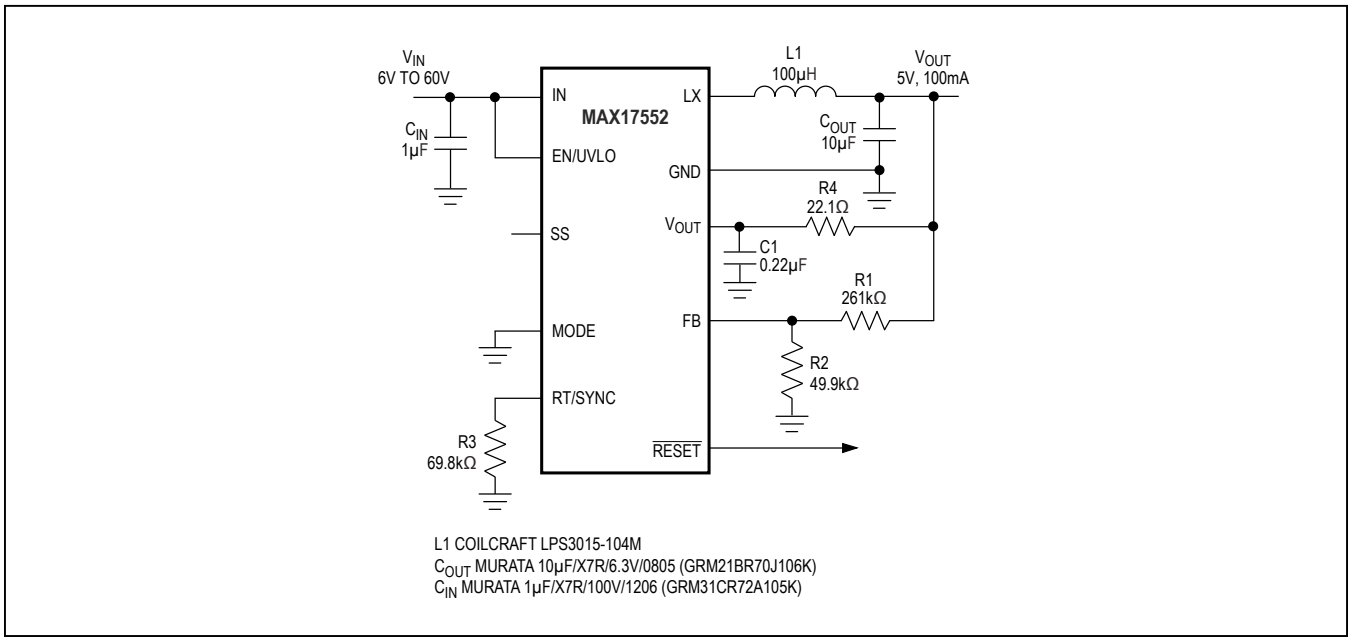


Figure 8. Small Footprint 5V, 100mA Regulator

Typical Application Circuits (continued)

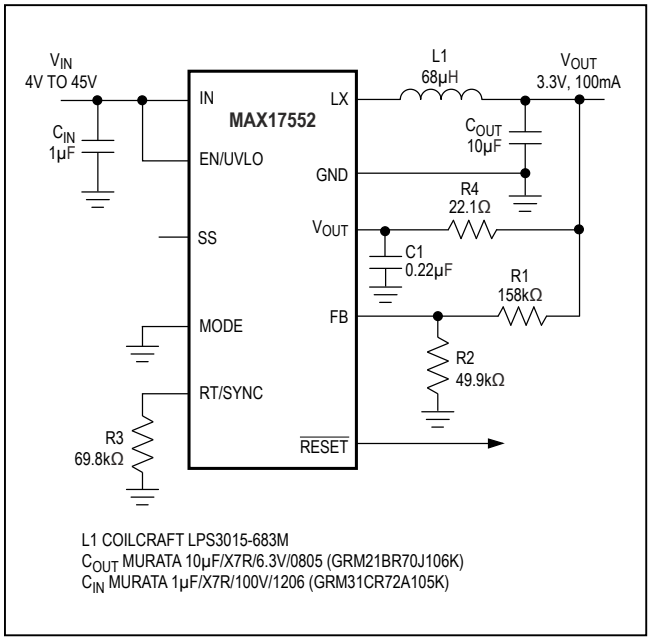


Figure 9. Small Footprint 3.3V, 100mA Regulator

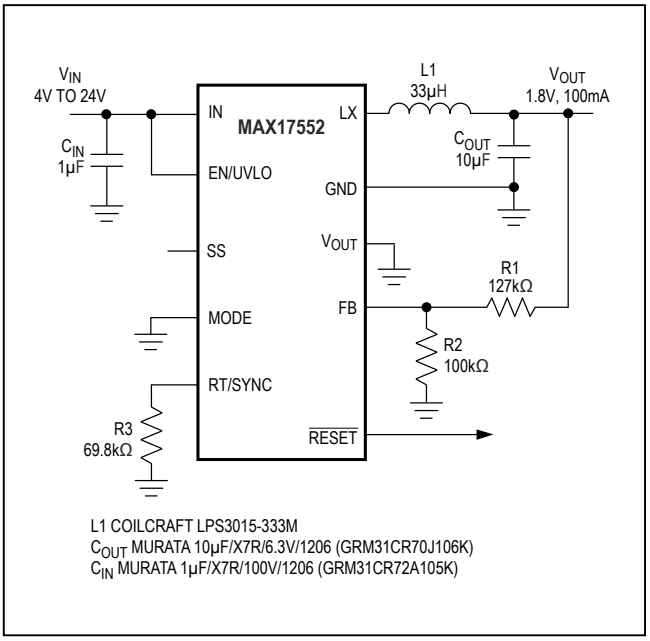


Figure 10. Small Footprint 1.8V, 100mA Regulator

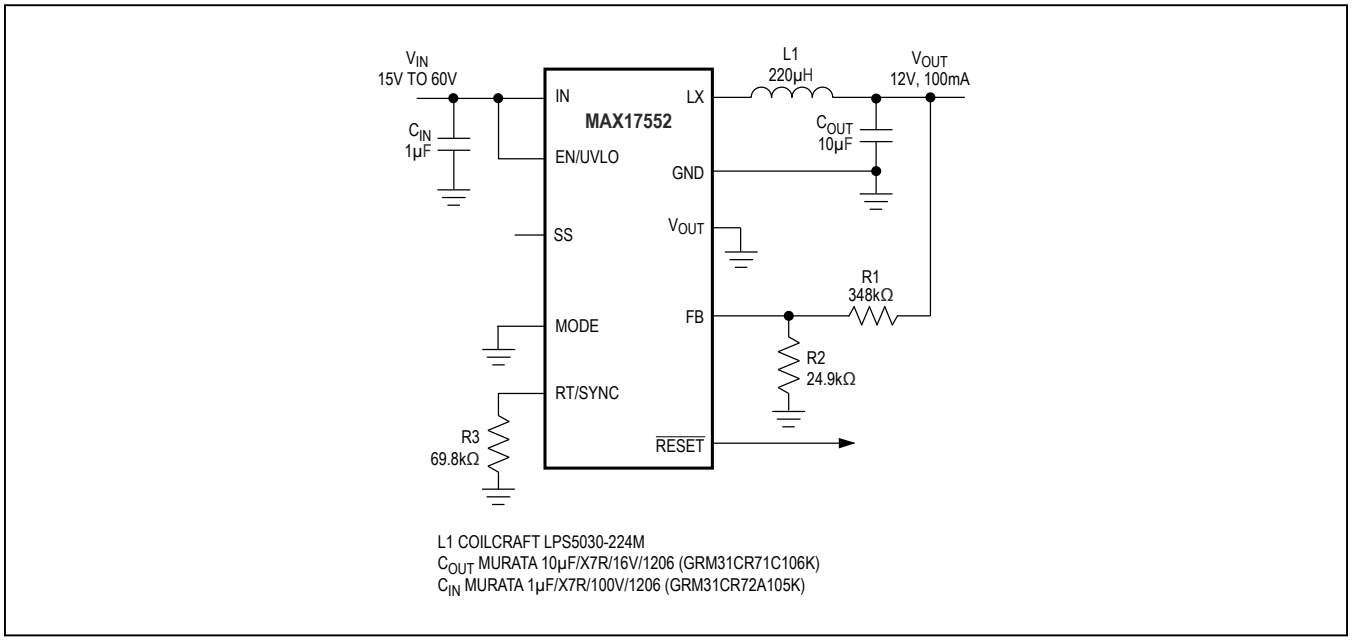


Figure 11. Small Footprint 12V, 100mA Step-Down Regulator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17552ATB+	-40°C to +125°C	10 TDFN-EP*
MAX17552AUB+	-40°C to +125°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1032N+1	**21-0429**	**90-0082**
10 µMAX	U10+5	**21-0061**	**90-0330**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/14	Initial release	—
1	6/14	Added statement regarding EN/UVLO connection	11

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