

16-Channel Low Harmonic Distortion High-Voltage Analog Switches

Features

- 16-channel High-voltage Analog Switch
- Low Harmonic Distortion
- Integrated Bleed Resistors on the Outputs for HV2705
- 3.3V Input Logic Level Compatible
- -60 dB typical OFF-isolation at 5 MHz
- 20 MHz Data Shift Clock Frequency
- 10 μ A Low-quiescent Power Dissipation
- Low Parasitic Capacitance
- DC to 50 MHz Small-signal Frequency Response
- CMOS logic Circuitry for Low Power
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltages

Applications

- Medical Ultrasound Imaging
- Non-destructive Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Optical MEMS Modules

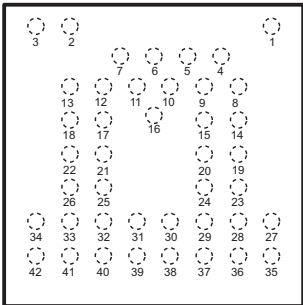
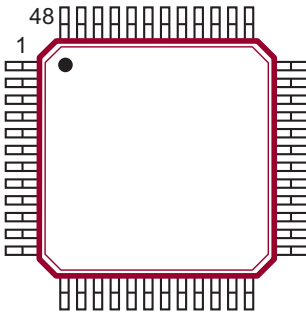
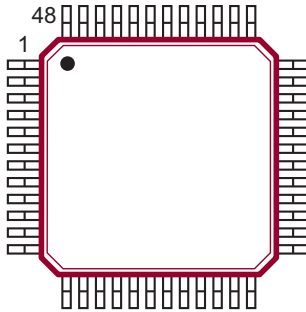
Description

The HV2605 and HV2705 are 16-channel low harmonic distortion high-voltage analog switch integrated circuits (ICs). These devices are designed for applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers. The HV2705 has integrated bleed resistors which eliminate voltage build-up on capacitive loads such as piezoelectric transducers.

These ICs shift input data into a 16-bit Shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. This device combines high-voltage, bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

The device is suitable for various combinations of high-voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V and +160V/-40V.

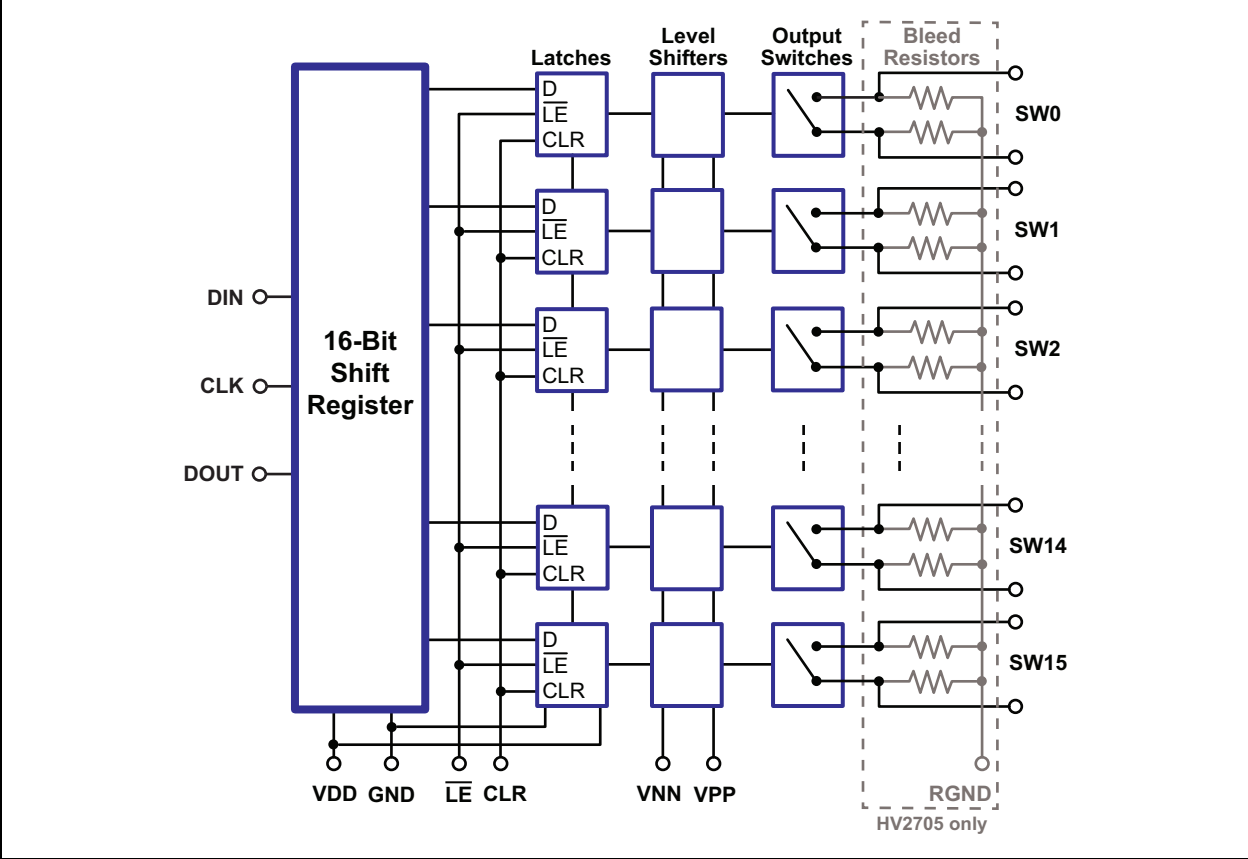
Package Types[†]

42-Ball Bumped Die (Top view)	48-lead TQFP (Top view)	48-lead LQFP (Top view)
		
<p>See Table 2-1 and Table 2-2 for pin information.</p>		

[†] **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

HV2605/HV2705

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[†]

Logic Supply, V_{DD}	-0.5V to +7V
Differential Supply, $V_{PP}-V_{NN}$	220V
Positive Supply, V_{PP}	-0.5V to $V_{NN} + 200V$
Negative Supply, V_{NN}	+0.5V to -200V
Logic Input Voltage	-0.5V to $V_{DD} + 0.3V$
Analog Signal Range	V_{NN} to V_{PP}
Peak Analog Signal Current/Channel	3A
Storage Temperature, T_S	-65°C to 150°C
Power Dissipation:	
42-Ball Bumped Die	1.5W
48-Lead TQFP/LQFP.....	1W

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Power Supply Voltage	V_{DD}	3	—	5.5	V	Note 1 , Note 3
Positive High-voltage Supply	V_{PP}	40	—	$V_{NN}+200V$	V	Note 1 , Note 3
Negative High-voltage Supply	V_{NN}	-40	—	-160	V	Note 1 , Note 3
High-level Input Voltage	V_{IH}	$0.9 V_{DD}$	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	$0.1 V_{DD}$	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	$V_{NN} + 10V$	—	$V_{PP}-10V$	V	Note 2

Note 1: Power-up/power-down sequence is arbitrary except GND must be powered up first and powered down last.

2: V_{SIG} must be within $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power-up/power-down transition.

3: Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1 millisecond.

HV2605/HV2705

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.											
Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch ON-resistance	R _{ONS}	—	30	—	26	38	—	48	Ω	I _{SIG} = 5 mA	V _{PP} = +40V
		—	25	—	22	27	—	32	Ω	I _{SIG} = 200 mA	V _{NN} = -160V
		—	25	—	22	27	—	30	Ω	I _{SIG} = 5 mA	V _{PP} = +100V
		—	18	—	18	24	—	27	Ω	I _{SIG} = 200 mA	V _{NN} = -100V
		—	23	—	20	25	—	30	Ω	I _{SIG} = 5 mA	V _{PP} = +160V
		—	22	—	16	25	—	27	Ω	I _{SIG} = 200 mA	V _{NN} = -40V
Small Signal Switch ON-resistance Matching	ΔR _{ONS}	—	20	—	5	20	—	20	%	I _{SIG} = 5 mA, V _{PP} = +100V, V _{NN} = -100V	
Large Signal Switch ON-resistance	R _{ONL}	—	—	—	15	—	—	—	Ω	V _{SIG} = V _{PP} -10V, I _{SIG} = 1A	
Output Bleed Resistor (HV2705 only)	R _{INT}	—	—	20	35	50	—	—	kΩ	Output Switch to R _{GND} I _{RINT} = 0.5 mA	
Switch OFF Leakage per Switch	I _{SOL}	—	5	—	1	10	—	15	μA	V _{SIG} = V _{PP} -10V and V _{NN} +10V (See Section 3.1 "Test Circuits" .)	
DC Offset Switch OFF	V _{OS}	—	300	—	100	300	—	300	mV	HV2605: 100 kΩ load HV2705: No load	
DC Offset Switch ON		—	500	—	100	500	—	500	mV	(See Section 3.1 "Test Circuits" .)	
Quiescent V _{PP} Supply Current	I _{PPQ}	—	—	—	10	50	—	—	μA	All switches off	
Quiescent V _{NN} Supply Current	I _{NNQ}	—	—	—	-10	-50	—	—	μA	All switches off	
Quiescent V _{PP} Supply Current	I _{PPQ}	—	—	—	10	50	—	—	μA	All switches on, I _{SW} = 5 mA	
Quiescent V _{NN} Supply Current	I _{NNQ}	—	—	—	-10	-50	—	—	μA	All switches on, I _{SW} = 5 mA	
Switch Output Peak Current	I _{SW}	—	3	—	3	2	—	2	A	V _{SIG} duty cycle < 0.1%	
Output Switching Frequency	f _{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V _{PP} Supply Current	I _{PP}	—	6.5	—	—	7	—	8	mA	V _{PP} = +40V V _{NN} = -160V	50 kHz output switching frequency with no load
		—	4	—	—	5.5	—	5.5	mA	V _{PP} = +100V V _{NN} = -100V	
		—	4	—	—	5	—	5.5	mA	V _{PP} = +160V V _{NN} = -40V	
Average V _{NN} Supply Current	I _{NN}	—	6.5	—	—	7	—	8	mA	V _{PP} = +40V V _{NN} = -160V	50 kHz output switching frequency with no load
		—	4	—	—	5	—	5.5	mA	V _{PP} = +100V V _{NN} = -100V	
		—	4	—	—	5	—	5.5	mA	V _{PP} = +160V V _{NN} = -40V	
Average V _{DD} Supply Current	I _{DD}	—	4	—	—	4	—	4	mA	f _{CLK} = 5 MHz, V _{DD} = 5V	
Quiescent V _{DD} Supply Current	I _{DDQ}	—	10	—	—	10	—	10	μA	All logic inputs are static.	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Data Out Source Current	I _{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	V _{OUT} = V _{DD} - 0.7V
Data Out Sink Current	I _{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	V _{OUT} = 0.7V
Logic Input Capacitance	C _{IN}	—	10	—	—	10	—	10	pF	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 5V, t_r = t_f ≤ 5 ns, 50% duty cycle and C_{LOAD} = 20 pF unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Set-up Time before Latch Enable Rises	t _{SD}	25	—	25	—	—	25	—	ns	
Time Width of $\overline{\text{LE}}$	t _{WLE}	56	—	—	56	—	56	—	ns	V _{DD} = 3V
		12	—	—	12	—	12	—	ns	V _{DD} = 5V
Clock Delay Time to Data Out	t _{DO}	50	100	50	78	100	50	100	ns	V _{DD} = 3V
		15	40	15	30	40	15	40	ns	V _{DD} = 5V
Time Width of CLR	t _{WCLR}	55	—	55	—	—	55	—	ns	
Set-up Time Data to Clock	t _{SU}	21	—	—	21	—	21	—	ns	V _{DD} = 3V
		7	—	—	7	—	7	—	ns	V _{DD} = 5V
Hold Time Data from Clock	t _H	2	—	2	—	—	2	—	ns	V _{DD} = 3V or 5V
Clock Frequency	f _{CLK}	—	10	—	—	10	—	10	MHz	V _{DD} = 3V
		—	20	—	—	20	—	20	MHz	V _{DD} = 5V
Clock Rise and Fall Times	t _r , t _f	—	50	—	—	50	—	50	ns	
Turn ON Time	T _{ON}	—	5	—	—	5	—	5	μs	V _{SIG} = V _{PP} - 10V, R _{LOAD} = 10 kΩ (See Section 3.1 "Test Circuits".)
Turn OFF Time	T _{OFF}	—	5	—	—	5	—	5	μs	V _{SIG} = V _{PP} - 10V, R _{LOAD} = 10 kΩ (See Section 3.1 "Test Circuits".)
Maximum V _{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	V _{PP} = +40V, V _{NN} = -160V
		—	20	—	—	20	—	20	V/ns	V _{PP} = +100V, V _{NN} = -100V
		—	20	—	—	20	—	20	V/ns	V _{PP} = +160V, V _{NN} = -40V
OFF Isolation	K _O	-30	—	-30	-33	—	-30	—	dB	f = 5 MHz, 1 kΩ//15 pF load (See Section 3.1 "Test Circuits".)
		-58	—	-58	—	—	-58	—	dB	f = 5 MHz, 50Ω load (See Section 3.1 "Test Circuits".)
Switch Crosstalk	K _{CR}	-60	—	-60	-70	—	-60	—	dB	f = 5 MHz, 50Ω load (See Section 3.1 "Test Circuits".)

HV2605/HV2705

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

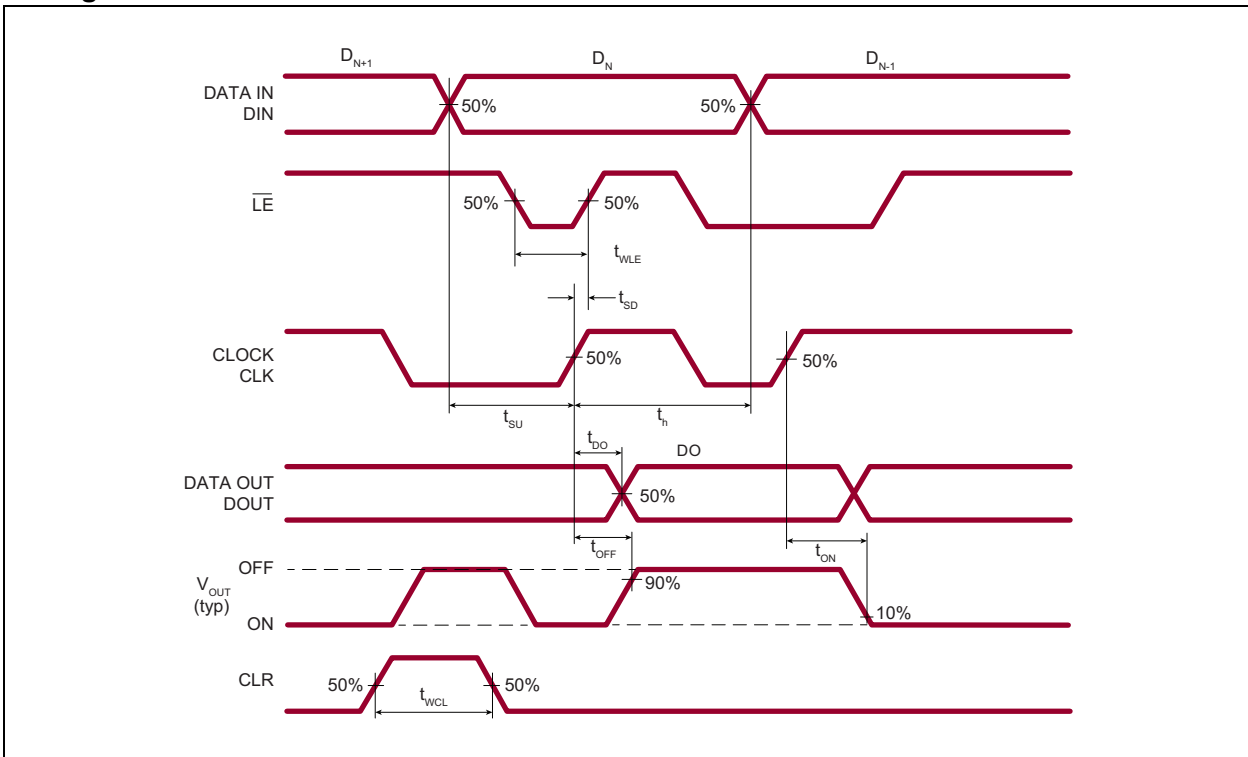
Electrical Specifications: $V_{DD} = 5V$, $t_r = t_f \leq 5 \text{ ns}$, 50% duty cycle and $C_{LOAD} = 20 \text{ pF}$ unless otherwise noted.										
Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle (See Section 3.1 “Test Circuits”).
OFF Capacitance SW to GND	$C_{SG(OFF)}$	—	15	—	10	15	—	15	pF	0V, $f = 1 \text{ MHz}$
ON Capacitance SW to GND	$C_{SG(ON)}$	—	18	—	13	18	—	18	pF	0V, $f = 1 \text{ MHz}$
Output Voltage Spike	+ V_{SPK}	—	—	—	—	150	—	—	mV	$V_{PP} = +40V$, $V_{NN} = -160V$, $R_{LOAD} = 50\Omega$ (See Section 3.1 “Test Circuits”).
	- V_{SPK}	—	—	—	—		—	—	mV	
	+ V_{SPK}	—	—	—	—	150	—	—	mV	$V_{PP} = +100V$, $V_{NN} = -100V$, $R_{LOAD} = 50\Omega$ (See Section 3.1 “Test Circuits”).
	- V_{SPK}	—	—	—	—		—	—	mV	
	+ V_{SPK}	—	—	—	—	150	—	—	mV	$V_{PP} = +160V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$ (See Section 3.1 “Test Circuits”).
	- V_{SPK}	—	—	—	—		—	—	mV	
Charge Injection	QC	—	—	—	820	—	—	—	pC	$V_{PP} = +40V$, $V_{NN} = -160V$, $V_{SIG} = 0V$ (See Section 3.1 “Test Circuits”).
		—	—	—	600	—	—	—	pC	$V_{PP} = +100V$, $V_{NN} = -100V$, $V_{SIG} = 0V$ (See Section 3.1 “Test Circuits”).
		—	—	—	350	—	—	—	pC	$V_{PP} = +160V$, $V_{NN} = -40V$, $V_{SIG} = 0V$ (See Section 3.1 “Test Circuits”).

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	70	$^\circ\text{C}$	
Storage Temperature	T_S	-65	—	150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
48-lead LQFP	θ_{JA}	—	52	—	$^\circ\text{C}/\text{W}$	Note 1

Note 1: Mounted on an FR-4 board, 25 mm x 25 mm x 1.57 mm

Timing Waveforms



HV2605/HV2705

2.0 PIN DESCRIPTION

The description of pins in the 42-ball bumped die, 48-lead TQFP and 48-lead LQFP packages are listed on [Table 2-1](#) and [Table 2-2](#), respectively. The locations of the pads/balls are listed in [Package Types†](#).

TABLE 2-1: 42-BALL BUMPED DIE PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
1	NC	—	No connection
	—	RGND	Ground for bleed resistor
2	VPP	VPP	Positive supply voltage
3	VNN	VNN	Negative supply voltage
4	DOUT	DOUT	Data out logic output
5	CLR	CLR	Latch clear logic input
6	CLK	CLK	Clock logic input for Shift register
7	GND	GND	Ground
8	SW15A	SW15A	Analog Switch 15 Terminal A
9	SW15B	SW15B	Analog Switch 15 Terminal B
10	LE	LE	Latch enable logic input, low active
11	VDD	VDD	Logic supply voltage
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	SW0B	SW0B	Analog Switch 0 Terminal B
14	SW14A	SW14A	Analog Switch 14 Terminal A
15	SW14B	SW14B	Analog Switch 14 Terminal B
16	DIN	DIN	Data in logic input
17	SW1A	SW1A	Analog Switch 1 Terminal A
18	SW1B	SW1B	Analog Switch 1 Terminal B
19	SW13A	SW13A	Analog Switch 13 Terminal A
20	SW13B	SW13B	Analog Switch 13 Terminal B
21	SW2A	SW2A	Analog Switch 2 Terminal A
22	SW2B	SW2B	Analog Switch 2 Terminal B
23	SW12A	SW12A	Analog Switch 12 Terminal A
24	SW12B	SW12B	Analog Switch 12 Terminal B
25	SW3A	SW3A	Analog Switch 3 Terminal A
26	SW3B	SW3B	Analog Switch 3 Terminal B
27	SW11A	SW11A	Analog Switch 11 Terminal A
28	SW11B	SW11B	Analog Switch 11 Terminal B
29	SW9B	SW9B	Analog Switch 9 Terminal B
30	SW8B	SW8B	Analog Switch 8 Terminal B
31	SW7A	SW7A	Analog Switch 7 Terminal A
32	SW6A	SW6A	Analog Switch 6 Terminal A
33	SW4A	SW4A	Analog Switch 4 Terminal A
34	SW4B	SW4B	Analog Switch 4 Terminal B
35	SW10B	SW10B	Analog Switch 10 Terminal B
36	SW10A	SW10A	Analog Switch 10 Terminal A
37	SW9A	SW9A	Analog Switch 9 Terminal A
38	SW8A	SW8A	Analog Switch 8 terminal A

TABLE 2-1: 42-BALL BUMPED DIE PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
39	SW7B	SW7B	Analog Switch 7 Terminal B
40	SW6B	SW6B	Analog Switch 6 Terminal B
41	SW5B	SW5B	Analog Switch 5 Terminal B
42	SW5A	SW5A	Analog Switch 5 Terminal A

TABLE 2-2: 48-LEAD TQFP/LQFP PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
1	NC	NC	No connection
2	NC	NC	No connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	SW3B	SW3B	Analog Switch 3 Terminal B
6	SW3A	SW3A	Analog Switch 3 Terminal A
7	SW2B	SW2B	Analog Switch 2 Terminal B
8	SW2A	SW2A	Analog Switch 2 Terminal A
9	SW1B	SW1B	Analog Switch 1 Terminal B
10	SW1A	SW1A	Analog Switch 1 Terminal A
11	SW0B	SW0B	Analog Switch 0 Terminal B
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	VNN	VNN	Negative supply voltage
14	NC	NC	No connection
15	VPP	VPP	Positive supply voltage
16	NC	NC	No connection
17	GND	GND	Ground
18	VDD	VDD	Logic supply voltage
19	DIN	DIN	Data in logic input
20	CLK	CLK	Clock logic input for Shift register
21	LE	LE	Latch-enable logic input, low active
22	CLR	CLR	Latch clear logic input
23	DOUT	DOUT	Data out logic output
24	NC	—	No connection
	—	RGND	Ground for bleed resistor
25	SW15B	SW15B	Analog Switch 15 Terminal B
26	SW15A	SW15A	Analog Switch 15 Terminal A
27	SW14B	SW14B	Analog Switch 14 Terminal B
28	SW14A	SW14A	Analog Switch 14 Terminal A
29	SW13B	SW13B	Analog Switch 13 Terminal B
30	SW13A	SW13A	Analog Switch 13 Terminal A
31	SW12B	SW12B	Analog Switch 12 Terminal B
32	SW12A	SW12A	Analog Switch 12 Terminal A
33	SW11B	SW11B	Analog Switch 11 Terminal B
34	SW11A	SW11A	Analog Switch 11 Terminal A

HV2605/HV2705

TABLE 2-2: 48-LEAD TQFP/LQFP PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
35	NC	NC	No connection
36	NC	NC	No connection
37	SW10B	SW10B	Analog Switch 10 Terminal B
38	SW10A	SW10A	Analog Switch 10 Terminal A
39	SW9B	SW9B	Analog Switch 9 Terminal B
40	SW9A	SW9A	Analog Switch 9 Terminal A
41	SW8B	SW8B	Analog Switch 8 Terminal B
42	SW8A	SW8A	Analog Switch 8 Terminal A
43	SW7B	SW7B	Analog Switch 7 Terminal B
44	SW7A	SW7A	Analog Switch 7 Terminal A
45	SW6B	SW6B	Analog Switch 6 Terminal B
46	SW6A	SW6A	Analog Switch 6 Terminal A
47	SW5B	SW5B	Analog Switch 5 Terminal B
48	SW5A	SW5A	Analog Switch 5 Terminal A

3.0 FUNCTIONAL DESCRIPTION

3.1 Test Circuits

Figure 3-1 to Figure 3-8 show the test circuits for HV2605/HV2705.

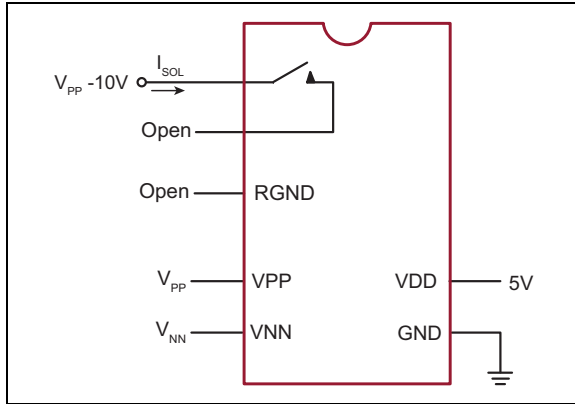


FIGURE 3-1: Switch Off Leakage per Switch.

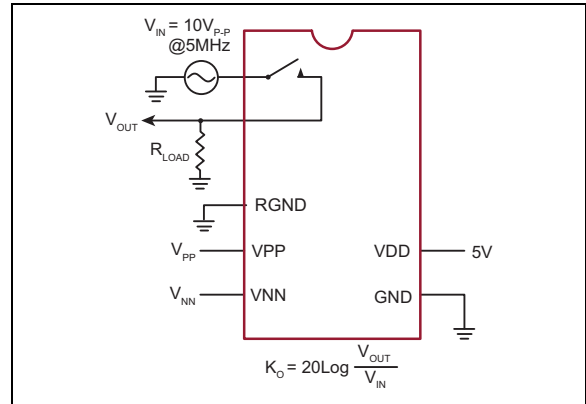


FIGURE 3-4: Off Isolation.

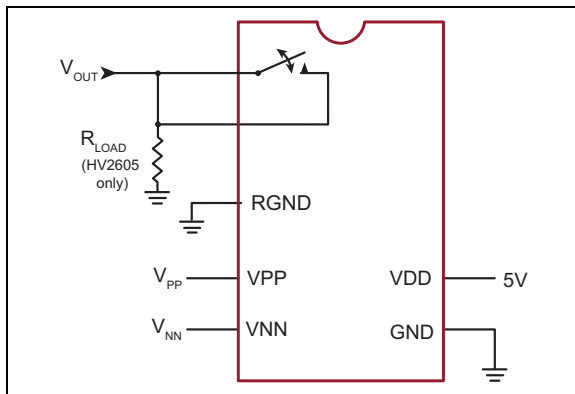


FIGURE 3-2: Switch DC Offset.

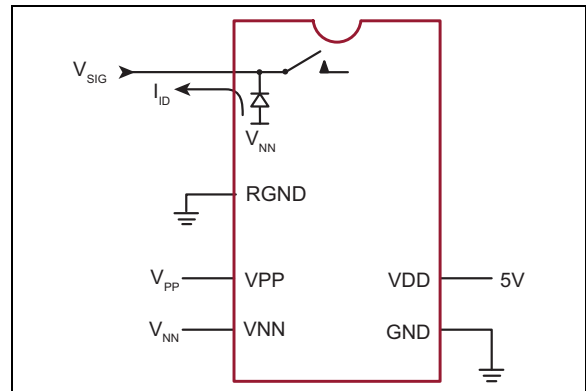


FIGURE 3-5: Output Switch Isolation Diode Current.

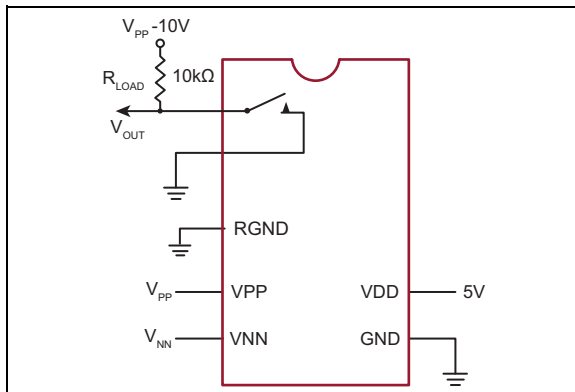


FIGURE 3-3: T_{ON}/T_{OFF} Test Circuit.

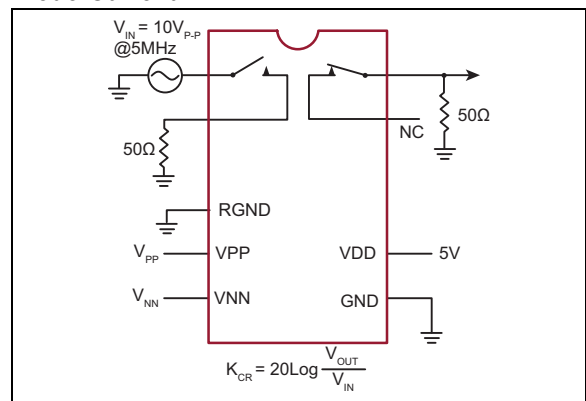


FIGURE 3-6: Switch Crosstalk.

HV2605/HV2705

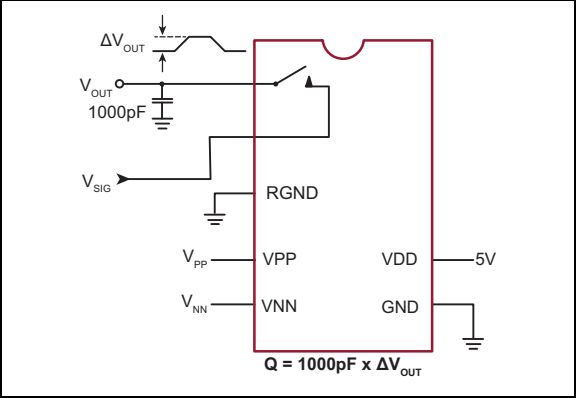


FIGURE 3-7: Charge Injection.

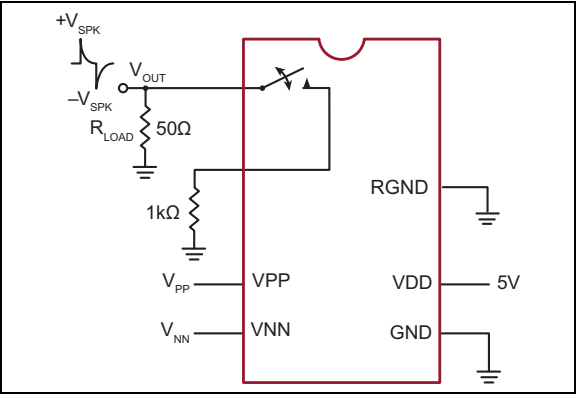


FIGURE 3-8: Output Voltage Spike.

TABLE 3-1: TRUTH FUNCTION TABLE

D0	D1	...	D7	D8	...	D15	\overline{LE}	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	—		—	—		—	L	L	OFF	—		—	—		—
H	—		—	—		—	L	L	ON	—		—	—		—
—	L		—	—		—	L	L	—	OFF		—	—		—
—	H		—	—		—	L	L	—	ON		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		L	—		—	L	L	—	—		OFF	—		—
—	—		H	—		—	L	L	—	—		ON	—		—
—	—	...	—	L	...	—	L	L	—	—	...	—	OFF	...	—
—	—		—	H		—	L	L	—	—		—	ON		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		L	L	L	—	—		—	—		OFF
—	—		—	—		H	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

- Note 1:** The 16 switches operate independently.
- 2:** Serial data is clocked in on the low-to-high transition of the clock.
- 3:** All 16 switches go to a state retaining their latched condition at the rising edge of \overline{LE} . When \overline{LE} is low, the Shift registers data flow through the latch.
- 4:** D_{OUT} is high when data in the Shift register 15 is high.
- 5:** Shift registers clocking has no effect on the switch states if \overline{LE} is high.
- 6:** The CLR clear input overrides all other inputs.

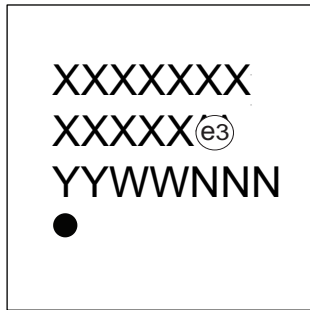
HV2605/HV2705

4.0 PACKAGING INFORMATION†

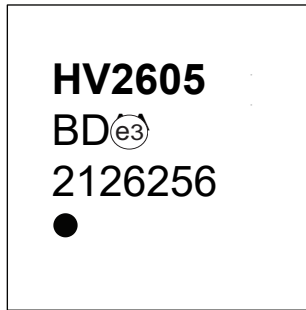
4.1 Package Marking Information

† **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

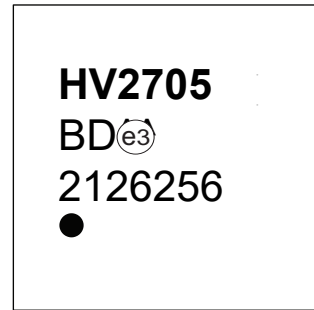
42-Ball Bumped Die



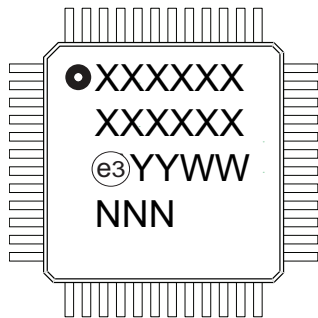
Example



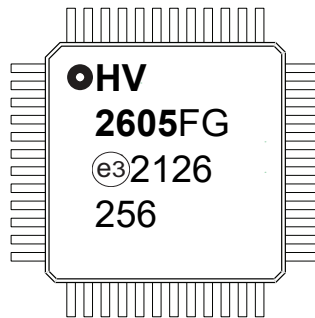
Example



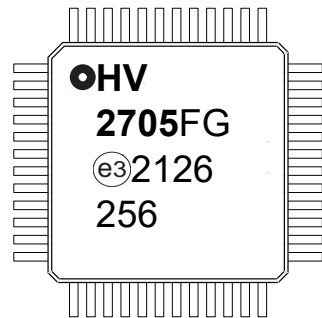
48-Lead LQFP



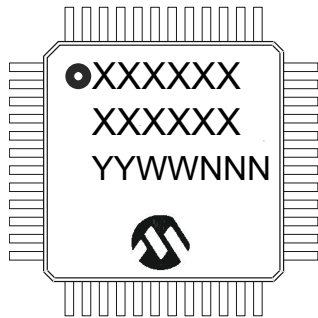
Example



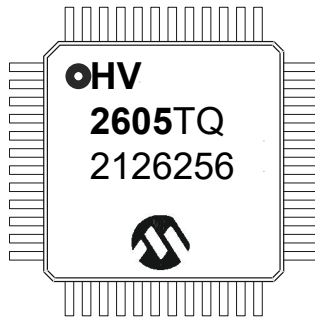
Example



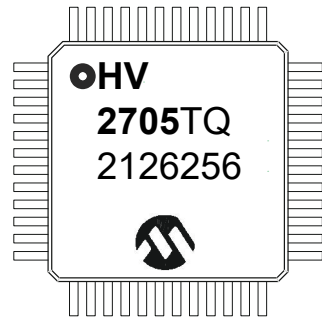
48-Lead TQFP



Example



Example



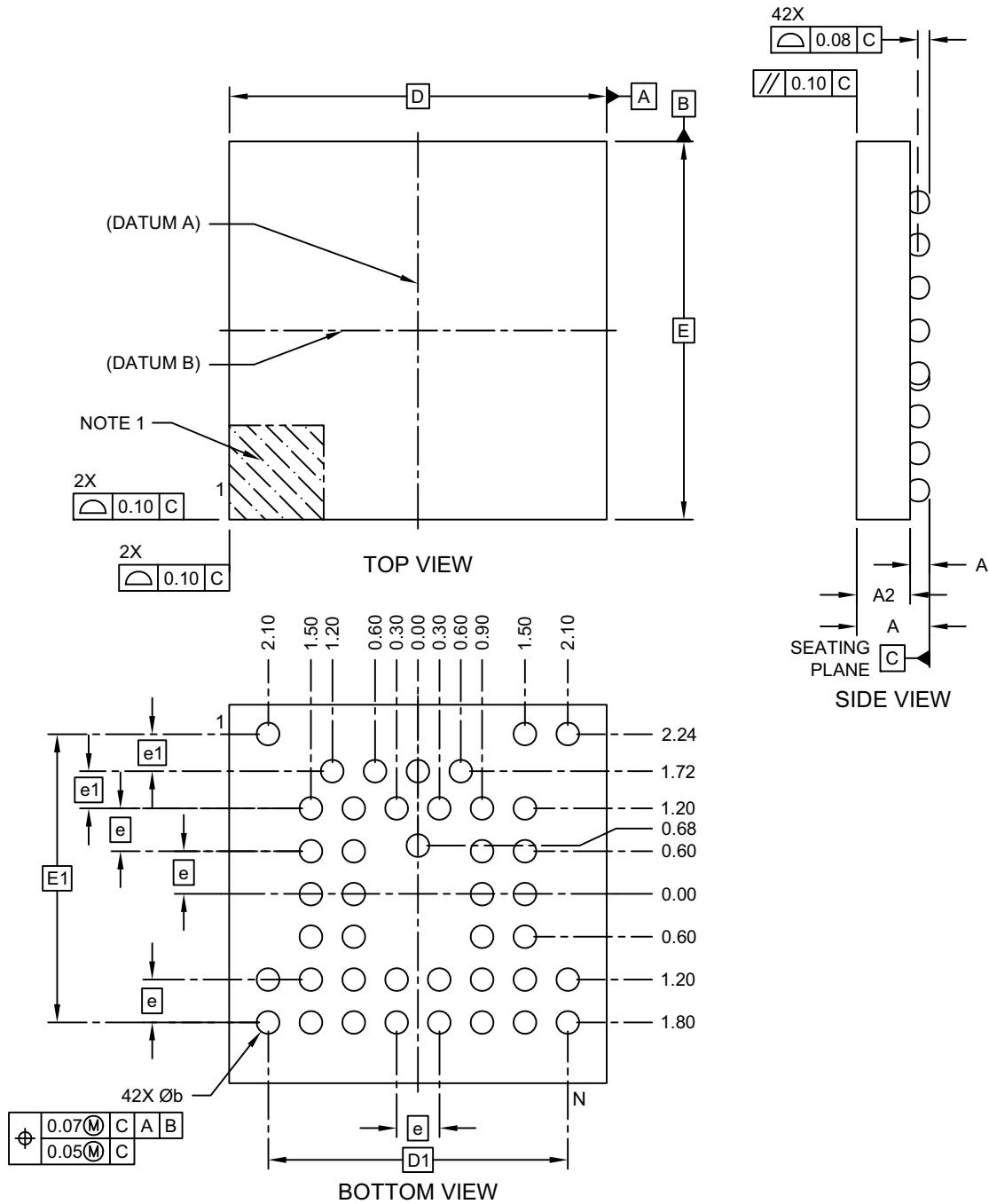
Legend:

- XX...X Product Code or Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week '01')
- NNN Alphanumeric traceability code
- (e3) Pb-free JEDEC® designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

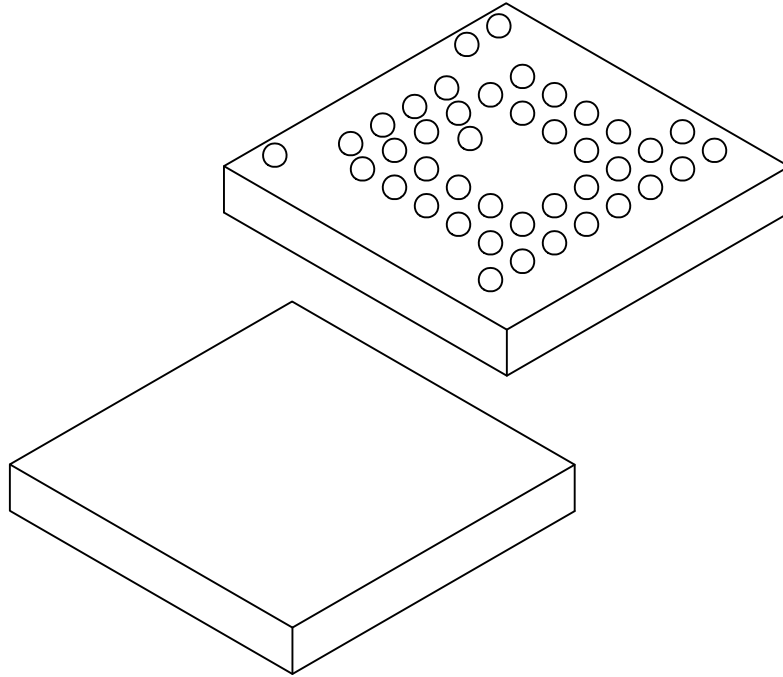


Microchip Technology Drawing C04-533-75X Rev B Sheet 1 of 2

HV2605/HV2705

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	42		
Terminal Pitch	e	0.60 BSC		
Terminal Pitch	e1	0.52 BSC		
Overall Height	A	0.91	0.965	1.02
Standoff	A1	0.21	0.24	0.27
Terminal Thickness	A2	0.70	0.725	0.75
Overall Length	D	5.29 BSC		
Exposed Pad Length	D1	4.20 BSC		
Overall Width	E	5.30 BSC		
Exposed Pad Width	E1	4.04 BSC		
Terminal Width	b	0.29	0.32	0.35

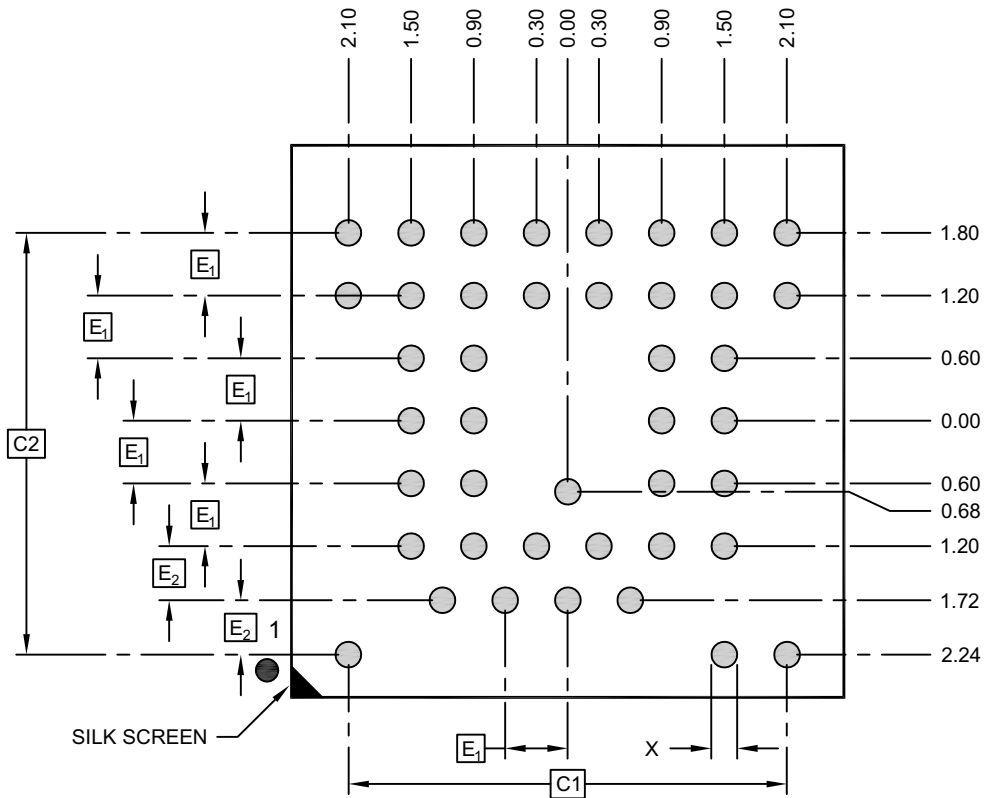
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-533-75X Rev B Sheet 2 of 2

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E_1	0.60 BSC		
Contact Pitch	E_2	0.52 BSC		
Contact Pad Spacing	C1	4.20 BSC		
Contact Pad Spacing	C2	4.04 BSC		
Contact Pad Width (Xnn)	X			0.25

Notes:

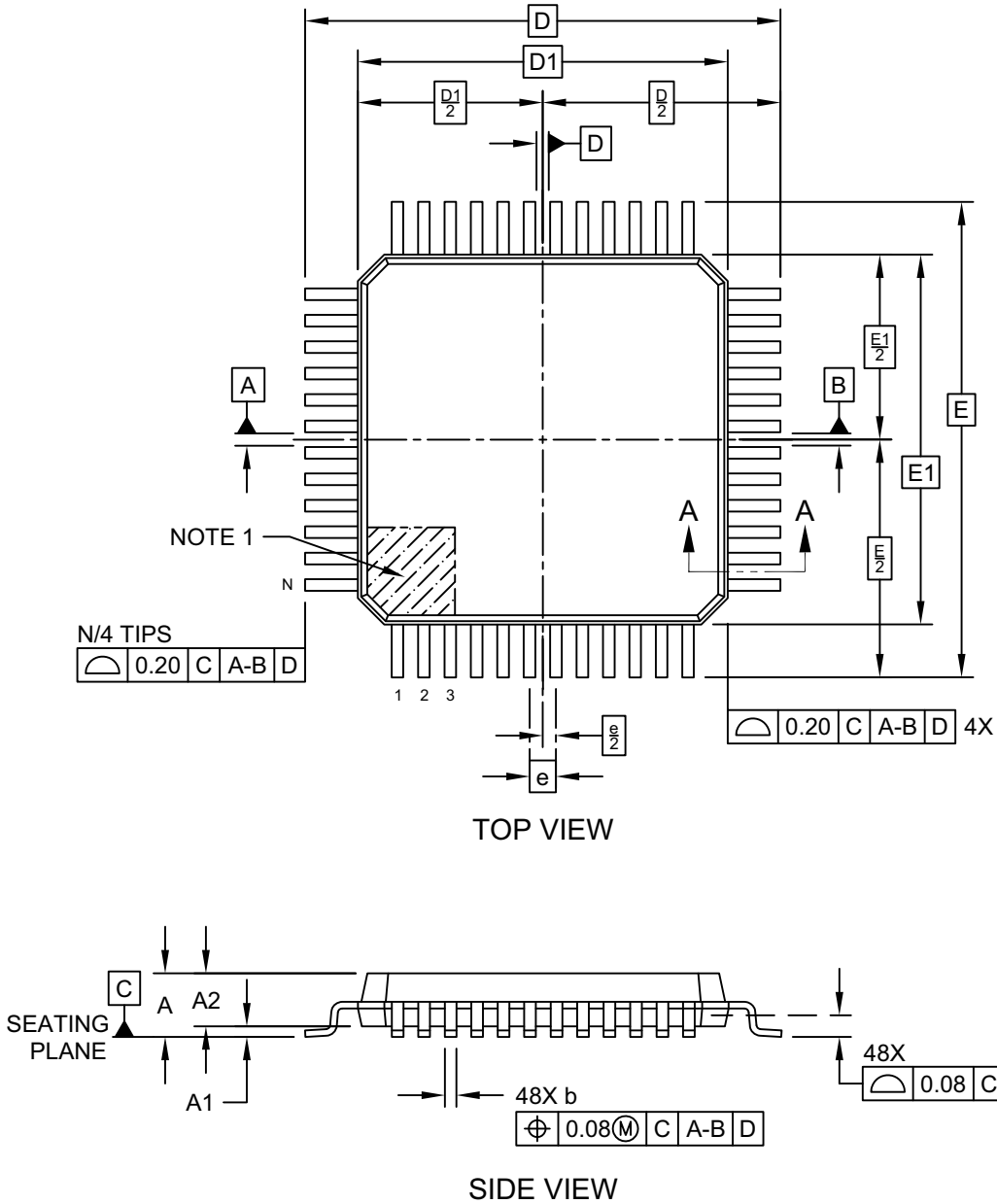
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2533-75X Rev B

HV2605/HV2705

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

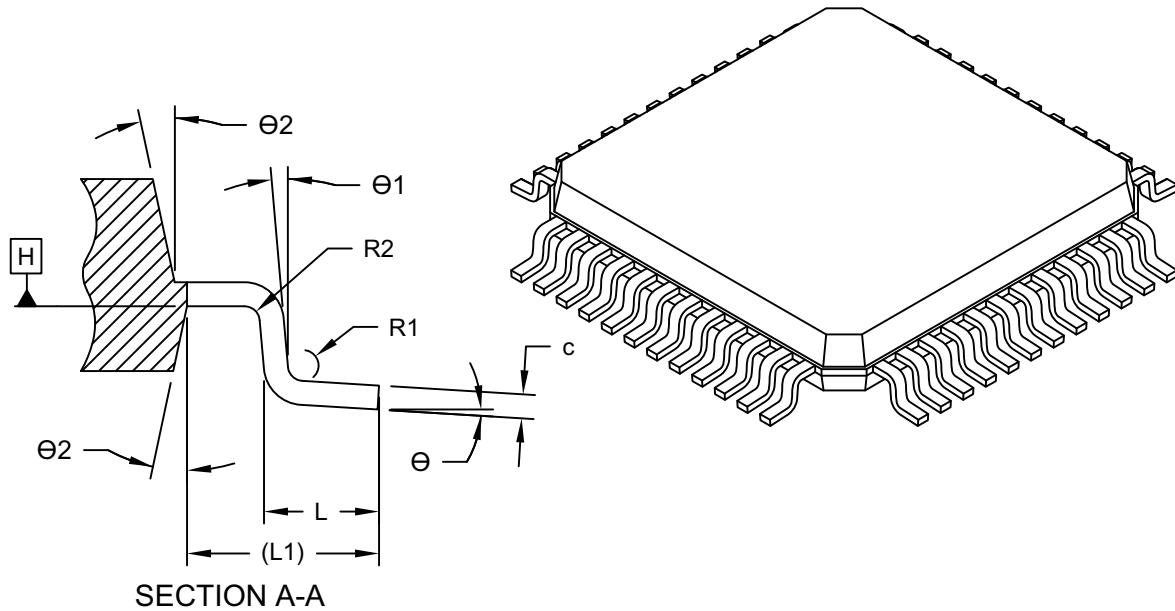
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-300-Y8X Rev D Sheet 1 of 2

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	48		
Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D	9.00 BSC		
Molded Package Length	D1	7.00 BSC		
Overall Width	E	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	θ	0°	3.5°	7°
Lead Angle	$\theta 1$	0°	-	-
Mold Draft Angle	$\theta 2$	11°	12°	13°

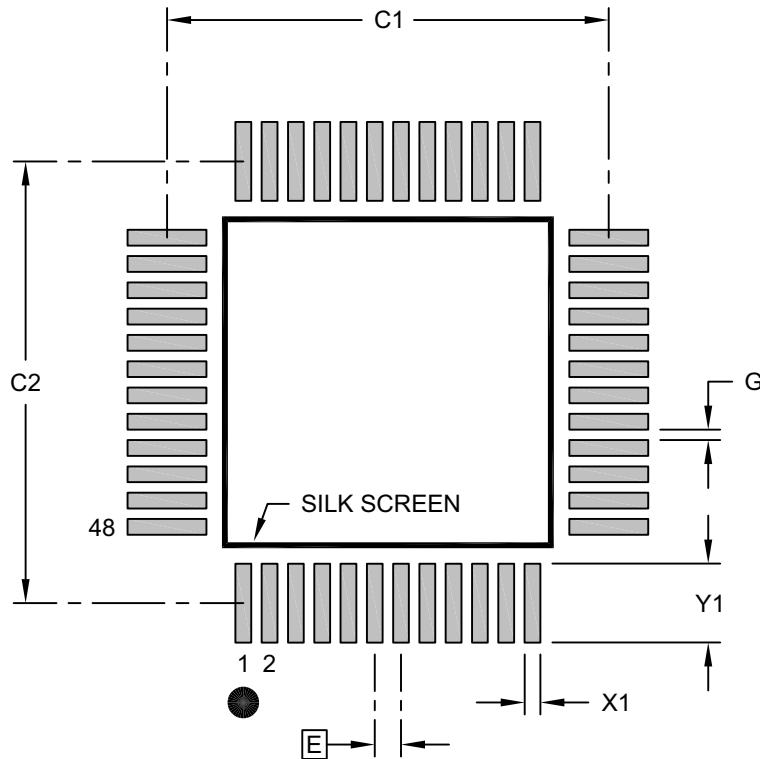
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

HV2605/HV2705

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

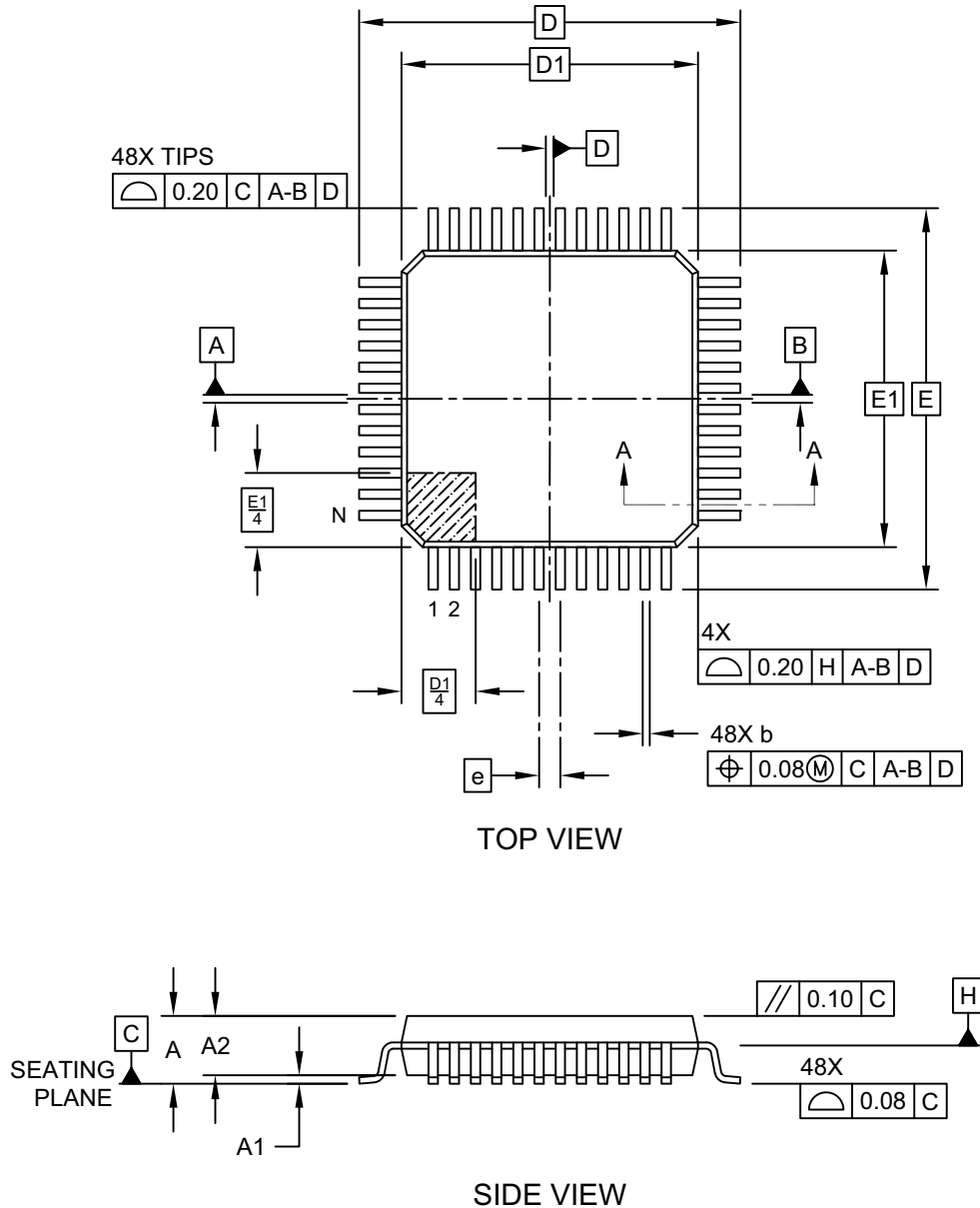
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-Y8X Rev D

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

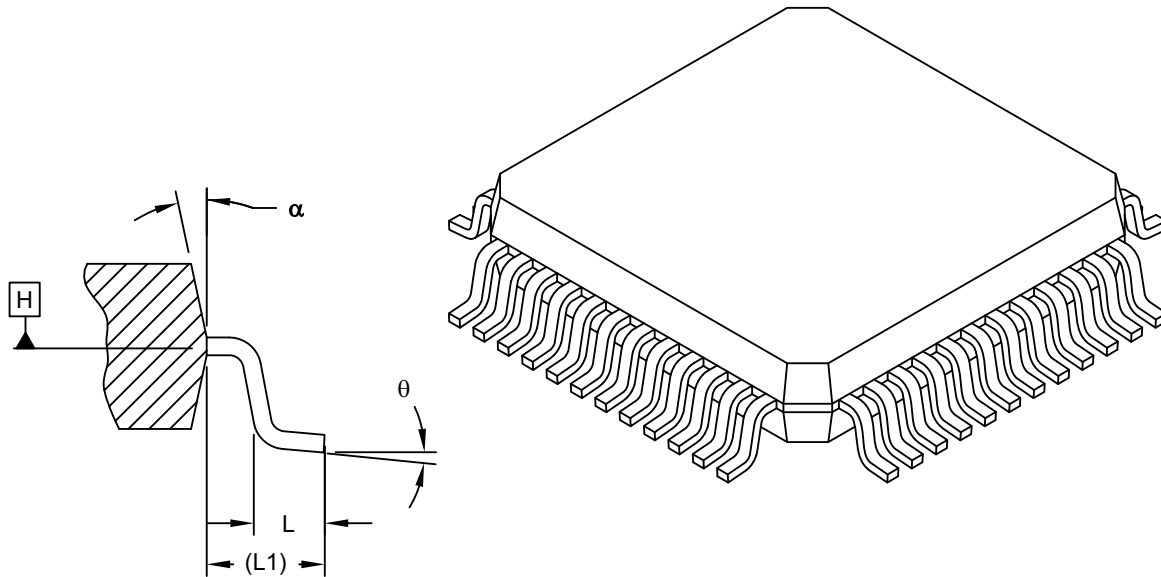
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



HV2605/HV2705

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



SECTION A-A

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	48		
Lead Pitch	e	0.50 BSC		
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	3.5°	7°
Overall Width	E	9.00 BSC		
Overall Length	D	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Molded Package Length	D1	7.00 BSC		
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

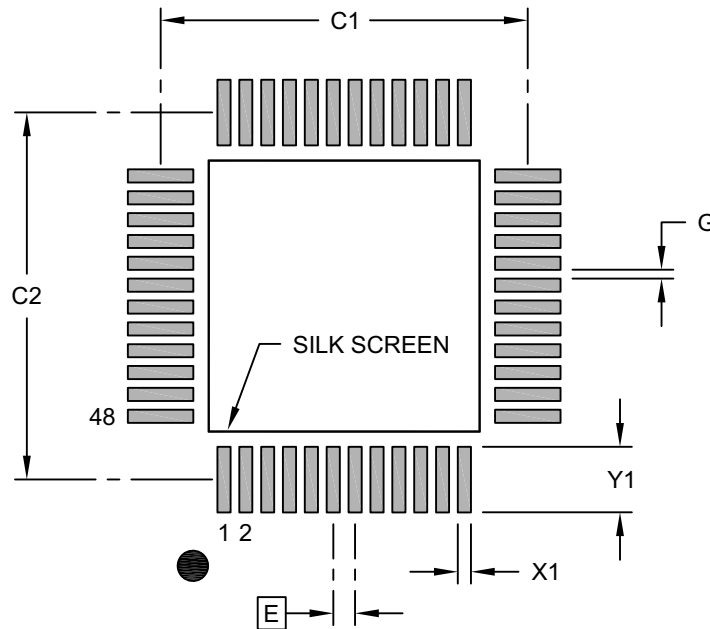
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-278A

HV2605/HV2705

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (May 2022)

- Minor layout changes.
- Added 48-Lead LQFP package notice to [Package Types†](#) and [Packaging Information†](#).

Revision B (August 2021)

- Added 48-Lead TQFP Package
- Updated table [Recommended Operating Conditions](#)
- Updated [Section 1.0 “Electrical Characteristics”](#)
- Updated [Section 4.0 “Packaging Information†”](#)

Revision A (November 2017)

- Converted Supertex Doc # DSFP-HV2605 and Doc # DSFP-HV2705-HV2706 to Microchip DS20005498C
- Removed HV2706 from the document. HV2706 is EOL.
- Combined HV2605 and HV2705 into one document
- Changed the package marking format
- Added information for 42-Ball Bumped Die package
- Removed the “HVCMOS technology for high performance” in the Features section
- Made minor text changes throughout the document

HV2605/HV2705

NOTES:

HV2605/HV2705

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	<u>-X</u>	<u>-XXXX</u>	Examples:
Device	Package	Environmental	Media Type	
Devices: HV2605 = 16-Channel Low Harmonic Distortion High-Voltage Analog Switch HV2705 = 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors				a) HV2605FG-G: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch, 48-lead LQFP Package, 250/Tray b) HV2605BD-M936: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch, 42-ball Bumped Die, 2500/Reel c) HV2705TQ-G: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors, 48-lead TQFP Package, 250 Tray d) HV2705FG-G-M931: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors, 48-lead LQFP Package, 1000/Reel
Packages: BD = 42-Ball Bumped Die FG = 48-lead LQFP TQ = 48-lead TQFP				
Environmental: G = Lead (Pb)-free/RoHS-compliant package (not used for BD packages)				
Media Types: (blank) = 250/Tray for FG package (blank) = 250/Tray for TQ package M931 = 1000/Reel for FG package M931 = 1600/Reel for TQ package M936 = 2500/Reel for BD package				

Note: HV2605BD and HV2705BD are RoHS-compliant products.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, QuietWire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017-2022, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-0324-5



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office

2355 West Chandler Blvd.

Chandler, AZ 85224-6199

Tel: 480-792-7200

Fax: 480-792-7277

Technical Support:

<http://www.microchip.com/support>

Web Address:

www.microchip.com

Atlanta

Duluth, GA

Tel: 678-957-9614

Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA

Tel: 774-760-0087

Fax: 774-760-0088

Chicago

Itasca, IL

Tel: 630-285-0071

Fax: 630-285-0075

Dallas

Addison, TX

Tel: 972-818-7423

Fax: 972-818-2924

Detroit

Novi, MI

Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN

Tel: 317-773-8323

Fax: 317-773-5453

Tel: 317-536-2380

Los Angeles

Mission Viejo, CA

Tel: 949-462-9523

Fax: 949-462-9608

Tel: 951-273-7800

Raleigh, NC

Tel: 919-844-7510

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110

Tel: 408-436-4270

Canada - Toronto

Tel: 905-695-1980

Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney

Tel: 61-2-9868-6733

China - Beijing

Tel: 86-10-8569-7000

China - Chengdu

Tel: 86-28-8665-5511

China - Chongqing

Tel: 86-23-8980-9588

China - Dongguan

Tel: 86-769-8702-9880

China - Guangzhou

Tel: 86-20-8755-8029

China - Hangzhou

Tel: 86-571-8792-8115

China - Hong Kong SAR

Tel: 852-2943-5100

China - Nanjing

Tel: 86-25-8473-2460

China - Qingdao

Tel: 86-532-8502-7355

China - Shanghai

Tel: 86-21-3326-8000

China - Shenyang

Tel: 86-24-2334-2829

China - Shenzhen

Tel: 86-755-8864-2200

China - Suzhou

Tel: 86-186-6233-1526

China - Wuhan

Tel: 86-27-5980-5300

China - Xian

Tel: 86-29-8833-7252

China - Xiamen

Tel: 86-592-2388138

China - Zhuhai

Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444

India - New Delhi

Tel: 91-11-4160-8631

India - Pune

Tel: 91-20-4121-0141

Japan - Osaka

Tel: 81-6-6152-7160

Japan - Tokyo

Tel: 81-3-6880-3770

Korea - Daegu

Tel: 82-53-744-4301

Korea - Seoul

Tel: 82-2-554-7200

Malaysia - Kuala Lumpur

Tel: 60-3-7651-7906

Malaysia - Penang

Tel: 60-4-227-8870

Philippines - Manila

Tel: 63-2-634-9065

Singapore

Tel: 65-6334-8870

Taiwan - Hsin Chu

Tel: 886-3-577-8366

Taiwan - Kaohsiung

Tel: 886-7-213-7830

Taiwan - Taipei

Tel: 886-2-2508-8600

Thailand - Bangkok

Tel: 66-2-694-1351

Vietnam - Ho Chi Minh

Tel: 84-28-5448-2100

EUROPE

Austria - Wels

Tel: 43-7242-2244-39

Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4485-5910

Fax: 45-4485-2829

Finland - Espoo

Tel: 358-9-4520-820

France - Paris

Tel: 33-1-69-53-63-20

Fax: 33-1-69-30-90-79

Germany - Garching

Tel: 49-8931-9700

Germany - Haan

Tel: 49-2129-3766400

Germany - Heilbronn

Tel: 49-7131-72400

Germany - Karlsruhe

Tel: 49-721-625370

Germany - Munich

Tel: 49-89-627-144-0

Fax: 49-89-627-144-44

Germany - Rosenheim

Tel: 49-8031-354-560

Israel - Ra'anana

Tel: 972-9-744-7705

Italy - Milan

Tel: 39-0331-742611

Fax: 39-0331-466781

Italy - Padova

Tel: 39-049-7625286

Netherlands - Drunen

Tel: 31-416-690399

Fax: 31-416-690340

Norway - Trondheim

Tel: 47-7288-4388

Poland - Warsaw

Tel: 48-22-3325737

Romania - Bucharest

Tel: 40-21-407-87-50

Spain - Madrid

Tel: 34-91-708-08-90

Fax: 34-91-708-08-91

Sweden - Gothenberg

Tel: 46-31-704-60-40

Sweden - Stockholm

Tel: 46-8-5090-4654

UK - Wokingham

Tel: 44-118-921-5800

Fax: 44-118-921-5820