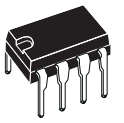
DUAL COMPARATOR AND VOLTAGE REFERENCE

COMPARATOR

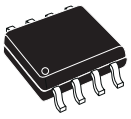
- LOW SUPPLY CURRENT (1.1mA) INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 25nA TYP
- LOW INPUT OFFSET VOLTAGE : ±1mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV TYP; (Io = 4mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE SUPPLY VOLTAGE
- WIDE POWER SUPPLY RANGE : ±1V to ±18V
- ESD PROTECTION : 1.5kV

VOLTAGE REFERENCE

- Fixed V_{ref} to 2.5V
- 0.4% AND 1% VOLTAGE PRECISION
- SINK CURRENT CAPABILITY : 1 to 100mA



N
DIP8



D
SO8

ORDER CODE

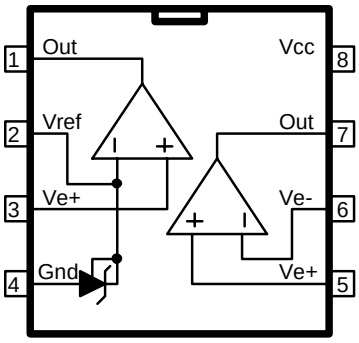
Part Number	Temperature Range	Package	
		N	D
TSM109	-40°C, +105°C	•	•
TSM109A	-40°C, +105°C	•	•

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

DESCRIPTION

The TSM109 is a monolithic IC that includes two comparators and a shunt voltage reference. This device offers space and cost savings in many applications including power supply management or data acquisition systems.

PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	36	V
V_{id}	Differential Input Voltage	36	V
V_{in}	Input Voltage	-0.3 to V_{cc} +0.3	V
Ik	Continuous Cathode current range	-100 to 150	mA
T_{oper}	Operating Free-air Temperature Range	-40 to105	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient (SO package)	175	°C/W
ESD	Electrostatic Discharge Protection	1.5	kV

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
I_{CC}	Total Supply Current, excluding current in the Voltage Reference				
	V_{CC} = +5V, no load		0.4	1	mA
	V_{CC} = +30V, no load		1	2.5	

ELECTRICAL CHARACTERISTICS

COMPARATOR (independent comparator)
V_{CC}^+ = +5V, V_{CC}^-= GND, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TSM109			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage - note 1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1	5 9	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		3	25 100	nA
I_{ib}	Input Bias Current (I^+ or I^-) - note 2) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		25	250 400	nA
A_{vd}	Large Signal Voltage Gain V_{CC} = 15V, R_L = 15kΩ, V_o = 1V to 11V	50	200		V/mV
V_{icm}	Input Common Mode Voltage Range - note 3) V_{CC} = 30V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	 0 0		 V_{CC}^+ -1.5 V_{CC}^+ -2	V
V_{id}	Differential Input Voltage -note 4)			V_{CC}^+	
V_{OL}	Low Level Output Voltage V_{id} = -1V, I_{sink} = 4mA T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		250	400 700	mV
I_{OH}	High Level Output Current (V_{id} = 1V) V_{CC} = V_o = 30V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		30	150 1	nA µA
I_{sink}	Output Sink Currrent V_{id}= 1V, V_o = 1.5V	10	20		mA
t_{re}	Response Time - note 5) R_L= 5.1kΩ connected to V_{CC}^+		1.3		µs
t_{rel}	Large Signal Response Time R_L= 5.1kΩ connected to V_{CC}^+, e_I = TTL, $V_{(ref)}$ = +1.4v		300		ns

1. At output switch point, $V_o \approx$ 1.4V, R_s = 0 with V_{CC}^+ from 5V to 30V, and over the full common-mode range (0V to V_{CC}^+ -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ -1.5V, but either or both inputs can go to +30V without damage.
4. Positive voltage excursions of one input may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide an appropriate output state. The low input voltage state must not be less than -0.3V (or 0.3V below the negative power supply, if used).
5. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals, 300ns can be obtained

COMPARATOR (comparator with inverting input connected to the internal Vref))
V_{CC}^+ = +5V, V_{CC}^-= GND, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TSM109			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage - note 1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1	5 9	mV
I_{ib}	Input Bias Current for positive input note 2) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		25	250 400	nA
A_{vd}	Large Signal Voltage Gain V_{CC} = 15V, R_L = 15kΩ, V_o = 1V to 11V	50	200		V/mV
V_{OL}	Low Level Output Voltage V_{id} = -1V, I_{sink} = 4mA T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		250	400 700	mV
I_{OH}	High Level Output Current (V_{id} = 1V) V_{CC} = V_o = 30V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		30	150 1	nA µA
I_{sink}	Output Sink Currrent V_{id}= 1V, V_o = 1.5V	10	20		mA
t_{re}	Response Time - note 3) R_L= 5.1kΩ connected to V_{CC}^+		1.3		µs
t_{rel}	Large Signal Response Time R_L= 5.1kΩ connected to V_{CC}^+, e_I = TTL, $V_{(ref)}$ = +1.4v		300		ns

1. At output switch point, $V_o \approx$ 1.4V, R_s = 0 with V_{CC}^+ from 5V to 30V, and over the full common-mode range (0V to V_{CC}^+ -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
3. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals, 300ns can be obtained.

ELECTRICAL CHARACTERISTICS

VOLTAGE REFERENCE

Symbol	Conditions	Value	Unit
I_K	Cathode Current	1 to 100	mA

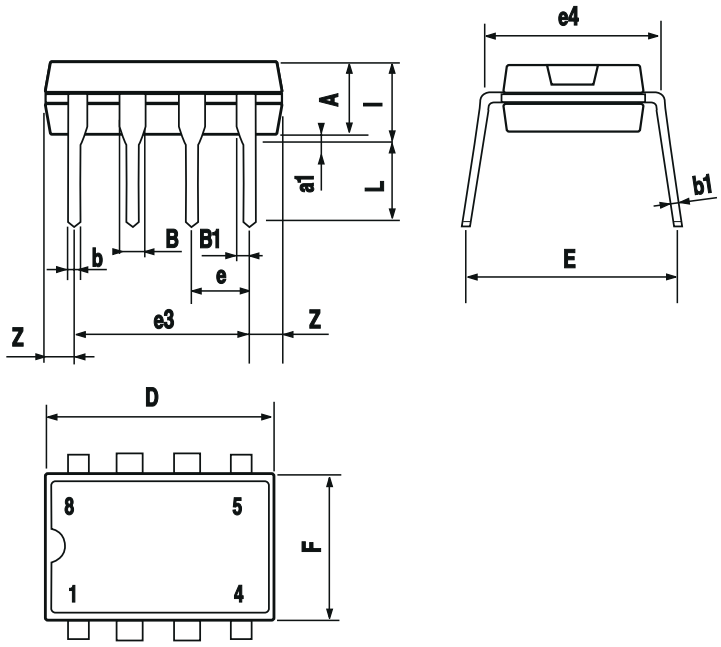
T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TSM109A			TSM109			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ref}	Reference Input Voltage, I_K = 10 mA T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	2.490 2.48	2.500	2.510 2.52	2.475 2.45	2.500	2.525 2.55	V
ΔV_{ref}	Reference Input Voltage Deviation OverTemperature Range I_K = 10 mA $T_{min} \le T_{amb} \le T_{max}$		7	30		7	30	mV
$\frac{\Delta Vref}{Vref \Delta T}$	Temperature Coefficient of Reference Input Voltage I_K = 10 mA, $T_{min} \le T_{amb} \le T_{max}$		±13	±90		±13	±90	ppm/°C
I_{min}	Minimum Cathode Current for Regulation		0.5	1		0.5	1	mA
$\|Z_{Vref}\|$	Dynamic Impedance - note 1) ΔV_{ref}, ΔI_K = 1 to 100mA, f < 1KHz		0.3	0.65		0.3	0.65	Ω

1. The dynamic impedance is defined as $[Z_{Vref}| = \Delta V_{Vref}/\Delta I_K$

PACKAGE MECHANICAL DATA

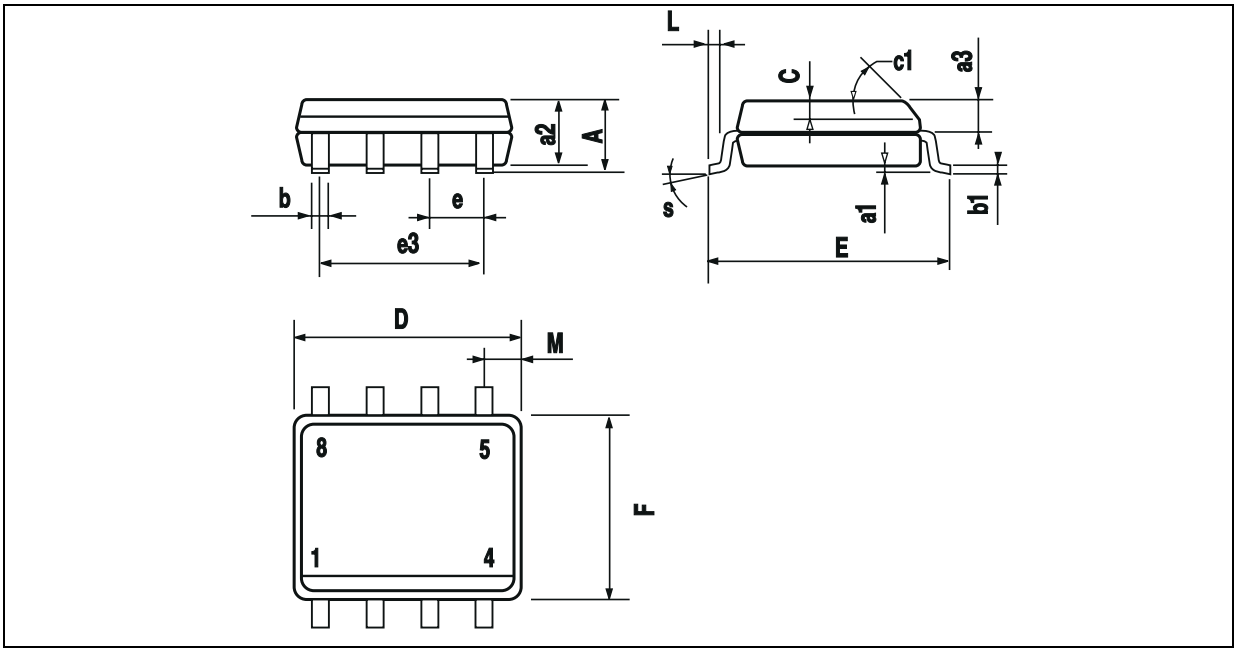
8 PINS - PLASTIC DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.100			0.043
A1	0.050	0.100	0.150	0.002	0.004	0.006
A2	0.780	0.860	0.940	0.031	0.034	0.037
b	0.250	0.330	0.400	0.010	0.013	0.016
c	0.130	0.180	0.230	0.005	0.007	0.009
D	2.900	3.000	3.100	0.114	0.118	0.122
E	4.750	4.900	5.050	0.187	0.193	0.199
E1	2.900	3.000	3.100	0.114	0.118	0.122
e		0.650			0.026	
L	0.400	0.550	0.700	0.016	0.022	0.028
L1		0.950			0.037	
k	0d	3d	6d	0d	3d	6d
aaa			0.100			0.004

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