Z86D73

40/44/48-Pin Low-Voltage IR OTP

Preliminary Product Specification

PS019402-1103

ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126-3432
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

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ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

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Features

Table 1 shows the features of the Z86D73.

Table 1. Features

Device	OTP (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86D73	32	236	31	2.0 V–3.6 V

Note: *General purpose

- Low power consumption–40 mW (typical)
- Three standby modes
  - Stop—2 µA (typical)
  - Halt—0.8 mA (typical)
  - Low voltage
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low-voltage detection with flag
- Programmable watch-dog/power-on reset circuits
- Two independent comparators with programmable interrupt polarity
- Mask selectable pull-up transistors on ports 0, 1, 2
- Programmable mask options
  - Oscillator selection: RC oscillator versus crystal or other clock source

- Oscillator operational mode: normal high-frequency operation enabled or 32-KHz operation enabled
- Port 0: 0–3 pull-ups
- Port 0: 4–7 pull-ups
- Port 1: 0–3 pull-ups
- Port 1: 4–7 pull-ups
- Port 2: 0–7 pull-ups
- Port 0: 0–3 mouse mode: normal mode (.5V_{DD} input threshold) versus mouse mode (.4V_{DD} input threshold)

Note: The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at V_{CC}=3 V and 450 KΩ ±50% at V_{CC}=2 V.

General Description

The Z86D73 is an OTP-based member of the MCU family of IR (infrared) microcontrollers. With 237 bytes of general-purpose RAM and 32 KB of ROM, ZiLOG's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86D73 architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86D73 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (see Figure 2).

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

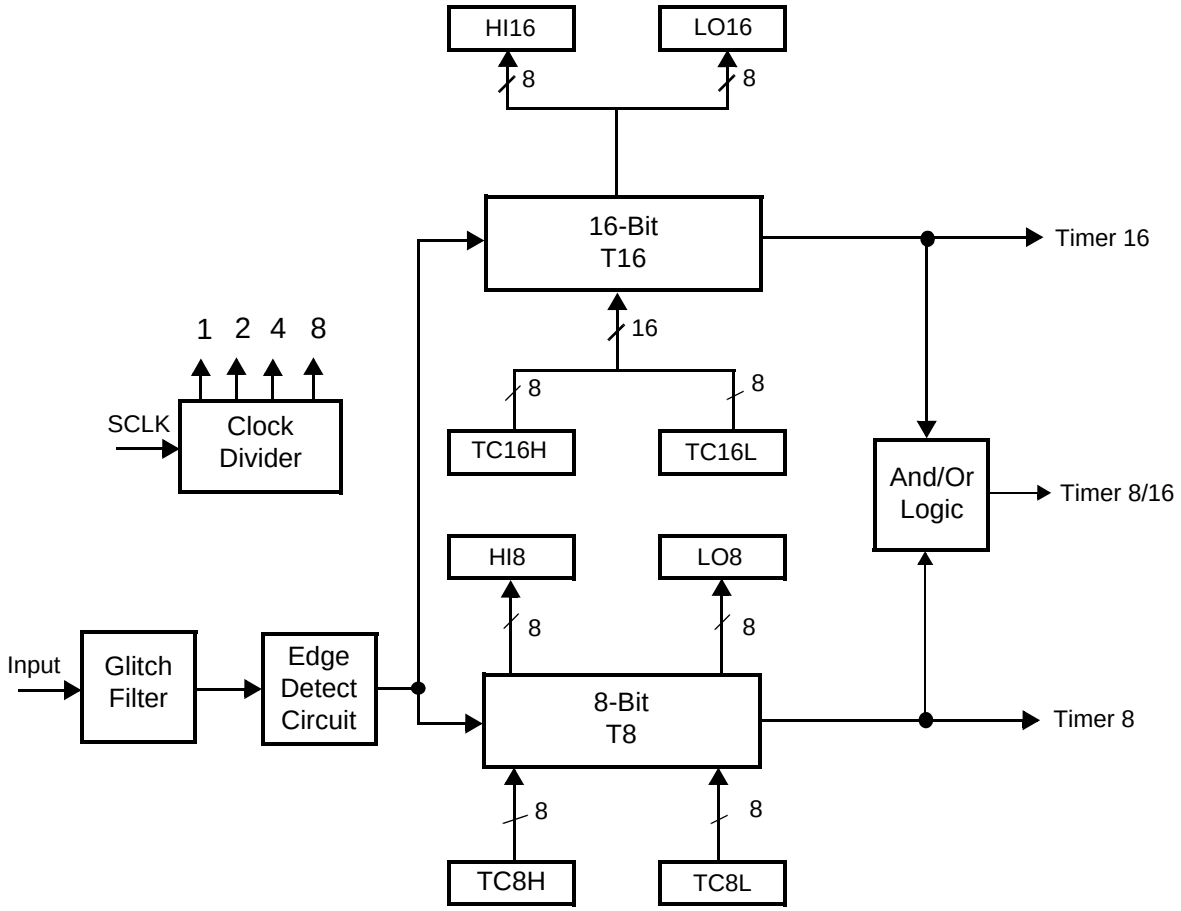


Figure 1. Counter/Timers Diagram

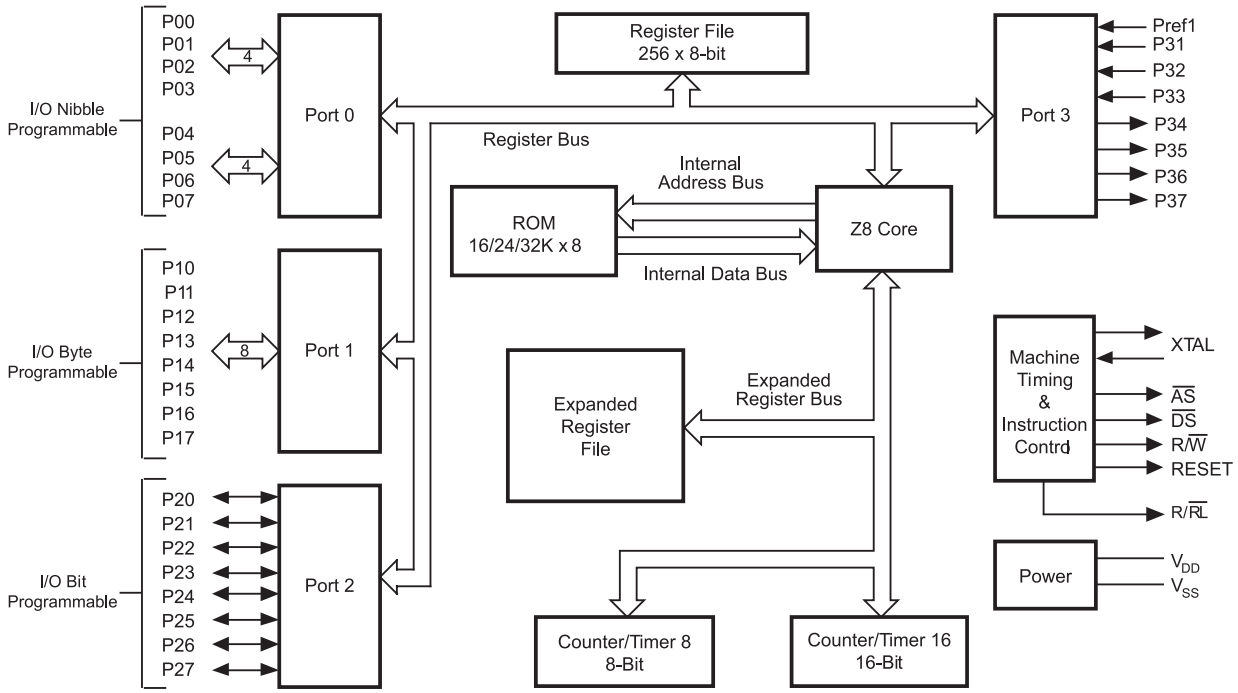


Figure 2. Functional Block Diagram

Pin Description

The pins are shown in Figure 3, Figure 4, Figure 5, and Figure 6. The pins are described in Table 3.

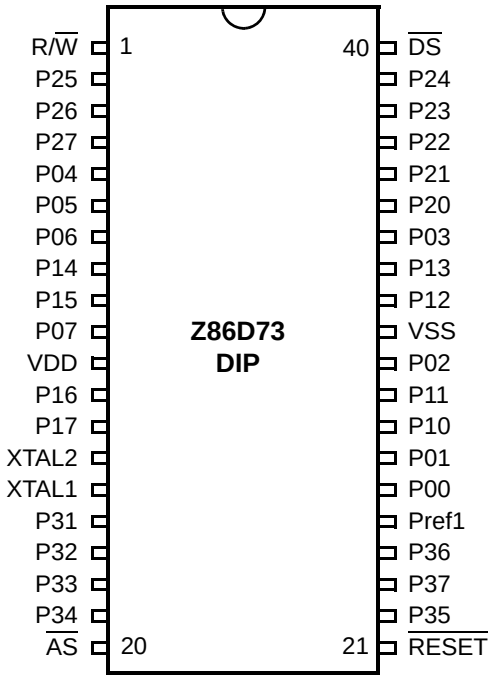


Figure 3. 40-Pin DIP Pin Assignment

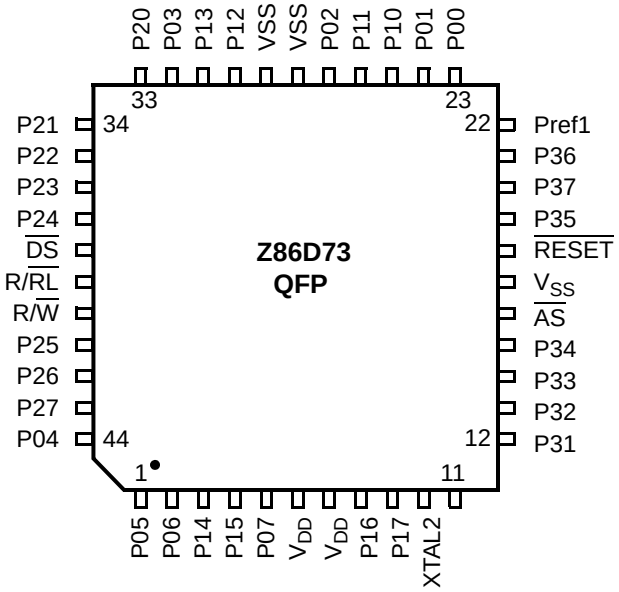


Figure 4. 44-Pin QFP Pin Assignment

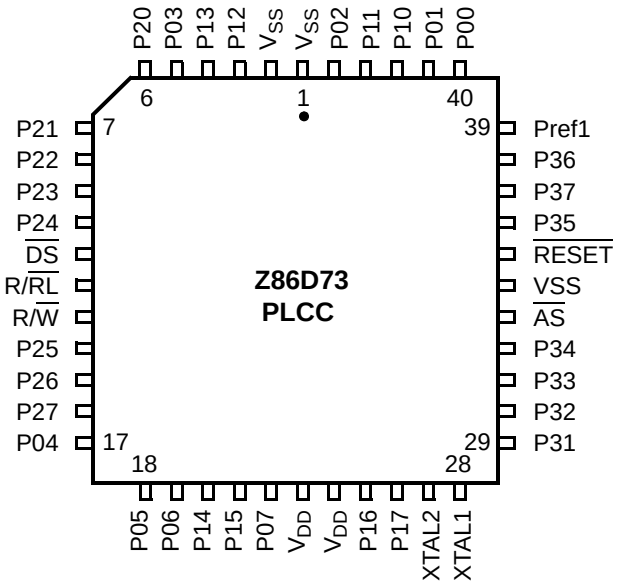


Figure 5. 44-Pin PLCC Assignment

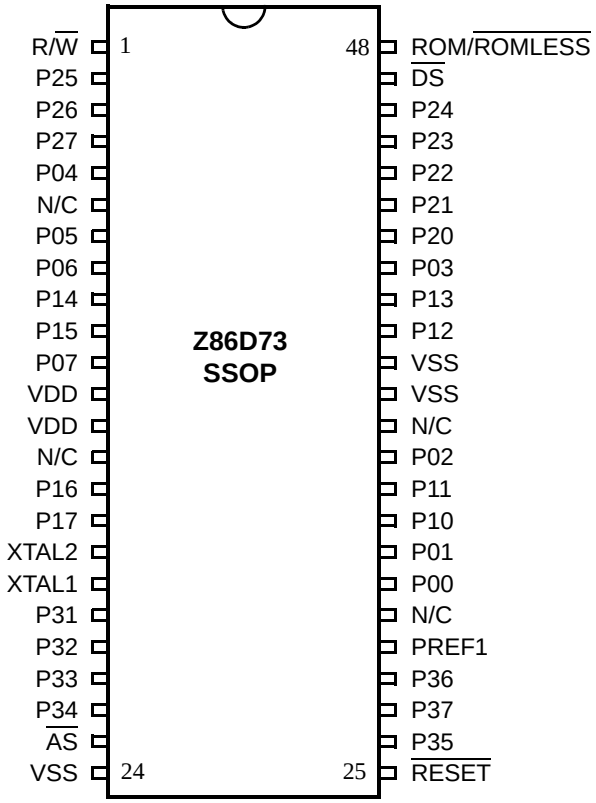


Figure 6. 48-Pin SSOP Assignment

Table 3. Pin Identification

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	48-Pin SSOP #	Symbol
26	40	23	31	P00
27	41	24	32	P01
30	44	27	35	P02
34	5	32	41	P03
5	17	44	5	P04
6	18	1	7	P05
7	19	2	8	P06
10	22	5	11	P07
28	42	25	33	P10

Table 3. Pin Identification (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	48-Pin SSOP #	Symbol
29	43	26	34	P11
32	3	30	39	P12
33	4	31	40	P13
8	20	3	9	P14
9	21	4	10	P15
12	25	8	15	P16
13	26	9	16	P17
35	6	33	42	P20
36	7	34	43	P21
37	8	35	44	P22
38	9	36	45	P23
39	10	37	46	P24
2	14	41	2	P25
3	15	42	3	P26
4	16	43	4	P27
16	29	12	19	P31
17	30	13	20	P32
18	31	14	21	P33
19	32	15	22	P34
22	36	19	26	P35
24	38	21	28	P36
23	37	20	27	P37
20	33	16	23	$\overline{AS}$
40	11	38	47	$\overline{DS}$
1	13	40	1	R/$\overline{W}$
21	35	18	25	$\overline{RESET}$
15	28	11	18	XTAL1
14	27	10	17	XTAL2
11	23, 24	6, 7	12, 13	V_{DD}

Table 3. Pin Identification (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	48-Pin SSOP #	Symbol
31	1, 2, 34	17, 28, 29	24, 37, 38	V_{SS}
25	39	22	29	Pref1
	12	39	48	R/$\overline{RL}$

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature.		†	C

Notes:
*Voltage on all pins with respect to GND.
†See Ordering Information on page 85.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

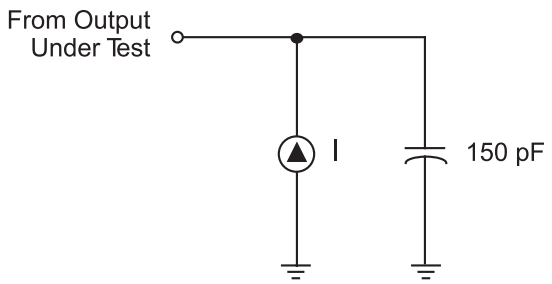


Figure 7. Test Load Diagram

Capacitance

The capacitances are listed in Table 5.

Table 5. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF
Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

Table 6. DC Characteristics

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
	Max Input Voltage	2.0 V		7	V	I_{IN} <250 µA	
		3.6 V		7	V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	2.0 V	0.8 V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
		3.6 V	0.8 V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
		3.6 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0 V	0.7 V_{CC}	V_{CC}+0.3	V		
		3.6 V	0.7 V_{CC}	V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0 V	V_{SS}–0.3	0.2 V_{CC}	V		
		3.6 V	V_{SS}–0.3	0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
		3.6 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
		3.6 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0 V		0.4	V	I_{OL} = 1.0 mA	
		3.6 V		0.4	V	I_{OL} = 4.0 mA	
V_{OL2*}	Output Low Voltage	2.0 V		0.8	V	I_{OL} = 5.0 mA	
		3.6 V		0.8	V	I_{OL} = 7.0 mA	
V_{OL2}	Output Low Voltage	2.0 V		0.8	V	I_{OL} = 10 mA	
	(P00, P01, P36, P37)	3.6 V		0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input	2.0 V		25	mV		
	Offset Voltage	3.6 V		25	mV		
V_{REF}	Comparator Reference	2.0 V	0	V_{DD}–1.75	mV		
	Voltage	3.6 V	0	V_{DD}–1.75	mV		
I_{IL}	Input Leakage	2.0 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
		3.6 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	

Table 6. DC Characteristics (Continued)

		T_A = 0°C to +70°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
I_{OL}	Output Leakage	2.0 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
		3.6 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
I_{CC}	Supply Current	2.0 V		10	mA	at 8.0 MHz	1, 2
		3.6 V		15	mA	at 8.0 MHz	1, 2
		2.0 V		250	µA	at 32 kHz	1, 2, 3
		3.6 V		850	µA	at 32 kHz	1, 2, 3
I_{CC1}	Standby Current (HALT Mode)	2.0 V		3	mA	V_{IN} = 0 V, V_{CC} at 8.0 MHz	1, 2
		3.6 V		5	mA	Same as above	1, 2
		2.0 V		2	mA	Clock Divide-by-16 at 8.0 MHz	1, 2
		3.6 V		4	mA	Same as above	1, 2
I_{CC2}	Standby Current (STOP Mode)	2.0 V		8	µA	V_{IN} = 0 V, V_{CC} WDT is not Running	4, 5
	Note: WDT, Comparators, Low Voltage Detection, and ADC (if applicable are disabled. The IC might draw more current if any of the above peripherals is enabled.	3.6 V		10	µA	Same as above	4, 5
		2.0 V		500	µA	V_{IN} = 0 V, V_{CC} WDT is Running	4, 5
		3.6 V		800	µA	Same as above	4, 5
I_{CC2}	Standby Current (Low Voltage)			25	µA	$V_{CC} < V_{BO}$	6
					µA		
T_{POR}	Power-On Reset	2.0 V	12	75	ms		
		3.6 V	5	20	ms		
V_{BO}	V_{CC} Low Voltage Protection			2.15	V	8 MHz max Ext. CLK Freq.	7
V_{LVD}	Vcc Low Voltage Detection			V_{BO} + 0.4	V	$V_{LVD} = V_{BO}$ + 0.4	8

Notes:

*All outputs excluding P00, P01, P36, and P37.

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. 32-kHz clock driver input.
4. The V_{BO} increases as the temperature decreases, except inputs at V_{CC}.
5. Oscillator stopped.
6. Oscillator stops when V_{CC} falls below V_{LV} limit.
7. V_{BO} increases as the temperature decreases.
8. Variance is 300 mV.

AC Characteristics

Figure 9 and Table 8 describe the external I/O or memory read and write timing.

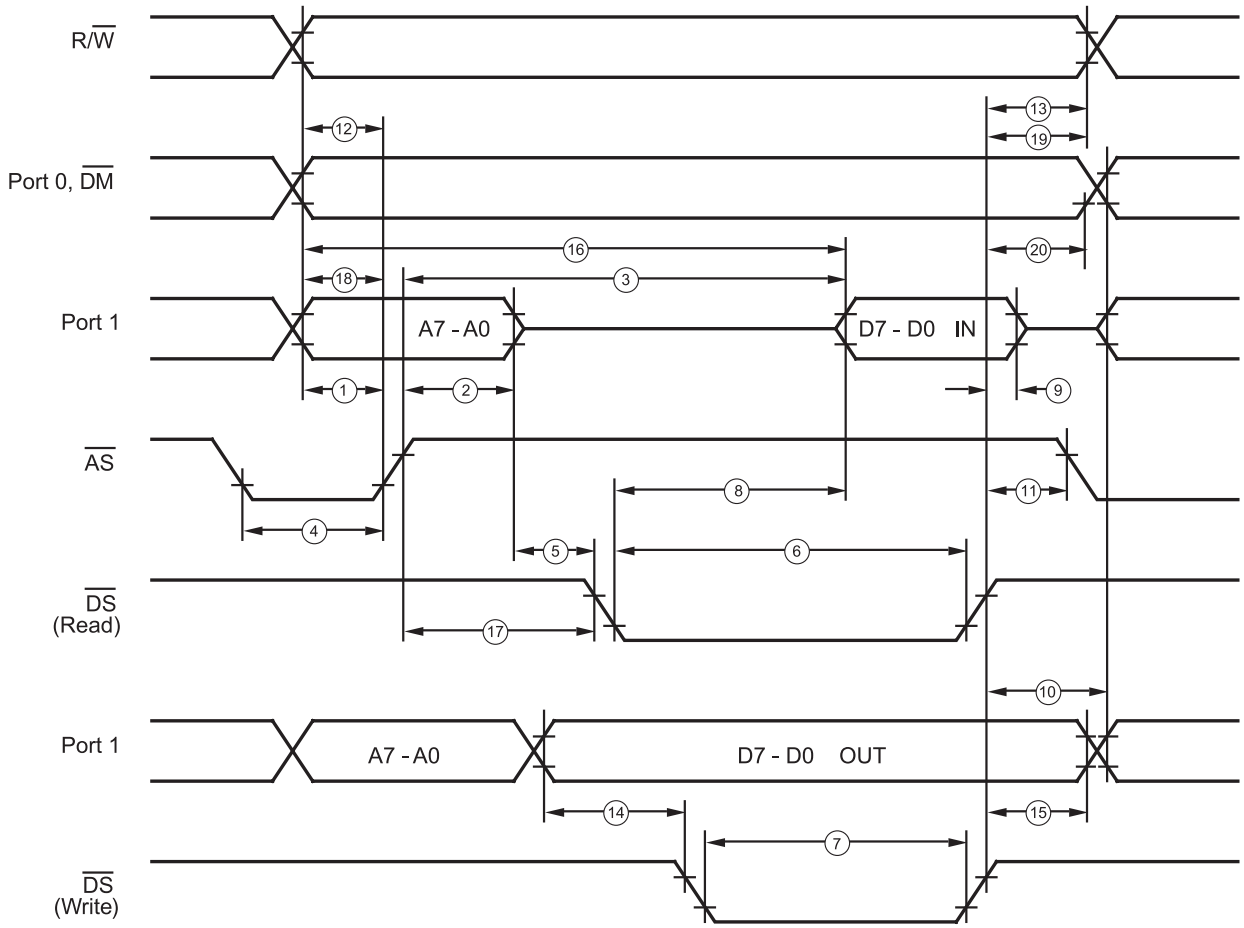


Figure 8. External I/O or Memory Read/Write Timing

Table 7. External I/O or Memory Read and Write Timing (Preliminary)

				T_A = 0 °C to +70 °C 8.0 MHz*			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rising Delay	2.0 V 3.6 V	55 55		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rising to Address Float Delay	2.0 V 3.6 V	70 70		ns ns	2 2
3	TdAS(DR)	$\overline{AS}$ Rising to Read Data Required Valid	2.0 V 3.6 V		400 400	ns ns	1, 2
4	TwAS	$\overline{AS}$ Low Width	2.0 V 3.6 V	80 80		ns ns	2
5	Td	Address Float to $\overline{DS}$ Falling	2.0 V 3.6 V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	2.0 V 3.6 V	300 300		ns ns	1, 2
7	TwDSW	$\overline{DS}$ (Write) Low Width	2.0 V 3.6 V	165 165		ns ns	1, 2
8	TdDSR(DR)	$\overline{DS}$ Falling to Read Data Required Valid	2.0 V 3.6 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rising Hold Time	2.0 V 3.6 V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rising to Address Active Delay	2.0 V 3.6 V	85 95		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rising to $\overline{AS}$ Falling Delay	2.0 V 3.6 V	60 70		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rising Delay	2.0 V 3.6 V	70 70		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rising to R/$\overline{W}$ Not Valid	2.0 V 3.6 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Falling (Write) Delay	2.0 V 3.6 V	80 80		ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rising to Write Data Not Valid Delay	2.0 V 3.6 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	2.0 V 3.6 V		475 475	ns ns	1, 2

Table 7. External I/O or Memory Read and Write Timing (Preliminary) (Continued)

				T_A = 0 °C to +70 °C 8.0 MHz*			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
17	TdAS(DS)	$\overline{AS}$ Rising to $\overline{DS}$ Falling Delay	2.0 V 3.6 V	100 100		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Falling Delay	2.0 V 3.6 V	55 55		ns ns	2
19	TdDS(DM)	$\overline{DS}$ Rise to $\overline{DM}$ Valid Delay	2.0 V 3.6 V	70 70		ns ns	
20	ThDS(A)	$\overline{DS}$ Rise to Address Valid Hold Time	2.0 V 3.6 V	70 70		ns	

Notes:
1.When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
* Standard Test Load: All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

Figure 9 and Table 8 describe additional timing characteristics.

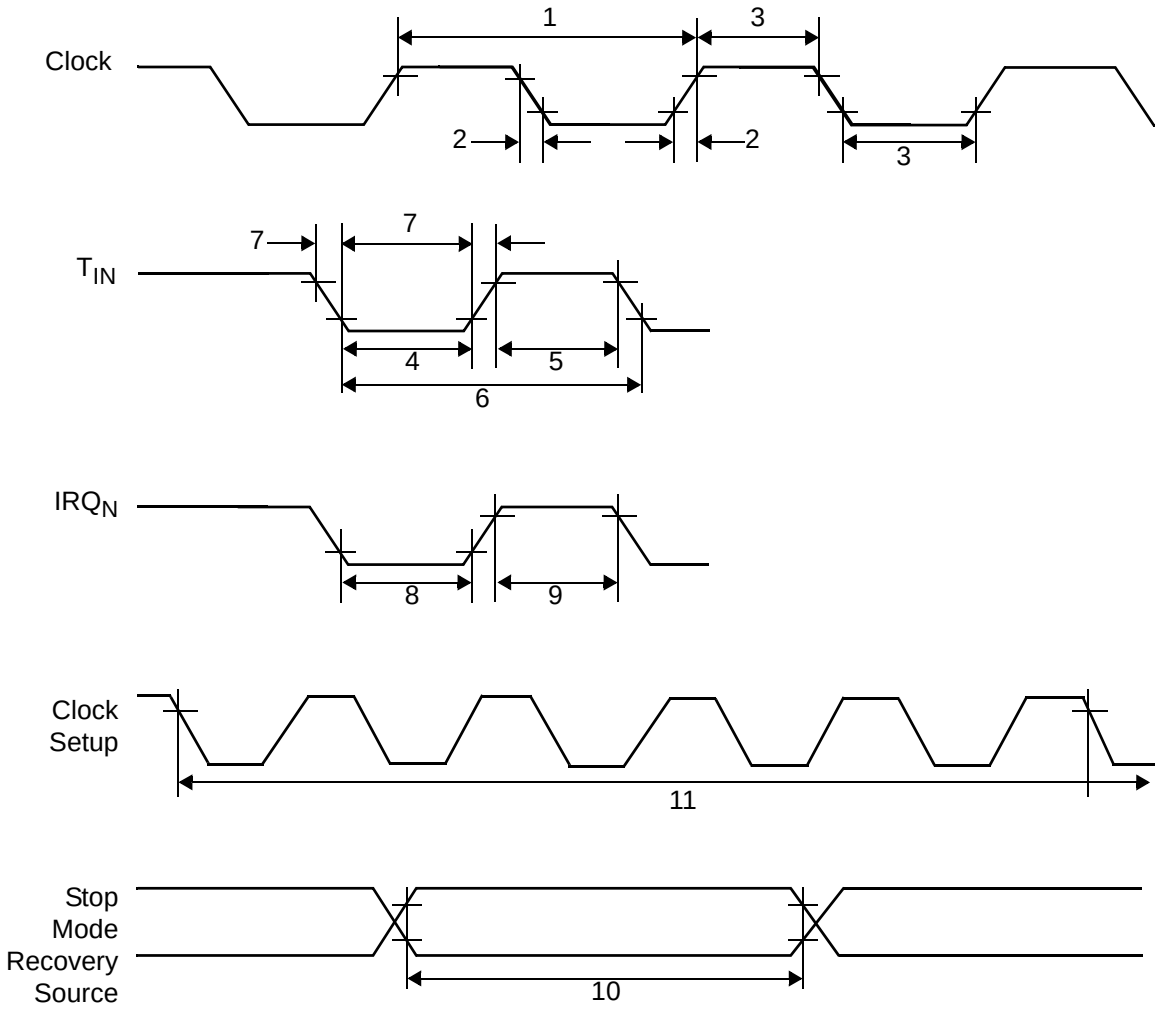


Figure 9. Additional Timing

Table 8. Additional Timing

				T_A = 0 °C to +70 °C 8.0 MHz				Stop-Mode Recovery
No	**Sym**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**	**(D1, D0)**
1	TpC	Input Clock Period	2.0 V	121	DC	ns	1	
			3.6 V	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0 V		25	ns	1	
			3.6 V		25	ns	1	
3	TwC	Input Clock Width	2.0 V	37		ns	1	
			3.6 V	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 V	100		ns	1	
			3.6 V	70		ns	1	
5	TwTinH	Timer Input High Width	2.0 V	3TpC			1	
			3.6 V	3TpC			1	
6	TpTin	Timer Input Period	2.0 V	8TpC			1	
			3.6 V	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0 V		100	ns	1	
			3.6 V		100	ns	1	
8A	TwIL	Interrupt Request Low Time	2.0 V	100		ns	1, 2	
			3.6 V	70		ns	1, 2	
8B	TwIL	Interrupt Request Low Time	2.0 V	5TpC			1, 3	
			3.6 V	5TpC			1, 3	
9	TwIH	Interrupt Request Input High Time	2.0 V	5TpC			1, 2	
			3.6 V	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0 V	12		ns		
			3.6 V	12		ns		
11	Tost	Oscillator Start-Up Time	2.0 V		5TpC		4	
			3.6 V		5TpC		4	

Table 8. Additional Timing (Continued)

				T_A = 0 °C to +70 °C 8.0 MHz				Stop-Mode Recovery
No	**Sym**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**	**(D1, D0)**
12	Twdt	Watch-Dog Timer	2.0 V	12		ms	5	0, 0
		Delay Time	3.6 V	5		ms	5	
			2.0 V	25		ms	5	0, 1
			3.6 V	10		ms	5	
			2.0 V	50		ms	5	1, 0
			3.6 V	20		ms	5	
			2.0 V	200		ms	5	1, 1
			3.6 V	80		ms	5	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0.
5. For internal RC oscillator.

Pin Functions

$\overline{DS}$ (Output, Active Low)

The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid.

$\overline{AS}$ (Output, Active Low)

Address Strobe is pulsed one time at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ Read/Write (Output, Write Low)

The R/$\overline{W}$ signal is Low when the CCP is writing to the external program or data memory.

R/$\overline{RL}$ (Input)

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble), depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode (if selected as an address output), along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ through P3M bits D4 and D3 (see Figure 10).

A ROM mask option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This option allows direct interface to mouse/trackball IR sensors.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

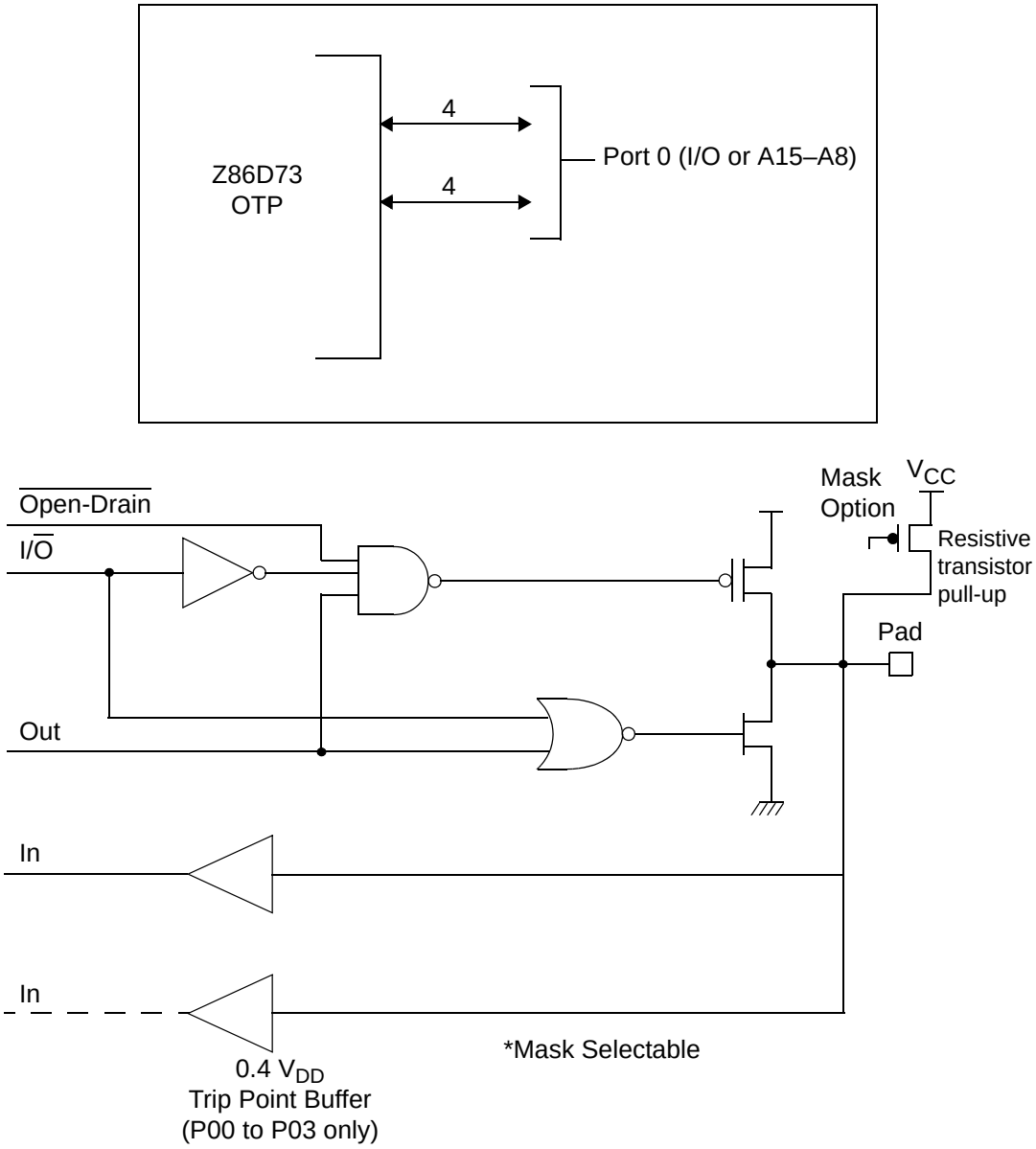


Figure 10. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 11) is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) lines and by the Read/Write (R/$\overline{W}$) and Data Memory (DM) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86D73 to share common resources in multiprocessor and DMA applications. Port 1 can also be configured for standard port output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

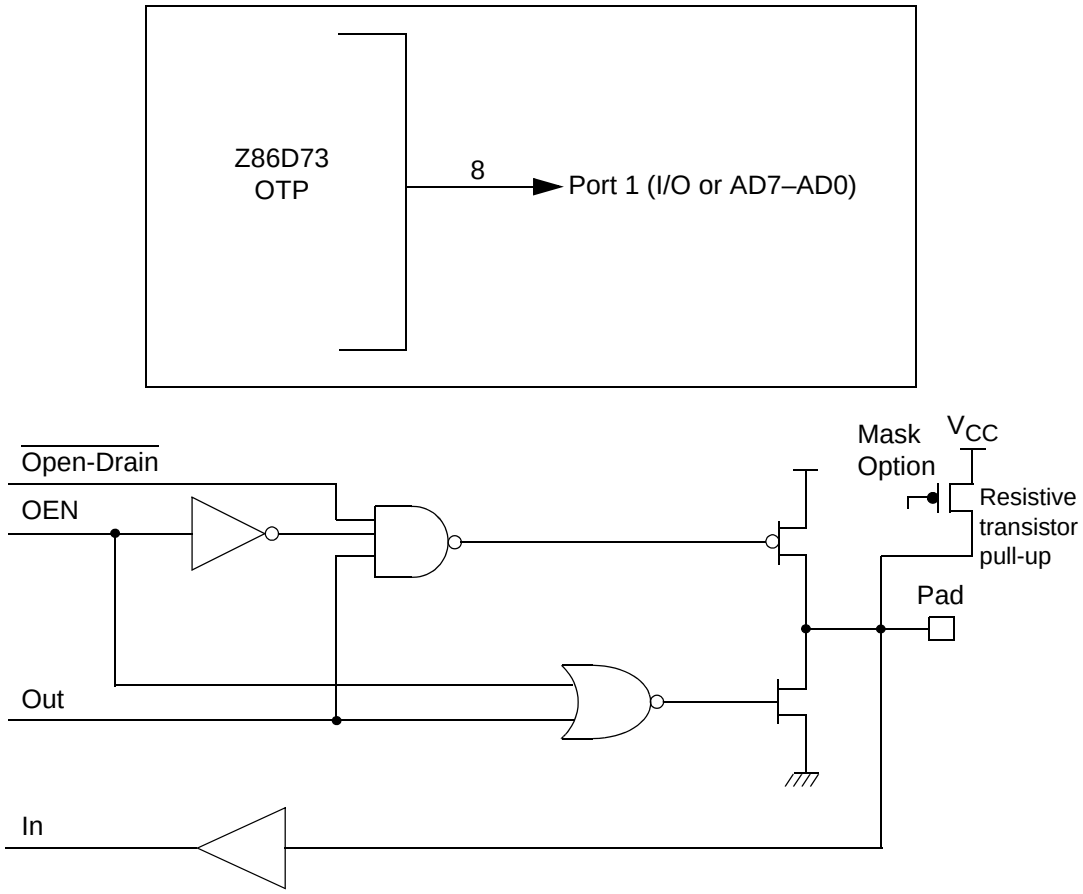


Figure 11. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 12). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

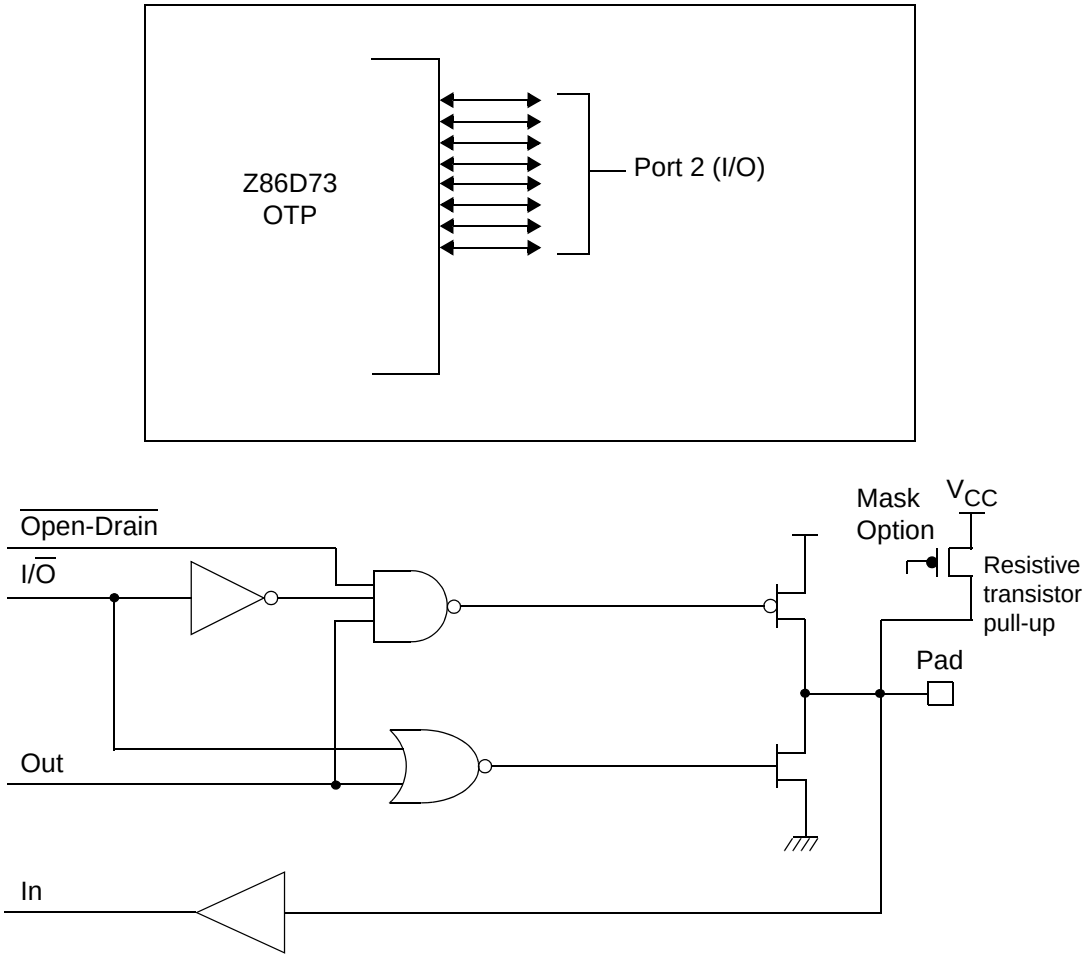


Figure 12. Port 2 Configuration

Port 3 (P37–P31)

Port 3 is a 7-bit, CMOS-compatible fixed I/O port (see Figure 13). Port 3 consists of three fixed input (P33–P31) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

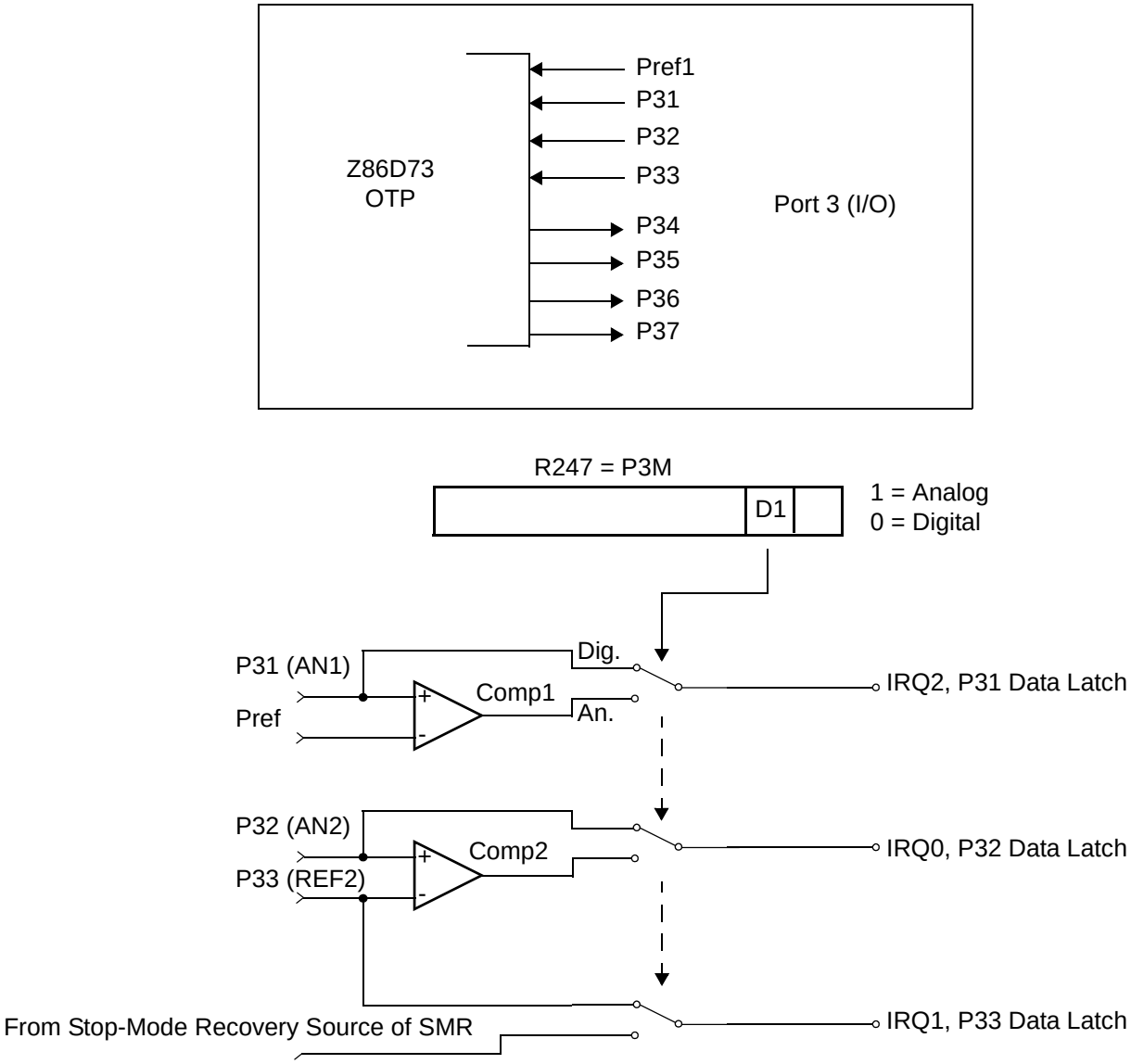


Figure 13. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “CTR1(D)01h” on page 37). Other edge detect and IRQ modes are described in Table 9.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 9. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 14). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

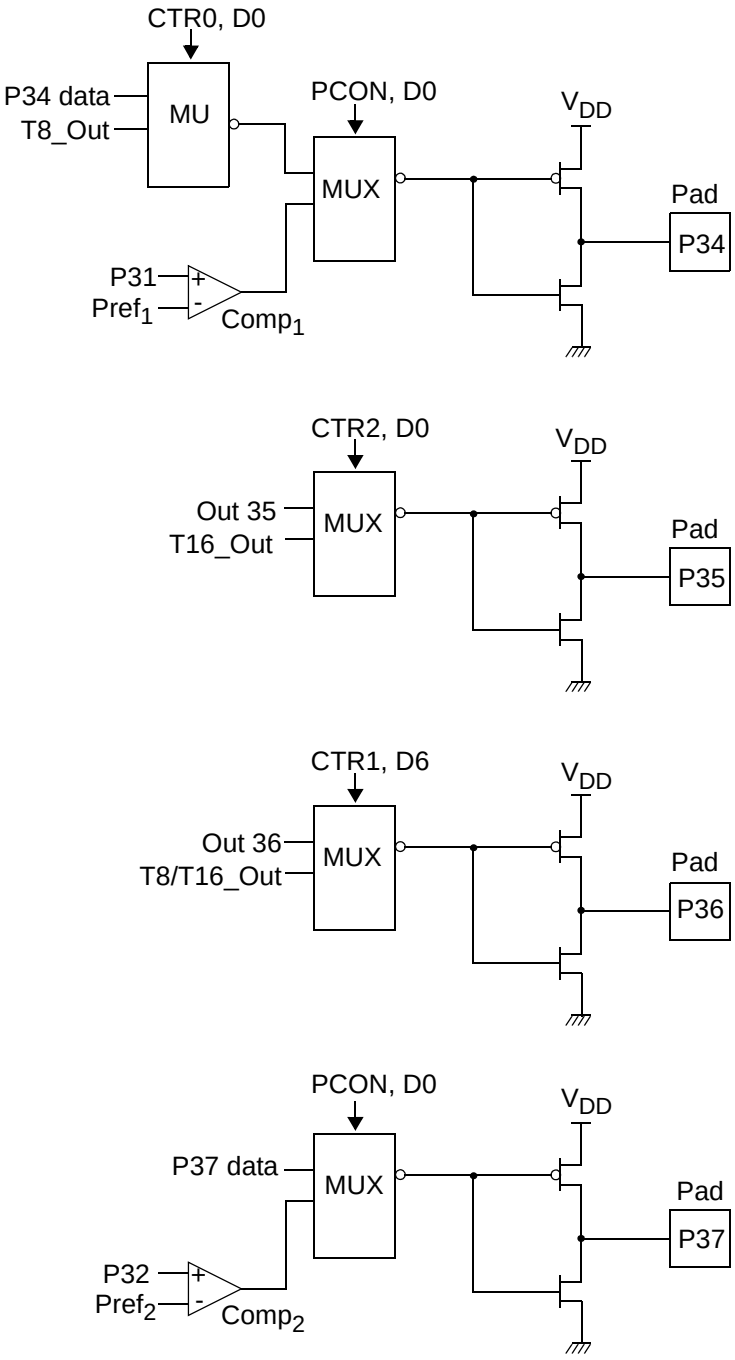


Figure 14. Port 3 Counter/Timer Output Configuration

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 13 on page 23. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

$\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line need to be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

Functional Description

The Z86D73 incorporates special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Program Memory

The Z86D73 addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors that correspond to the five available interrupts.

RAM

The Z86D73 device features 256 bytes of RAM. See Figure 15.

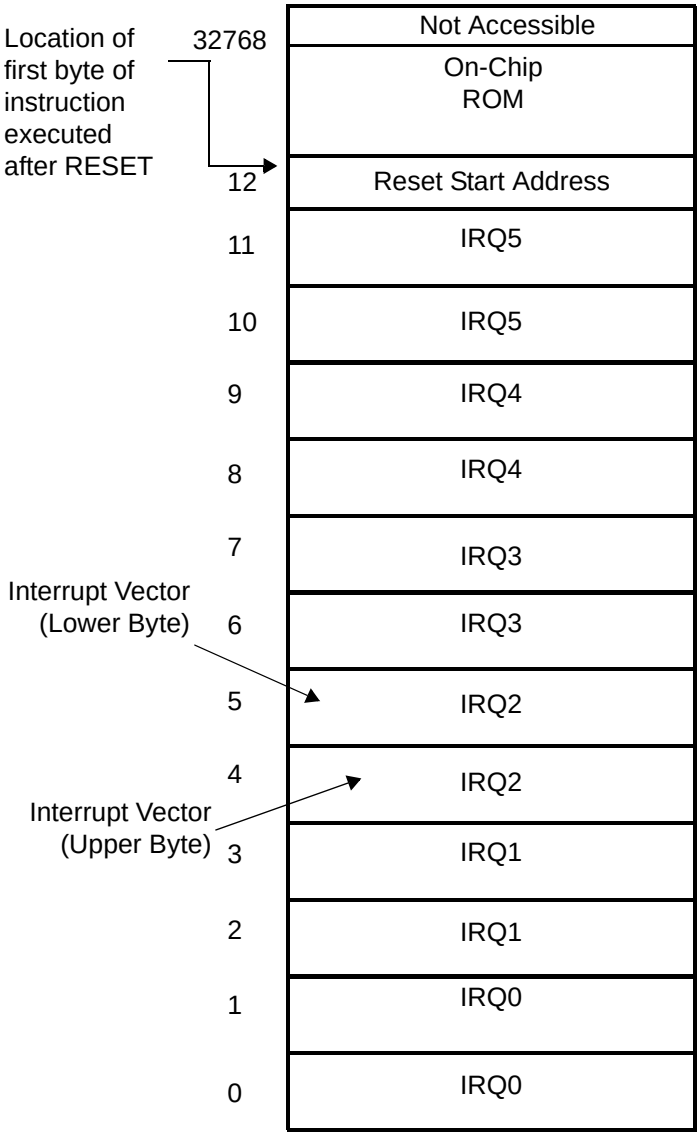


Figure 15. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: An expanded register bank is also referred to as an expanded register group (see Figure 16).

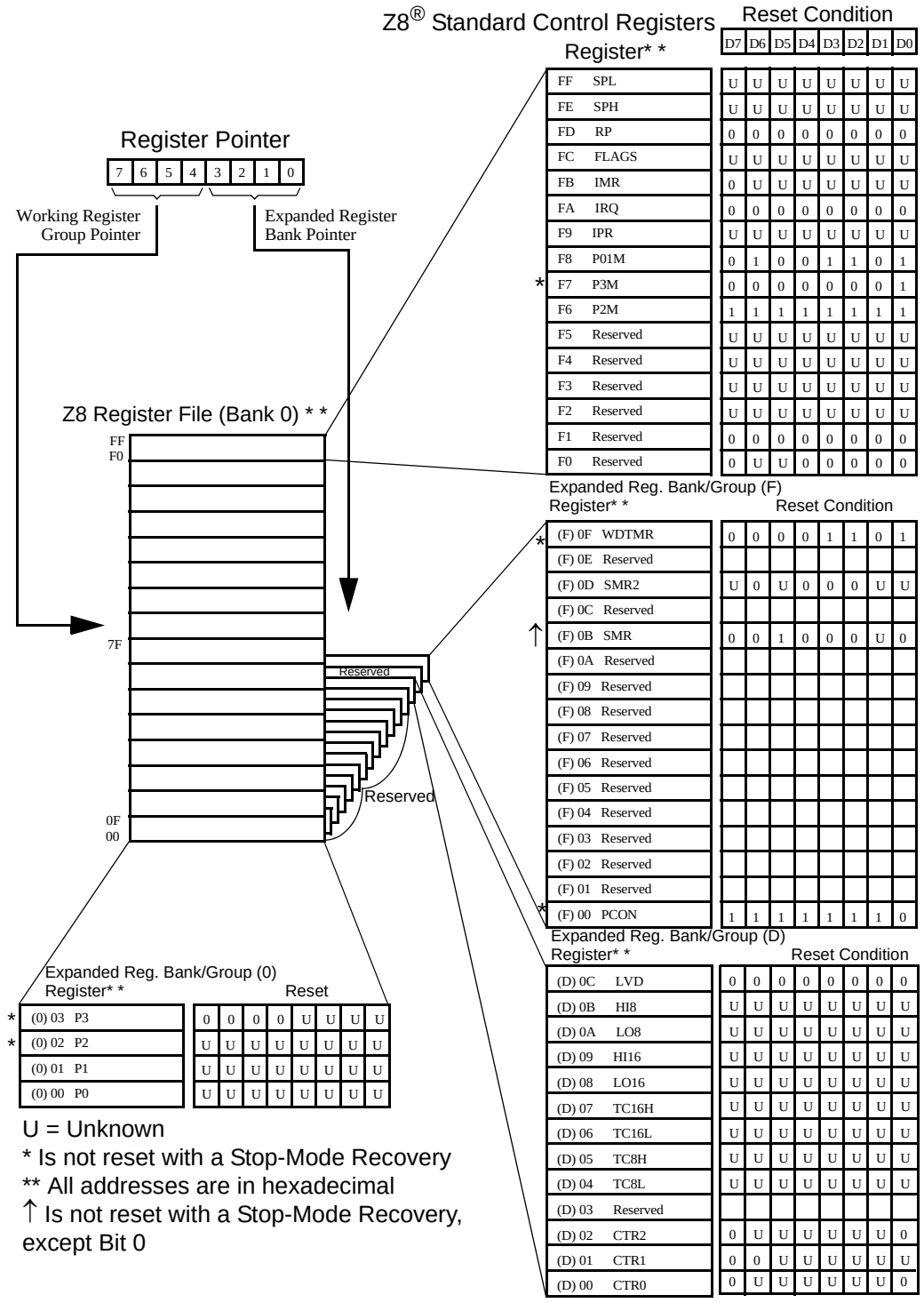


Figure 16. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 17) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z86D73 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from `1h` to `Fh` exchanges the lower 16 registers to an expanded register bank.

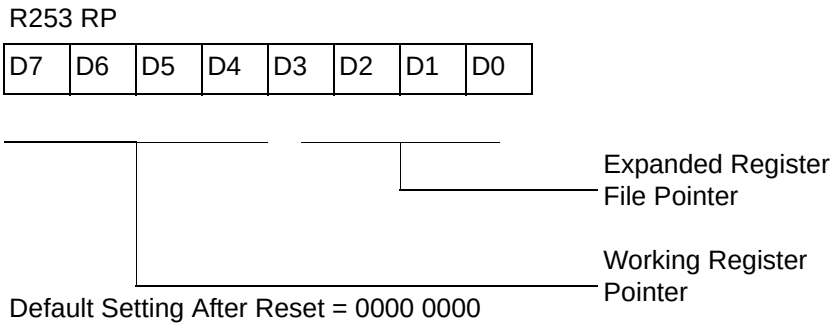


Figure 17. Register Pointer

Example: Z86D73: (See Figure 16 on page 29)

R253 RP = 00h
- R0 = Port 0
- R1 = Port 1
- R2 = Port 2
- R3 = Port 3

But if:

R253 RP = 0Dh
- R0 = CTRL0
- R1 = CTRL1
- R2 = CTRL2
- R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD    RP, #0Dh     ; Select ERF D for access to bank D
                   ; (working register group 0)
LD    R0,#xx       ; load CTRL0
LD    1, #xx       ; load CTRL1
LD    R1, 2        ; CTRL2→CTRL1
```

```
LD    RP, #0Dh     ; Select ERF D for access to bank D
                   ; (working register group 0)
LD    RP, #7Dh     ; Select expanded register bank D and working
                   ; register group 7 of bank 0 for access.
LD    71h, 2       ; CTRL2→register 71h
LD    R1, 2        ; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 10) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 18). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

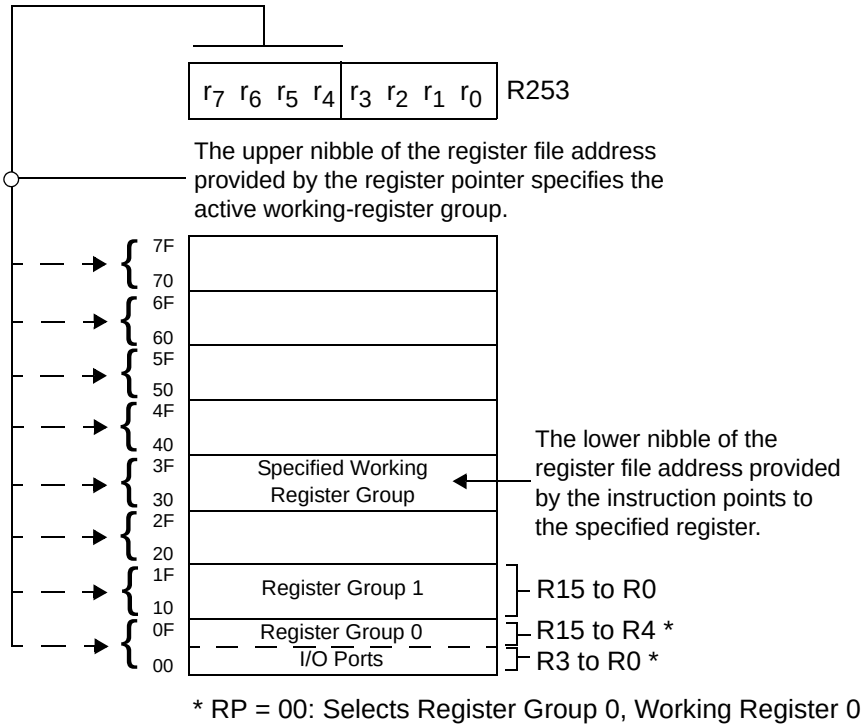


Figure 18. Register Pointer—Detail

Stack

The Z86D73 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed

Table 10. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

Register Description

LVD(D)0Ch Low-Voltage Detection Register

Note: The LVD flag will be valid after enabling the detection for 20 µS (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Field	Bit Position			Description
LVD	765432--			Reserved No Effect
	------1-	R	1 0*	LV flag set LV flag reset
	-------0	R/W	1 0*	Enable LVD Disable LVD

*Default after POR

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

HI8(D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register is used to hold the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	76543210	R W	Captured Data No Effect

L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register is used to hold the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	76543210	R W	Captured Data No Effect

HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/ Timer16. this register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)07h Counter/Timer2 MS-Byte Hold Register

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Counter/Timer2 LS-Byte Hold Register

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h Counter/Timer8 High Hold Register

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h Counter/Timer8 Low Hold Register

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

CTR0 Counter/Timer8 Control Register

Table 11 lists and briefly describes the fields for this register.

Table 11. CTR0 (D)00 Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:
***Indicates the value upon Power-On Reset.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to its location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Therefore, reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

Example

When the status of bit 5 is 1, a timer reset condition occurs.

T8 Clock

This bit defines the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)01h

This register controls the functions in common with the T8 and T16.

Table 12 lists and briefly describes the fields for this register.

Table 12. CTR(D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode Demodulation Mode
P36_Out/ Demodulator_Input	-6------	R/W		**Transmit Mode**
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/ Edge _Detect	--54----	R/W		**Transmit Mode**
			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/ Glitch_Filter	----32--	R/W		**Transmit Mode**
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	------1-			**Transmit Mode**
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Table 12. CTR(D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Initial_T16_Out/ Falling_Edge	-------0			**Transmit Mode**
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If the result is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/ Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the Ping-Pong mode or in independent normal operation mode. Setting this field to “Normal Operation Mode” terminates the “Ping-Pong Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This

ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register

Table 13 lists and briefly describes the fields for this register.

Table 13. CTR2 (D)02h: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		**Transmit Mode**
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Timeout
			1	Counter Timeout Occurred
		W	0	No Effect
			1	Reset Flag to 0

Table 13. CTR2 (D)02h: Counter/Timer16 Control Register (Continued)

Field	Bit Position		Value	Description
T16 _Clock	---43---	R/W	00 01 10 11	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0 1	Disable Data Capture Int. Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Timeout Int. Enable Timeout Int.
P35_Out	-------0	R/W	0* 1	P35 as Port Output T16 Output on P35

Note:
*Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In Transmit Mode, when set to 0, the counter reloads the initial value when the terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 50.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2 Stop-Mode Recovery Register 2

Table 14 lists and briefly describes the fields for this register.

Table 14. SMR2(F)0Dh: Stop-Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0†	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Port pins configured as outputs are ignored as a SMR recovery source.
† Indicates the value upon Power-On Reset

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 19).

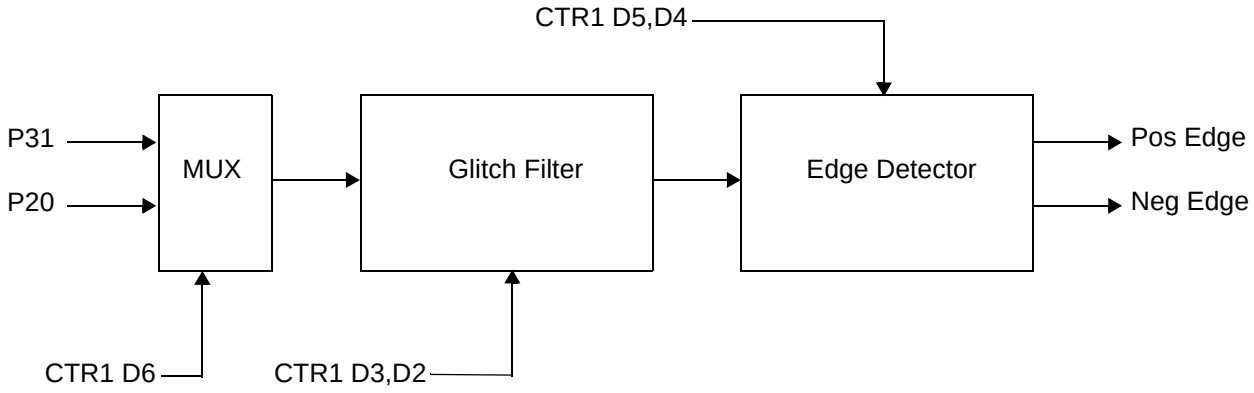


Figure 19. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 20.

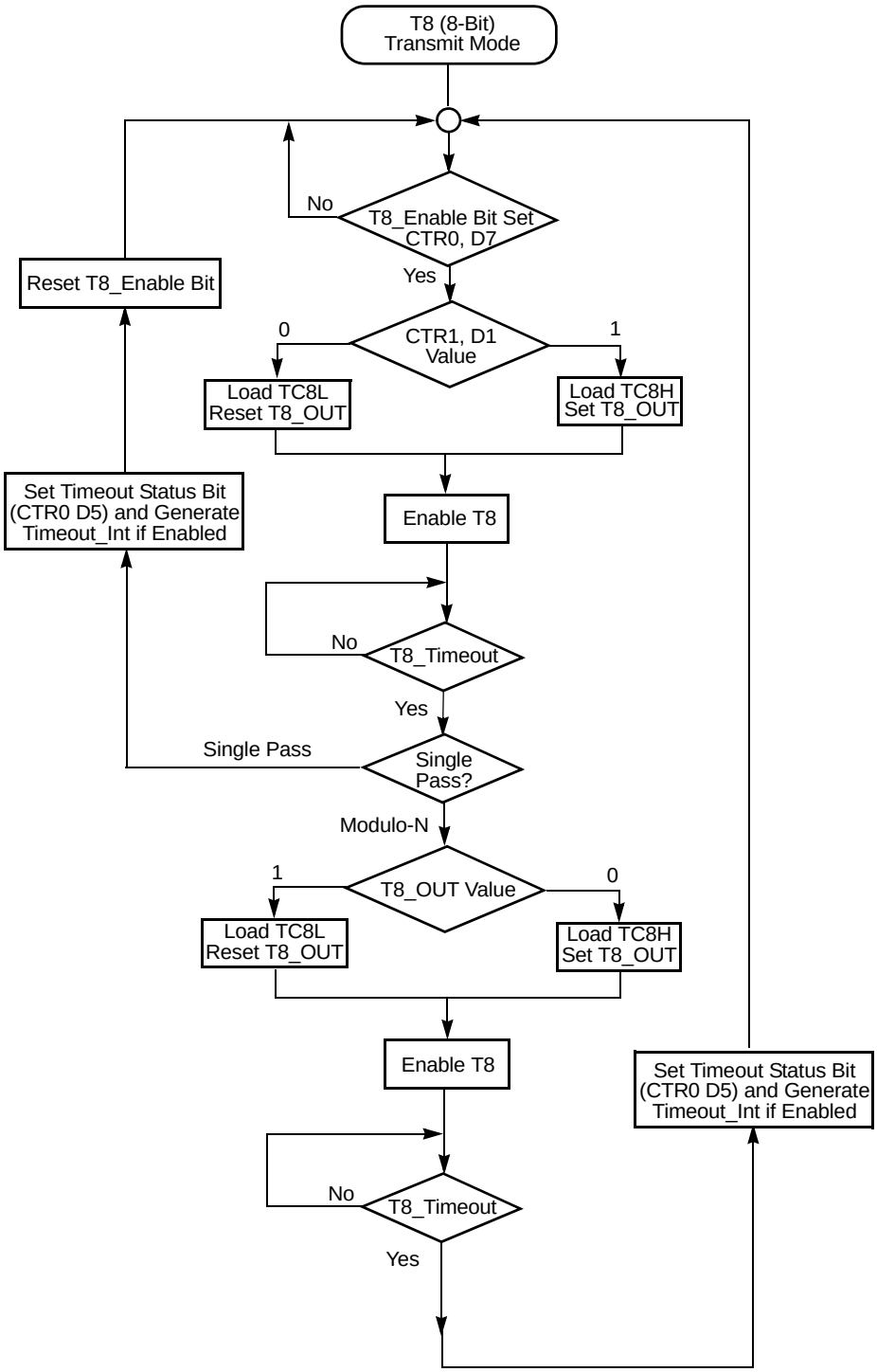


Figure 20. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In Single-Pass Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 21.

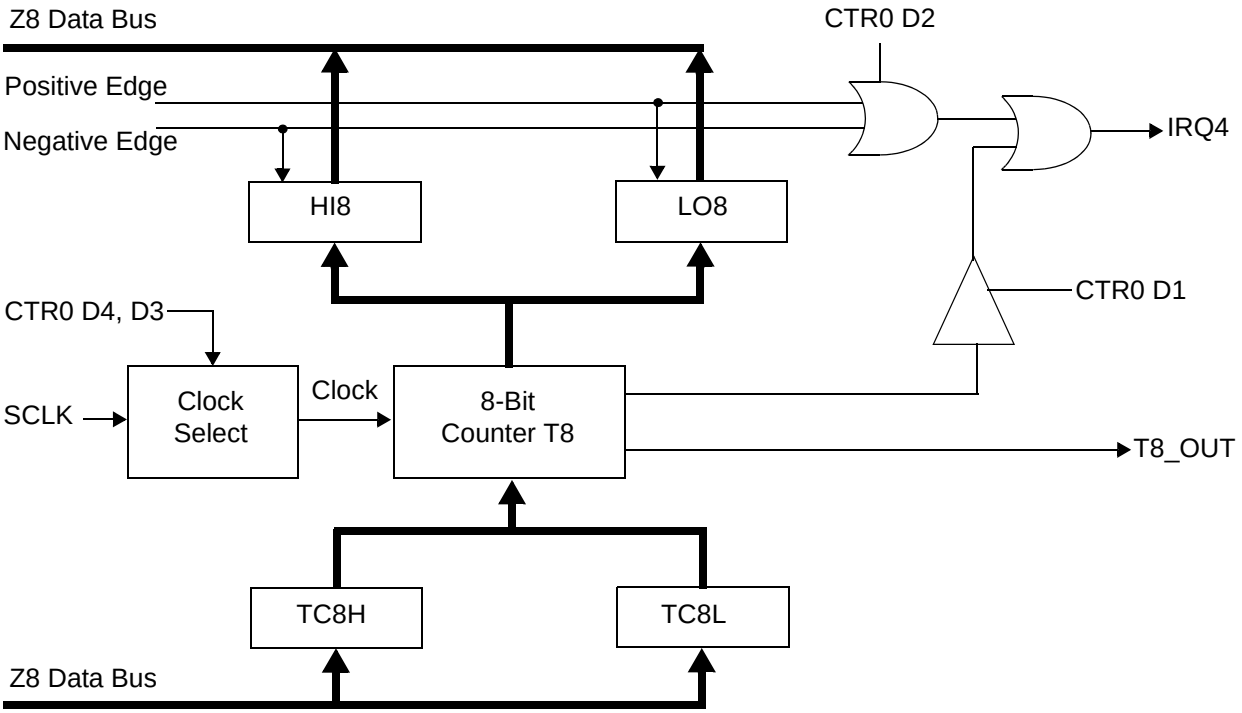


Figure 21. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: Do not write these registers at the time the values are to be loaded into the counter/timer to ensure known operation. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to `FFh` to `FEh`.

Note: The letter `h` is used for hexadecimal values.

Transition from 0 to `FFh` is not a timeout condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 22 and Figure 23.

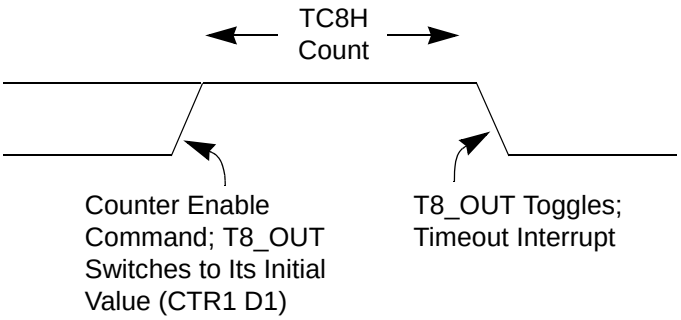


Figure 22. T8_OUT in Single-Pass Mode

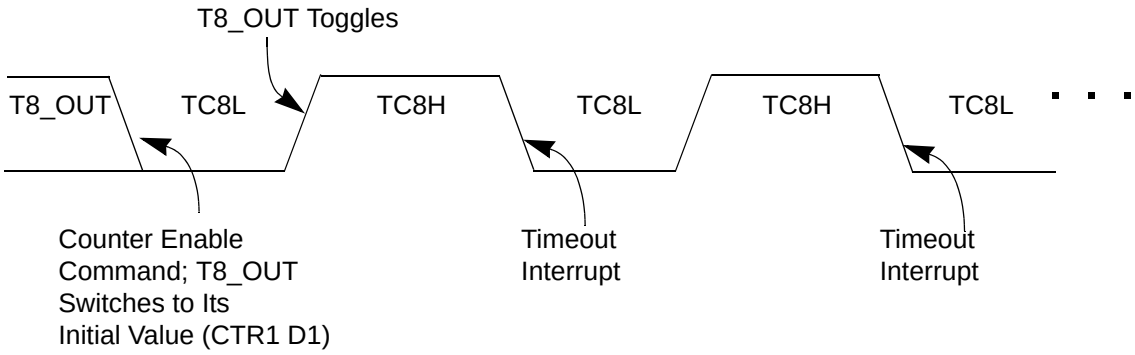


Figure 23. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

Program TC8L and TC8H to `FFh`. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with `FFh` and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from `FFh` (see Figure 24 and Figure 25).

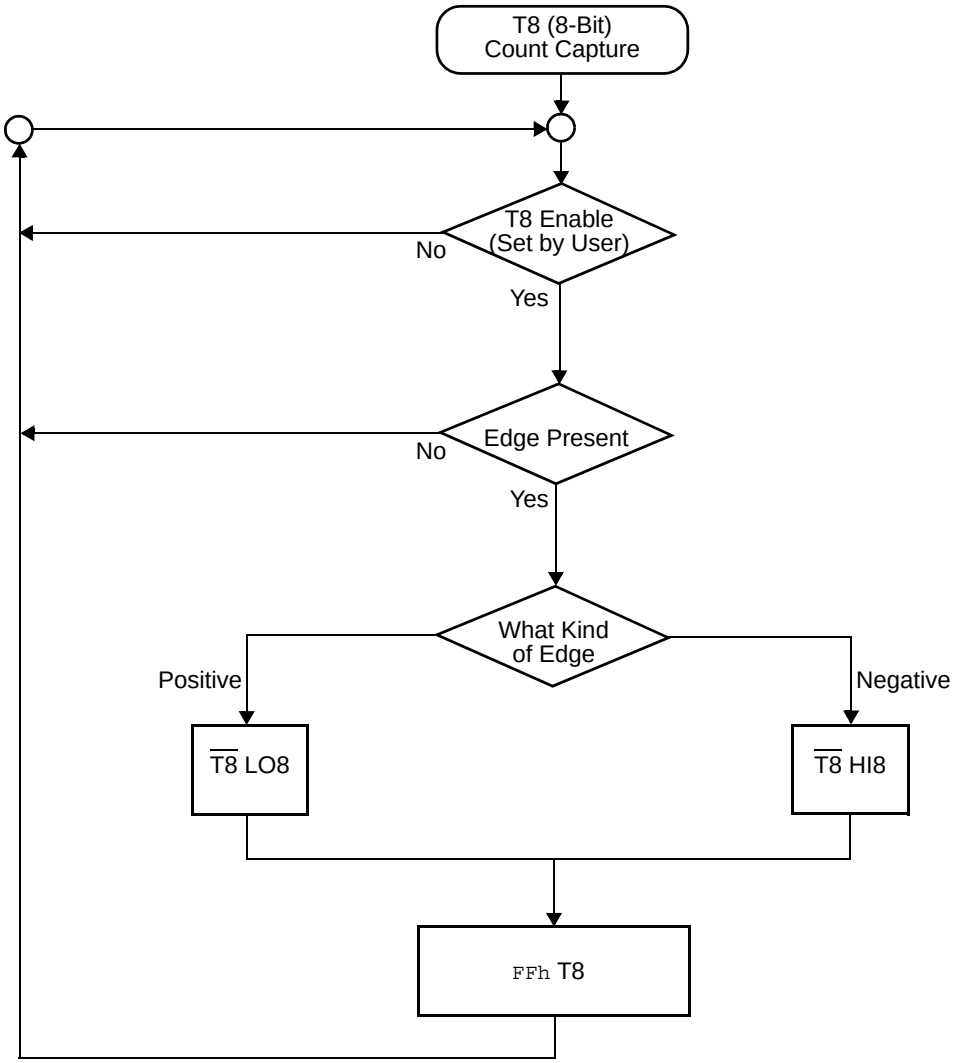


Figure 24. Demodulation Mode Count Capture Flowchart

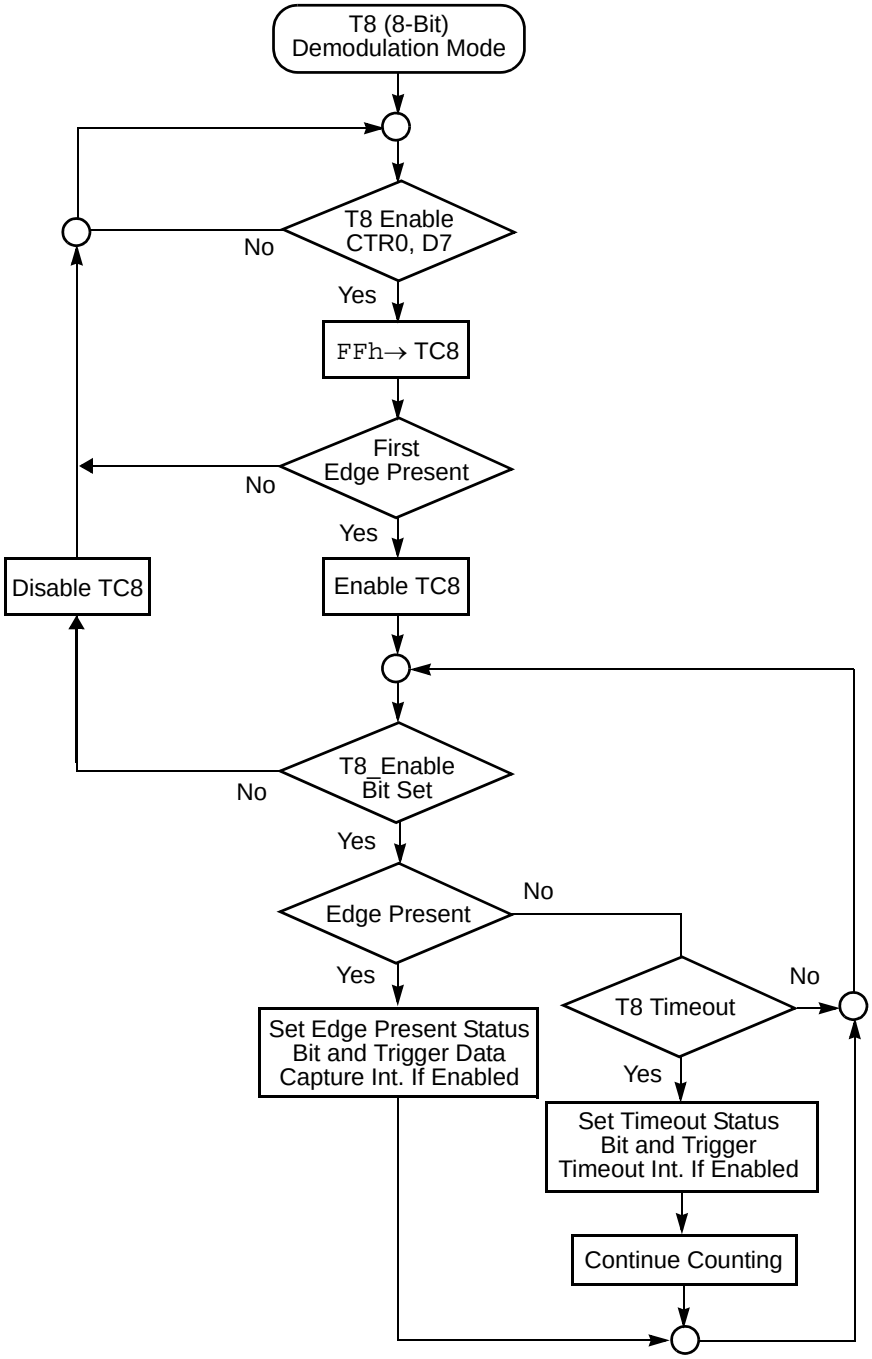


Figure 25. Demodulation Mode Flowchart

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 26.

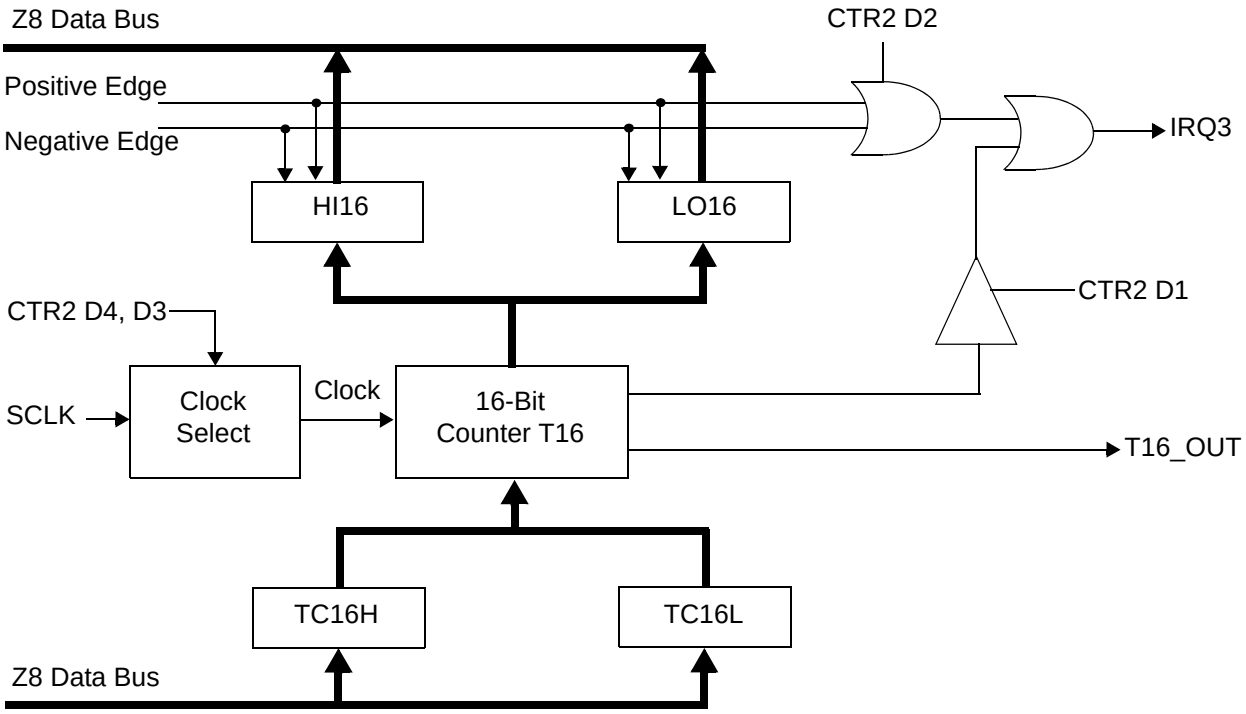


Figure 26. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in “Interrupts” on page 53.

If T16 is in Single-Pass Mode, it is stopped at this point (see Figure 27). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 28).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to `FFFFh` to `FFFEh`. Transition from 0 to `FFFFh` is not a timeout condition.

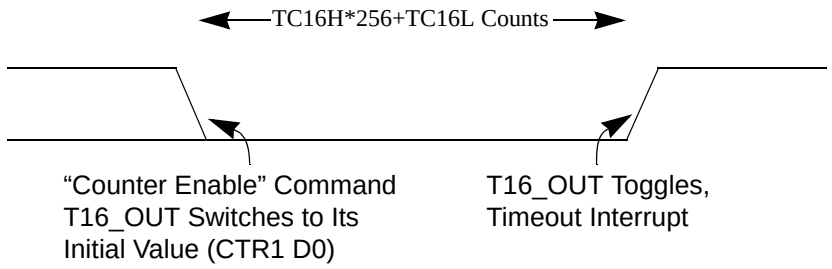


Figure 27. T16_OUT in Single-Pass Mode

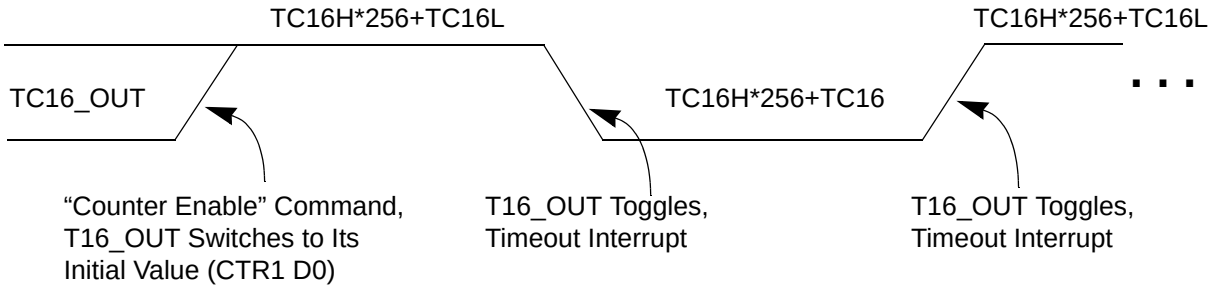


Figure 28. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

Program TC16L and TC16H to `FFh`. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with `FFFFh` and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode is generally used to measure mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 must be programmed in Single-Pass Mode (CTR0, D6; CTR2, D6), and Ping-Pong Mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 29.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

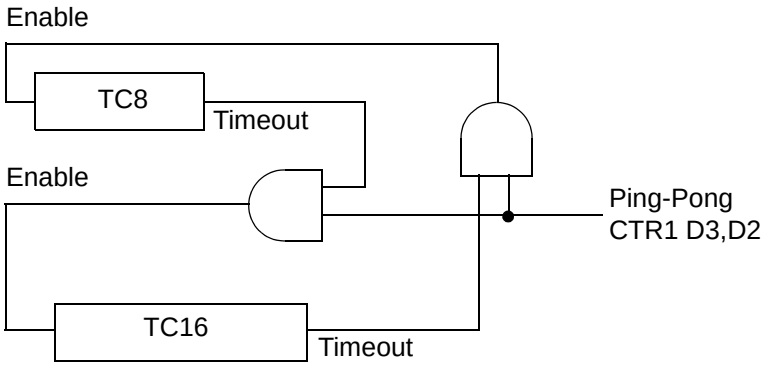


Figure 29. Ping-Pong Mode

Initiating Ping-Pong Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass Mode (CTR0, D6), set T16 into Single-Pass Mode (CTR2, D6), and set the Ping-Pong Mode (CTR1, D2; D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 30.

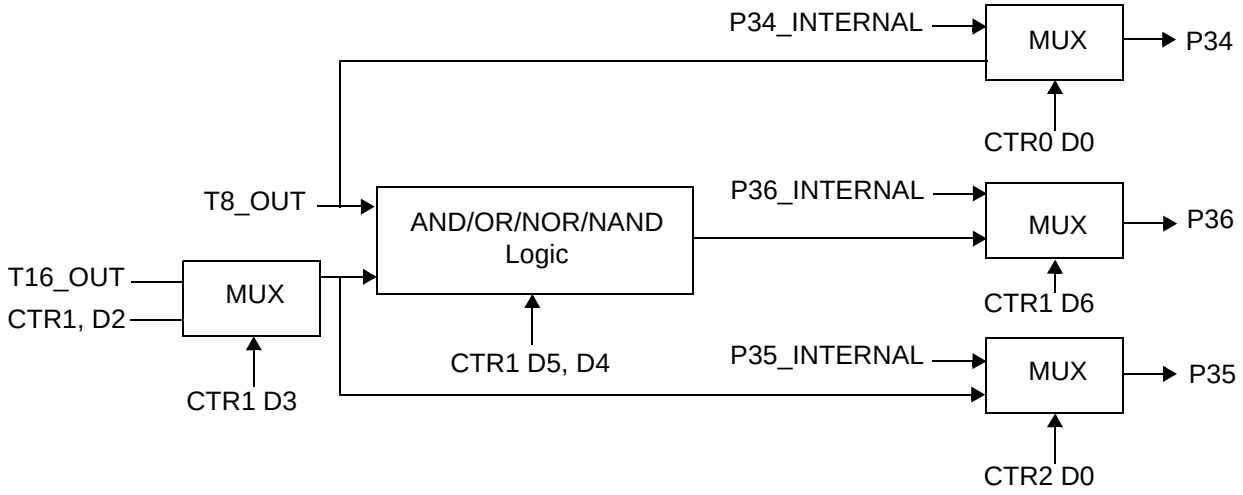


Figure 30. Output Circuit

The initial value of T8 or T16 must not be `1`. If you stop the timer and start the timer again, reload the initial value to avoid an unknown previous value.

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The Z86D73 feature six different interrupts (Table 15). The interrupts are maskable and prioritized (Figure 31). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and two by the counter/timers (Table 15). The Interrupt Mask Register (globally or individually) enables or disables the five interrupt requests.

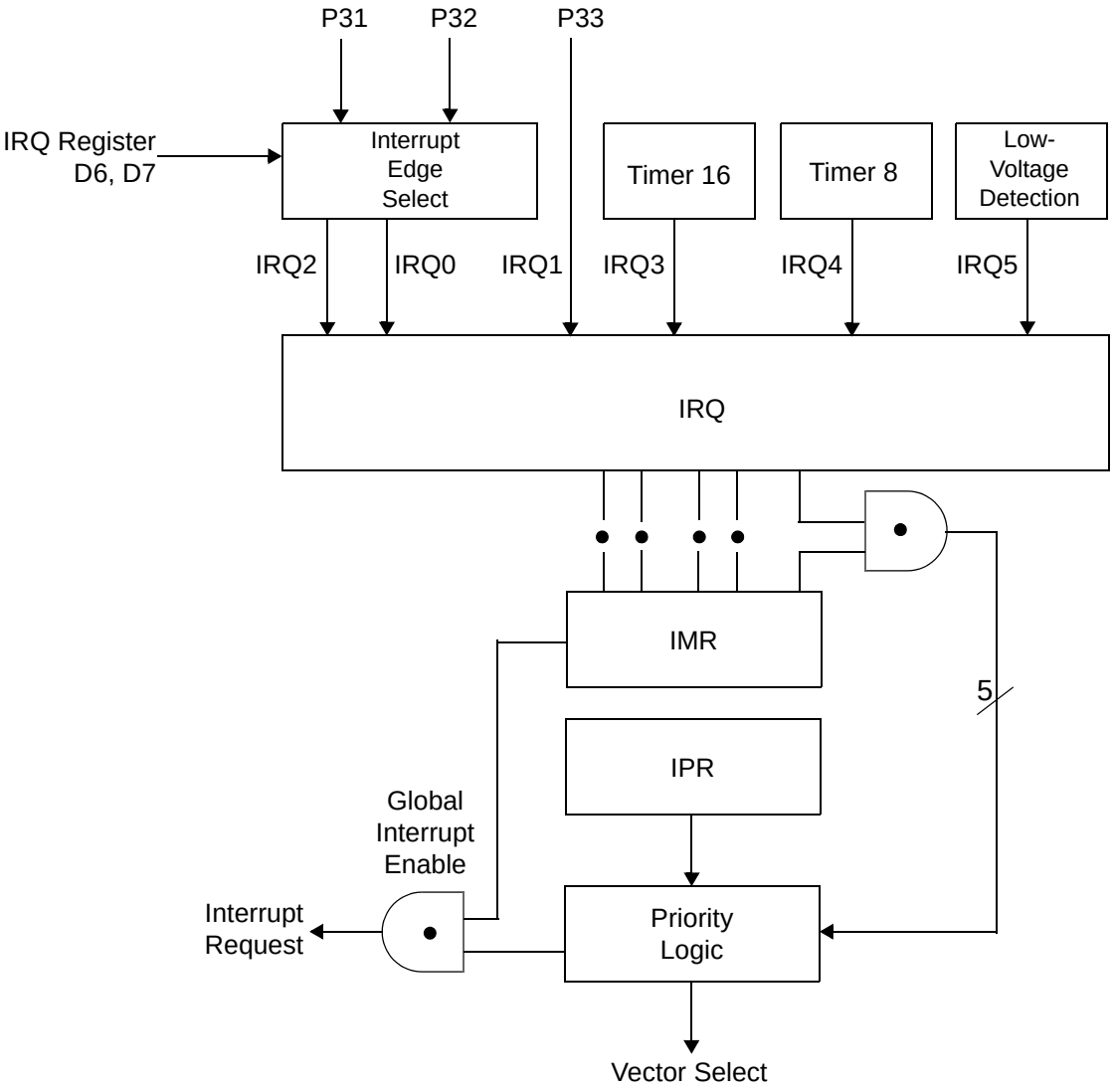


Figure 31. Interrupt Block Diagram

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86D73 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 16.

Table 16. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

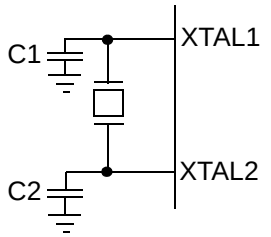
Notes: F = Falling Edge; R = Rising Edge
***In stop mode, the comparators are turned off.**

Clock

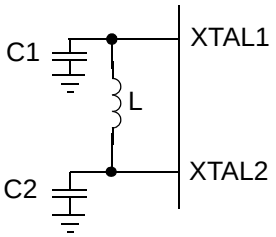
The Z86D73 on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The Z86D73 on-chip oscillator can be driven with a low-cost RC network or other suitable external clock source.

For 32-kHz crystal operation, an external feedback (Rf) and a serial resistor (Rd) are required. See Figure 32.

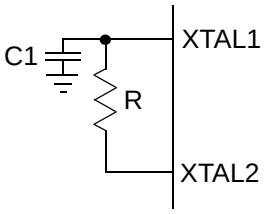
The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 32).



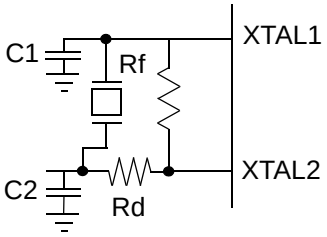
Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz



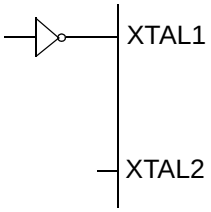
LC
C1, C2 = 22 pF
L = 130 µH *
f = 3 MHz *



RC
@ 3V VCC (TYP)
C1 = 33 pF *
R = 1K *



32 kHz XTAL
C1 = 20 pF, C = 33 pF
Rd = 56 - 470K
Rf = 10 M



External Clock

* Preliminary value including pin parasitics

Figure 32. Oscillator Configuration

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation, thereby reducing the standby current to 10 µA or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR, or external reset. This condition causes the processor to restart the application program at address `000Ch`. In order to enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction, as follows:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
```

or

```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Port Configuration Register (PCON)

The PCON register (Figure 33) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON (FH) 00H

D7	D6	D5	D4	D3	D2	D1	D0

Comparator Output Port 3
0 P34, P37 Standard Output*
1 P34, P37 Comparator Output

Port 1
0: Open-Drain
1: Push-Pull*

Port 0
0: Open-Drain
1: Push-Pull*

Reserved (Must be 1)

* Default setting after reset

Figure 33. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the 0ort to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 34). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 or the SMR register specify the source of the Stop-Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address `0Bh`.

SMR (0F) 0B

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0 OFF * *
1 ON

Reserved (Must be 0)

Stop-Mode Recovery Source
000 POR Only *
001 Reserved
010 P31
011 P32
100 P33
101 P27
110 P2 NOR 0-3
111 P2 NOR 0-7

Stop Delay
0 OFF
1 ON *

Stop Recovery Level * * *
0 Low *
1 High

Stop Flag
0 POR *
1 Stop Recovery * *

* Default setting after reset
* * Default setting after reset and stop-mode recovery
* * * At the XOR gate input

Figure 34. Stop-Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 35). The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

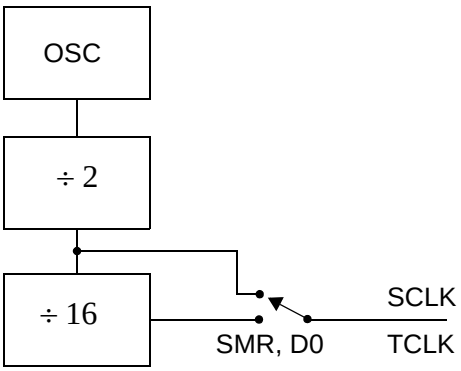


Figure 35. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 36 and Table 17).

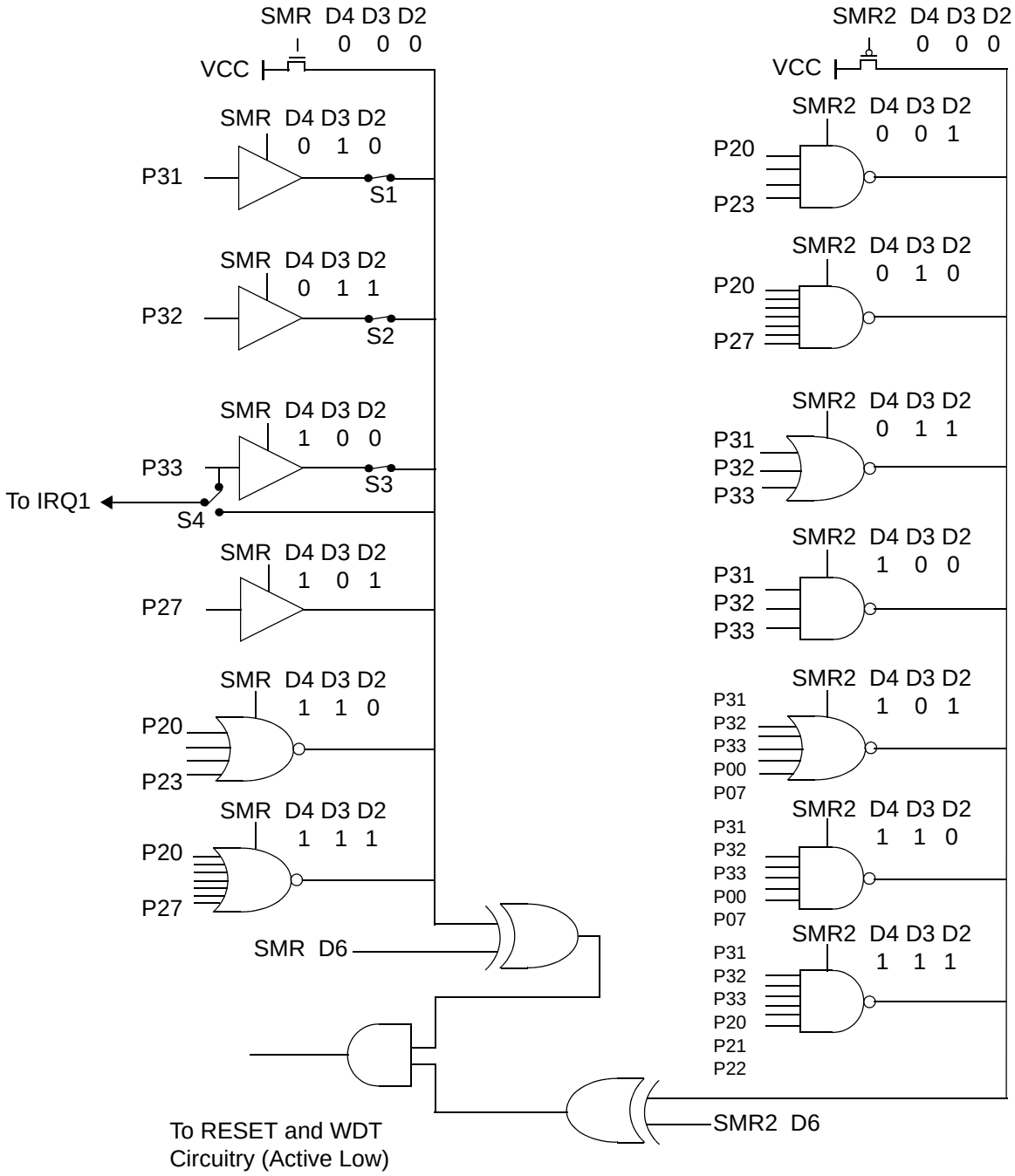


Figure 36. Stop-Mode Recovery Source

Table 17. Stop-Mode Recovery Source

SMR:432			Operation
D4	**D3**	**D2**	**Description of Action**
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 63 for other recover sources.

Stop-Mode Recovery Delay Select (D5)

This bit, if low, disables the 5 ms $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86D73 from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

Stop-Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop-Mode Recovery for SMR2 (Figure 37).

SMR2 (0F) DH

D7	D6	D5	D4	D3	D2	D1	D0

D0: Reserved (Must be 0)

D1: Reserved (Must be 0)

D3–D2: Stop-Mode Recovery Source 2
000 POR Only *
001 NAND P20, P21, P22, P23
010 NAND P20, P21, P22, P23, P24, P25, P26, P27
011 NOR P31, P32, P33
100 NAND P31, P32, P33
101 NOR P31, P32, P33, P00, P07
110 NAND P31, P32, P33, P00, P07
111 NAND P31, P32, P33, P20, P21, P22

D4: Reserved (Must be 0)

D5: Recovery Level * *
0 Low *
1 High

D6: Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.
* Default setting after reset
* * At the XOR gate input

Figure 37. Stop-Mode Recovery Register 2 ((0F) DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop-Mode Recovery.

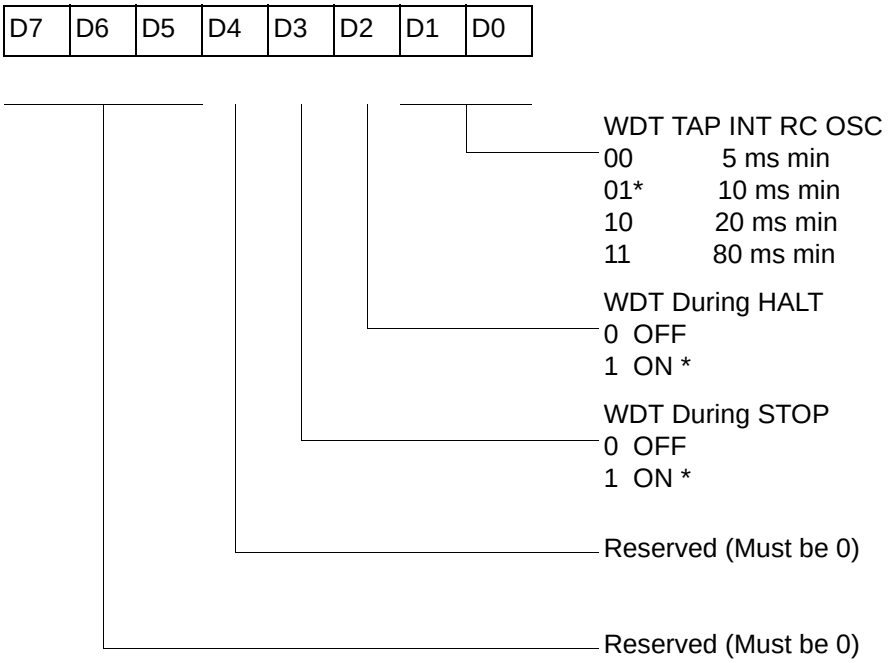
Note: Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bits 0 and 1 control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 38). This register is accessible only during the first 61 processor cycles (122 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 37). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location `0Fh`. It is organized as shown in Figure 38.

WDTMR (0F) 0F



* Default setting after reset

Figure 38. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 18.

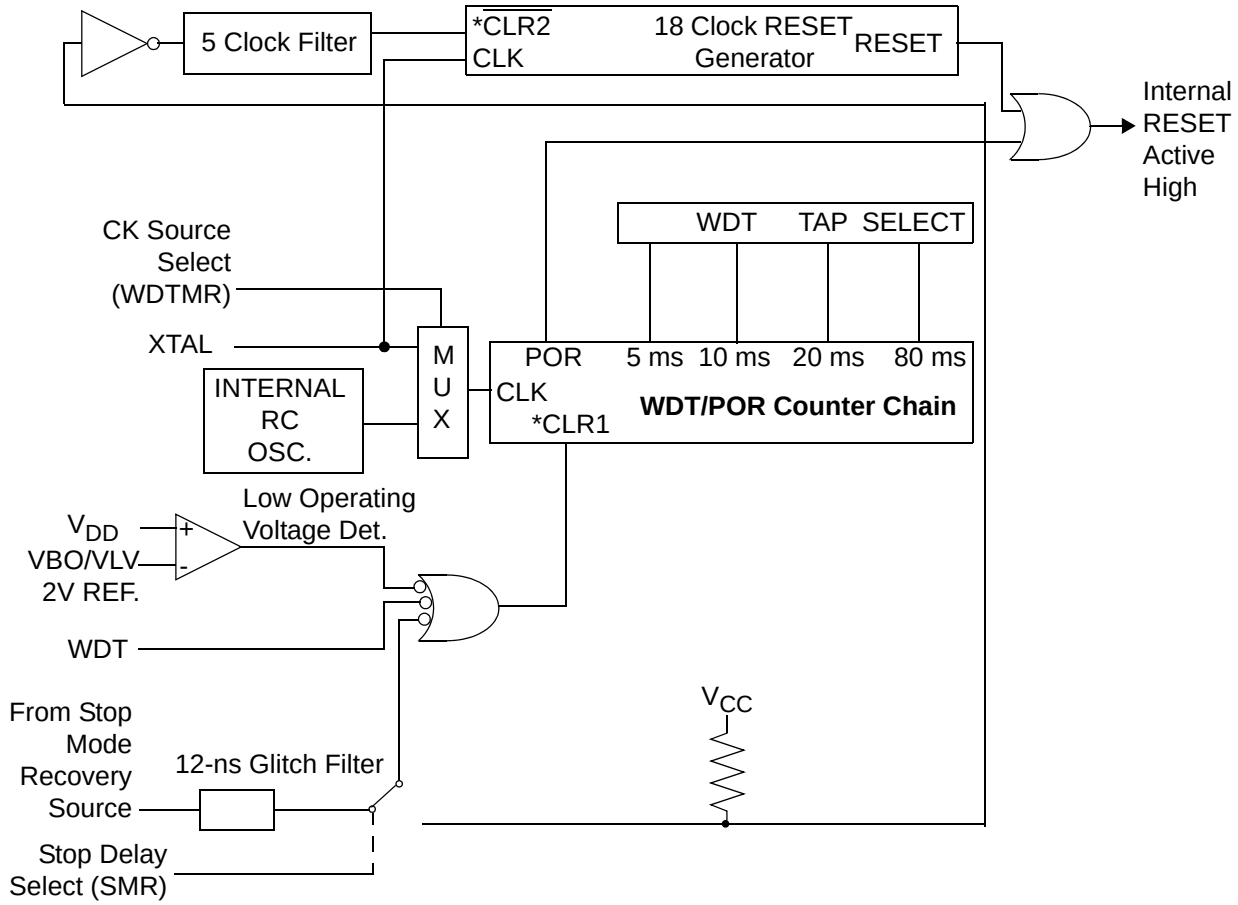
Table 18. WDT Time Select*

D1	D0	Timeout of Internal RC OSC	Timeout of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 Tpc
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Note:
***TpC = XTAL clock cycle. The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 39.



* $\overline{CLR1}$ and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers upon a Low-to-High input translation.

Figure 39. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

Mask Selectable Options

There are seven Mask Selectable Options to choose from based on ROM code requirements. These are listed in Table 19.

Table 19. Mask Selectable Options

RC/Other	RC/XTAL
32 kHz XTAL	On/Off
Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
Port 3: Pull-Ups	On/Off
Port 0: 0–3 Normal Mode (0.5 V_{DD} Input Threshold) versus Mouse Mode (0.4 V_{DD} Input Threshold)	

Brown-Out Voltage/Standby

An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{BO}. A small drop in V_{CC} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. Typical Low-Voltage power consumpion in this Low Voltage Standby mode (I_{LV}) is about 20 µA. If the V_{CC} is allowed to stay above Vram, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection and Flag

A Low-Voltage Detection circuit can be used optionally when the voltage decreases to V_{LVD}. Expanded Register Bank `0Dh` register `0Ch` bits 0 and 1 are used for this option. Bit D0 is used to enable/disable this function; bit D1 is the status flag bit of the LVD.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are shown in Figure 40 through Figure 43.

CTR0 (0D) 0H

D7	D6	D5	D4	D3	D2	D1	D0

0 P34 as Port Output *
1 Timer8 Output

0 Disable T8 Timeout Interrupt
1 Enable T8 Timeout Interrupt

0 Disable T8 Data Capture Interrupt
1 Enable T8 Data Capture Interrupt

00 SCLK on T8
01 SCLK/2 on T8
10 SCLK/4 on T8
11 SCLK/8 on T8

R 0 No T8 Counter Timeout
R 1 T8 Counter Timeout Occurred
W 0 No Effect
W 1 Reset Flag to 0

0 Modulo-N
1 Single Pass

R 0 T8 Disabled *
R 1 T8 Enabled
W 0 Stop T8
W 1 Enable T8

* Default setting after reset

Figure 40. TC8 Control Register ((0D) OH: Read/Write Except Where Noted)

CTR1 (0D) 1H

D7	D6	D5	D4	D3	D2	D1	D0

Transmit Mode
R/W 0 T16_OUT is 0 initially
1 T16_OUT is 1 initially

Demodulation Mode
R 0 No Falling Edge Detection
R 1 Falling Edge Detection

W 0 No Effect
W 1 Reset Flag to 0

Transmit Mode
R/W 0 T8_OUT is 0 initially
1 T8_OUT is 1 initially

Demodulation Mode
R 0 No Rising Edge Detection
R 1 Rising Edge Detection

W 0 No Effect
W 1 Reset Flag to 0

Transmit Mode
0 0 Normal Operation
0 1 Ping-Pong Mode
1 0 T16_OUT = 0
1 1 T16_OUT = 1

Demodulation Mode
0 0 No Filter
0 1 4 SCLK Cycle Filter
1 0 8 SCLK Cycle Filter
1 1 Reserved

Transmit Mode/T8/T16 Logic
0 0 AND
0 1 OR
1 0 NOR
1 1 NAND

Demodulation Mode
0 0 Falling Edge Detection
0 1 Rising Edge Detection
1 0 Both Edge Detection
1 1 Reserved

Transmit Mode
0 P36 as Port Output *
1 P36 as T8/T16_OUT

Demodulation Mode
0 P31 as Demodulator Input
1 P20 as Demodulator Input

Transmit/Demodulation Mode
0 Transmit Mode *
1 Demodulation Mode

* Default setting after reset

Figure 41. T8 and T16 Common Control Functions ((0D) 1h: Read/Write)

Notes: Care must be taken in differentiating Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be done without disabling the counter/timers.

CTR2 (0D) 02H

D7	D6	D5	D4	D3	D2	D1	D0

0 P35 is Port Output *
1 P35 is TC16 Output

0 Disable T16 Timeout Interrupt
1 Enable T16 Timeout Interrupt

0 Disable T16 Data Capture Interrupt
1 Enable T16 Data Capture Interrupt

0 0 SCLK on T16
0 1 SCLK/2 on T16
1 0 SCLK/4 on T16
1 1 SCLK/8 on T16

R 0 No T16 Timeout
R 1 T16 Timeout Occurs
W 0 No Effect
W 1 Reset Flag to 0

Transmit Mode
0 Modulo-N for T16
0 Single Pass for T16

Demodulator Mode
0 T16 Recognizes Edge
1 T16 Does Not Recognize Edge

R 0 T16 Disabled *
R 1 T16 Enabled
W 0 Stop T16
W 1 Enable T16

* Default setting after reset

Figure 42. T16 Control Register ((0D) 2h: Read/Write Except Where Noted)

LVD (0D) 0CH

D7	D6	D5	D4	D3	D2	D1	D0

Low-Voltage Detection at V_{BO} + 0.4 V
0: Disable *
1: Enable

LVD Flag (Read only)
0: LVD flag reset *
1: LVD flag set

Reserved (Must be 0)

* Default

Figure 43. Low-Voltage Detection

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are shown in Figure 44 through Figure 57.

SMR (0F) 0B

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0 OFF *
1 ON

Reserved (Must be 0)

Stop-Mode Recovery Source
000 POR Only *
001 Reserved
010 P31
011 P32
100 P33
101 P27
110 P2 NOR 0–3
111 P2 NOR 0–7

Stop Delay
0 OFF
1 ON *

Stop Recovery Level * * *
0 Low *
1 High

Stop Flag
0 POR *
1 Stop Recovery * *

* Default setting after reset
* * Default setting after reset and stop-mode recovery
* * * At the XOR gate input

Figure 44. Stop-Mode Recovery Register ((0F) 0Bh: D6–D0=Write Only, D7=Read Only)

SMR2 (0F) DH

D7	D6	D5	D4	D3	D2	D1	D0

Reserved (Must be 0)

Reserved (Must be 0)

Stop-Mode Recovery Source 2
000 POR Only *
001 NAND P20, P21, P22, P23
010 NAND P20, P21, P22, P23, P24, P25, P26, P27
011 NOR P31, P32, P33
100 NAND P31, P32, P33
101 NOR P31, P32, P33, P00, P07
110 NAND P31, P32, P33, P00, P07
111 NAND P31, P32, P33, P20, P21, P22

Reserved (Must be 0)

Recovery Level * *
0 Low
1 High

Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.
* Default setting after reset
* * At the XOR gate input

Figure 45. Stop-Mode Recovery Register 2 ((0F) 0Dh:D2–D4, D6 Write Only)

WDTMR (0F) 0F

D7	D6	D5	D4	D3	D2	D1	D0

WDT TAP INT RC OSC
00 5 ms min
01* 10 ms min
10 20 ms min
11 80 ms min

WDT During HALT
0 OFF
1 ON *

WDT During STOP
0 OFF
1 ON *

Reserved (Must be 0)

Reserved (Must be 0)

* Default setting after reset

Figure 46. Watch-Dog Timer Register ((0F) 0Fh: Write Only)

PCON (FH) 00H

D7	D6	D5	D4	D3	D2	D1	D0

Comparator Output Port 3
0 P34, P37 Standard Output *
1 P34, P37 Comparator Output

Port 1
0: Open-Drain
1: Push-Pull*

Port 0
0: Open-Drain
1: Push-Pull *

Reserved (Must be 1)

* Default setting after reset

Figure 47. Port Configuration Register (PCON) ((0F) 0h: Write Only)

R246 P2M

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

* Default setting after reset

Figure 48. Port 2 Mode Register (F6h: Write Only)

R247 P3M

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 Digital Mode
1= P31, P32 Analog Mode

Reserved (Must be 0)

00: P33 = Input
P34 = Output
01: P33 = Input
10: P34 = DM
11: Reserved

Reserved (Must be 0)

Reserved (Must be 0)

* Default setting after reset

Figure 49. Port 3 Mode Register (F7h: Write Only)

R248 P01M

D7	D6	D5	D4	D3	D2	D1	D0

P00–P03 Mode
00: Output
01: Input *
1X: A11–A8

Stack Selection
0: External
1: Internal *

P17–P10 Mode
00: Byte Output
01: Byte Input
10: AD7–AD0
11: High-Impedance AD7–AD0, $\overline{AS}$, $\overline{DS}$, $\overline{R/W}$, A11–A8, A15–A12, if selected

External Memory Timing
0: Normal *
1: Extended

P07–P04 Mode
00: Output
01: Input *
1X: A15–A12

* Default setting after reset; only P00 and P07 are available on Z86L71

Figure 50. Port 0 and 1 Mode Register (F8h: Write Only)

R249 IPR

D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Group Priority
000 Reserved
001 C > A > B
010 A > B >C
011 A > C > B
100 B > C > A
101 C > B > A
110 B > A > C
111 Reserved

IRQ1, IRQ4, Priority
(Group C)
0: IRQ1 > IRQ4
1: IRQ4 > IRQ1

IRQ0, IRQ2, Priority
(Group B)
0: IRQ2 > IRQ0
1: IRQ0 > IRQ2

IRQ3, IRQ5, Priority
(Group A)
0: IRQ5 > IRQ3
1: IRQ3 > IRQ5

Reserved; must be 0

Figure 51. Interrupt Priority Register (F9h: Write Only)

R250 IRQ

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = T16
IRQ4 = T8
IRQ5 = LVD

Inter Edge
P31↓ P32↓ = 00
P31↓ P32↑ = 01
P31↑ P32↓ = 10
P31↑↓ P32↑↓ = 11

Figure 52. Interrupt Request Register (FAh: Read/Write)

R251 IMR

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5–IRQ0
(D0 = IRQ0)

Reserved (Must be 0)

0 Master Interrupt Disable *
1 Master Interrupt Enable * *

* Default setting after reset
* * Only by using E1, D1 instruction; D1 is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBh: Read/Write)

R252 Flags

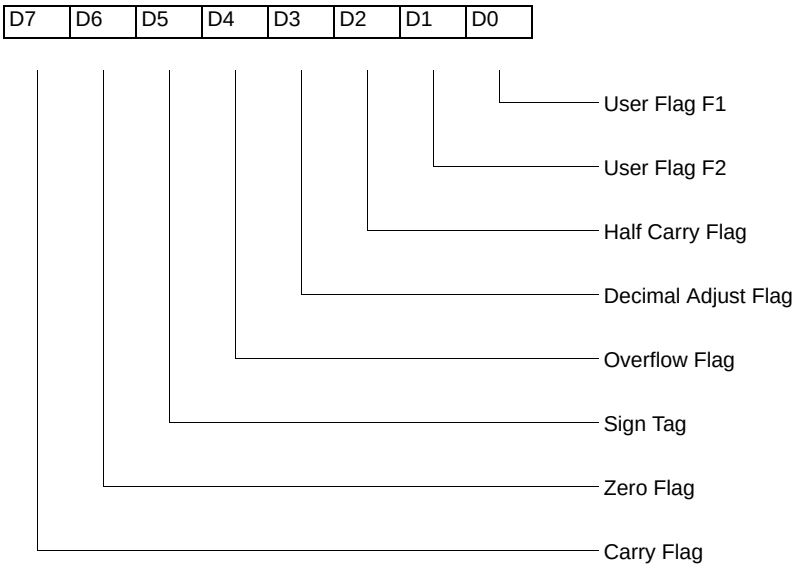
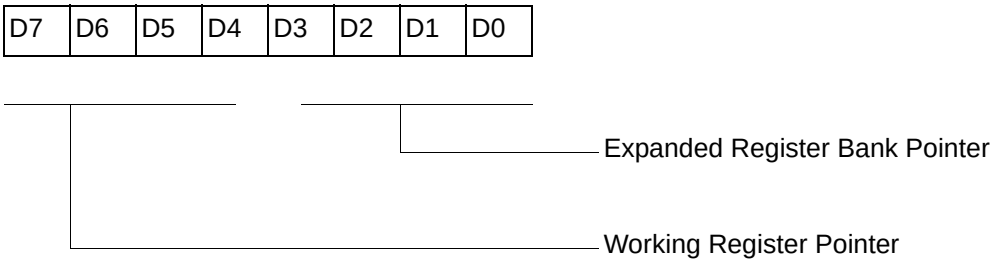


Figure 54. Flag Register (FCh: Read/Write)

R253 RP



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDh: Read/Write)

R254 SPH

D7	D6	D5	D4	D3	D2	D1	D0

General-Purpose Register or Stack Pointer High (SP15–SP8) if external memory is used

Figure 56. Stack Pointer High (FEh: Read/Write)

R255 SPL

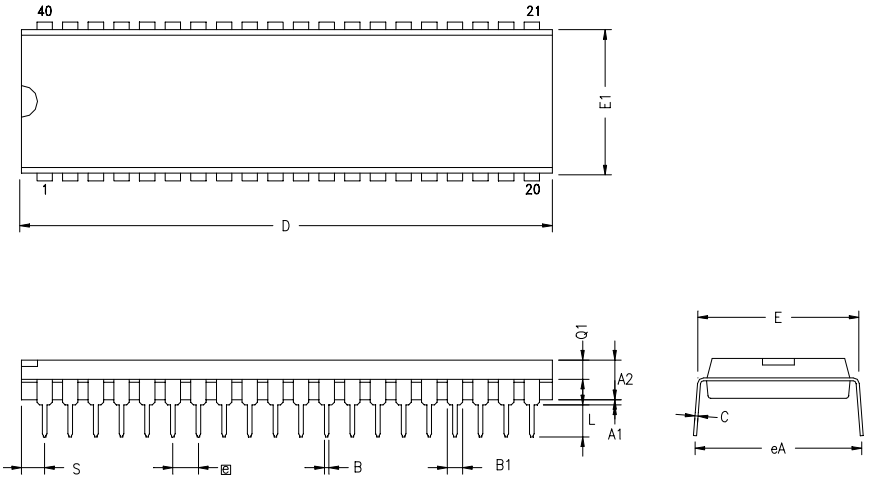
D7	D6	D5	D4	D3	D2	D1	D0

Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFh: Read/Write)

Package Information

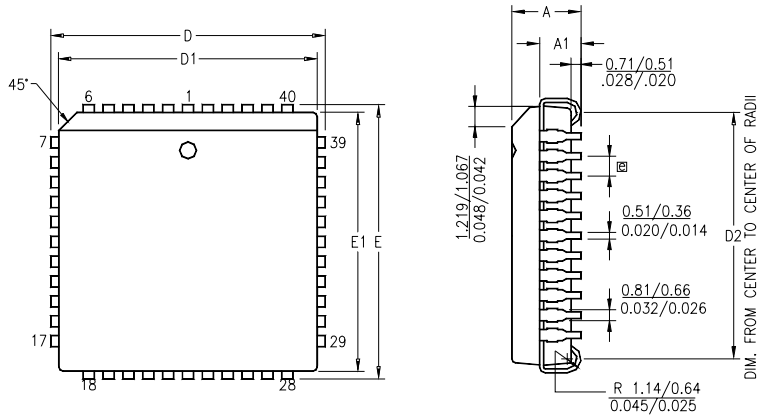
Package information is shown in Figure 58, Figure 59, Figure 60, and Figure 61.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

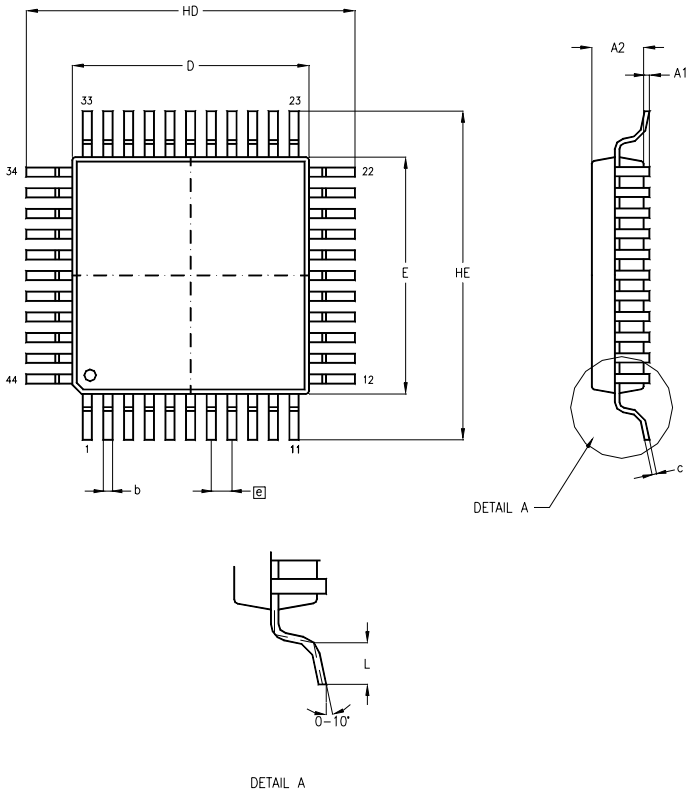
Figure 58. 40-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

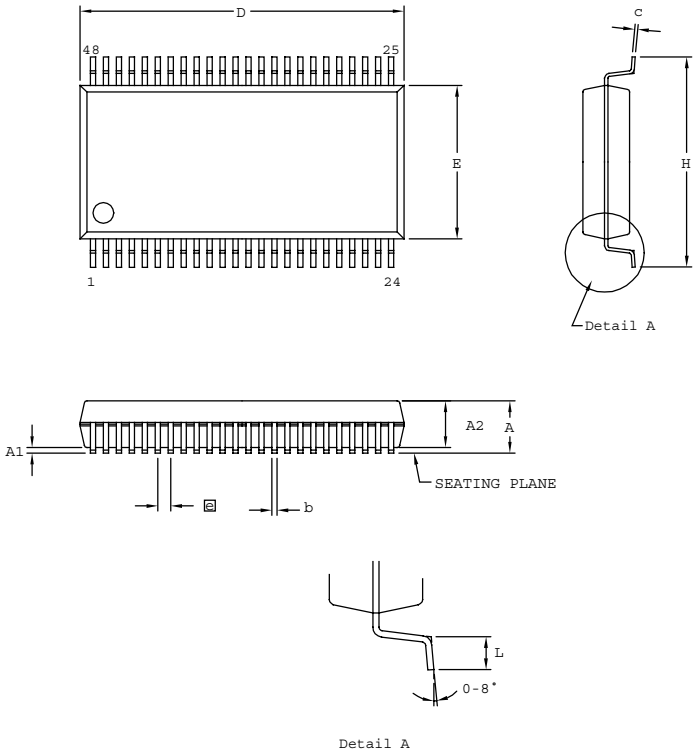
Figure 59. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 60. 44-Pin QFP Package Design



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 61. 48-Pin SSOP Package Design

Note: Please check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

Ordering Information

Table 20. Z86D73 Ordering Information

8.0 MHz 40-Pin DIP	8.0 MHz 44-Pin PLCC	8.0 MHz 44-Pin QFP	8.0 MHz 48-Pin SSOP
Z86D7308PSC	Z86D7308VSC	Z86D7308FSC	Z86D7308HSC
Die Form	Please contact ZiLOG.		

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

Package

P = Plastic DIP
F = Plastic Quad Flat Pack
H = SSOP
V = Plastic Chip Carrier

Speed

8 = 8 MHz

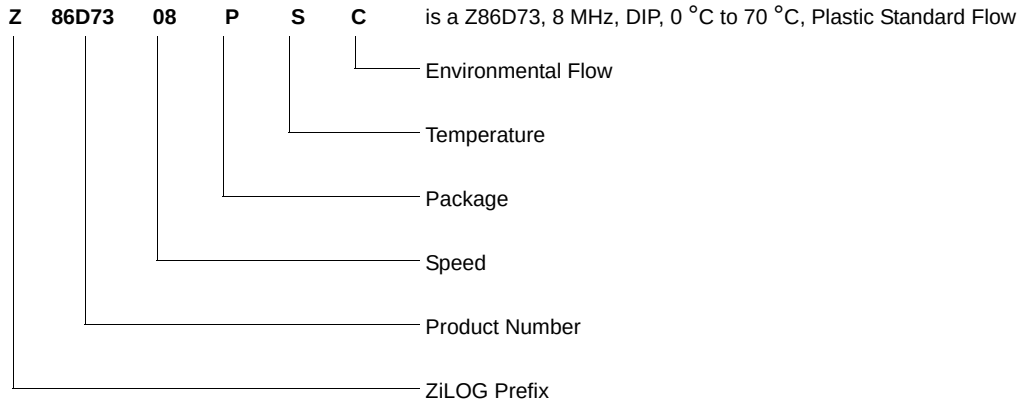
Environmental

C = Plastic Standard

Temperature

S = 0 °C to +70 °C

Example



Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

ZiLOG, Inc.

532 Race Street

San Jose, CA 95126-3432

Telephone: (408) 558-8500

FAX: 408 558-8300

Internet: HTTP://WWW.ZILOG.COM