National Semiconductor

December 1994

ADC1251 Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample-and-Hold

General Description

The ADC1251 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter. On request, the ADC1251 goes through a self-calibration cycle that adjusts for any zero, full scale, or linearity errors. The ADC1251 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC1251 is tracked and held by the internal circuitry, so an external sample-and-hold is not required. The ADC1251 has an $\overline{S}$/H control input which directly controls the track-and-hold state of the A/D. A unipolar analog input voltage range (0 to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit data result is available on the eight outputs of the ADC1251 in two bytes, high-byte first and sign extended. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Features

- Self-calibration provides excellent temperature stability
- Internal sample-and-hold
- 8-bit μP/DSP interface
- Bipolar input range with a single +5V reference
- No missing codes over temperature
- TTL/MOS input/output compatible

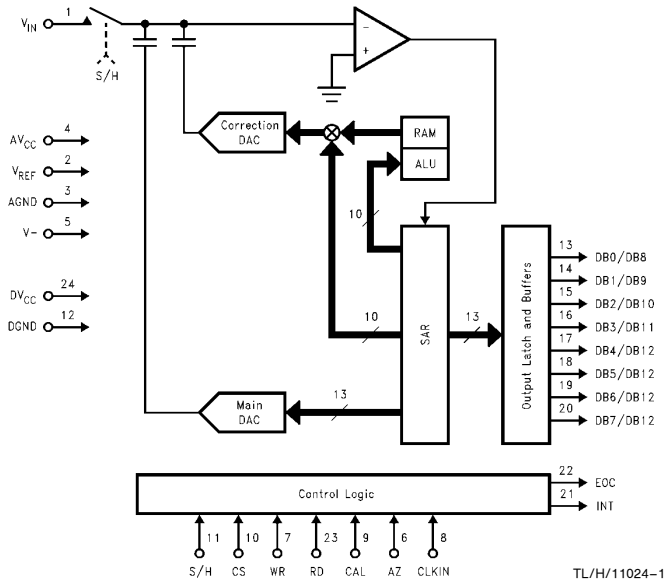
Key Specifications

■ Resolution	12 bits plus sign
■ Conversion Time	8 μs (max)
■ Sampling Rate	83 kHz (max)
■ Linearity Error	±0.6 LSB (±0.0146%) (max)
■ Zero Error	±1 LSB (max)
■ Full Scale Error	±1.5 LSB (max)
■ Power Consumption @ ±5V	113 mW (max)

Applications

- Digital signal processing
- High resolution process control
- Instrumentation

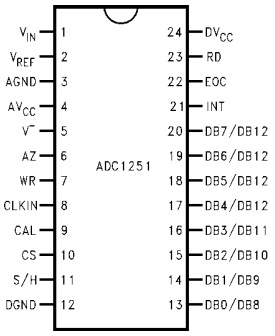
Simplified Block Diagram



TL/H/11024–1

Connection Diagram

Dual-In-Line Package



TL/H/11024–2

Top View

Ordering Information

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC1251BIJ, ADC1251CIJ	J24A
Military ($-55°C \le T_A \le +125°C$)	**Package**
ADC1251CMJ, ADC1251CMJ/883	J24A

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Inputs (V_{REF}, V_{IN})	(V^- − 0.3V) to (V_{CC} + 0.3V)
AV_{CC}-DV_{CC} (Note 7)	0.3V
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 sec.)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1251BIJ, ADC1251CIJ	−40°C ≤ T_A ≤ +85°C
ADC1251CMJ	−55°C ≤ T_A ≤ +125°C
ADC1251CMJ/883	−55°C ≤ T_A ≤ +125°C
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, $\overline{AZ}$ = "1", f_{CLK} = 3.5 MHz and tested using $\overline{WR}$ control unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error	ADC1251BIJ	After Auto-Cal (Notes 11 & 12)		**±0.6**	LSB(max)
		ADC1251CIJ			**±1**	LSB(max)
		ADC1251CMJ			**±1**	LSB(max)
	Negative Integral Linearity Error	ADC1251BIJ	After Auto-Cal (Notes 11 and 12)		**±0.6**	LSB(max)
		ADC1251CIJ			**±1**	LSB(max)
		ADC1251CMJ			**±1**	LSB(max)
	Missing Codes		After Auto-Cal (Notes 11 and 12)		**0**	
	Zero Error (Notes 12 and 13)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±2**	LSB(max)
			After Auto-Cal Only		±2.0/**±3.0**	LSB(max)
	Positive Full-Scale Error (Note 12)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±1.5**	LSB(max)
			After Auto-Cal Only		±1.5/**±2.0**	LSB(max)
	Negative Full-Scale Error (Note 12)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±1.5**	LSB(max)
			After Auto-Cal Only		±1.5/**±2.0**	LSB(max)
C_{REF}	V_{REF} Input Capacitance (Note 18)			80		pF
C_{IN}	Analog Input Capacitance			65		pF
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB

Converter Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, $\overline{AZ}$ = "1" and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
DYNAMIC CHARACTERISTICS					
S/(N + D)	Unipolar Signal-to-Noise + Distortion Ratio (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	72		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 4.85\ V_{p-p}$	72		dB
S/(N + D)	Bipolar Signal-to-Noise + Distortion Ratio (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	76		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 4.85V$	76		dB
	−3 dB Unipolar Full Power Bandwidth	$V_{IN} = 4.85V$, (Note 17)	32		kHz
	−3 dB Bipolar Full Power Bandwidth	$V_{IN} = \pm 4.85V$, (Note 17)	25		kHz
t_{Ap}	Aperture Time		100		ns
	Aperture Jitter		100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA(max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V(min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V(max)
V_H	CLK IN Hysteresis $[V_T^+(min) - V_T^-(max)]$		0.7	**0.4**	V(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA		**0.4**	V(max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA(max)
		$V_{OUT} = 5V$	0.01	**3**	μA(max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA(min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA(min)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS}$ = "1"	1	**2.5**	mA(max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS}$ = "1"	4	**10**	mA(max)
I^-	V^- Supply Current	$\overline{CS}$ = "1"	2.8	**10**	mA(max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
f_{CLK}	Clock Frequency		0.5 6.0	 **3.5**	MHz MHz(min) MHz(max)
	Clock Duty Cycle		50	 **40** **60**	% %(min) %(max)
t_C	Conversion Time Using $\overline{WR}$ to Start a Conversion		27($1/f_{CLK}$)	**27($1/f_{CLK}$) + 250 ns**	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	7.7	**7.95**	μs(max)
		$f_{CLK} = 1.75$ MHz, $\overline{AZ}$ = "0"	15.4	**15.65**	μs(max)
t_C	Conversion Time Using $\overline{S}$/H to Start a Conversion	$\overline{AZ}$ = "1"	34($1/f_{CLK}$)	**34($1/f_{CLK}$) + 250 ns**	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	9.7	**9.95**	μs(max)
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$	3.5	**3.5**	μs(min)
t_{IA}	Internal Acquisition Time (When Using $\overline{WR}$ Control Only)		7($1/f_{CLK}$)	**7($1/f_{CLK}$)**	(max)
t_{ZA}	Auto Zero Time + Acquisition Time		33($1/f_{CLK}$)	**33($1/f_{CLK}$) + 250 ns**	(max)
		$f_{CLK} = 1.75$ MHz	18.8	**19.05**	μs(max)
$t_{D(EOC)L}$	Delay from Hold Command to Falling Edge of EOC	Using $\overline{WR}$ Control	200	**350**	ns(max)
		Using $\overline{S}$/H Control	100	**150**	ns(max)
$t_{\overline{CAL}}$	Calibration Time		1399($1/f_{CLK}$)	**1399 ($1/f_{CLK}$)**	(max)
		$f_{CLK} = 3.5$ MHz	399	**400**	μs(max)
$t_{W(\overline{CAL})L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns(min)
$t_{W(\overline{WR})L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns(min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	**95**	ns(max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	**70**	ns(max)
$t_{PD(\overline{INT})}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns(max)
t_{RR}	Delay between Successive $\overline{RD}$ Pulses		30	**60**	ns(min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

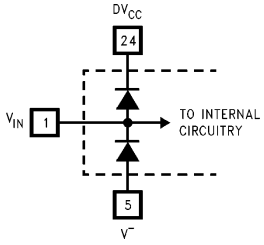
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$, the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The power dissipation of this device under normal operation should never exceed 191 mW (Quiescent Power Dissipation + 1 TTL Load on each digital output). Caution should be taken not to exceed absolute maximum power rating when the device is operating in severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$, and the typical thermal resistance (θ_{JA}) of the ADC1251 with CMJ, BIJ, and CIJ suffixes when board mounted is 51°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

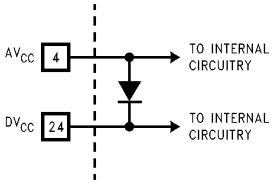
Electrical Characteristics (Continued)

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (-4.75 V_{DC}), the analog input full-scale voltage must be $\leq \pm 4.8$ V_{DC}.



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Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at $f_{CLK} = 3.5$ MHz. At higher or lower clock frequencies accuracy may degrade. See the Typical Performance Characteristics curves.

Note 9: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*).

Note 12: The ADC1251's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ± 0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started. See the typical performance characteristic curves.

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

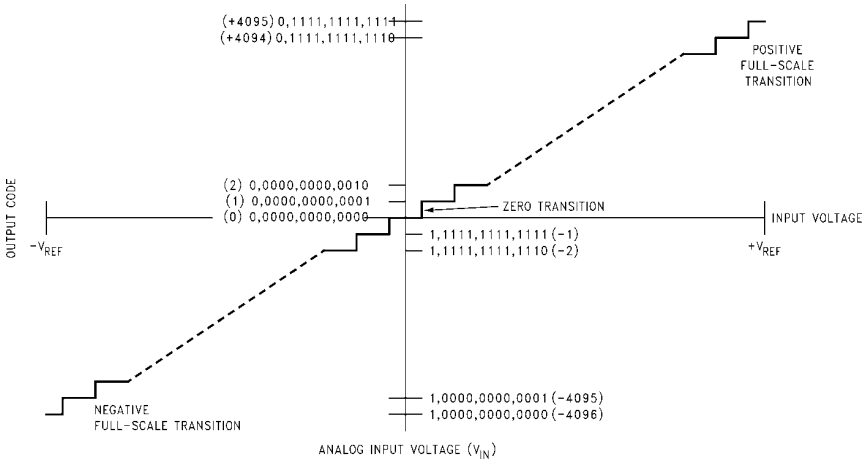
Note 15: When using the $\overline{WR}$ control to start a conversion if the clock is asynchronous to the rising edge of $\overline{WR}$ an uncertainty of one clock period will exist in the end of the interval t_A, therefore making t_A end a minimum 6 clock periods or a maximum 7 clock periods after the rising edge of $\overline{WR}$. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will end exactly 6.5 clock periods after the rising edge of $\overline{WR}$. This does not occur when $\overline{S}/H$ control is used.

Note 16: The $\overline{CAL}$ line must be high before a conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: The ADC1251 reference ladder is composed solely of capacitors.

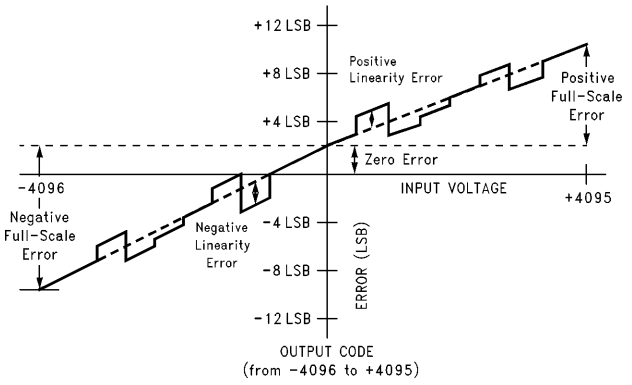
Note 19: A Military RETS Electrical Test Specification is available on request. At time of printing the ADC1251CMJ/883 RETS specification complies fully with the **boldface** limits in this column.



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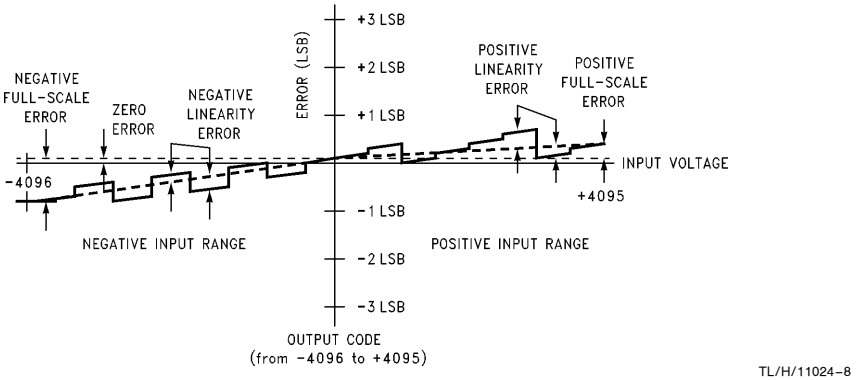
FIGURE 1a. Transfer Characteristic

Electrical Characteristics (Continued)



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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

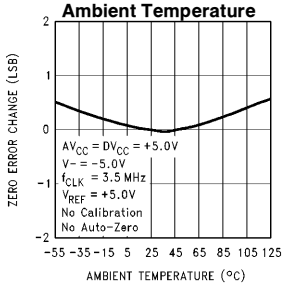


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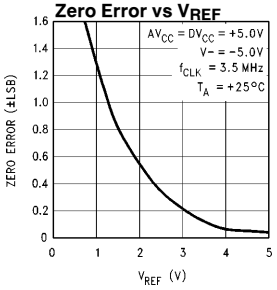
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics

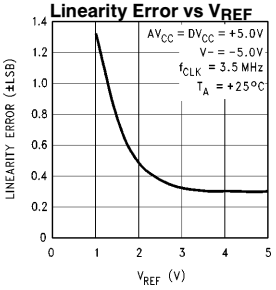
Zero Error Change vs Ambient Temperature



Zero Error vs V_{REF}



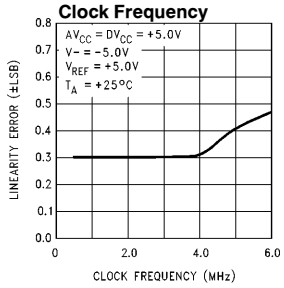
Linearity Error vs V_{REF}



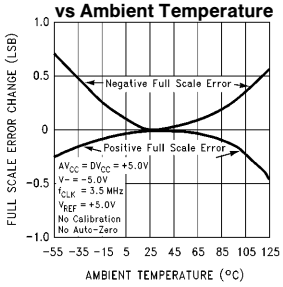
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Typical Performance Characteristics (Continued)

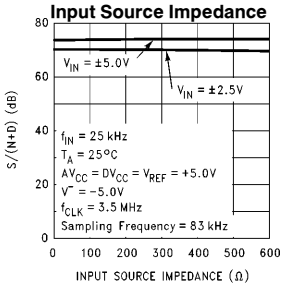
Linearity Error vs Clock Frequency



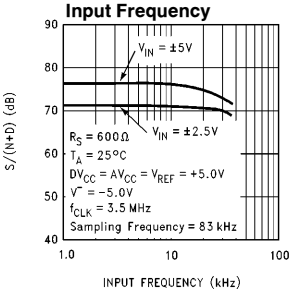
Full Scale Error Change vs Ambient Temperature



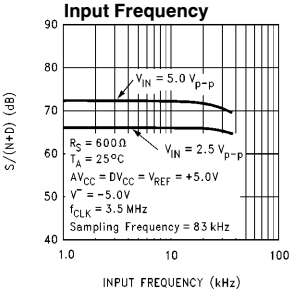
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance



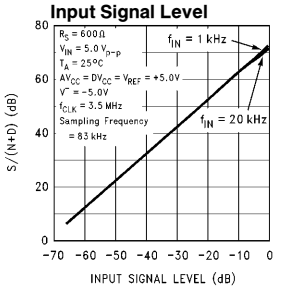
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



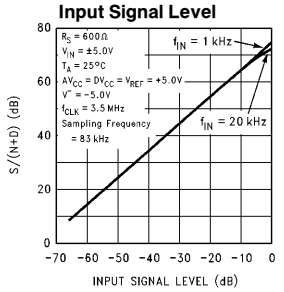
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



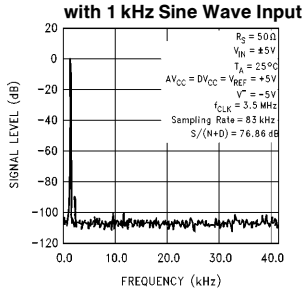
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



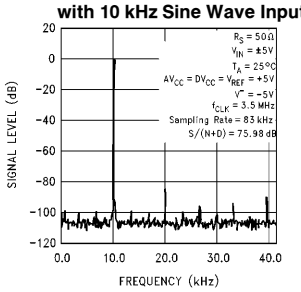
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



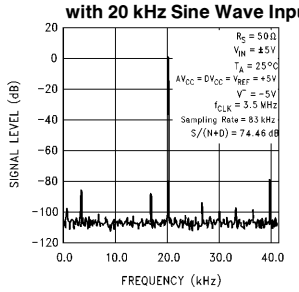
Bipolar Spectral Response with 1 kHz Sine Wave Input



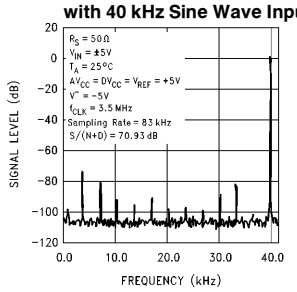
Bipolar Spectral Response with 10 kHz Sine Wave Input



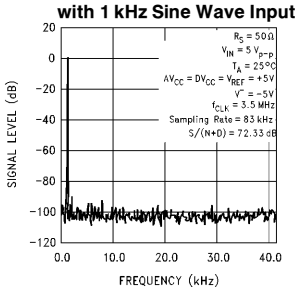
Bipolar Spectral Response with 20 kHz Sine Wave Input



Bipolar Spectral Response with 40 kHz Sine Wave Input



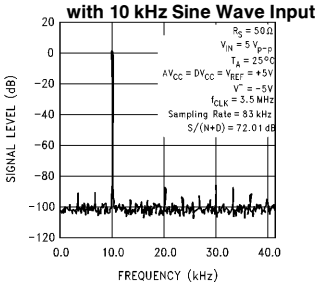
Unipolar Spectral Response with 1 kHz Sine Wave Input



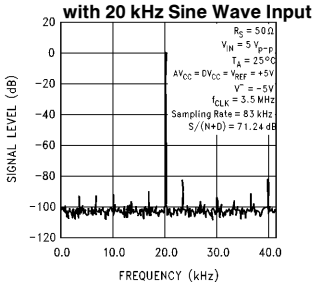
TL/H/11024–10

Typical Performance Characteristics (Continued)

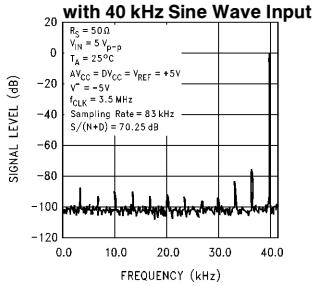
Unipolar Spectral Response with 10 kHz Sine Wave Input



Unipolar Spectral Response with 20 kHz Sine Wave Input

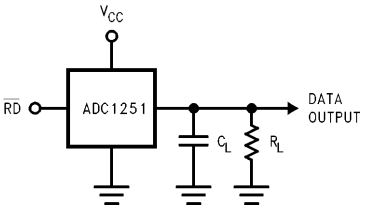


Unipolar Spectral Response with 40 kHz Sine Wave Input

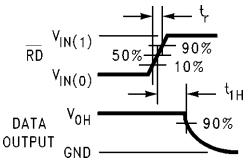


TL/H/11024–11

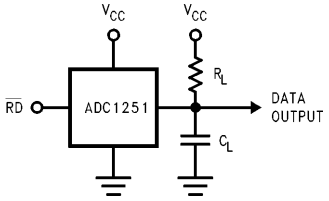
Test Circuits



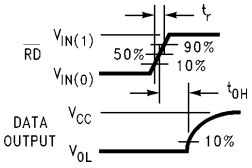
TL/H/11024–12



TL/H/11024–13



TL/H/11024–14

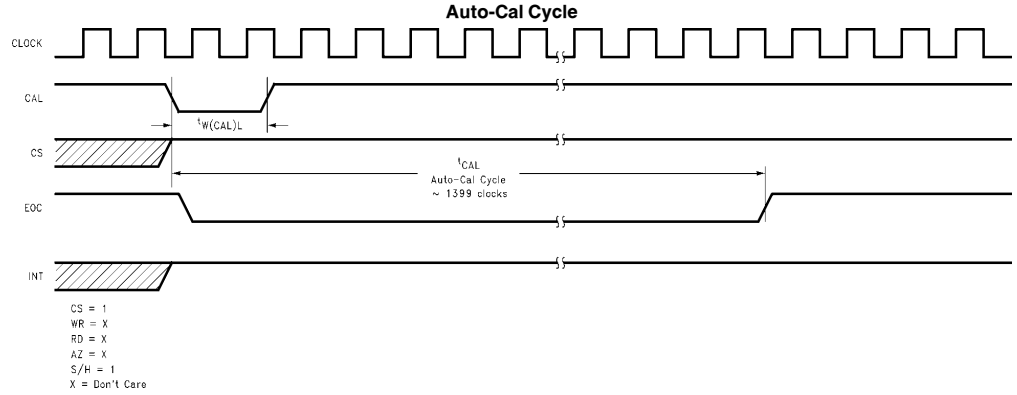


TL/H/11024–15

FIGURE 2. TRI-STATE Test Circuits and Waveforms

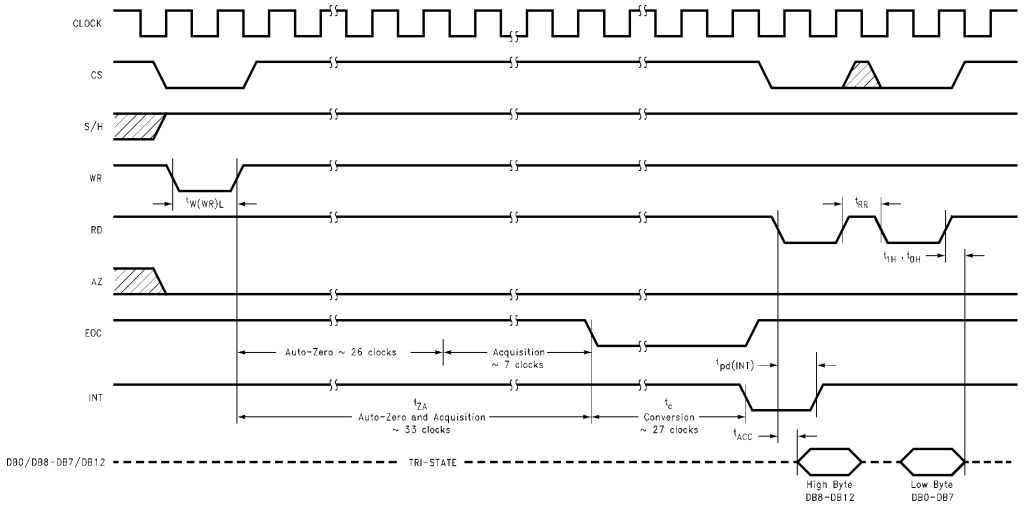
Timing Diagrams

Auto-Cal Cycle



TL/H/11024–16

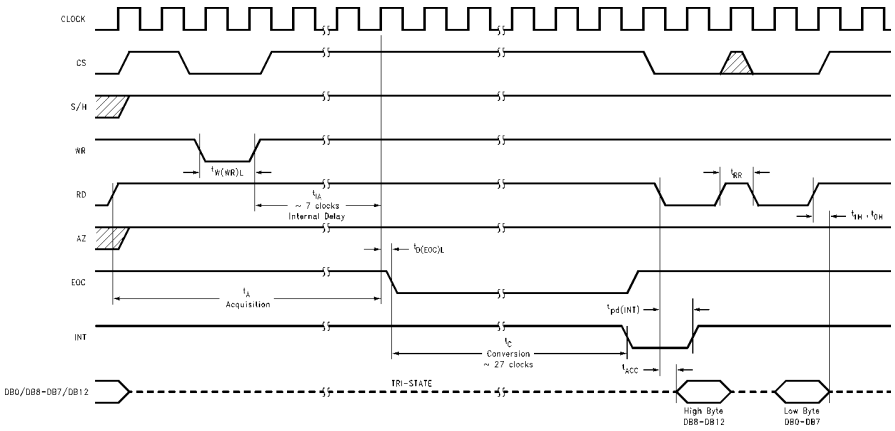
Using $\overline{WR}$ Control to Start a Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



TL/H/11024–17

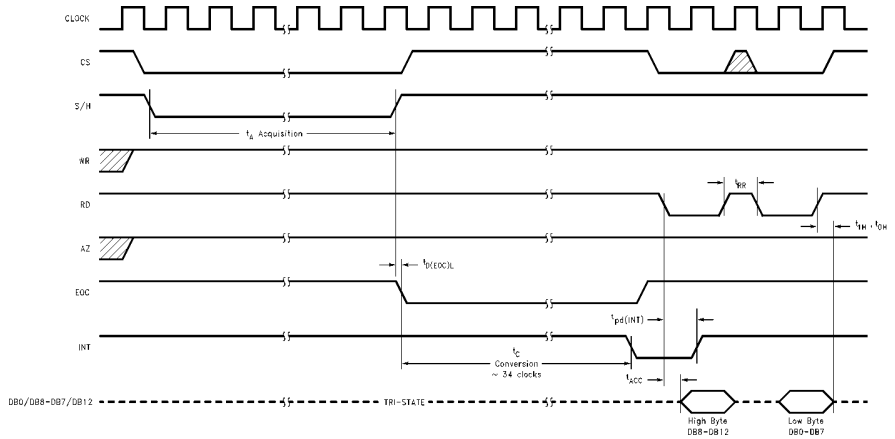
Timing Diagrams (Continued)

Using $\overline{WR}$ Control to Start a Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



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Using $\overline{S}$/H Control to Start a Conversion without Auto-Zero ($\overline{AZ}$ = 1, $\overline{CAL}$ = 1)



TL/H/11024–19

1.0 Pin Descriptions

DV_{CC} (24), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC1251 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass capacitors (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs bypass capacitors of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (12), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below +3.5 V_{DC}.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$, $\overline{RD}$ and $\overline{S}/H$ functions.

$\overline{RD}$ (23) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The conversion is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low. When this control line is used the end of the analog input voltage acquisition window is internally controlled by the ADC1251.

$\overline{S}/H$ (11) — The sample and hold control input. This control input can also be used to start a conversion. With $\overline{CS}$ low the falling edge of $\overline{S}/H$ starts the analog input acquisition window. The rising edge of $\overline{S}/H$ ends the acquisition window and starts a conversion.

CLKIN (8) — The external clock input pin. The typical clock frequency range is 500 kHz to 6.0 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC1251 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC1251 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (22) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (21) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0/DB8–DB7/DB12 (13–20) — The TRI-STATE output pins. Twelve bit plus sign output data access is accomplished using two successive $\overline{RD}$s of one byte each, high byte first (DB8–DB12). The data format used is two's complement sign bit extended with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC1251 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC1251 without the need for trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC1251 at any time, which ensures accuracy over temperature and time.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$ and $\overline{S}/H$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1399 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch errors are found. Correction factors for these errors are then stored in internal RAM.

A conversion can be initiated by taking $\overline{CS}$ and $\overline{WR}$ low. If $\overline{AZ}$ is low an Auto-Zero cycle, which takes approximately 26 clock periods, is inserted before the analog input is sampled and the actual conversion is started. $\overline{AZ}$ must remain low during the complete conversion sequence. After Auto-Zero the acquisition opens and the analog input is sampled for approximately 7 clock periods. If $\overline{AZ}$ is high, the Auto-Zero cycle is not inserted after the rising edge of $\overline{WR}$. In this case the acquisition window opens when the ADC1251 completes a conversion, signaled by the rising edge of EOC. At the end of the acquisition window EOC goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

2.0 Functional Description (Continued)

A conversion sequence can also be controlled by the $\overline{S}$/H and $\overline{CS}$ inputs. Taking $\overline{CS}$ and $\overline{S}$/H low starts the acquisition window for the analog input voltage. The rising edge of $\overline{S}$/H immediately puts the A/D in the hold mode and starts the conversion. Using $\overline{S}$/H will simplify synchronizing the end of the acquisition window to other signals, which may be necessary in a DSP environment.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC1251. Next $\overline{INT}$ goes low and EOC goes high to signal the end of the conversion.

The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0/DB8–DB7/DB12 output buffers. The high byte of data is relayed first on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
Bit 8	Bit 9	Bit 10	MSB	Sign Bit	Sign Bit	Sign Bit	Sign Bit

Taking $\overline{CS}$ and $\overline{RD}$ low a second time will relay the low byte of data on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7

The table in *Figure 3* summarizes the effect of the digital control inputs on the function of the ADC1251. The Test Mode, where $\overline{RD}$ and $\overline{S}$/H are high and $\overline{CS}$ and $\overline{CAL}$ are low, is used during manufacture to thoroughly check out the operation of the ADC1251. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

The ADC1251 is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ or $\overline{S}$/H low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore requiring an Auto-Cal cycle before the next conversion. When using $\overline{WR}$ or $\overline{S}$/H without Auto-Zero ($\overline{AZ}$ = 1) to start a conversion, a new conversion can be restarted only after EOC has gone high, signaling the end of the current conversion. When using $\overline{WR}$ with Auto-Zero ($\overline{AZ}$ = 0) a new conversion can be restarted during the first 26 clock periods after the rising edge of $\overline{WR}$ (t_Z) or after EOC has returned high without corrupting the Auto-Cal correction factors.

The Calibration Cycle cannot be reset once started. On power-up the ADC1251 automatically goes through a Calibration Cycle that takes typically 1399 clock cycles. For reasons that will be discussed in Section 3.8, a new calibration cycle needs to be started after the completion of the automatic one.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 4* is an example of a very stable reference that is appropriate for use with the ADC1251.

Digital Control Inputs						A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{S}$/H	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊓	⊓	1	1	1	1	Start Conversion without Auto-Zero
⊓	1	⊓	1	1	1	Start Conversion synchronous with rising edge of $\overline{S}$/H without Auto-Zero
⊓	1	1	⊓	1	1	Read Conversion Result without Auto-Zero
⊓	⊓	1	1	1	0	Start Conversion with Auto-Zero
⊓	1	1	⊓	1	0	Read Conversion Result with Auto-Zero
1	X	1	X	⊓	X	Start Calibration Cycle
0	X	X	1	0	X	Test Mode (DB2, DB3, DB5, and DB6 become active)

FIGURE 3. Function of the A/D Control Inputs

3.0 Analog Considerations (Continued)

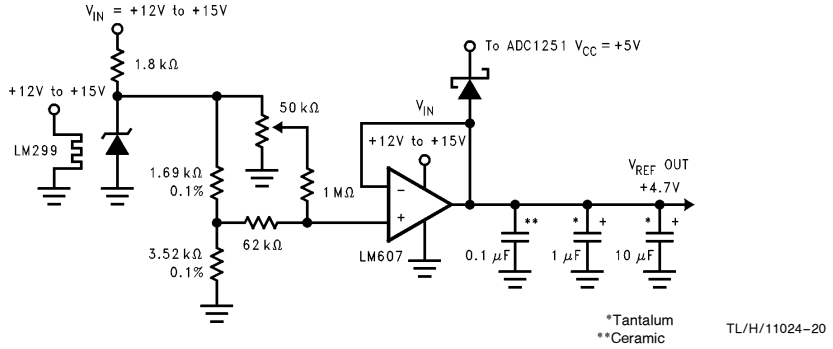


FIGURE 4. Low Drift Extremely Stable Reference Circuit

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 ACQUISITION WINDOW

As shown in the timing diagrams there are three different methods of starting a conversion, each of which affects the acquisition window and timing.

With Auto-Zero high a conversion can be started with the $\overline{WR}$ or $\overline{S}$/H controls. In either method of starting a conversion the rising edge of EOC signals the actual beginning of the acquisition window. At this time a voltage spike may be noticed on the analog input of the ADC1251 whose amplitude is dependent on the input voltage and the source resistance. The timing diagrams for these two methods of starting a conversion do not show the acquisition window starting at this time because the acquisition time (t_A) must start after the conversion result high and low bytes have been read. This is necessary since activating and deactivating the digital outputs (DB0/DB7–DB8/DB12) causes current fluctuations in the ADC1251's internal DV_{CC} lines. This generates digital noise which couples into the capacitive ladder that stores the analog input voltage. Therefore, the time interval between the rising edge of EOC and the second read is inappropriate for analog input voltage acquisition.

When $\overline{WR}$ is used to start a conversion with $\overline{AZ}$ low the Auto-Zero cycle is inserted before the acquisition window. In this method the acquisition window is internally controlled by the ADC1251 and lasts for approximately 7 clock periods. Since the acquisition window needs to be at least 3.5 μs at all times, when using Auto-Zero the maximum clock frequency is limited to 2 MHz. The zero error with the Auto-Zero cycle is production tested at a clock frequency of 1.75 MHz. This accommodates easy switching between a conversion with the Auto-Zero cycle (f_{CLK} = 1.75 MHz) and without (f_{CLK} = 3.5 MHz) as shown in *Figure 5*.

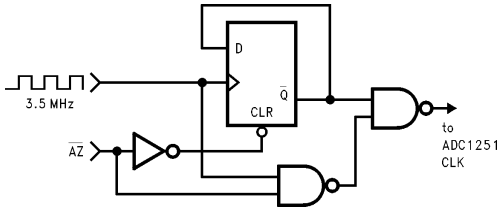


FIGURE 5. Switching between a Conversion with and without Auto-Zero when Using $\overline{WR}$ Control

3.3 INPUT CURRENT

Because the input network of the ADC1251 is made up of a switch and a network of capacitors a charging current will flow into or out of (depending on the input voltage polarity) the analog input pin (V_{IN}) on the start of the analog input sampling period. The peak value of this current will depend on the actual input voltage applied and the source resistance.

3.4 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.0 Analog Considerations (Continued)

3.5 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.6 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 6*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With $t_A = 3.5\ \mu s$, $R_S \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.7 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the Auto-Zero or -Cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors should be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.8 THE CALIBRATION CYCLE

On power up the ADC1251 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full scale, offset, and linearity errors down to the specified limits. Full scale error typically changes ± 0.2 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if Auto-Zero is used to correct the zero error change. Since Auto-Zero cannot be activated with $\overline{S}$/H conversion method it may be necessary to do a calibration cycle more than once.

3.9 THE AUTO-ZERO CYCLE

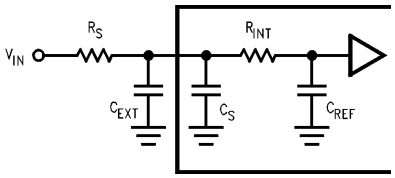
To correct for any change in the zero (offset) error of the A/D, the Auto-Zero cycle can be used. It may be necessary to do an Auto-Zero cycle whenever the ambient temperature changes significantly. (See the curve titled ''Zero Error Change vs Ambient Temperature'' in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ± 1 LSB. An Auto-Zero cycle will maintain the zero error to ± 1 LSB or less.

4.0 Dynamic Performance

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) is calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/(N + D) are shown in the table of Electrical Characteristics, and spectral plots are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) drops 3 dB).



TL/H/11024–22

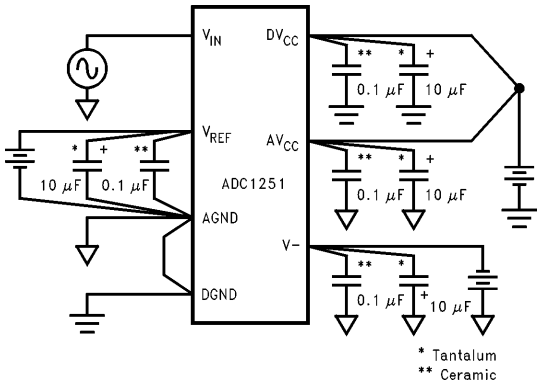
FIGURE 6. Analog Input Equivalent Circuit

4.0 Dynamic Performance (Continued)

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC1251 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC1251 when using the $\overline{S}$/H control to start a conversion, the hold command is generated by the rising edge of $\overline{S}$/H. The delay between the rising edge of $\overline{S}$/H and the time that the ADC1251 actually holds the input signal is the aperture time. For the ADC1251, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC1251 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

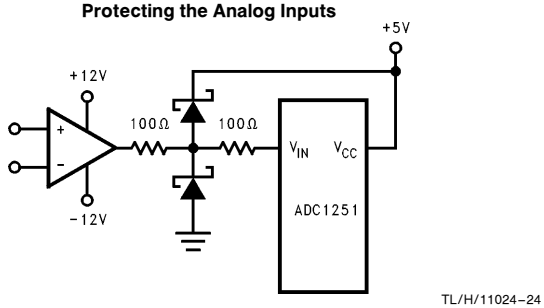
5.0 Typical Applications

Power Supply Bypassing



TL/H/11024–23

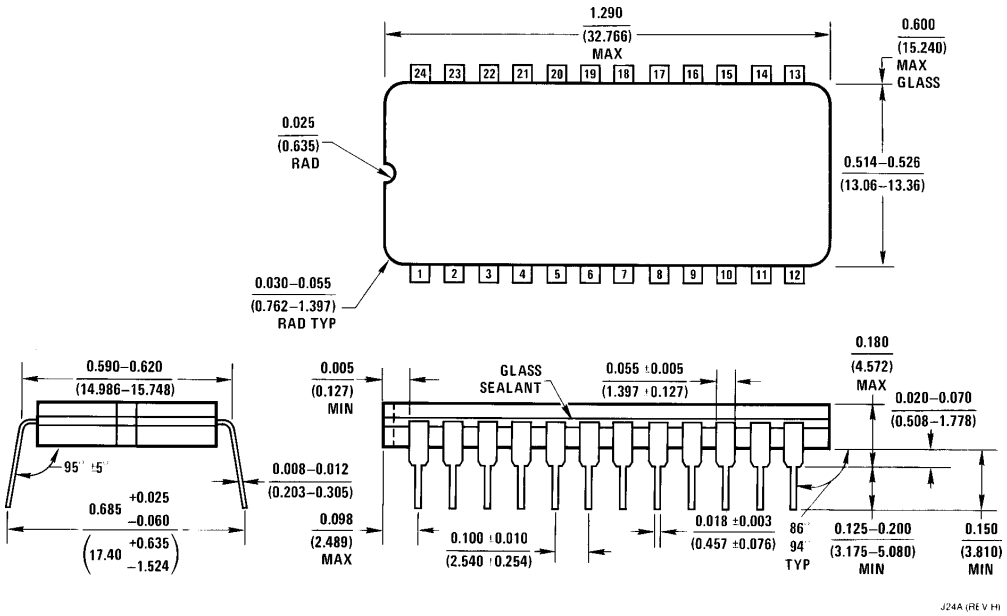
Protecting the Analog Inputs



TL/H/11024–24

Note: External protection diodes should be able to withstand the op amp current limit.

Physical Dimensions inches (millimeters)



Order Number ADC1251CMJ, ADC1251CMJ/883, ADC1251BIJ or ADC1251CIJ
NS Package Number J24A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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