

FSQ0565R, FSQ0765R

Green-Mode Fairchild Power Switch (FPS™) for Quasi-Resonant Operation - Low EMI and High Efficiency

Features

- Optimized for Quasi-Resonant Converter (QRC)
- Low EMI through Variable Frequency Control and AVS (Alternating Valley Switching)
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Simple Scheme for Sync Voltage Detection
- Pulse-by-Pulse Current Limit
- Various Protection functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output Short Protection (OSP)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage Sense FET (650V)
- Built-in Soft-Start (15ms)

Applications

- Power Supply for LCD TV and Monitor, VCR, SVR, STB, and DVD & DVD Recorder
- Adapter

Related Resources

Visit: <http://www.fairchildsemi.com/apnotes/> for:

- AN-4134: *Design Guidelines for Offline Forward Converters Using Fairchild Power Switch (FPS™)*
- AN-4137: *Design Guidelines for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*
- AN-4140: *Transformer Design Consideration for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*
- AN-4141: *Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- AN-4145: *Electromagnetic Compatibility for Power Converters*
- AN-4147: *Design Guidelines for RCD Snubber of Flyback*
- AN-4148: *Audible Noise Reduction Techniques for Fairchild Power Switch Fairchild Power Switch(FPS™) Applications*
- AN-4150: *Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch (FPS™)*

Description

A Quasi-Resonant Converter (QRC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ-series is an integrated Pulse-Width Modulation (PWM) controller and SenseFET specifically designed for quasi-resonant operation and Alternating Valley Switching (AVS). The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for a loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSQ-series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of quasi-resonant switching flyback converters.

Ordering Information

| Product Number | PKG. (5) | Operating Temp. | Current Limit | R _{DS(ON)} Max. | Maximum Output Power ⁽¹⁾ | | | | Replaces Devices |
|----------------|------------|-----------------|---------------|--------------------------|--|---------------------------|------------------------|---------------------------|-------------------------|
| | | | | | 230V _{AC} ±15% ⁽²⁾ | | 85-265V _{AC} | | |
| | | | | | Adapter ⁽³⁾ | Open Frame ⁽⁴⁾ | Adapter ⁽³⁾ | Open Frame ⁽⁴⁾ | |
| FSQ0565R | TO-220F-6L | -25 to +85°C | 3.0A | 2.2Ω | 70W | 80W | 41W | 60W | FSCM0565R FSDM0565RB |
| FSQ0765R | TO-220F-6L | -25 to +85°C | 3.5A | 1.6Ω | 80W | 90W | 48W | 70W | FSCM0765R FSDM0765RB |

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. Pb-free package per JEDEC J-STD-020B.

Application Diagram

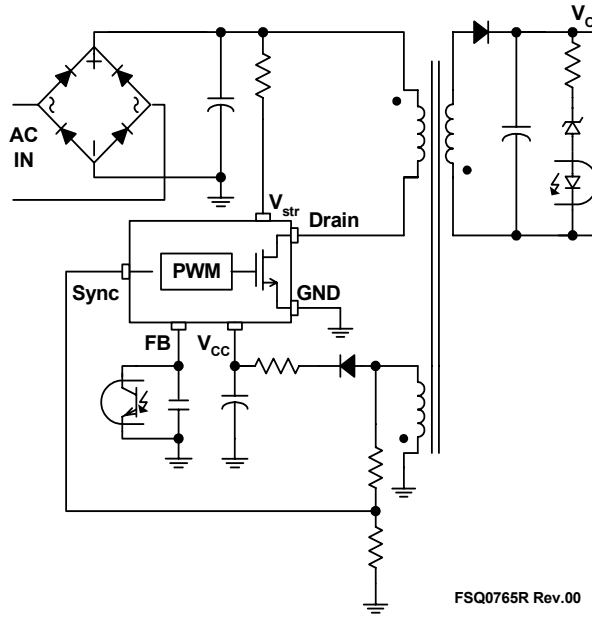


Figure 1. Typical Flyback Application

Internal Block Diagram

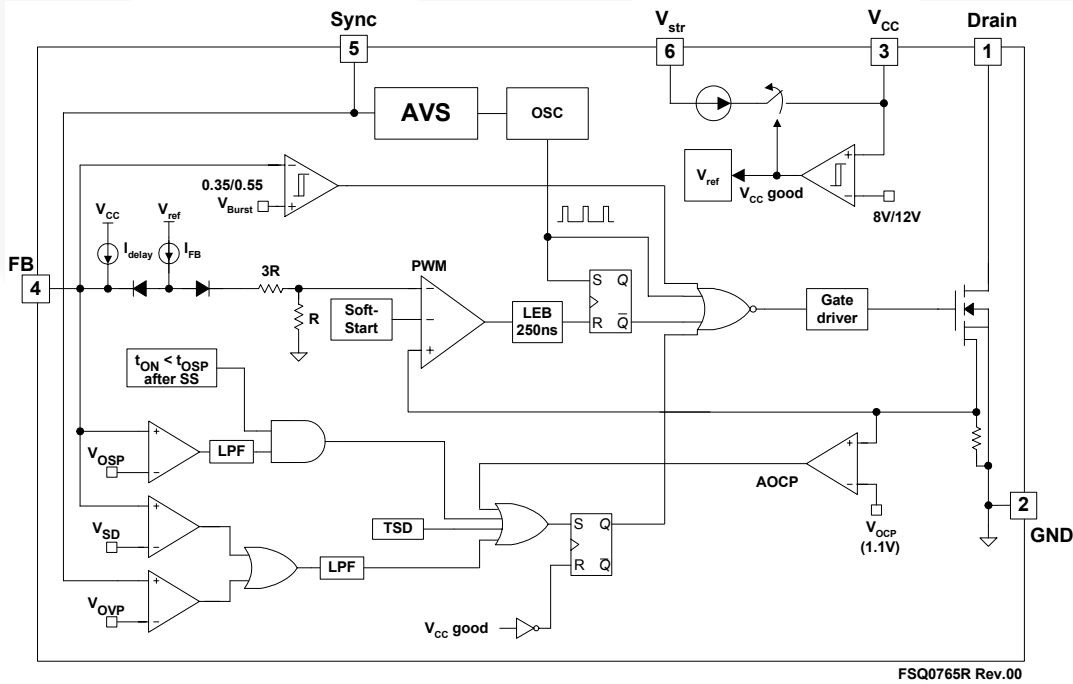


Figure 2. Internal Block Diagram

Pin Configuration

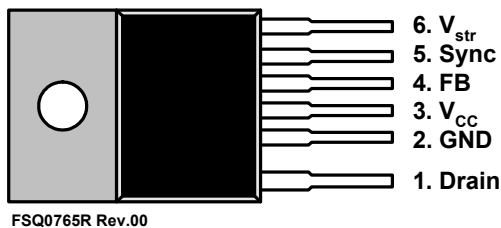


Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|-----------|--|
| 1 | Drain | SenseFET drain. High-voltage power SenseFET drain connection. |
| 2 | GND | Ground. This pin is the control ground and the SenseFET source. |
| 3 | V_{CC} | Power Supply. This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation. |
| 4 | FB | Feedback. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the FPS. |
| 5 | Sync | Sync. This pin is internally connected to the sync-detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 1.2V/1.0V. |
| 6 | V_{str} | Start-up. This pin is connected directly, or through a resistor, to the high-voltage DC link. At start-up, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source is disabled. It is not recommended to connect V_{str} and Drain together. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A = 25^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | | Min. | Max. | Unit |
|------------|--|----------|---------------------------|------|------------------|
| V_{str} | V _{str} Pin Voltage | | 500 | | V |
| V_{DS} | Drain Pin Voltage | | 650 | | V |
| V_{CC} | Supply Voltage | | | 20 | V |
| V_{FB} | Feedback Voltage Range | | -0.3 | 13 | V |
| V_{Sync} | Sync Pin Voltage | | -0.3 | 11 | V |
| I_{DM} | Drain Current Pulsed | FSQ0565R | | 11 | A |
| | | FSQ0765R | | 15 | A |
| I_D | Continuous Drain Current ⁽⁶⁾ | FSQ0565R | $T_C = 25^\circ\text{C}$ | 2.8 | A |
| | | | $T_C = 100^\circ\text{C}$ | 1.7 | |
| | | FSQ0765R | $T_C = 25^\circ\text{C}$ | 3.8 | A |
| | | | $T_C = 100^\circ\text{C}$ | 2.4 | |
| E_{AS} | Single Pulsed Avalanche Energy ⁽⁷⁾ | FSQ0565R | | 190 | mJ |
| | | FSQ0765R | | 370 | mJ |
| P_D | Total Power Dissipation($T_C=25^\circ\text{C}$) | | | 45 | W |
| T_J | Operating Junction Temperature | | Internally limited | | $^\circ\text{C}$ |
| T_A | Operating Ambient Temperature | | -25 | +85 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | | -55 | +150 | $^\circ\text{C}$ |
| ESD | Electrostatic Discharge Capability, Human Body Model | | 2.0 | | kV |
| | Electrostatic Discharge Capability, Charged Device Model | | 2.0 | | kV |

Notes:

6. Repetitive rating: Pulse width limited by maximum junction temperature.

7. $L=14\text{mH}$, starting $T_J=25^\circ\text{C}$.

Thermal Impedance

$T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Package | Value | Unit |
|---------------|---|------------|-------|--------------------|
| θ_{JA} | Junction-to-Ambient Thermal Resistance ⁽⁸⁾ | TO-220F-6L | 50 | $^\circ\text{C/W}$ |
| θ_{JC} | Junction-to-Case Thermal Resistance ⁽⁹⁾ | | 2.8 | $^\circ\text{C/W}$ |

Notes:

8. Free standing with no heat-sink under natural convection.

9. Infinite cooling condition - refer to the SEMI G30-88.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|---|---|---|------|------|------|
| SENSEFET SECTION | | | | | | |
| BV _{DSS} | Drain Source Breakdown Voltage | V _{CC} = 0V, I _D = 100μA | 650 | | | V |
| I _{DSS} | Zero-Gate-Voltage Drain Current | V _{DS} = 560V | | | 250 | μA |
| R _{DS(ON)} | Drain-Source On-State Resistance | FSQ0565R | T _J = 25°C, I _D = 0.5A | 1.76 | 2.20 | Ω |
| | | FSQ0765R | T _J = 25°C, I _D = 0.5A | 1.4 | 1.6 | |
| C _{OSS} | Output Capacitance | FSQ0565R | V _{GS} = 0V, V _{DS} = 25V, f = 1MHz | 78 | | pF |
| | | FSQ0765R | | 100 | | |
| t _{d(on)} | Turn-On Delay Time | FSQ0565R | V _{DD} = 350V, I _D = 25mA | 22 | | ns |
| | | FSQ0765R | | 25 | | |
| t _r | Rise Time | FSQ0565R | V _{DD} = 350V, I _D = 25mA | 52 | | ns |
| | | FSQ0765R | | 60 | | |
| t _{d(off)} | Turn-Off Delay Time | FSQ0565R | V _{DD} = 350V, I _D = 25mA | 95 | | ns |
| | | FSQ0765R | | 115 | | |
| t _f | Fall Time | FSQ0565R | V _{DD} = 350V, I _D = 25mA | 50 | | ns |
| | | FSQ0765R | | 65 | | |
| CONTROL SECTION | | | | | | |
| t _{ON,MAX} | Maximum On Time | T _J = 25°C | 8.8 | 10.0 | 11.2 | μs |
| t _B | Blanking Time | T _J = 25°C, V _{sync} = 5V | 13.2 | 15.0 | 16.8 | μs |
| t _W | Detection Time Window | T _J = 25°C, V _{sync} = 0V | | 6.0 | | μs |
| f _S | Initial Switching Frequency | | 59.6 | 66.7 | 75.8 | kHz |
| Δf _S | Switching Frequency Variation ⁽⁹⁾ | -25°C < T _J < 85°C | | ±5 | ±10 | % |
| t _{AVS} | AVS Triggering Threshold ⁽⁹⁾ | On Time | at V _{IN} = 240V _{DC} , L _m = 360μH (AVS triggered when V _{AVS} > spec & t _{AVS} < spec.) | 4.0 | | μs |
| V _{AVS} | | Feedback Voltage | | 1.2 | | V |
| t _{SW} | Switching Time Variance by AVS ⁽⁹⁾ | Sync = 500kHz sine input V _{FB} = 1.2V, t _{ON} = 4.0μs | 13.5 | | 20.5 | μs |
| I _{FB} | Feedback Source Current | V _{FB} = 0V | 700 | 900 | 1100 | μA |
| D _{MIN} | Minimum Duty Cycle | V _{FB} = 0V | | | 0 | % |
| V _{START} | UVLO Threshold Voltage | | 11 | 12 | 13 | V |
| V _{STOP} | | After turn-on | 7 | 8 | 9 | V |
| t _{S/S} | Internal Soft-Start Time | With free-running frequency | | 17.5 | | ms |
| BURST-MODE SECTION | | | | | | |
| V _{BURH} | Burst-Mode Voltages | T _J = 25°C, t _{PD} = 200ns ⁽⁸⁾ | 0.45 | 0.55 | 0.65 | V |
| V _{BURL} | | | 0.25 | 0.35 | 0.45 | V |
| Hysteresis | | | | 200 | | mV |

Continued on the following page...

Electrical Characteristics (Continued)

 $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | | Condition | Min. | Typ. | Max. | Unit |
|-----------------------------|--|------------------------------|--|------|------|------|------------------|
| PROTECTION SECTION | | | | | | | |
| I_{LIMIT} | Peak Current Limit | FSQ0565R | $T_J = 25^\circ\text{C}$, $di/dt = 370\text{mA}/\mu\text{s}$ | 2.64 | 3.00 | 3.36 | A |
| | | FSQ0765R | $T_J = 25^\circ\text{C}$, $di/dt = 460\text{mA}/\mu\text{s}$ | 3.08 | 3.50 | 3.92 | |
| V_{SD} | Shutdown Feedback Voltage | | $V_{CC} = 15\text{V}$ | 5.5 | 6.0 | 6.5 | V |
| I_{DELAY} | Shutdown Delay Current | | $V_{FB} = 5\text{V}$ | 4 | 5 | 6 | μA |
| t_{LEB} | Leading-Edge Blanking Time ⁽⁹⁾ | | | | 250 | | ns |
| t_{OSP} | Output Short Protection ⁽⁹⁾ | Threshold Time | $T_J = 25^\circ\text{C}$ OSP triggered when $t_{ON} < t_{OSP}$, $V_{FB} > V_{OSP}$ & lasts longer than t_{OSP_FB} | | 1.2 | 1.4 | μs |
| V_{OSP} | | Threshold Feedback Voltage | | 1.8 | 2.0 | | V |
| t_{OSP_FB} | | Feedback Blanking Time | | 2 | 2.5 | 3.0 | μs |
| T_{SD} | Thermal Shutdown ⁽⁹⁾ | Shutdown Temperature | | 125 | 140 | 155 | $^\circ\text{C}$ |
| Hys | | Hysteresis | | | 60 | | |
| SYNC SECTION | | | | | | | |
| V_{SH1} | Sync Threshold Voltage 1 | | $V_{CC} = 15\text{V}$, $V_{FB} = 2\text{V}$ | 1.0 | 1.2 | 1.4 | V |
| V_{SL1} | | | | 0.8 | 1.0 | 1.2 | |
| t_{sync} | Sync Delay Time ⁽⁹⁾⁽¹⁰⁾ | | | | 230 | | ns |
| V_{SH2} | Sync Threshold Voltage 2 | | $V_{CC} = 15\text{V}$, $V_{FB} = 2\text{V}$ | 4.3 | 4.7 | 5.1 | V |
| V_{SL2} | | | | 4.0 | 4.4 | 4.8 | |
| V_{CLAMP} | Low Clamp Voltage | | $I_{SYNC_MAX} = 800\mu\text{A}$ $I_{SYNC_MIN} = 50\mu\text{A}$ | 0.0 | 0.4 | 0.8 | V |
| V_{OVP} | Over-Voltage Protection | Threshold Voltage | $V_{CC} = 15\text{V}$, $V_{FB} = 2\text{V}$ | 7 | 8 | 9 | V |
| t_{OVP} | | Blanking Time ⁽⁹⁾ | | 1.0 | 1.7 | 2.4 | μs |
| TOTAL DEVICE SECTION | | | | | | | |
| I_{OP} | Operating Supply Current (Control Part Only) | | $V_{CC} = 13\text{V}$ | 1 | 3 | 5 | mA |
| I_{START} | Start Current | | $V_{CC} = 10\text{V}$ (before V_{CC} reaches V_{START}) | 350 | 450 | 550 | μA |
| I_{CH} | Start-up Charging Current | | $V_{CC} = 0\text{V}$, $V_{STR} = \text{minimum } 50\text{V}$ | 0.65 | 0.85 | 1.00 | mA |
| V_{STR} | Minimum V_{STR} Supply Voltage | | | | 26 | | V |

Notes:

8. Propagation delay in the control IC.
9. Guaranteed by design; not tested in production.
10. Includes gate turn-on time.

Comparison Between FSDM0x65RNB and FSQ-Series

| Function | FSDM0x65RE | FSQ-Series | FSQ-Series Advantages |
|----------------------|--------------------------|--|---|
| Operation Method | Constant Frequency PWM | Quasi-Resonant Operation | <ul style="list-style-type: none"> ■ Improved efficiency by valley switching ■ Reduced EMI noise ■ Reduced components to detect valley point |
| EMI Reduction | Frequency Modulation | Reduce EMI Noise | <ul style="list-style-type: none"> ■ Valley Switching ■ Inherent Frequency Modulation ■ Alternate Valley Switching |
| Hybrid Control | | CCM or AVS Based on Load and Input Condition | <ul style="list-style-type: none"> ■ Improves efficiency by introducing hybrid control |
| Burst-Mode Operation | Burst-Mode Operation | Advanced Burst-Mode Operation | <ul style="list-style-type: none"> ■ Improved standby power by AVS in burst-mode |
| Strong Protections | OLP, OVP | OLP, OVP, AOCP, OSP | <ul style="list-style-type: none"> ■ Improved reliability through precise AOCP ■ Improved reliability through precise OSP |
| TSD | 145°C without Hysteresis | 140°C with 60°C Hysteresis | <ul style="list-style-type: none"> ■ Stable and reliable TSD operation ■ Converter temperature range |

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

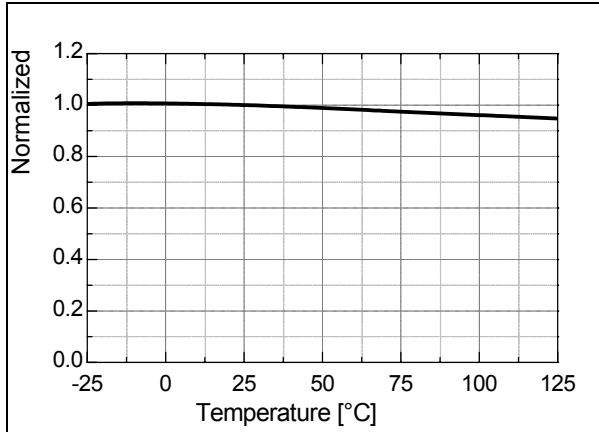


Figure 4. Operating Supply Current (I_{OP}) vs. T_A

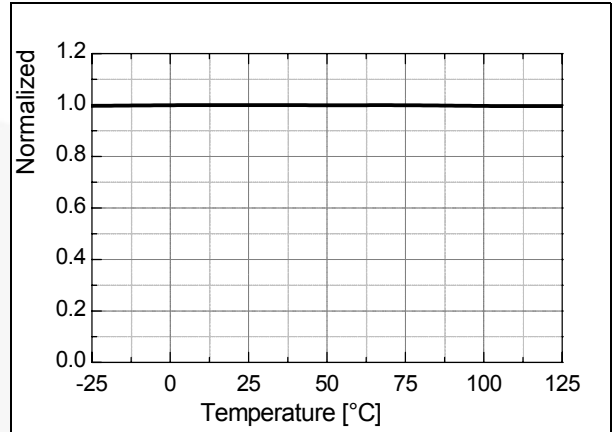


Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

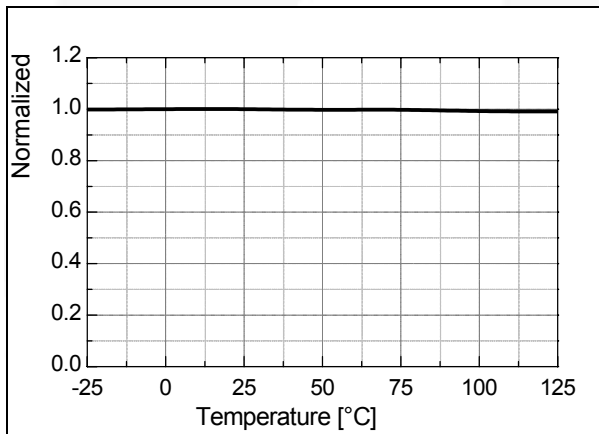


Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

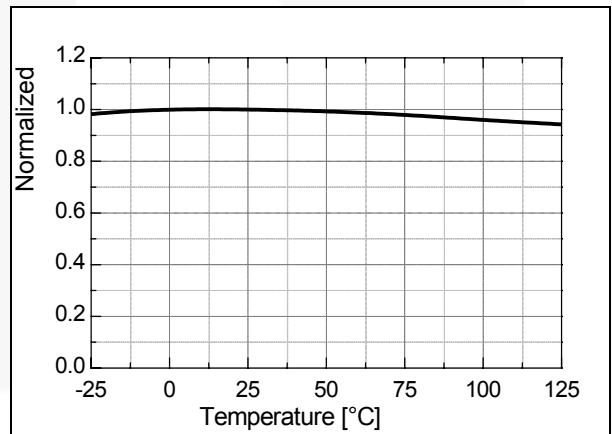


Figure 7. Start-up Charging Current (I_{CH}) vs. T_A

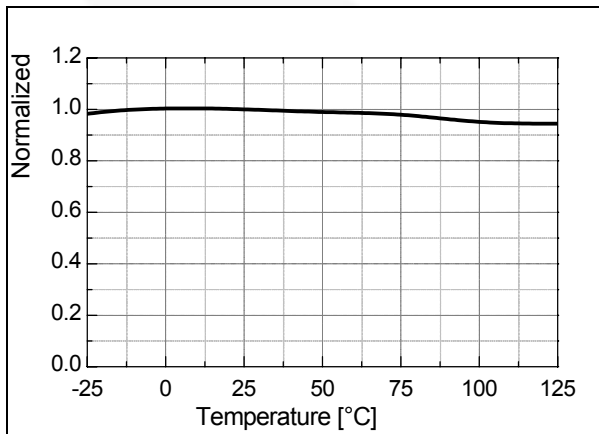


Figure 8. Initial Switching Frequency (f_S) vs. T_A

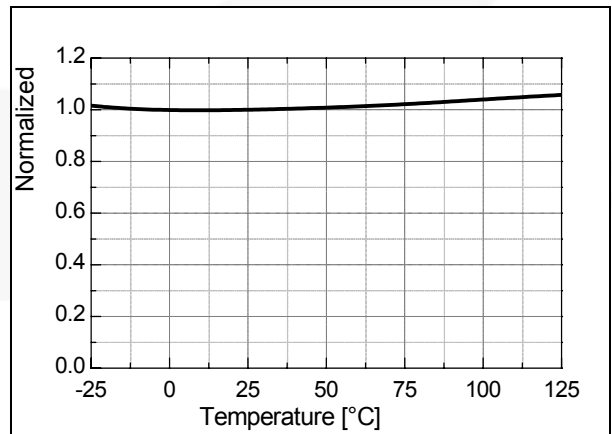


Figure 9. Maximum On Time ($t_{ON.MAX}$) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

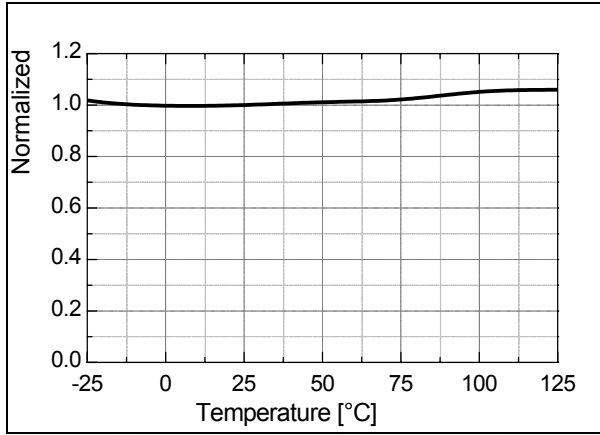


Figure 10. Blanking Time (t_B) vs. T_A

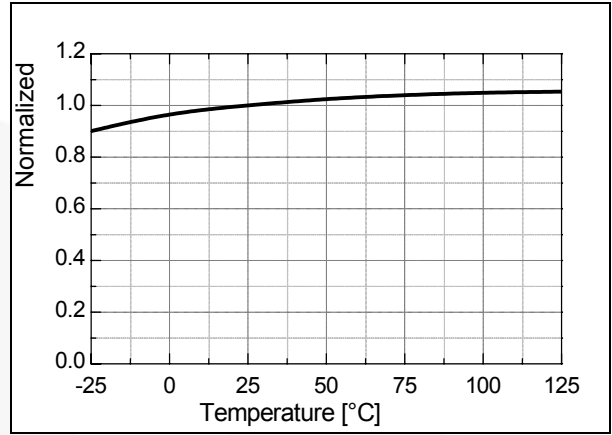


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

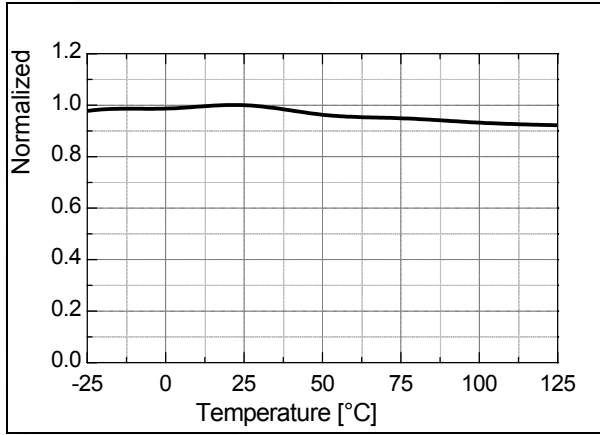


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

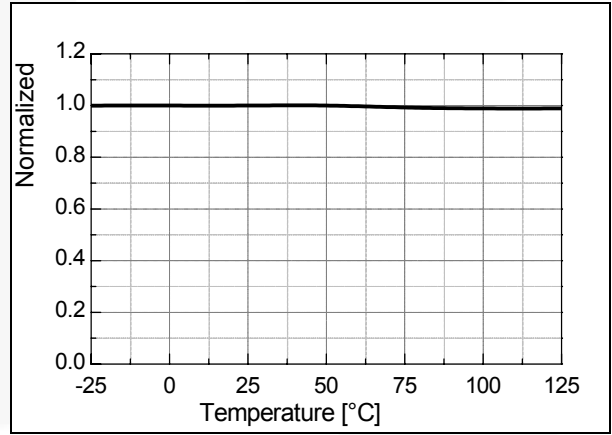


Figure 13. Burst-Mode High Threshold Voltage (V_{burh}) vs. T_A

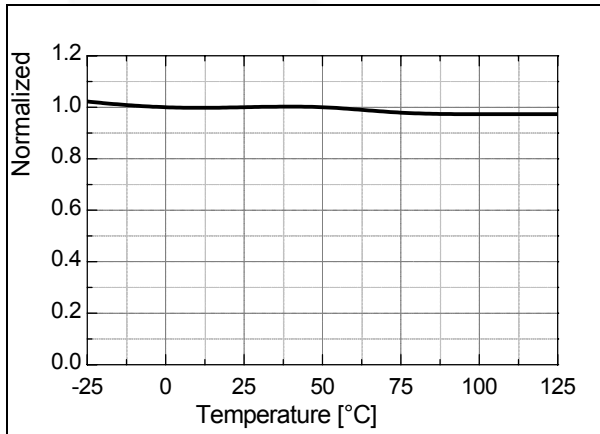


Figure 14. Burst-Mode Low Threshold Voltage (V_{burl}) vs. T_A

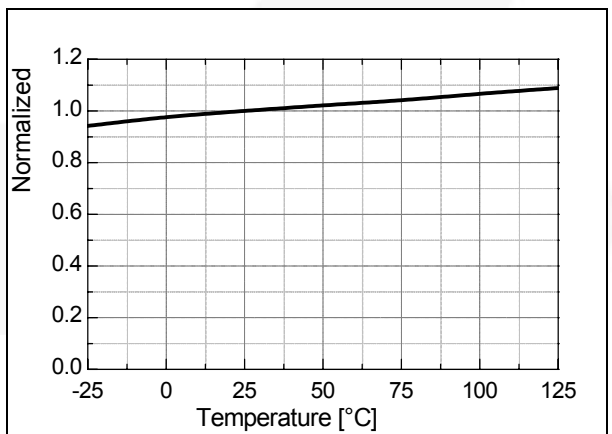


Figure 15. Peak Current Limit (I_{LIM}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

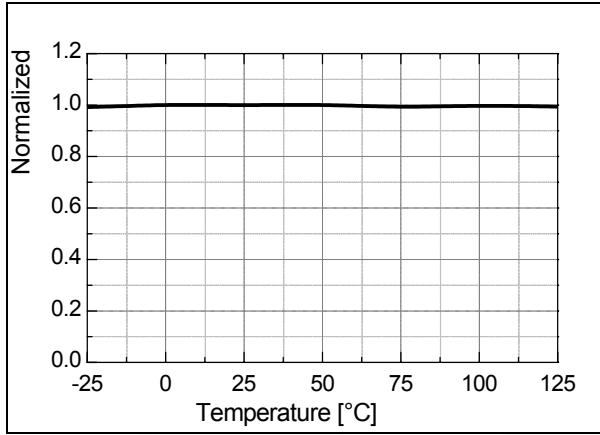


Figure 16. Sync High Threshold Voltage 1 (V_{SH1}) vs. T_A

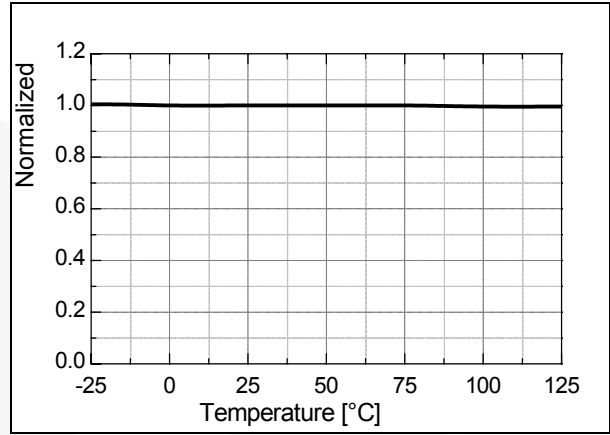


Figure 17. Sync Low Threshold Voltage 1 (V_{SL1}) vs. T_A

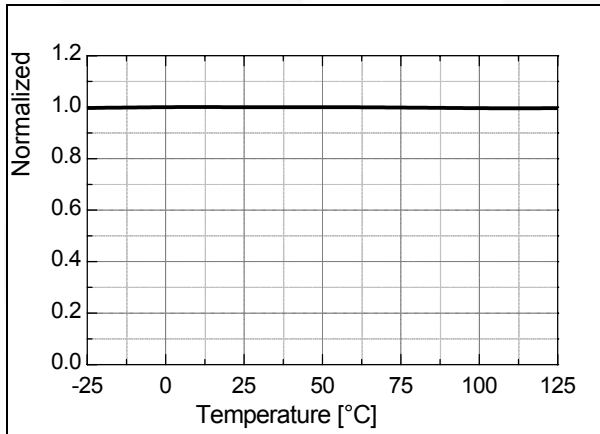


Figure 18. Shutdown Feedback Voltage (V_{SD}) vs. T_A

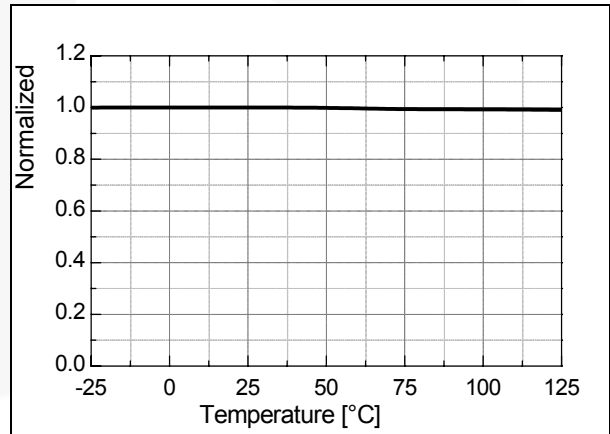


Figure 19. Over-Voltage Protection (V_{OV}) vs. T_A

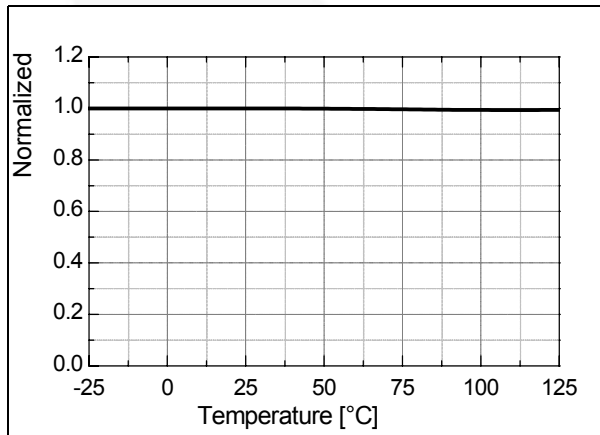


Figure 20. Sync High Threshold Voltage 2 (V_{SH2}) vs. T_A

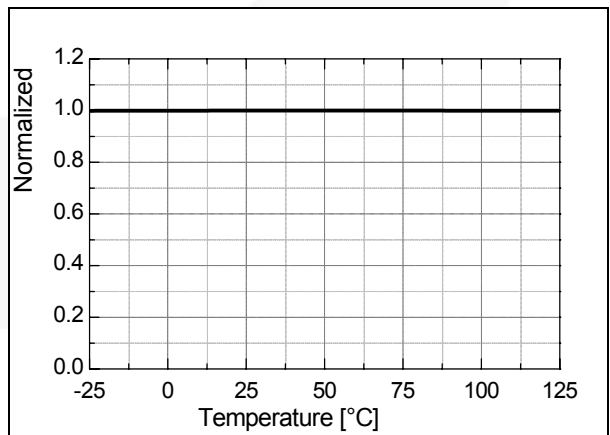


Figure 21. Sync Low Threshold Voltage 2 (V_{SL2}) vs. T_A

Functional Description

1. Start-up: At start-up, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 22. When V_{CC} reaches 12V, the FPS™ begins switching and the internal high-voltage current source is disabled. The FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

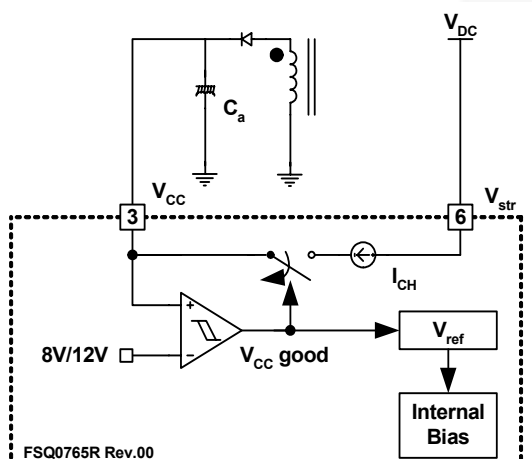


Figure 22. Start-up Circuit

2. Feedback Control: FPS employs current-mode control, as shown in Figure 23. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}^*), as shown in Figure 23. Assuming that the 0.9mA current source flows only through the internal resistor ($3R + R = 2.8k$), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}^* . Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

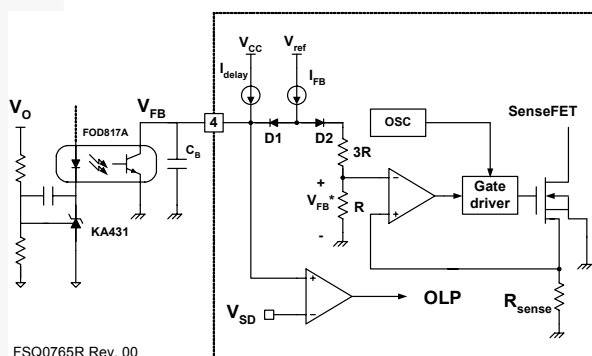


Figure 23. Pulse-Width-Modulation (PWM) Circuit

3. Synchronization: The FSQ-series employs a quasi-resonant switching technique to minimize the switching noise and loss. The basic waveforms of the quasi-resonant converter are shown in Figure 24. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, which is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 24.

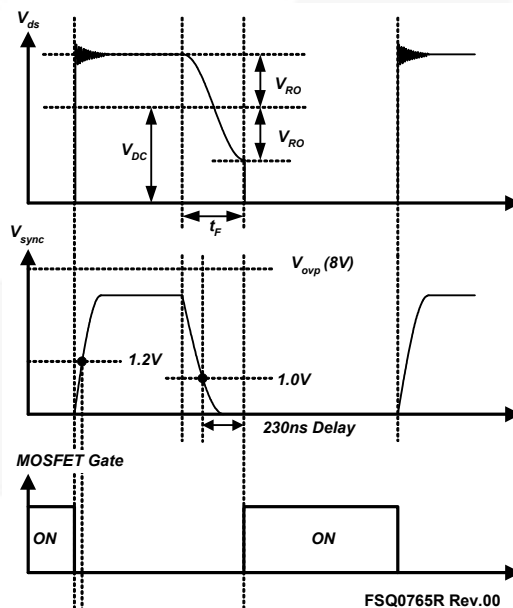


Figure 24. Quasi-Resonant Switching Waveforms

The switching frequency is the combination of blank time (t_B) and detection time window (t_W). In case of a heavy load, the sync voltage remains flat after t_B and waits for valley detection during t_W . This leads to a low switching frequency not suitable for heavy loads. To correct this drawback, additional timing is used. The timing conditions are described in Figures 25, 26, and 27. When the V_{sync} remains flat higher than 4.4V at the end of t_B that is t_x , the next switching cycle starts after internal delay time from t_x . In the second case, the next switching occurs on the valley when the V_{sync} goes below 4.4V within t_B . Once V_{sync} detects the first valley within t_B , the other switching cycle follows classical QRC operation.

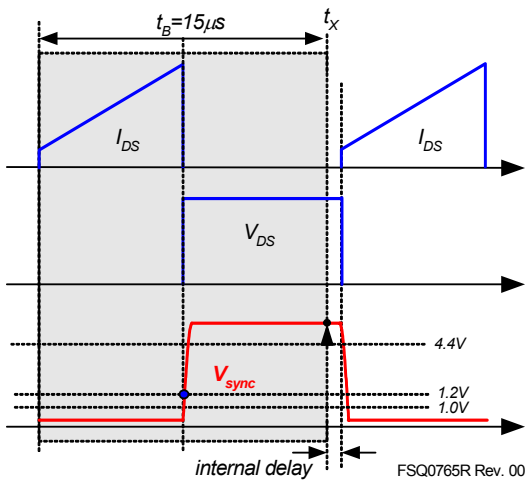


Figure 25. $V_{sync} > 4.4V$ at t_x

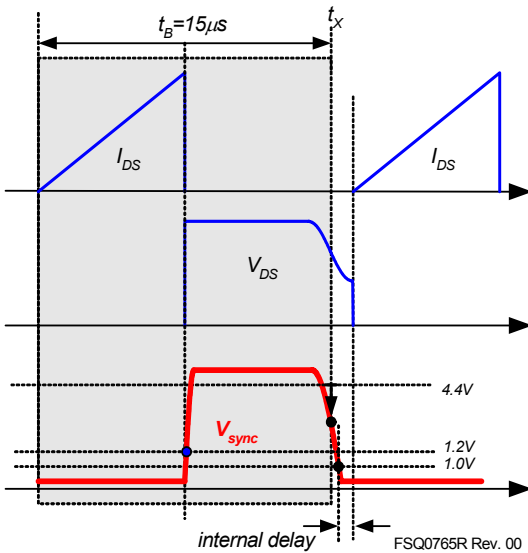


Figure 26. $V_{sync} < 4.4V$ at t_x

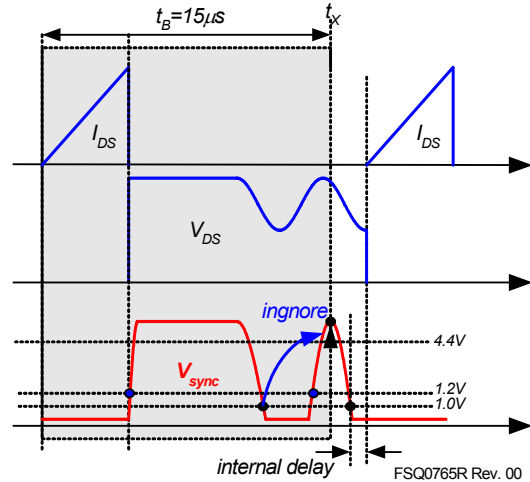


Figure 27. After V_{sync} Finds First Valley

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 8V, the protection is reset and the start-up circuit charges the V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12V, normal operation resumes. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

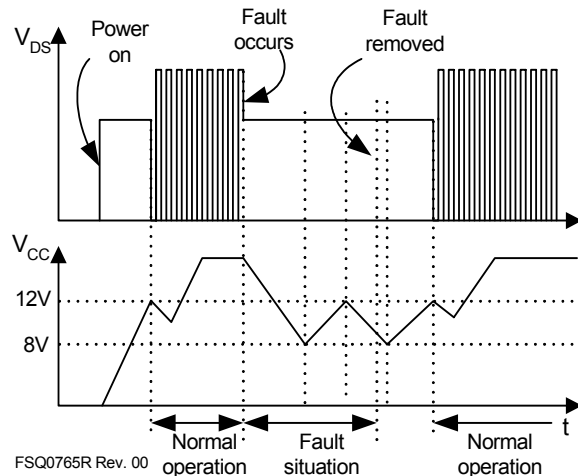


Figure 28. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 5 μ A current source starts to charge CB slowly up to V_{CC} . In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 29. The delay time for shutdown is the time required to charge C_{FB} from 2.5V to 6V with 5 μ A. A 20 ~ 50ms delay time is typical for most applications.

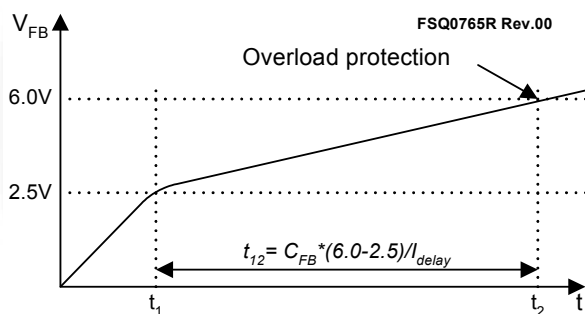


Figure 29. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has overload protection, it is not enough to protect the FSQ-series in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP circuit shown in Figure 30. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

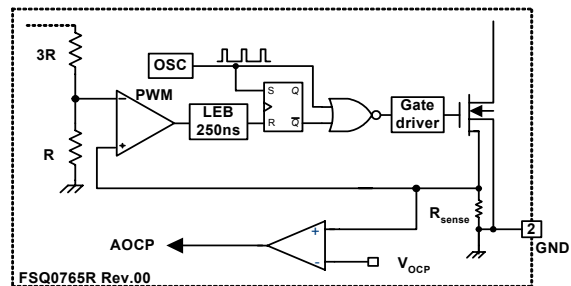


Figure 30. Abnormal Over-Current Protection

4.3 Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Such a steep current brings high voltage stress on drain of SenseFET when turned off. To protect the device from such an abnormal condition, OSP is included in the FSQ-series. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2V and the SenseFET turn-on time is lower than 1.2 μ s, the FPS recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{start} again. An abnormal condition output short is shown in Figure 31.

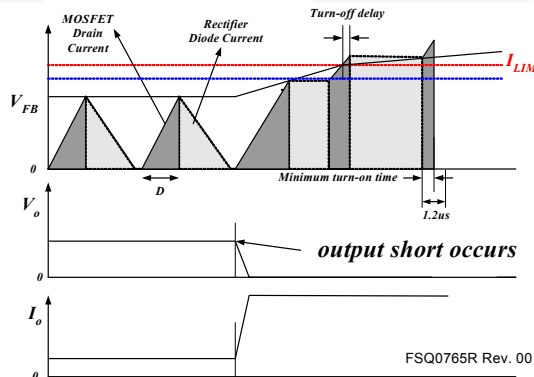


Figure 31. Output Short Waveforms

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-series

uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 8V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, there are two points considered, as depicted in Figure 32. The peak voltage of the sync signal should be designed below 6V and the spike of the SYNC pin must be as low as possible to avoid getting longer than t_{OVP} by decreasing the leakage inductance shown at V_{CC} winding coil.

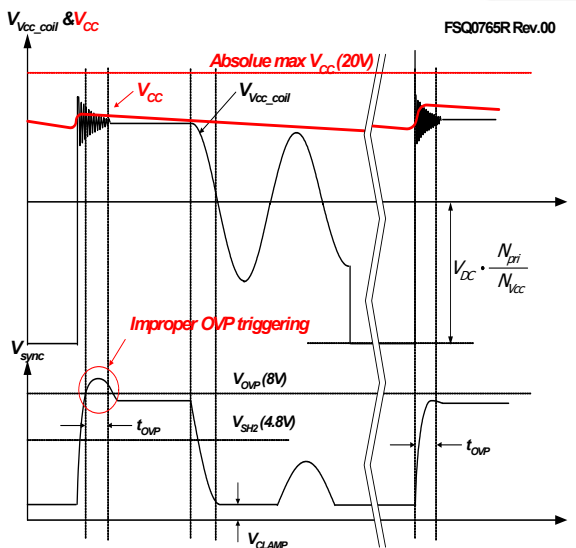


Figure 32. OVP Triggering

4.5 Thermal Shutdown with Hysteresis (TSD): The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormally high temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers IC shutdown. The IC recovers its operation when the junction temperature decreases 60°C from TSD temperature and V_{CC} reaches start-up voltage (V_{start}).

5. Soft-Start: The FPS has an internal soft-start circuit that increases PWM comparator inverting input voltage with the SenseFET current slowly after it starts up. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This mode helps prevent transformer saturation and reduces stress on the secondary diode during start-up.

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 33, the device automatically enters burst-mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

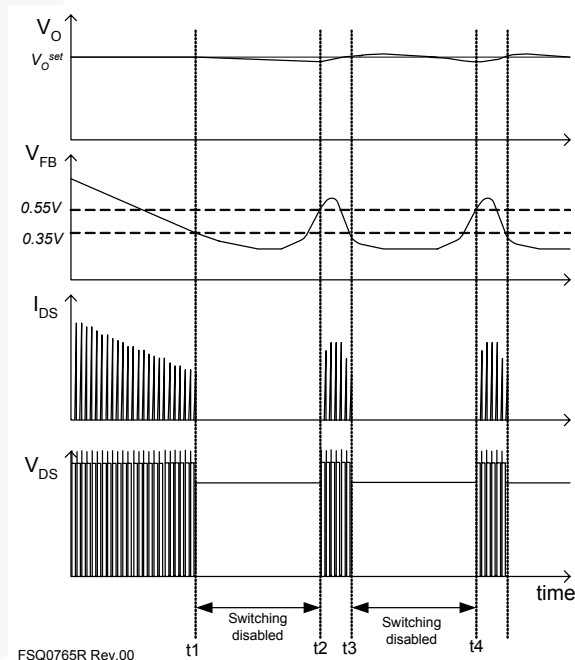


Figure 33. Waveforms of Burst Operation

7. Switching Frequency Limit: To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in quasi-resonant operation. However, this causes switching frequency to increase at light load conditions. As the load decreases or input voltage increases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light-load condition, as well as intermittent switching and audible noise. These problems create limitations for the quasi-resonant converter topology in a wide range of applications.

To overcome these problems, FSQ-series employs a frequency-limit function, as shown in Figures 34 and 35. Once the SenseFET is turned on, the next turn-on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figures 34 and Figure 35 (Cases A, B, and C).

If no valley is found during t_{w} , the internal SenseFET is forced to turn on at the end of t_w (Case D). Therefore, the devices have a minimum switching frequency of 48kHz and a maximum switching frequency of 67kHz.

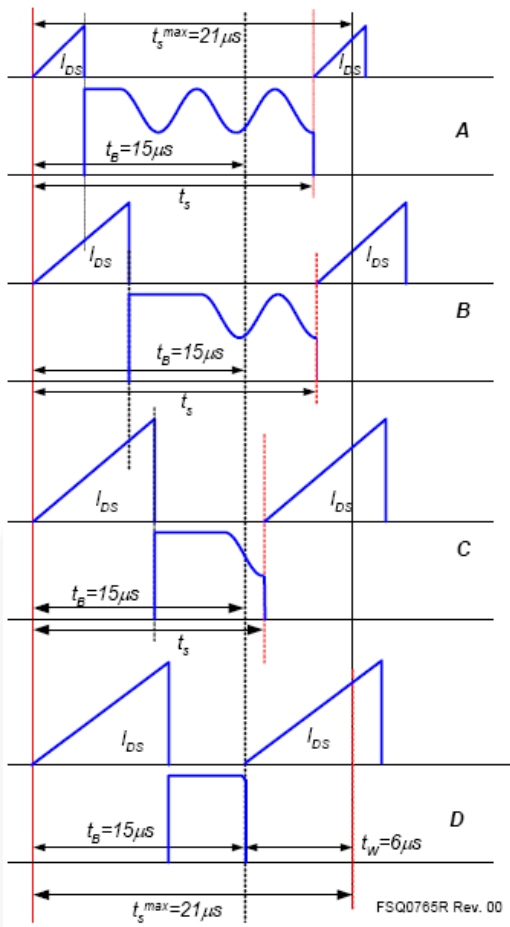


Figure 34. QRC Operation with Limited Frequency

8. AVS (Alternating Valley Switching): Due to the quasi-resonant operation with limited frequency, the switching frequency varies depending on input voltage, load transition, and so on. At high input voltage, the switching on time is relatively small compared to low input voltage. The input voltage variance is small and the switching frequency modulation width becomes small. To improve the EMI performance, AVS is enabled when input voltage is high and the switching on time is small.

Internally, quasi-resonant operation is divided into two categories; one is first valley switching and the other is second-valley switching after blanking time. In AVS, two successive occurrences of first-valley switching and the other two successive occurrences of second-valley switching is alternatively selected to maximize frequency modulation. As depicted in Figure 35, the switching frequency hops when the input voltage is high. The internal timing diagram of AVS is described in Figure 36.

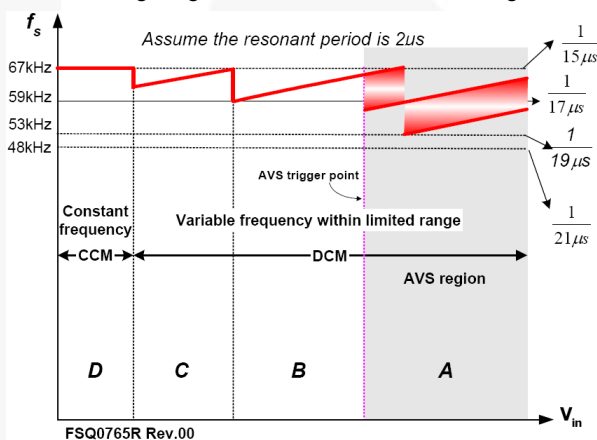


Figure 35. Switching Frequency Range

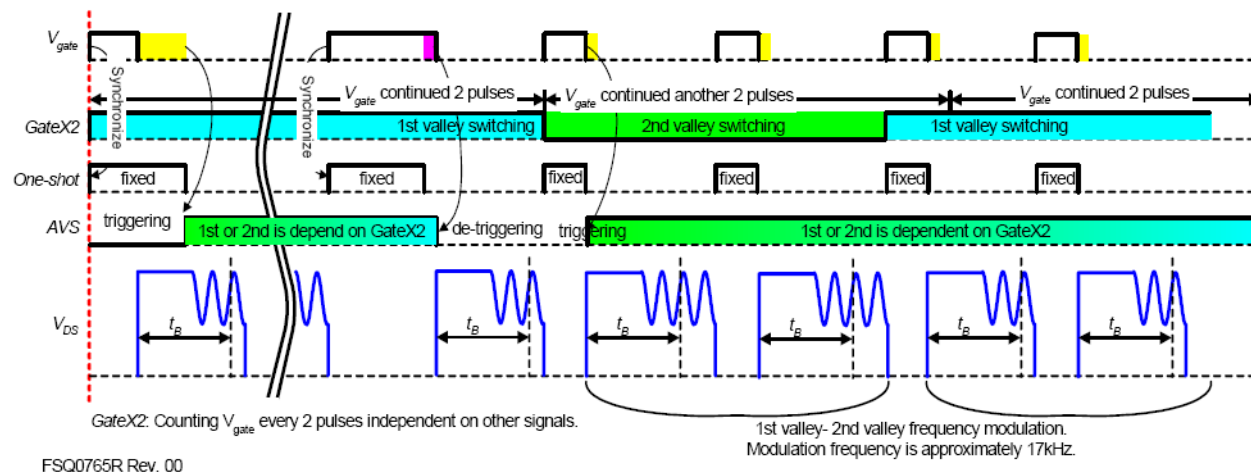


Figure 36. Alternating Valley Switching (AVS)

PCB Layout Guide

Due to the combined scheme, FPS shows better noise immunity than conventional PWM controller and MOSFET discrete solution. Further more, internal drain current sense eliminates the possibility of noise generation caused by a sensing resistor. There are some recommendations for PCB layout to enhance noise immunity and suppress natural noise inevitable in power-handling components.

There are typically two grounds in the conventional SMPS: power ground and signal ground. The power ground is the ground for primary input voltage and power, while the signal ground is ground for PWM controller. In FPS, those two grounds share the same pin, GND. Normally the separate grounds do not share the same trace and meet only at one point, the GND pin. More, wider patterns for both grounds are good for large currents by decreasing resistance.

Capacitors at the VCC and FB pins should be as close as possible to the corresponding pins to avoid noise from the switching device. Sometimes Mylar® or ceramic capacitors with electrolytic for V_{CC} is better for smooth operation. The ground of these capacitors needs to connect to the signal ground (not power ground).

The cathode of the snubber diode should be close to the drain pin to minimize stray inductance. The Y-capacitor between primary and secondary should be directly connected to the power ground of DC link to maximize surge immunity.

Because the voltage range of feedback and sync line is small, it is affected by the noise of the drain pin. Those traces should not draw across or close to the drain line.

When the heat sink is connected to the ground, it should be connected to the power ground. If possible, avoid using jumper wires for power ground and drain.

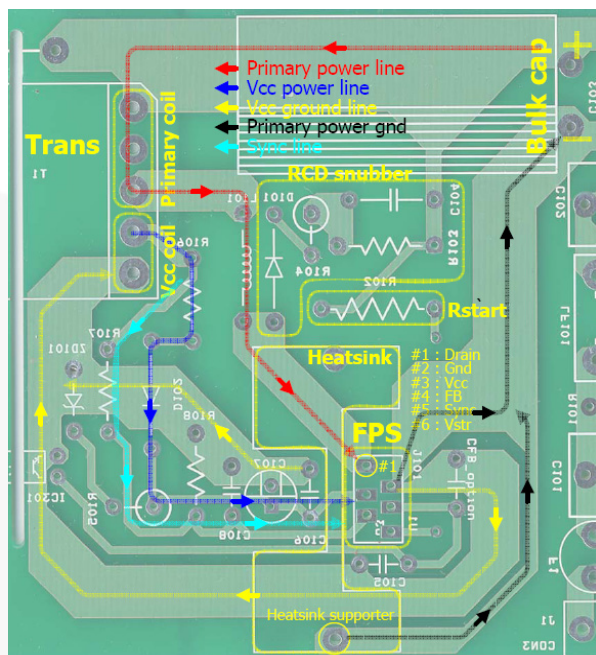


Figure 37. Recommended PCB Layout

Mylar® is a registered trademark of DuPont Teijin Films.

2. Transformer

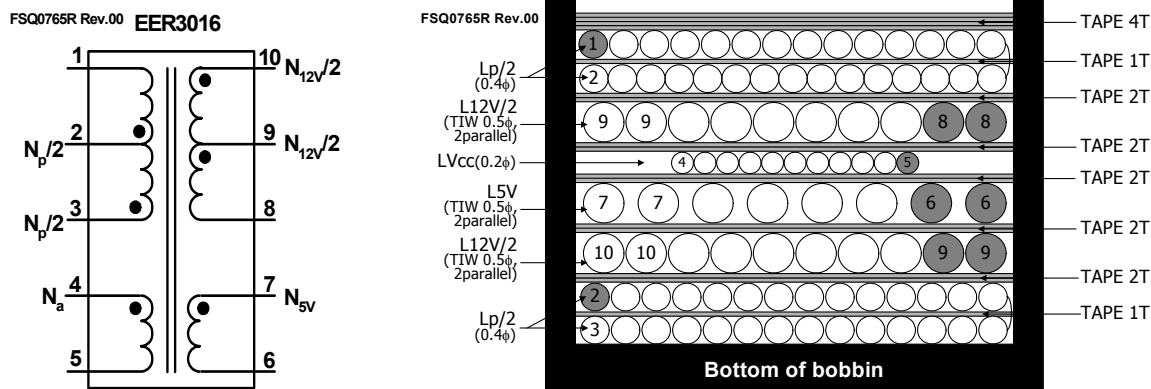


Figure 39. Transformer Schematic Diagram of FSQ0565R

3. Winding Specification

| Position | No | Pin (s→f) | Wire | Turns | Winding Method |
|--|--|-----------|--------------------------------|-------|--------------------------|
| ↑ Top ↓ Bottom | Insulation: Polyester Tape t = 0.025mm, 4 Layers | | | | |
| | $N_p/2$ | 2 → 1 | $0.4\phi \times 1$ | 20 | 2-Layer Solenoid Winding |
| | Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| | $N_{12V/2}$ | 9 → 8 | $0.5\phi \times 2(\text{TIW})$ | 4 | Center Solenoid Winding |
| | Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| | N_a | 4 → 5 | $0.15\phi \times 1$ | 10 | Center Solenoid Winding |
| | Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| | N_{5V} | 7 → 6 | $0.5\phi \times 2(\text{TIW})$ | 4 | Center Solenoid Winding |
| | Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| | $N_{12V/2}$ | 10 → 9 | $0.5\phi \times 2(\text{TIW})$ | 5 | Center Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | | |
| | $N_p/2$ | 3 → 2 | $0.4\phi \times 1$ | 32 | 2-Layer Solenoid Winding |

4. Electrical Characteristics

| | Pin | Specification | Remarks |
|------------|-------|---------------------------|----------------------|
| Inductance | 1 - 3 | $360\mu\text{H} \pm 10\%$ | 100kHz, 1V |
| Leakage | 1 - 3 | 15μH Maximum | Short all other pins |

5. Core & Bobbin

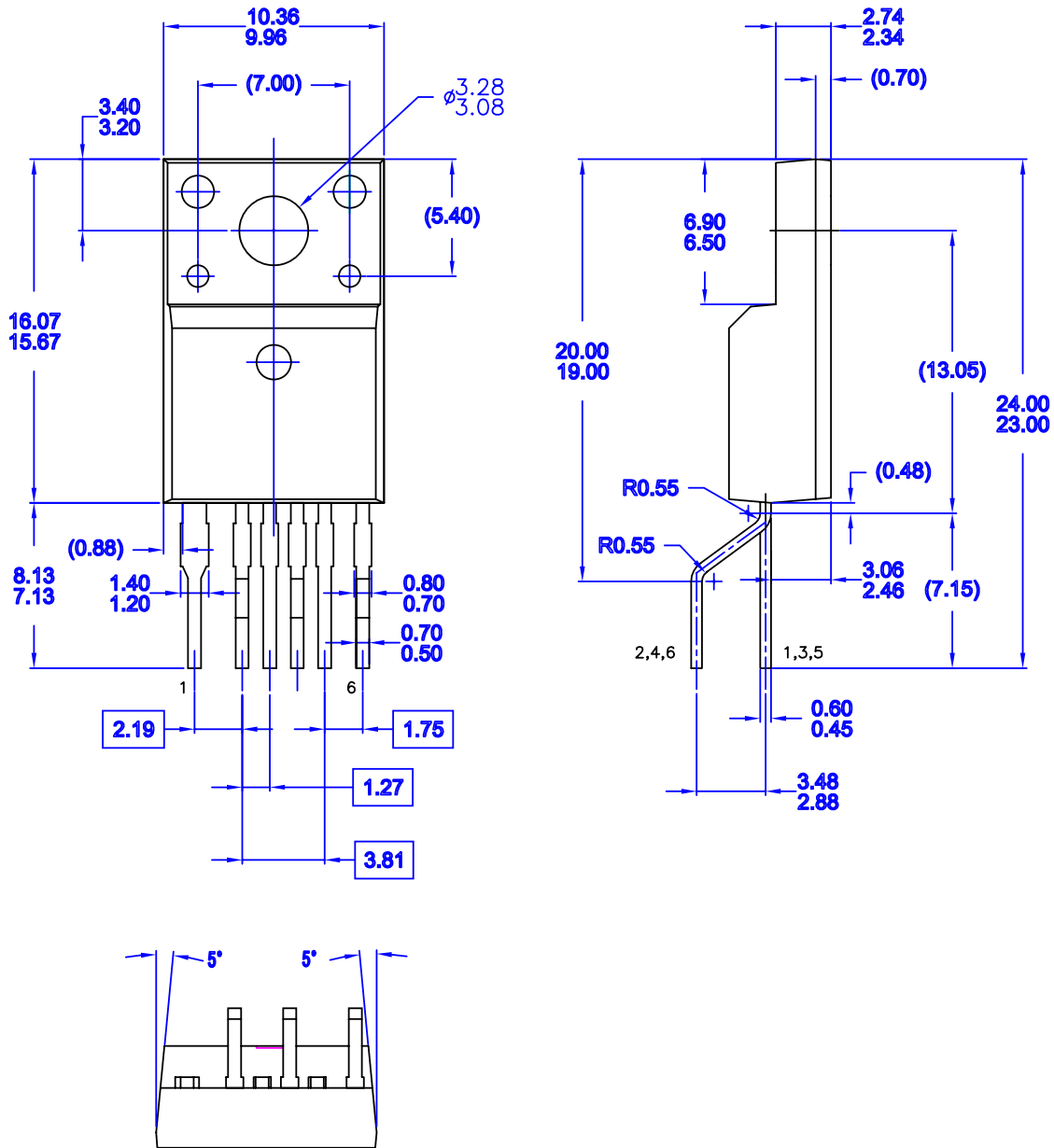
- Core: EER3016 ($A_e=109.7\text{mm}^2$)
- Bobbin: EER3016

6. Demo Board Part List

| Part | Value | Note | Part | Value | Note |
|------------------|--------------------------|--------------------------------|---------------------|---------------|-------------------------------------|
| Resistor | | | C205 | 47nF/50V | Ceramic Capacitor |
| R101 | 2MΩ | 1W | C301 | 4.7nF/1kV | Ceramic Capacitor |
| R102 | 68kΩ | 1/2W | Inductor | | |
| R103 | 33kΩ | 1W | L201 | 5μH | 5A Rating |
| R104 | 20Ω | 1W | L202 | 5μH | 5A Rating |
| R105 | 100Ω | <i>optional, 1/4W</i> | Diode | | |
| R107 | 18kΩ | 1/4W | D101 | IN4007 | 1A, 1000V General-Purpose Rectifier |
| R108 | 12kΩ | 1/4W | D102 | UF4004 | 1A, 400V Ultrafast Rectifier |
| R201 | 1kΩ | 1/4W | ZD101 | 1N4745A | 1W 16V Zener Diode (optional) |
| R202 | 1.2kΩ | 1/4W | D201 | MBRF10H100 | 10A, 100V Schottky Rectifier |
| R203 | 1.2kΩ | 1/4W | D202 | MBRF1060 | 10A, 60V Schottky Rectifier |
| R204 | 5.2kΩ | 1/4W | IC | | |
| R205 | 4.7kΩ | 1/4W | IC101 | FSQ0565R | FPS™ |
| Capacitor | | | IC201 | KA431 (TL431) | Voltage Reference |
| C101 | 150nF/275V _{AC} | Box Capacitor | IC202 | FOD817A | Opto-Coupler |
| C102 | 150nF/275V _{AC} | Box Capacitor | Fuse | | |
| C103 | 100μF/400V | Electrolytic Capacitor | Fuse | 2A/250V | |
| C104 | 4.7nF/630V | Film Capacitor | NTC | | |
| C105 | 33nF/50V | Ceramic Capacitor | RT101 | 5D-9 | |
| C106 | 100nF/50V | SMD (1206) | Bridge Diode | | |
| C107 | 47μF/50V | Electrolytic Capacitor | BD101 | 2KBP06M2N257 | Bridge Diode |
| C201 | 1000μF/25V | Low ESR Electrolytic Capacitor | Line Filter | | |
| C202 | 1000μF/25V | Low ESR Electrolytic Capacitor | LF101 | 34mH | |
| C203 | 1000μF/10V | Low ESR Electrolytic Capacitor | Transformer | | |
| C204 | 1000μF/10V | Low ESR Electrolytic Capacitor | T1 | EER3016 | Ae=109.7mm ² |

Package Dimensions

TO-220F-6L (Forming)



MKT-TO220A06revB

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) LEADFORM OPTION A

Figure 40. 6-Lead, TO-220 Package



TRADEMARKS

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|-------------------------------------|----------------------|----------------------------|----------------------------------|
| ACEx® | Green FPS™ | Power247® | SuperSOT™-8 |
| Build it Now™ | Green FPS™ e-Series™ | POWEREDGE® | SyncFET™ |
| CorePLUS™ | GTO™ | Power-SPM™ | The Power Franchise® |
| CROSSVOLT™ | <i>i-Lo</i> ™ | PowerTrench® | power the franchise |
| CTL™ | IntelliMAX™ | Programmable Active Droop™ | TinyBoost™ |
| Current Transfer Logic™ | ISOPLANAR™ | QFET® | TinyBuck™ |
| EcoSPARK® | MegaBuck™ | QST™ | TinyLogic® |
| F ® | MICROCOUPLER™ | QT Optoelectronics™ | TINYOPTO™ |
| Fairchild® | MicroFET™ | Quiet Series™ | TinyPower™ |
| Fairchild Semiconductor® | MicroPak™ | RapidConfigure™ | TinyPWM™ |
| FACT Quiet Series™ | MillerDrive™ | SMART START™ | TinyWire™ |
| FACT® | Motion-SPM™ | SPM® | μSerDes™ |
| FAST® | OPTOLOGIC® | STEALTH™ | UHC® |
| FastvCore™ | OPTOPLANAR® | SuperFET™ | UniFET™ |
| FPS™ | | SuperSOT™-3 | VCX™ |
| FRFET® | | SuperSOT™-6 | |
| Global Power Resource SM | PDP-SPM™ | | |
| | Power220® | | |

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|------------------------|--|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only. |

Rev. I31