TEXAS INSTRUMENTS
LM74502-Q1, LM74502H-Q1
SNOSDE0A – FEBRUARY 2022 – REVISED MAY 2022

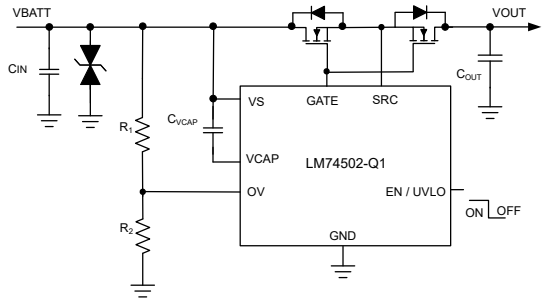
LM74502-Q1, LM74502H-Q1 Automotive Low IQ Reverse Polarity Protection Controller with Overvoltage Protection

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3.2-V to 65-V input range (3.9-V start-up)
- –65-V input reverse voltage rating
- Integrated charge pump to drive
  - External back-to-back N-Channel MOSFETs
  - External high side switch MOSFET
  - External reverse polarity protection MOSFET
- Gate drive variants
  - LM74502-Q1: 60-µA peak gate drive source capacity
  - LM74502H-Q1: 11-mA peak gate drive source capacity
- 2-A peak gate sink capacity
- 1-µA shutdown current (EN/UVLO = Low)
- 45-µA typical operating quiescent current (EN/UVLO = High)
- Adjustable overvoltage and undervoltage protection
- Meets automotive ISO7637 pulse 1 transient requirements with additional TVS diode
- Available in 8-pin SOT-23 package 2.90 mm × 1.60 mm

2 Applications

- Body electronics and lighting
- Automotive infotainment systems – digital cluster, head unit
- Automotive USB hubs



LM74502-Q1 Typical Application Schematic

3 Description

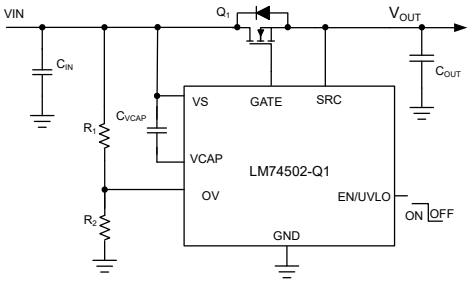
The LM74502-Q1, LM74502H-Q1 is an automotive AEC-Q100 qualified controller which operates in conjunction with an external back-to-back connected N-channel MOSFETs as a low loss reverse polarity protection and load disconnect solution. The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V, 24-V and 48-V automotive battery systems. The 3.2-V input voltage support is particularly well suited for severe cold crank requirements in automotive systems. The device can withstand and protect the loads from negative supply voltages down to –65 V. The LM74502-Q1, LM74502H-Q1 does not have reverse current blocking and is suitable for input reverse polarity protection of loads that can potentially deliver energy back to the input supply such as automotive body control module motor loads.

The LM74502-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The high voltage rating of LM74502-Q1 helps to simplify the system designs for automotive ISO7637 protection. With the enable pin low, the controller is off and draws approximately 1 µA of current, thus offering low system current when put into sleep mode. LM74502-Q1 offers programmable overvoltage and undervoltage protection which cuts off the load from the input source in case of these faults.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74502-Q1 LM74502H-Q1	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LM74502-Q1 as a Load Switch Controller with Overvoltage Protection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2022) to Revision A (May 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

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5 Device Comparison Table

Parameter	LM74502-Q1	LM74502H-Q1
Gate drive strength	60 µA	11 mA

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6 Pin Configuration and Functions

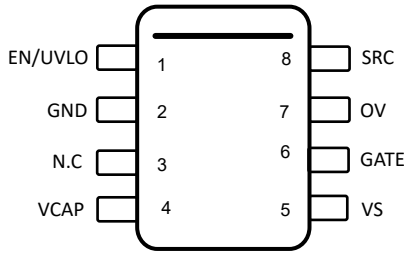


Figure 6-1. DDF Package 8-Pin SOT-23 LM74502-Q1, LM74502H-Q1 Top View

Table 6-1. LM74502-Q1, LM74502H-Q1 Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	EN/UVLO input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling this pin low below V(ENF) makes the device enter into low Iq shutdown mode. For UVLO, connect an external resistor ladder from input supply to EN/UVLO to GND.
2	GND	G	Ground pin
3	N.C	—	No connection
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	VS	I	Input power supply pin to the controller. Connect a 100-nF capacitor across VS and GND pins.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	OV	I	Adjustable overvoltage threshold input. Connect a resistor ladder across input and output. When the voltage at OV pin exceeds the overvoltage cutoff threshold, then the GATE is pulled low. GATE turns ON when the OV pin voltage goes below the OV protection falling threshold. Connect OV pin to GND if OV feature is not used.
8	SRC	I	Source pin. Connect to common source point of external back-to-back connected N-channel MOSFETs or the source pin of the high side switch MOSFET.

(1) I = Input, O = Output, G = GND

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS to GND	–65	65	V
	EN/UVLO, OV to GND, $V_{(VS)}$ > 0 V	–0.3	65	V
	EN/UVLO, OV, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(65 + $V_{(VS)}$)	
	SRC to GND, $V_{(VS)}$ ≤ 0 V		($V_{(VS)}$ + 0.3)	V
Input Pins	SRC to GND, $V_{(VS)}$ > 0 V	–(70 – $V_{(VS)}$)	$V_{(VS)}$	V
Output Pins	GATE to SRC	0	15	V
	VCAP to VS	–0.3	15	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN, VCAP, SRC, VS)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS to GND	–60		60	V
	EN/UVLO, OV, SRC to GND	–60		60	
External capacitance	VS	22			nF
	VCAP to VS	0.1			µF
External MOSFET max V_{GS} rating	GATE to SRC	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *electrical characteristics*
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

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7.4 Thermal Information

THERMAL METRIC[1]		LM74502-Q1 LM74502H-Q1 DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		4		60	V
$V_{(VS_POR)}$	VS POR Rising threshold				3.9	V
	VS POR Falling threshold		2.2	2.8	3.1	V
$V_{(VS\ POR(Hys))}$	VS POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN/UVLO)}$ = 0 V		0.9	1.5	µA
$I_{(Q)}$	Operating Quiescent Current	I_{GND}		45	65	µA
$I_{(REV)}$	I(S) leakage current during input reverse polarity	0 V ≤ $V_{(VS)}$ ≤ – 65 V		100	150	µA
ENABLE INPUT						
$V_{(EN_UVLOF)}$	Enable/UVLO falling threshold		1.027	1.14	1.235	V
$V_{(EN_UVLOR)}$	Enable/UVLO rising threshold		1.16	1.24	1.32	
$V_{(ENF)}$	Enable threshold voltage for low I_Q shutdown		0.32	0.64	0.94	V
$V_{(EN_Hys)}$	Enable Hysteresis		38	90	132	mV
$I_{(EN)}$	Enable sink current	$V_{(EN/UVLO)}$ = 12 V		3	5	µA
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(GATE)} – V_{(SRC)}$ = 5 V	40	60	77	µA
$I_{(GATE)}$	Peak source current	$V_{(GATE)} – V_{(SRC)}$ = 5 V, LM74502H-Q1	3	11		mA
	Peak sink current	EN/UVLO= High to Low $V_{(GATE)} – V_{(SRC)}$ = 5 V		2370		mA
RDS_{ON}	discharge switch RDS_{ON}	EN/UVLO = High to Low $V_{(GATE)} – V_{(SRC)}$ = 100 mV	0.4		2	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} – V_{(S)}$ = 7 V	162	300	600	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} – V_{(S)}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(VS)}$	Charge pump voltage at $V_{(S)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA	8			V
$V_{(VCAP)} – V_{(VS)}$	Charge pump turn-on voltage		10.3	11.6	13	V
$V_{(VCAP)} – V_{(VS)}$	Charge pump turn-off voltage		11	12.4	13.9	V
$V_{(VCAP)} – V_{(VS)}$	Charge Pump Enable comparator Hysteresis		0.45	0.8	1.25	V

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7.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(VS)}$ UV release at rising edge		5.7	6.5	7.5	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(VS)}$ UV threshold at falling edge		5.05	5.4	6.2	V
OVERVOLTAGE PROTECTION						
$V_{(OVR)}$	Overvoltage threshold input, rising		1.165	1.25	1.333	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.063	1.143	1.222	V
$V_{(OV_Hys)}$	OV Hysteresis			100		mV
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 5 V	12	50	110	nA

7.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	EN high to Gate Turn-on delay	$V_{(VCAP)}$ > $V_{(VCAP\ UVLOR)}$, $V_{(EN/UVLO)}$ step from (0 V to > $V_{(EN_UVLOR)}$) , $V_{(GATE-SRC)}$ > 5 V, $C_{(GATE-SRC)}$ = 4.7 nF, LM74502H-Q1		75	110	µs
$t_{EN_OFF(deg)_GATE}$	GATE Turn-off delay during EN/UVLO	$V_{(EN/UVLO)}$ ↓ to $V_{(GATE-SRC)}$ < 1 V, $C_{(GATE-SRC)}$ = 4.7 nF		2		µs
$t_{OVP_OFF(deg)_GATE}$	GATE Turn-off delay during OV	$V_{(OV)}$ ↑ to $V_{(GATE-SRC)}$ < 1 V, $C_{(GATE-SRC)}$ = 4.7 nF		0.6	1	µs
$t_{OVP_ON(deg)_GATE}$	GATE Turn-on delay during OV	$V_{(OV)}$ ↓ to $V_{(GATE-SRC)}$ > 5 V, $C_{(GATE-SRC)}$ = 4.7 nF LM74502H-Q1,		5	10	µs

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7.7 Typical Characteristics

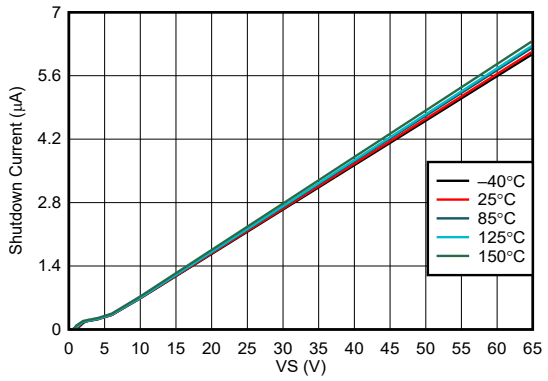


Figure 7-1. Shutdown Supply Current vs Supply Voltage

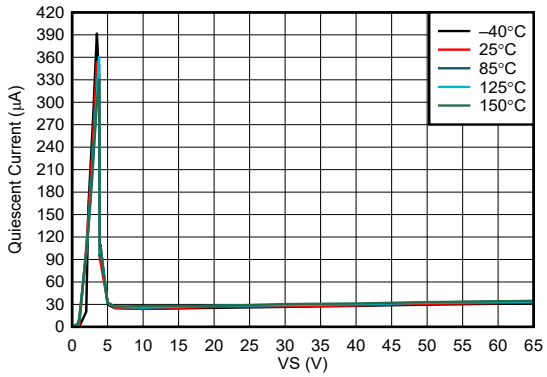


Figure 7-2. Operating Quiescent Current vs Supply Voltage

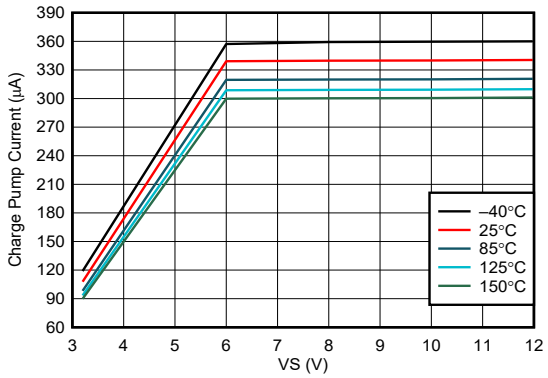


Figure 7-3. Charge Pump Current vs Supply Voltage at V_{CAP} = 6 V

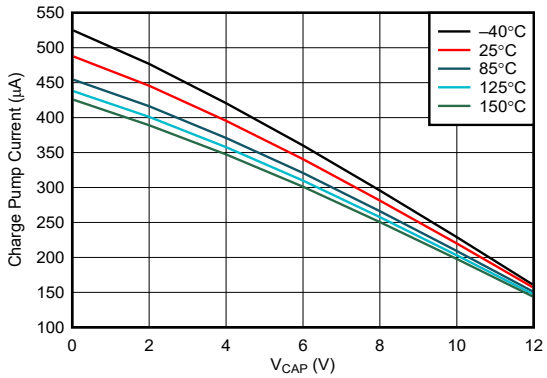


Figure 7-4. Charge Pump V-I Characteristics at VS > = 12 V

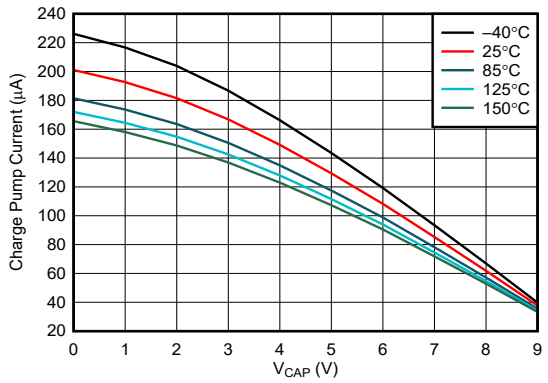


Figure 7-5. Charge Pump V-I Characteristics at VS = 3.2 V

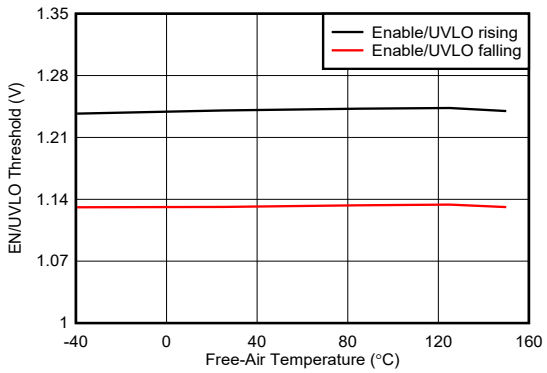


Figure 7-6. EN/UVLO Rising and Falling threshold vs Temperature

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7.7 Typical Characteristics (continued)

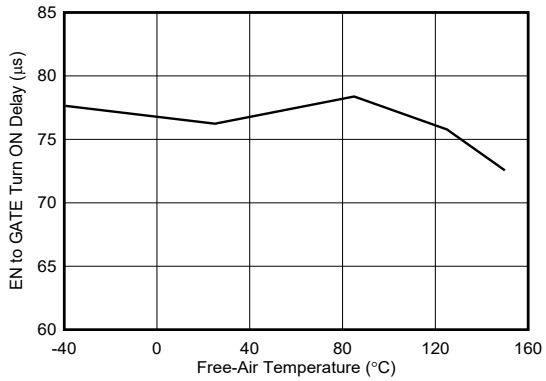


Figure 7-7. Enable to Gate Delay vs Temperature (LM74502H-Q1)

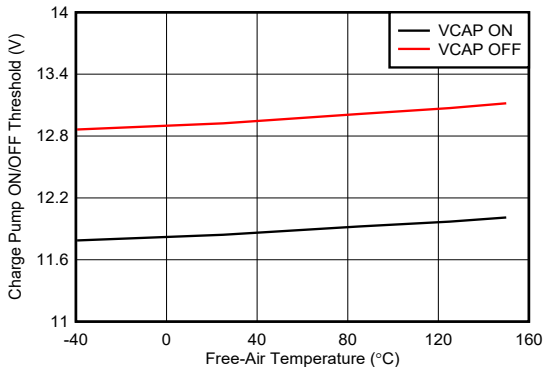


Figure 7-8. Charge Pump ON and OFF Threshold vs Temperature

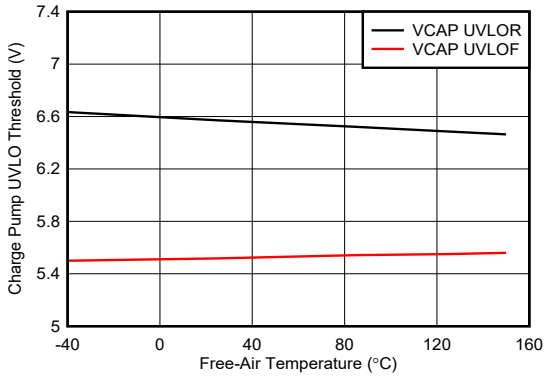


Figure 7-9. Charge Pump UVLO Threshold vs Temperature

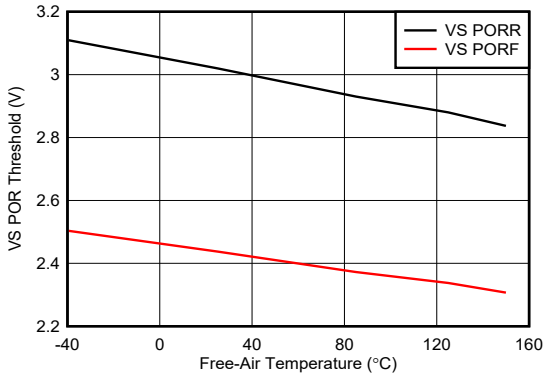


Figure 7-10. VS POR Threshold vs Temperature

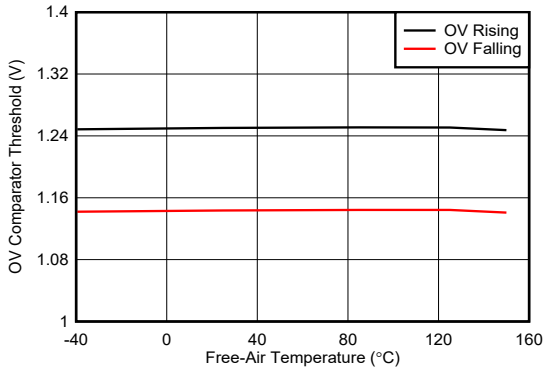


Figure 7-11. OV Comparator Threshold vs Temperature

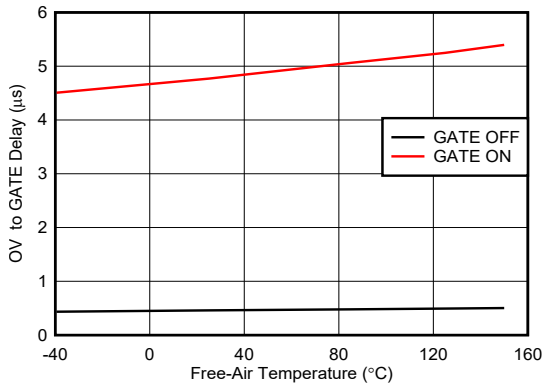


Figure 7-12. OV to GATE Delay vs Temperature (LM74502H-Q1)

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8 Parameter Measurement Information

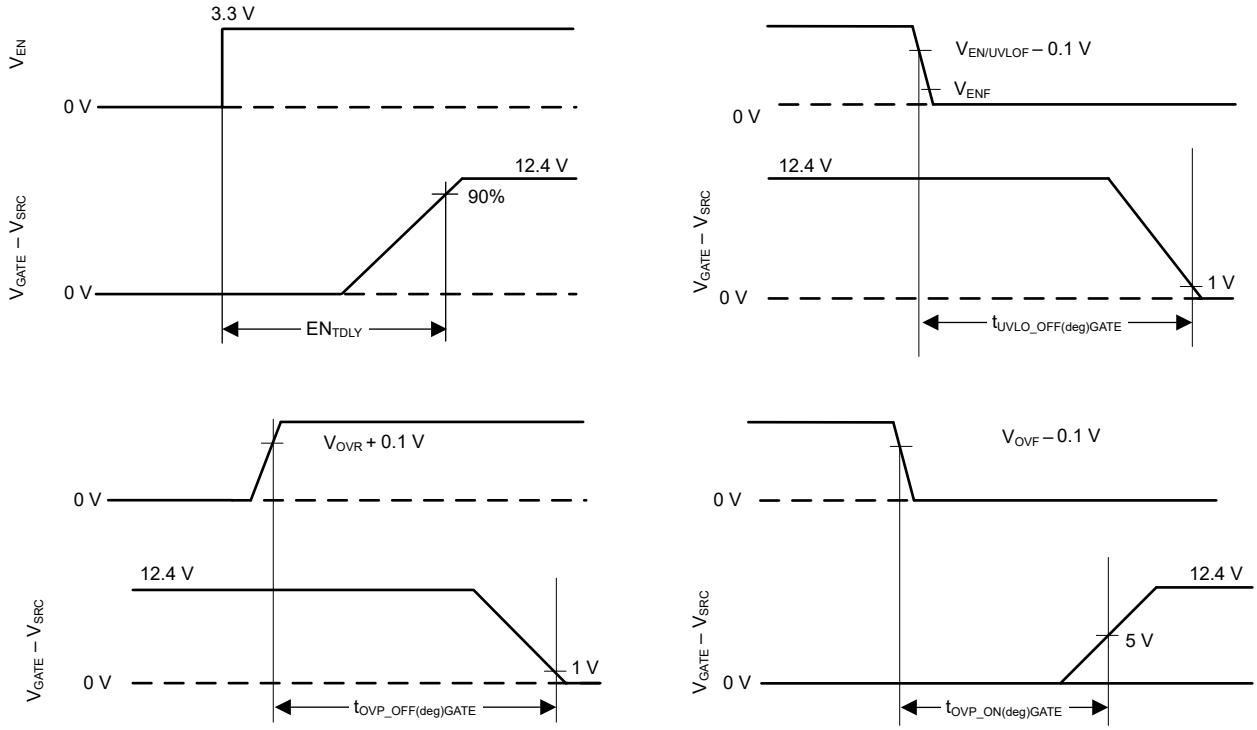


Figure 8-1. Timing Waveforms

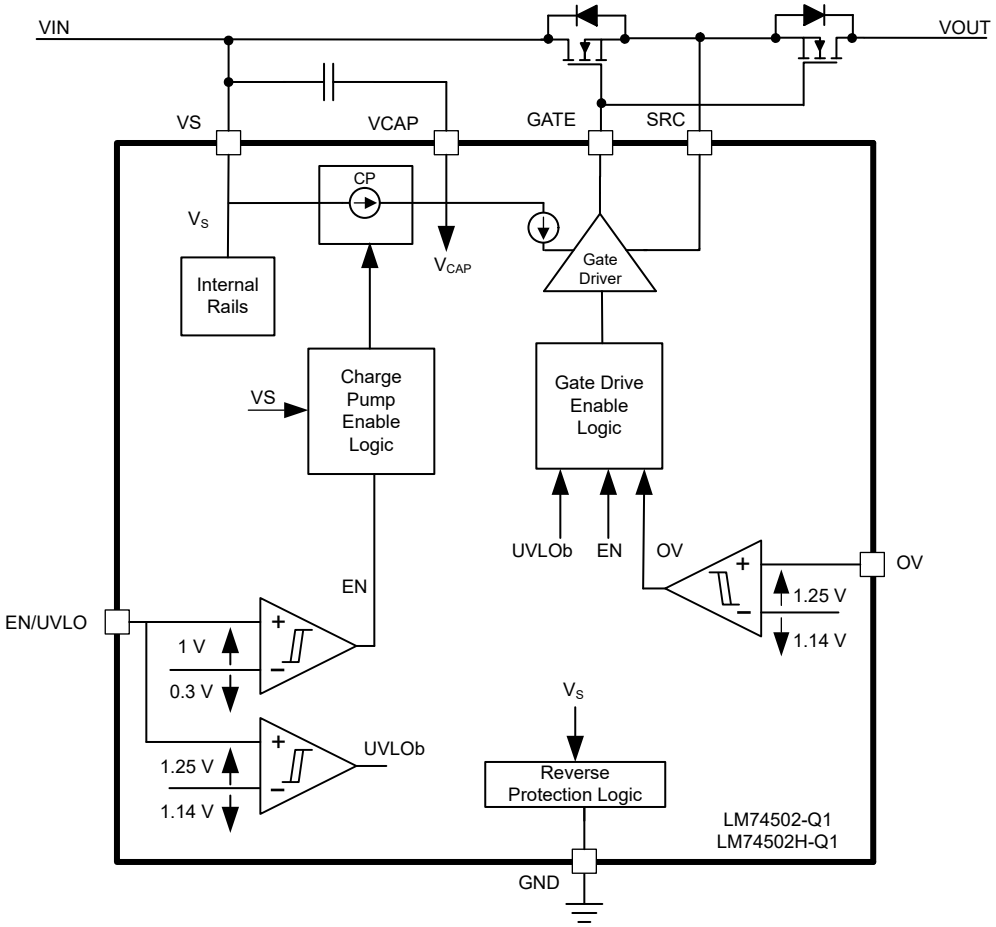
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9 Detailed Description

9.1 Overview

The LM74502-Q1, LM74502H-Q1 controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit with load disconnect function. This easy to use reverse polarity protection controller is paired with an external back-to-back connected N-channel MOSFETs to replace other reverse polarity schemes such as a P-channel MOSFETs. The wide input supply of 4 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated charge pump drives external back-to-back connected N-channel MOSFETs with gate drive voltage of approximately 12.4 V to realize reverse polarity protection and load disconnect function in case of overvoltage and undervoltage event. LM74502-Q1 with it's typical gate drive strength of 60 µA provides smooth start-up with inherent inrush current control due to its lower gate drive strength. LM74502H-Q1 with it's 11-mA typical peak gate drive strength is suitable for applications which need faster turn on such as load switch applications. LM74502-Q1 features an adjustable overvoltage cutoff protection feature using a programming resistor divider to OV terminal. LM74502-Q1 features enable control. With the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low 1 µA of current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage (VS)

The VS pin is used to power the LM74502-Q1's internal circuitry, typically drawing 45 µA when enabled and 1 µA when disabled. If the VS pin voltage is greater than the POR Rising threshold, then LM74502-Q1 operates in either shutdown mode or conduction mode in accordance with the EN/UVLO pin voltage. The voltage from VS to GND is designed to vary from 65 V to –65 V, allowing the LM74502-Q1 to withstand negative voltage transients.

9.3.2 Charge Pump (VCAP)

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and VS pin to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN/UVLO pin, voltage must be above the specified input high threshold, $V_{(EN_IH)}$. When enabled the charge pump sources a charging current of 300-µA typically. If EN/UVLO pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to VS voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV_EN)} = 75\ \mu s + C_{(VCAP)} \times \frac{V_{(VCAP_UVLOR)}}{300\ \mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across VS and VCAP pins
- $V_{(VCAP_UVLOR)}$ = 6.5 V (typical)

To remove any chatter on the gate drive approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to VS voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the VCAP to VS voltage is below to 11.6 V typically at which point the charge pump is enabled. The voltage between VCAP and VS continue to charge and discharge between 11.6 V and 12.4 V as shown in Figure 9-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74502-Q1 is reduced. When the charge pump is disabled it sinks 5-µA typical.

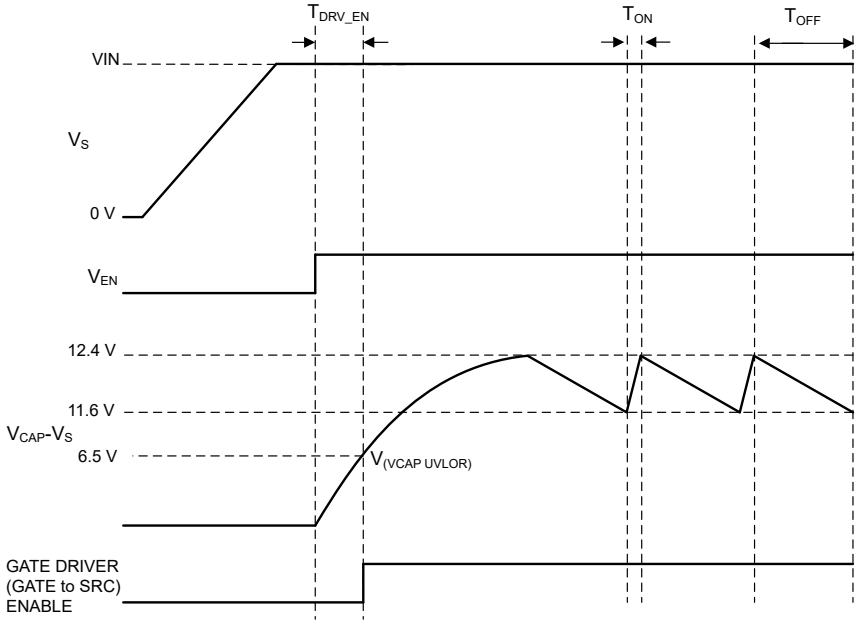


Figure 9-1. Charge Pump Operation

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9.3.3 Gate Driver (GATE an SRC)

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE to SRC voltage.

Before the gate driver is enabled following three conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The VCAP to VS voltage must be greater than the undervoltage lockout voltage.
- The VS voltage must be greater than V_S POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the SRC pin, assuring that the external MOSFET is disabled. After these conditions are achieved the gate driver operates in the conduction mode enhancing the external MOSFET completely.

The controller offers two gate drive variants. LM74502-Q1 with typical peak gate drive strength of 60 µA is suitable to achieve smooth start-up with inherent inrush current control due to its lower gate drive strength.

LM74502H-Q1 with its 11-mA typical peak gate drive strength is suitable for applications which need faster turn-on such as load switch applications.

LM74502-Q1, LM74502H-Q1 SRC pin is capable of handling negative voltage which also makes it suitable for load disconnect switch applications with loads which are inductive in nature.

9.3.3.1 Inrush Current Control

An external circuit as shown in Figure 9-2 can be added on the GATE pin of the LM74502-Q1 to have additional inrush current control for the applications which have large capacitive loads.

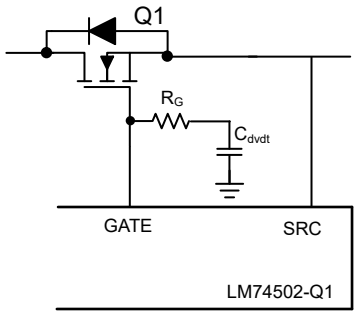


Figure 9-2. Inrush Current Limiting Using LM74502-Q1

The C_{dVdT} capacitor is required for slowing down the GATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate C_{dVdT} capacitance value.

$$C_{dvdt} = \frac{I_{GATE} \times C_{OUT}}{I_{INRUSH}} \quad (2)$$

where I_{GATE} is 60 µA (typical), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_G, in series with the C_{dVdT} capacitor acts as an isolation resistor between C_{dvdt} and gate of the MOSFET.

The inrush current control scheme shown in Figure 9-2 is not applicable to LM74502H-Q1 as its gate drive is optimized for fast turn-on load switch applications.

9.3.4 Enable and Undervoltage Lockout (EN/UVLO)

The LM74502-Q1 has an enable pin, EN/UVLO. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74502-Q1

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in shutdown mode. The EN/UVLO pin can withstand a voltage as large as 65 V and as low as –65 V. This feature allows for the EN/UVLO pin to be connected directly to the VS pin if enable functionality is not needed. In conditions where EN/UVLO is left floating, the internal sink current of 3 uA pulls EN/UVLO pin low and disables the device.

An external resistor divider connected from input to EN/UVLO to ground can be used to implement the input Undervoltage Lockout (UVLO) functionality. When EN/UVLO pin voltage is lower than UVLO comparator falling threshold ($V_{EN/UVLOR}$) but higher than enable falling threshold (V_{ENF}), the device disables gate drive voltage, however, charge pump is kept on. This action ensures quick recovery of gate drive when UVLO condition is removed. If UVLO functionality is not required, connect EN/UVLO pin to VS.

9.3.5 Overvoltage Protection (OV)

LM74502-Q1 provides programmable overvoltage protection feature with OV pin. A resistor divider can be connected from input source to OV pin to ground to set overvoltage threshold. An internal comparator compares the input voltage against fixed reference (1.25 V) and disables the gate drive as soon as OV pin voltage goes above the OV comparator reference. When the resistor divider is referred from input supply side, the device is configured for overvoltage cutoff functionality. When the resistor divider is referred from output side (V_{OUT}), the device is configured for overvoltage clamp functionality.

When OV pin voltage goes above OV comparator V_{OVR} threshold (1.25-V typical), the device disables gate drive, however, charge pump remains active. When OV pin voltage falls below V_{OVF} threshold (1.14-V typical), the gate is quickly turned on as charge pump is kept on and the device does not go through the device start-up process. When OV pin is not used, it can be connected to ground.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The LM74502-Q1 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold $V_{(EN_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74502-Q1 enters low I_Q operation with the VS pin only sinking 1 µA.

9.4.2 Conduction Mode

For the LM74502-Q1, LM74502H-Q1 to operate in conduction mode the gate driver must be enabled as described in the *Gate Driver (GATE an SRC)* section. If these conditions are achieved the GATE pin is

- Internally driven through 60-µA current source in case of LM74502-Q1
- Internally connected to the VCAP for fast turn-on of external FET in case of LM74502H-Q1

LM74502-Q1, LM74502H-Q1 gate drive is disabled when OV pin voltage is above V_{OVR} threshold or EN/UVLO pin voltage is lower than $V_{EN/UVLOF}$ threshold.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM74502-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in Figure 10-1 where the LM74502-Q1 is used to drive back-to-back connected MOSFETs Q1 and Q2 in series with a battery to realize reverse polarity protection and load disconnect solution. The TVS is not required for the LM74502-Q1 to operate, but they are used to clamp the positive and negative voltage surges. TI recommends the output capacitor C_{OUT} to protect the immediate output voltage collapse as a result of line disturbance.

10.2 Typical Application

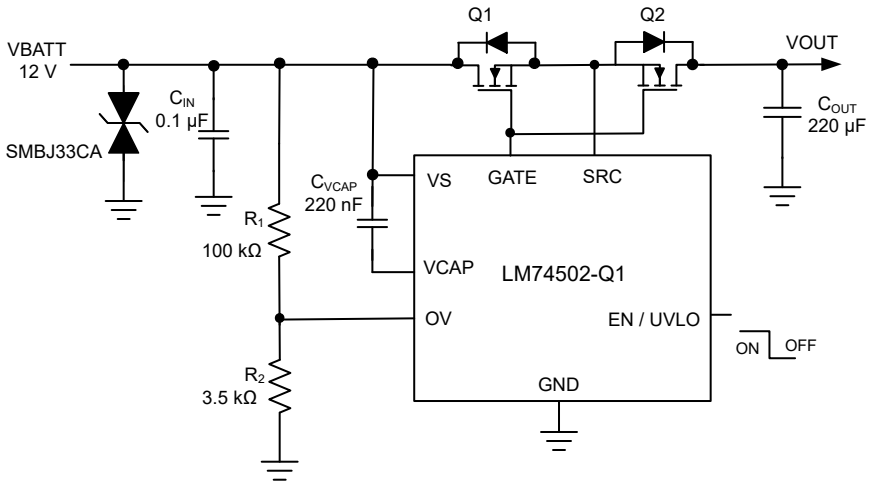


Figure 10-1. Typical Application Circuit

10.2.1 Design Requirements

Table 10-1 list design examples with system design parameters.

Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output voltage	3.2 V during cold crank to 35-V load dump
Output current range	3-A nominal, 5-A maximum
Output capacitance	220-µF typical output capacitance
Overvoltage Protection	37-V typical
Automotive EMC compliance	ISO 7637-2 and ISO 16750-2

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10.2.2 Detailed Design Procedure

10.2.2.1 Design Considerations

- Input operating voltage range, including overvoltage conditions
- Nominal load current and maximum load current

10.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current, I_D, the maximum drain-to-source voltage, $V_{DS(MAX)}$, the maximum source current through body diode, and the drain-to-source On resistance, R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This requirement includes any anticipated fault conditions. TI recommends to use MOSFETs with voltage rating up to 60-V maximum with the LM74502-Q1 because SOURCE pin maximum voltage rating is 65 V. The maximum V_{GS} LM74502-Q1 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected. If a MOSFET with V_{GS} rating < 15 V is selected, a Zener diode can be used to clamp V_{GS} to safe level.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred. Selecting a MOSFET with $RDS_{(ON)}$ that gives VDS drop 20 mV to 50 mV at full load provides good trade off in terms of power dissipation and cost.

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

10.2.2.3 Overvoltage Protection

Resistors R1 and R2 connected in series is used to program the overvoltage threshold. Connecting R1 to VIN provides overvoltage cutoff and switching the connection to VOUT provides overvoltage clamp response. The resistor values required for setting the overvoltage threshold V_{OV} to 37 V are calculated by solving Equation 3

$$V_{OVR} = \frac{R_2 \times V_{OV}}{R_1 + R_2} \tag{3}$$

For minimizing the input current drawn from the supply through resistors R1 and R2, TI recommends to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OV pin. Select (R1 + R2) such that current through resistors is around 100 times higher than the leakage through OV pin. Based on the device electrical characteristics, V_{OVR} is 1.25 V, select (R1) = 100 kΩ and R2 = 3.5 kΩ as a standard resistor value to set overvoltage cutoff of 37 V.

Based on application use case, overvoltage threshold can be set at the lower voltage as it enables lower rated downstream components, thus providing solution size and lower cost benefit.

10.2.2.4 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: Minimum recommended value of VCAP (µF) ≥ 10 × $C_{ISS(MOSFET_effective)}$ (µF),

  C_{VCAP} of 0.22 µF is selected
- C_{IN}: Typical input capacitor of 0.1 µF
- C_{OUT}: Typical output capacitor 220 µF

10.2.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in Figure 10-1, a bi-directional TVS diode is used to protect from positive and negative

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transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

The two important specifications of the TVS are breakdown voltage and clamping voltage. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a Zener diode and is specified at a low current value typical 1 mA and the breakdown voltage must be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum input voltage rating of LM74502-Q1 (65 V). The breakdown voltage of TVS– must be higher than maximum reverse battery voltage –16 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and must not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This action translates to 15 A flowing through the TVS– and the voltage across the TVS is close to its clamping voltage.

The next criterion is that the absolute minimum rating of source voltage of the LM74502-Q1 (–65 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen.

SMBJ series of TVS' are rated up to 600-W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

10.2.4 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

Typical 24-V battery protection application circuit shown in Figure 10-2 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.

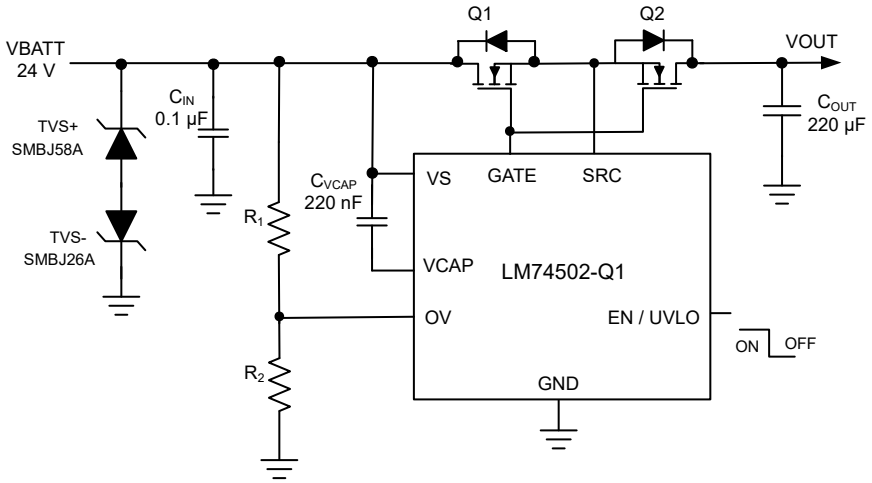


Figure 10-2. Typical 24-V Battery Protection with Two Uni-Directional TVS

The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of source and enable pin of LM74502-Q1 (65 V) and must withstand 65-V suppressed load dump. The breakdown voltage of TVS– must be lower than maximum reverse battery voltage –32 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 48 V, maximum negative clamping voltage is ≤ –65 V . Two uni-directional TVS connected back-to-back must be used at the input. For positive side TVS+, TI recommends SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical). For the negative side TVS–, TI recommends SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42 V.

For 24-V battery protection, TI recommends a 75-V rated MOSFET to be used along with SMBJ26A and SMBJ58A connected back-to-back at the input.

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10.2.5 Application Curves

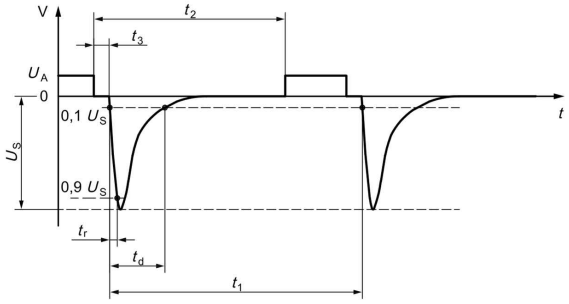
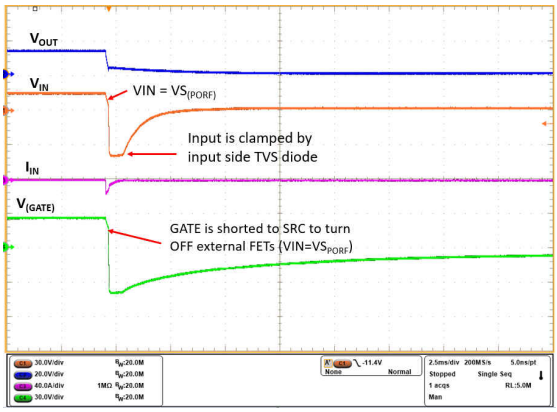
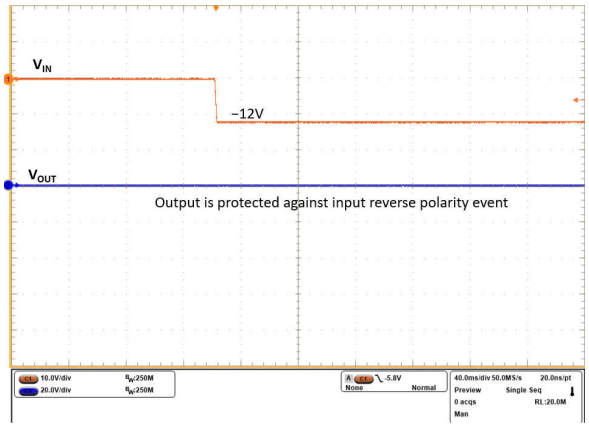


Figure 10-3. ISO 7637-2 Pulse 1



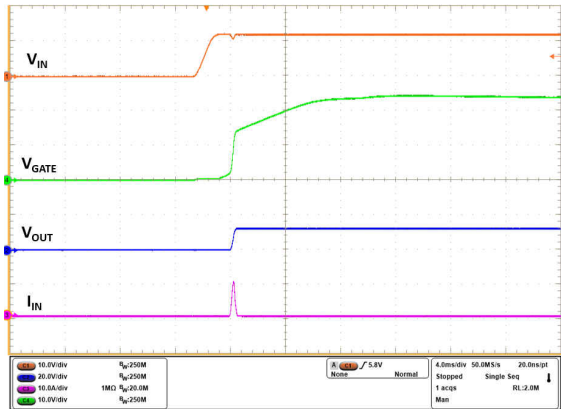
Time (2.5 ms/DIV)

Figure 10-4. Response to ISO 7637-2 Pulse 1 (–150 V)



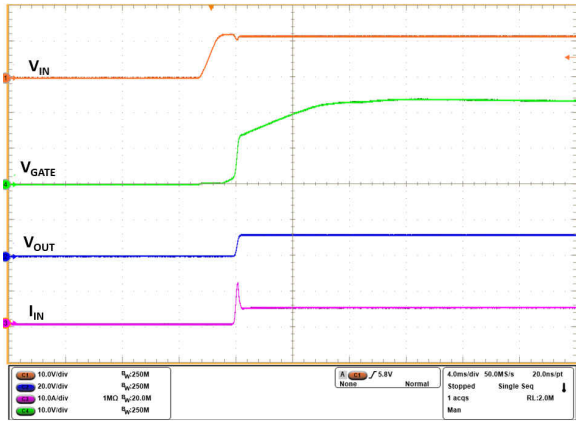
Time (40 ms/DIV)

Figure 10-5. Start-up with Input Reverse Voltage (–12 V)



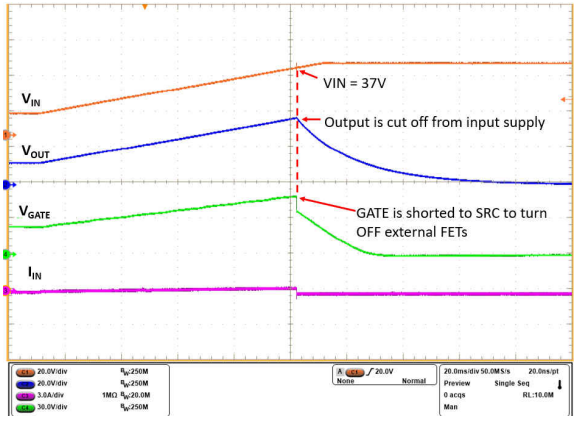
Time (4 ms/DIV)

Figure 10-6. Start-up with No Load



Time (4 ms/DIV)

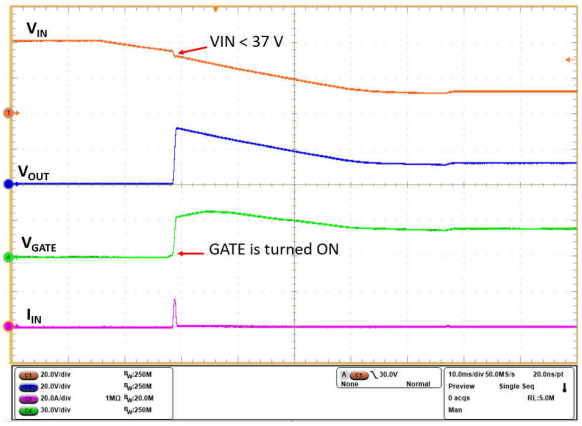
Figure 10-7. Start-up with 5-A Load



Time (20 ms/DIV)

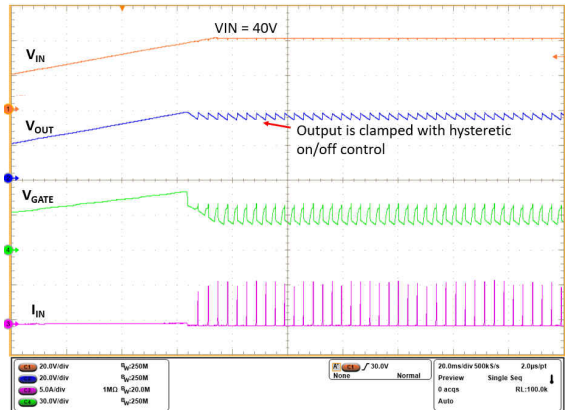
Figure 10-8. Overvoltage Cutoff Response (37 V)

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Time (10 ms/DIV)

Figure 10-9. Overvoltage Recovery



Time (20 ms/DIV)

Figure 10-10. Overvoltage Clamp Response

10.3 Surge Stopper Using LM74502-Q1, LM74502H-Q1

Many automotive applications are designed to comply with unsuppressed load dump transients specified by ISO16750-2 Pulse 5A. LM74502, LM74502H can be configured as input surge stopper to provide overvoltage along with input reverse supply protection and protect the downstream loads in case of unsuppressed load dump event.

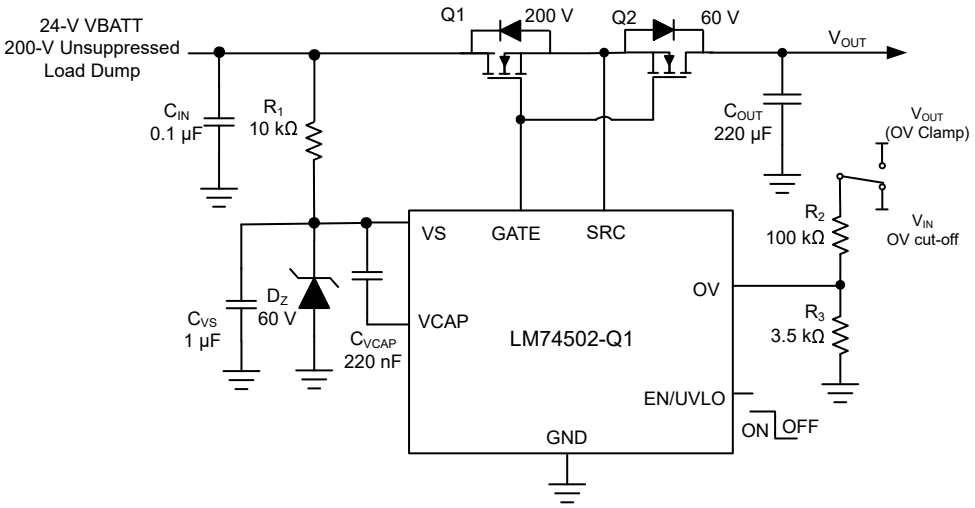


Figure 10-11. Typical Surge Stopper Application for 24-V Powered Systems

As shown in Figure 10-11, MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and LM74502 from input transient. Note that only the VS pin is exposed to input transient through a resistor, R1. A 60-V rated Zener diode is used to clamp and protect the VS pin within recommended operating condition. Th rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level.

10.3.1 VS Capacitance, Resistor R_1 and Zener Clamp (D_Z)

A minimum of 1-µF C_{VS} capacitance is required. During input overvoltage transient, resistor R1 and Zener diode, D_Z, are used to protect VS pin from exceeding the maximum ratings by clamping V_{VS} to 60 V. Choosing R1 = 10 kΩ, the peak power dissipated in Zener diode D_Z can be calculated using Equation 4 .

$$P_{DZ} = V_{DZ} \times \frac{(V_{IN(MAX)} - V_{DZ})}{R_1} \tag{4}$$

Where V_{DZ} is the breakdown voltage of Zener diode. Select the Zener diode that can handle peak power requirement.

Peak power dissipated in resistor R1 can be calculated using Equation 5.

$$P_{R1} = \frac{(V_{IN(MAX)} - V_{DZ})^2}{R_1} \tag{5}$$

Select a resistor package which can handle peak power and maximum DC voltage.

10.3.2 Overvoltage Protection

For the overvoltage setting, refer to the resistor selection procedure described in *Overvoltage Protection*. Select (R2) = 100 kΩ and R3 = 3.5 kΩ as a standard resistor value to set overvoltage cutoff of 37 V.

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10.3.3 MOSFET Selection

The VDS rating of the MOSFET Q1 must be minimum $V_{IN(max)}$ for designs with output overvoltage cutoff where output can reach 0 V with higher loads. For designs with output overvoltage clamp, MOSFET VDS rating must be ($V_{IN(max)}$ – V_{OUT_CLAMP}). The VGS rating is based on GATE-SRC maximum voltage of 15 V. TI recommends a 20-V VGS rated MOSFET. Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET must be considered with sufficient design margin for reliable operation. An additional Zener diode from GATE to SRC can be needed to protect the external FET in case output is expected to drop to the level where it can exceed external FET $V_{GS(max)}$ rating.

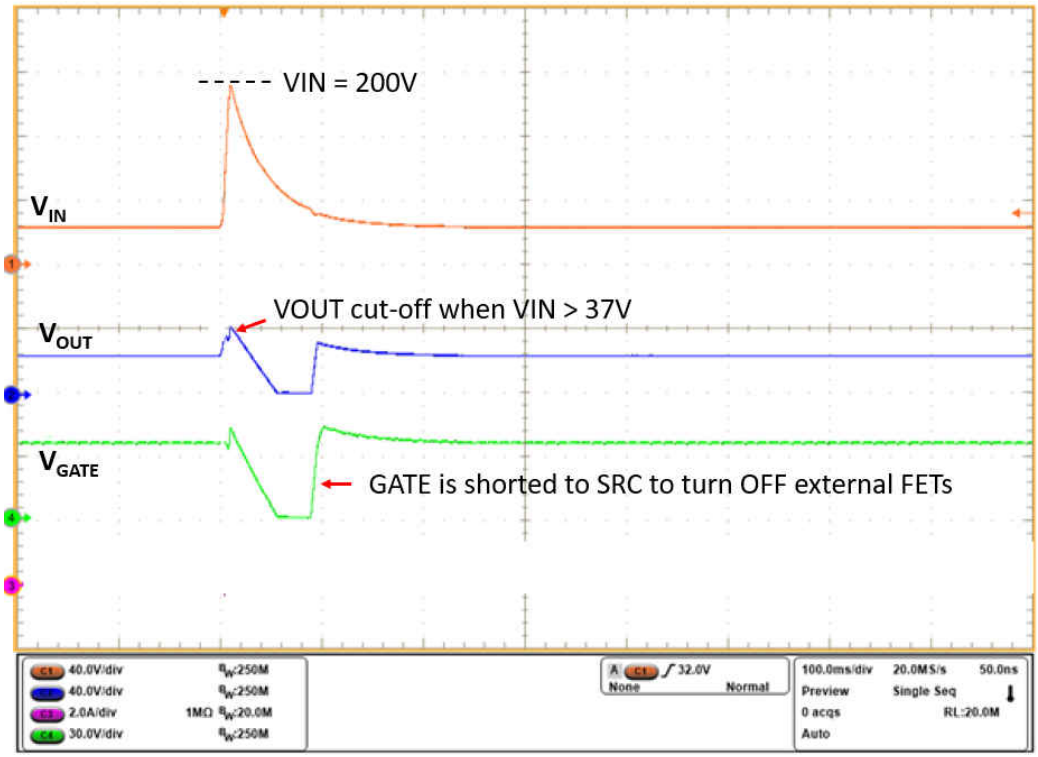


Figure 10-12. 200-V Surge Stopper with Overvoltage Cutoff Using LM74502-Q1

10.4 Fast Turn-On and Turn-Off High Side Switch Driver Using LM74502H-Q1

In automotive load driving applications N-Channel MOSFET based high side switch is very commonly used to disconnect the loads from supply line in case of faults such as overvoltage event . LM74502-Q1, LM74502H-Q1 can be used to drive external MOSFET to realize simple high side switch with overvoltage protection. Figure 10-13 shows a typical application circuit where LM74502H-Q1 is used to drive external MOSFET Q1 as a main power path connect and disconnect switch. A resistor divider from input to OV pin to ground can be used the set the overvoltage threshold.

If VOUT node (SRC pin) of the device is expected to drop in case of events such as overcurrent or short-circuit on load side then additional Zener diode is required across gate and source pin of external MOSFET to protect it from exceeding its maximum V_{GS} rating.

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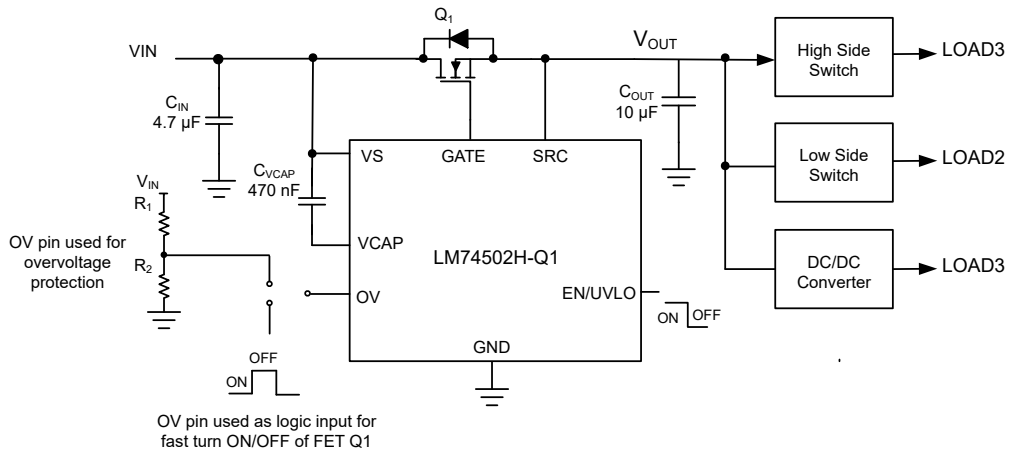


Figure 10-13. Fast Turn-ON and OFF High Side Switch Using LM74502H-Q1

Many safety applications require fast switching off of the MOSFET in case of fault events such as overvoltage or overcurrent fault. Some of the load driving path applications also require PWM operation of high side switch. LM74502H-Q1 OV pin can be used as control input to realize fast turn-on and turn-off load switch functionality. With OV pin pulled above V_{OVR} threshold of (1.25-V typical), LM74502H-Q1 turns off the external MOSFET (with Ciss = 4.7 nF) within 1 µs typically. When OV pin is pulled low, LM74502H-Q1 with its peak gate drive strength of 11 mA turns on external MOSFET with turn-on speed of 7-µs typical. Figure 10-14 shows LM74502H-Q1 GATE to SRC response when OV pin is toggled with ON/OFF logic input.

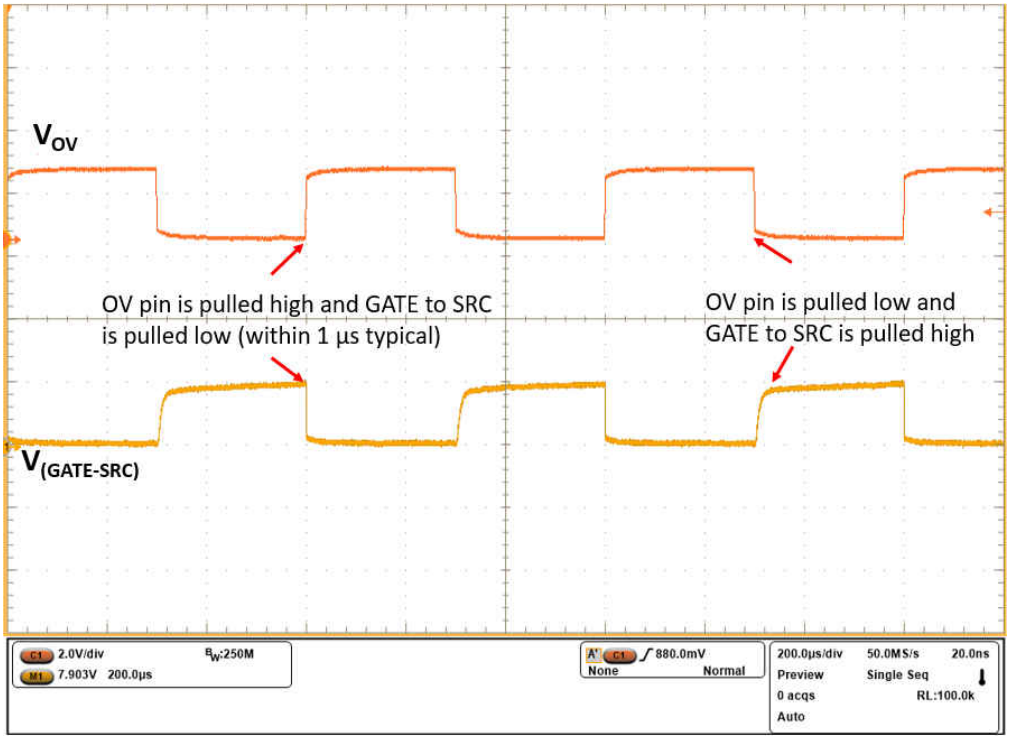


Figure 10-14. Fast Turn-On and Turn-Off High Side Switch Driver Using LM74502H-Q1

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11 Power Supply Recommendations

The LM74502-Q1, LM74502H-Q1 reverse polarity protection controller is designed for the supply voltage range of 3.2 V ≤ V_S ≤ 65 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 0.1 µF. Based on system requirements, a higher input bypass capacitor can be needed with LM74502H-Q1 to avoid supply glitch in case of high inrush current start-up event. To prevent LM74502-Q1 and surrounding components from damage under the conditions of a direct output short circuit, use a power supply having overload and short-circuit protection.

12 Layout

12.1 Layout Guidelines

- Connect GATE and SRC pin of LM74502-Q1 close to the MOSFET's gate and source pin.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- Keep the charge pump capacitor across VCAP and VS pin away from the MOSFET to lower the thermal effects on the capacitance value.
- Connect the GATE pin of the LM74502-Q1 to the MOSFET gate with short trace. Avoid excessively thin and long running trace to the Gate Drive.

12.2 Layout Example

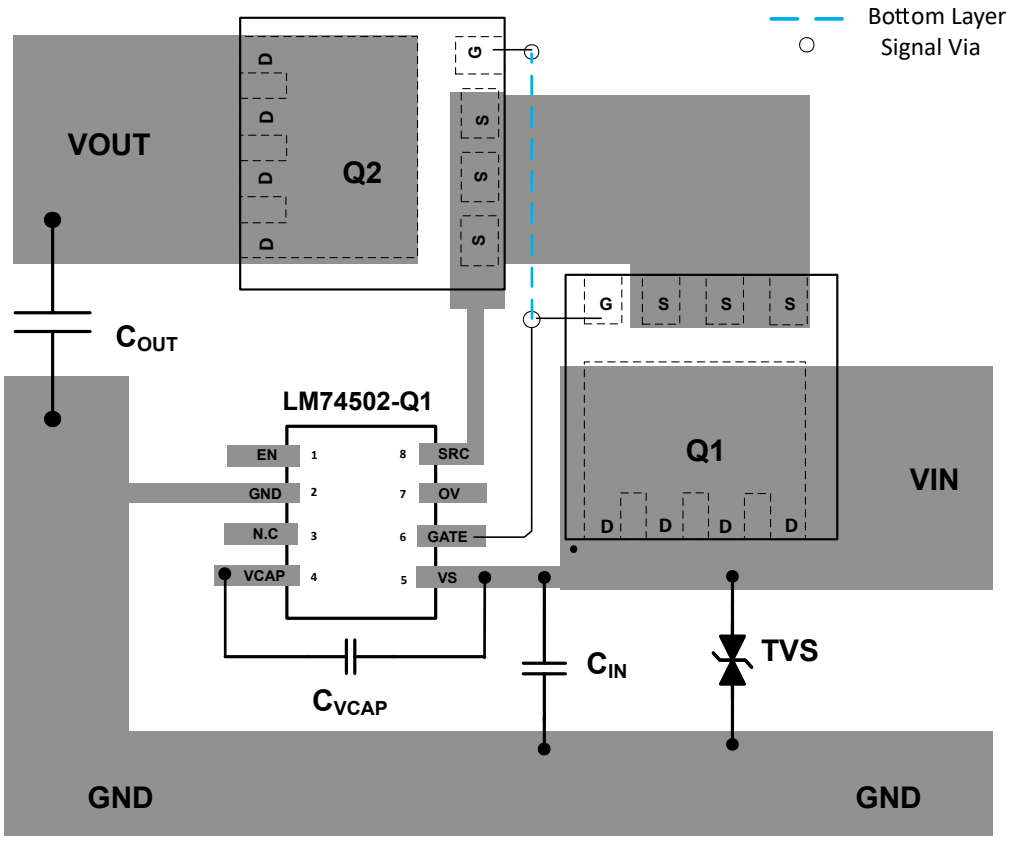


Figure 12-1. Layout Example

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74502HQDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	502HQ	Samples
LM74502QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L502Q	Samples
PLM74502HQDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLM74502QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM74502-Q1, LM74502H-Q1 :

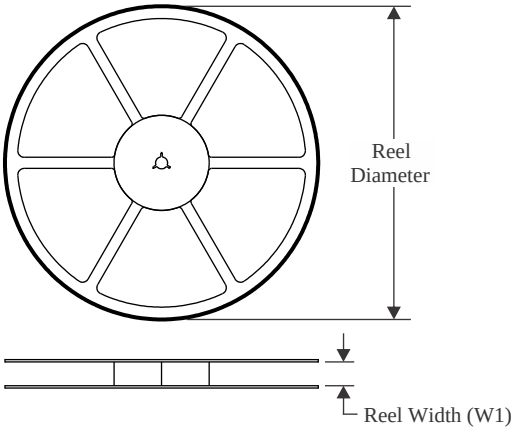
- Catalog : LM74502, LM74502H

NOTE: Qualified Version Definitions:

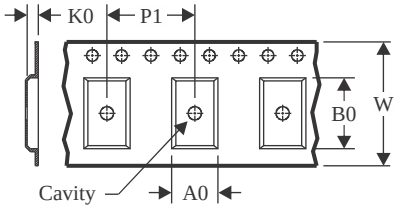
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

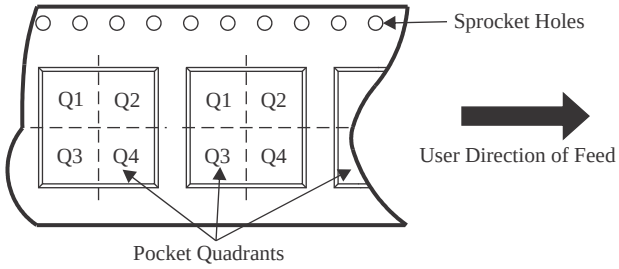


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

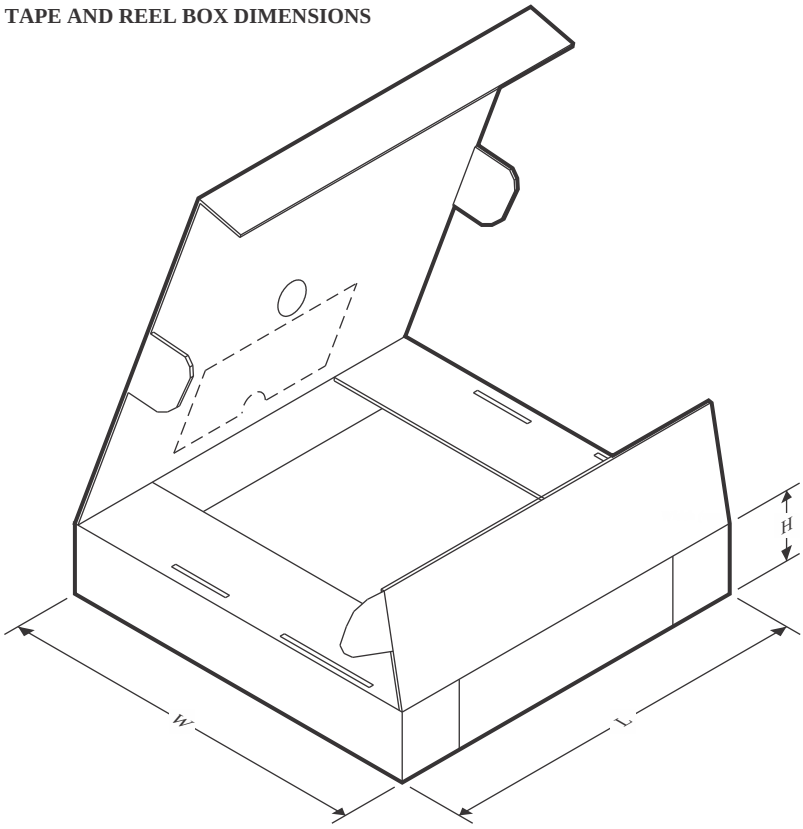
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74502HQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM74502QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

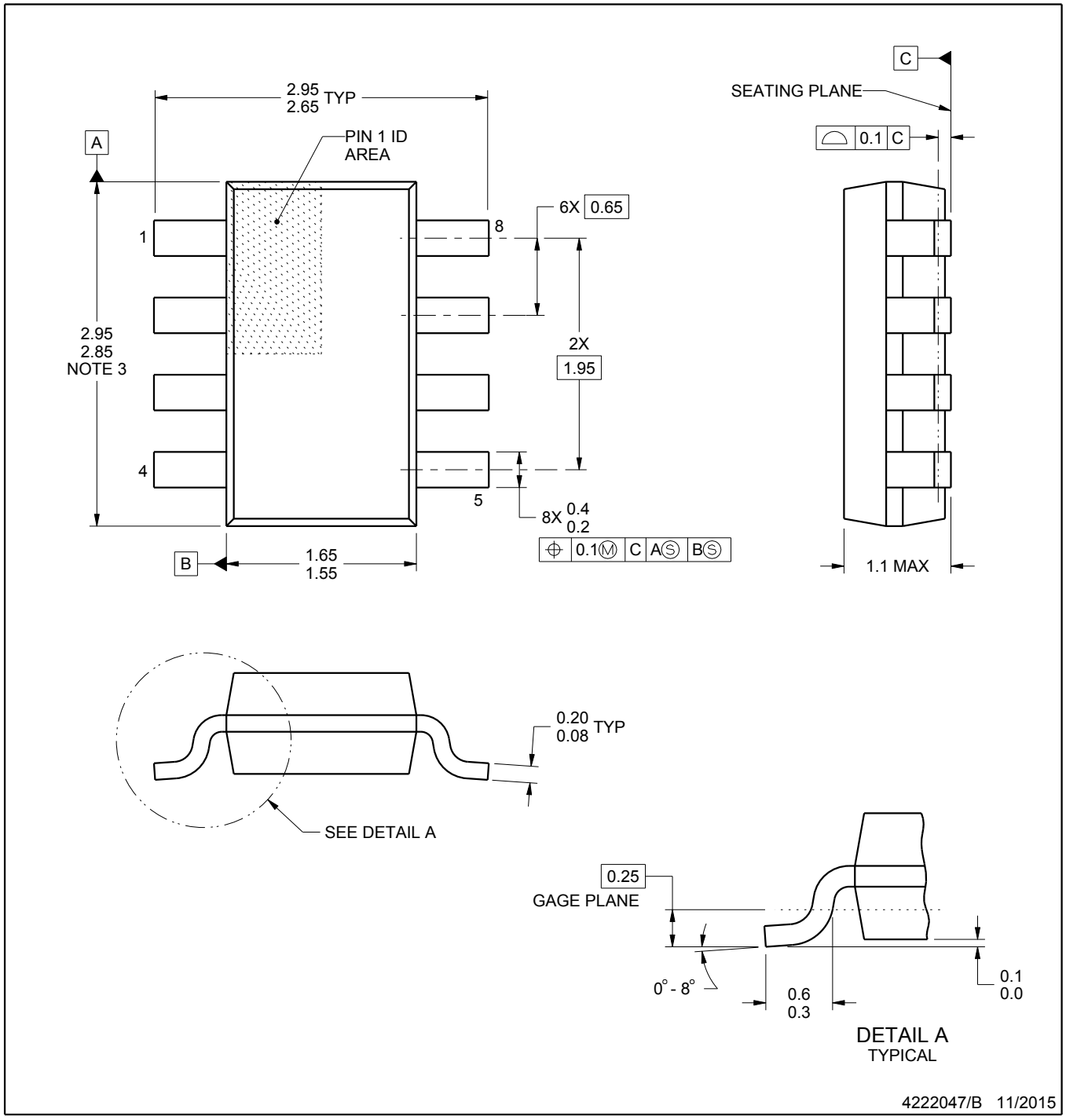
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74502HQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM74502QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

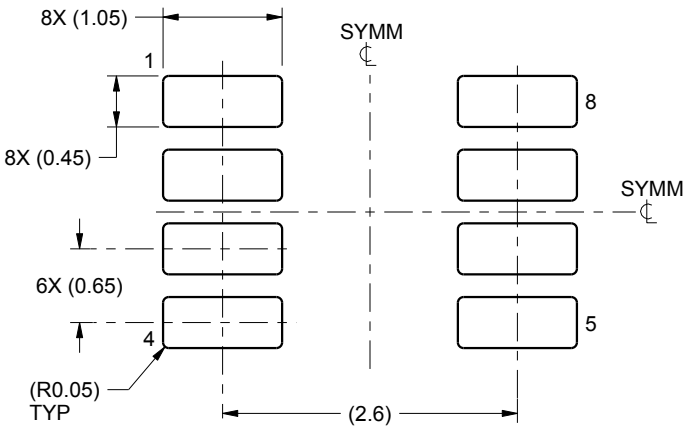
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

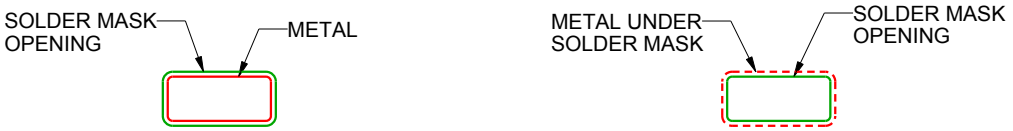


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

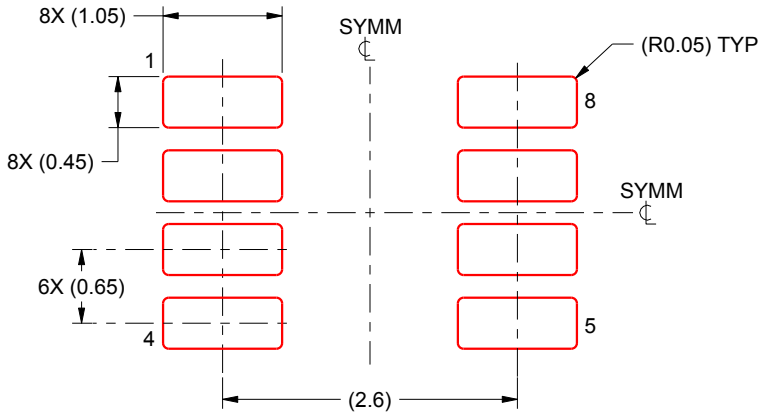
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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