LVDS Interface ICs

56bit LVDS Transmitter
56:8 Serializer

BU7988KVT

●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

●Features

- ■Wide dot clock range : Single(112MHz)/Dual(224MHz)(NTSC, VGA, SVGA, WXGA UXGA)
- ■Support spread spectrum clock generator.
- ■Clock edge selectable.
- ■Support reduced swing LVDS for low EMI.
- ■Power down mode.
- ■Package TQFP100V

●Applications

Flat Plane Display

●Precaution

■This chip is not designed to protect from radioactivity.

Jun. 2008

●Block Diagram

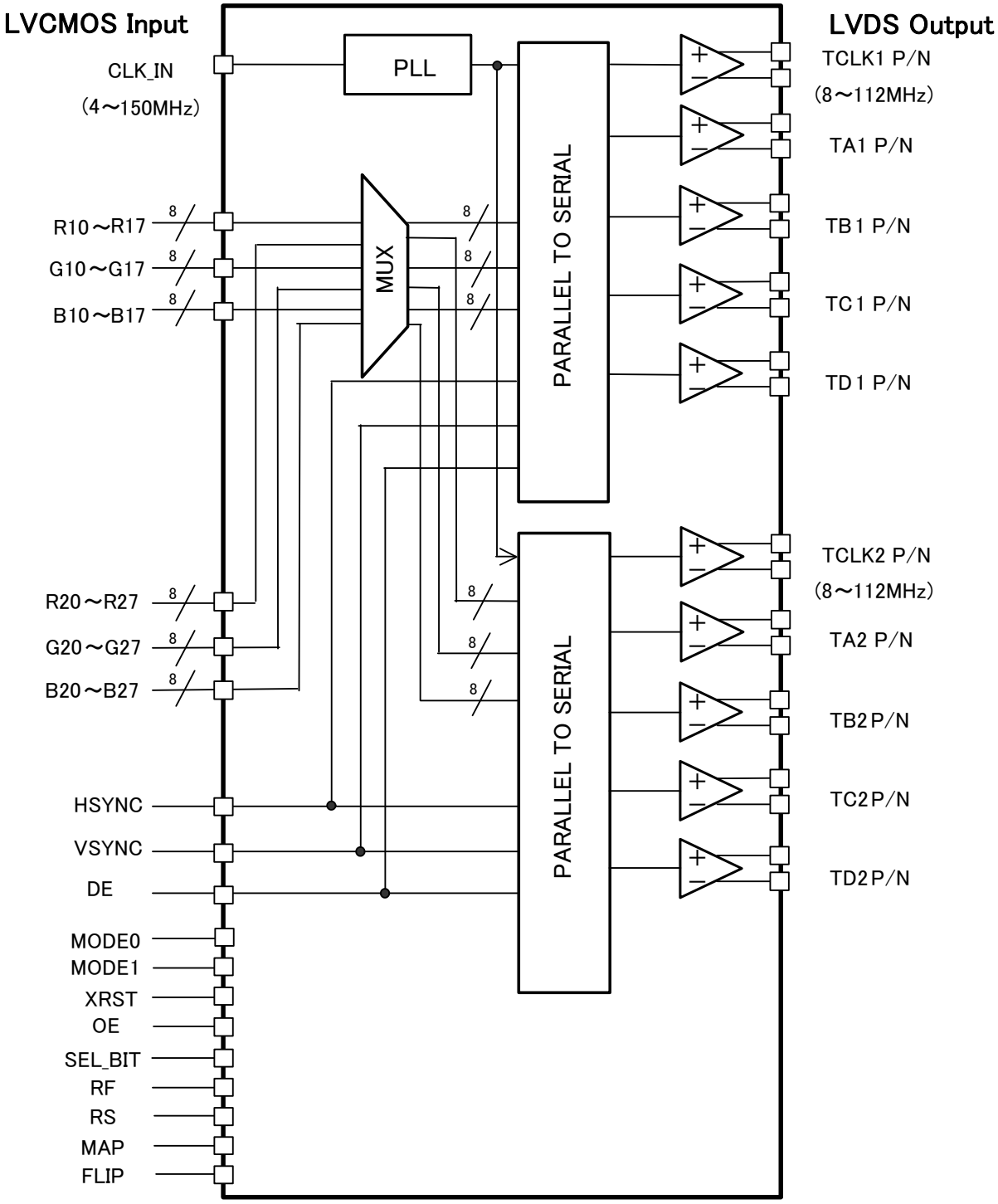


Figure-1　Block Diagram

●TQFP100V　Package Outline and Specification

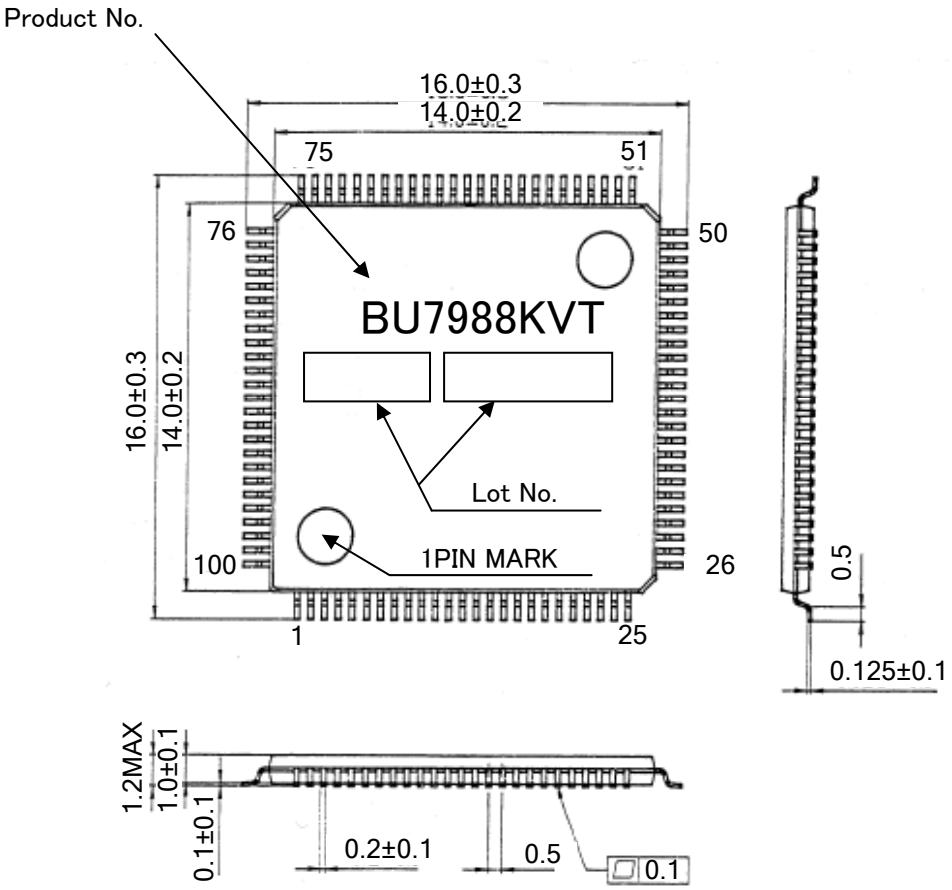


Figure-2　TQFP100V Package Outline and Specification

● Pin configuration

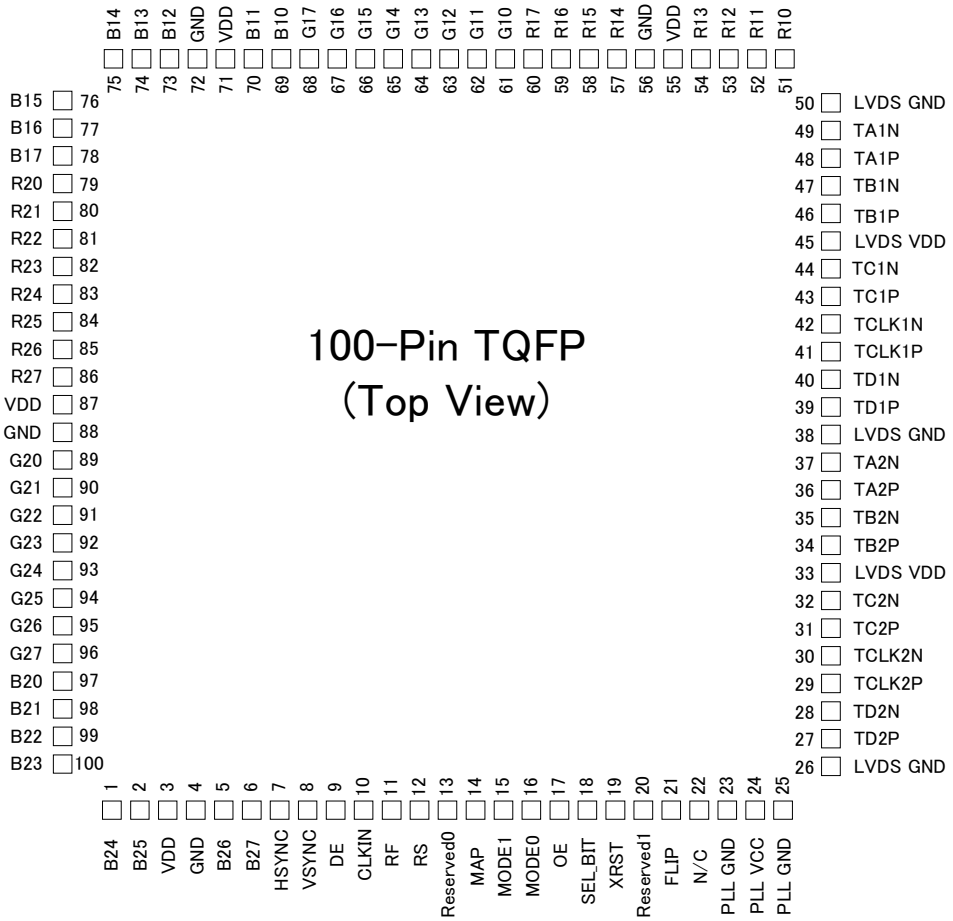


Figure-3　Pin Diagram (Top View)

●Pin Description

Table 1 : Pin Description

Pin Name	Pin No.	Type	Descriptions
TA1P, TA1N	48, 49	LVDS OUT	LVDS data out
TB1P, TB1N	46, 47	LVDS OUT	
TC1P, TC1N	43, 44	LVDS OUT	
TD1P, TD1N	39, 40	LVDS OUT	
TCLK1P, TCLK1N	41, 42	LVDS OUT	LVDS clock out
TA2P, TA2N	36, 37	LVDS OUT	LVDS data out
TB2P, TB2N	34, 35	LVDS OUT	
TC2P TC2N	31, 32	LVDS OUT	
TD2P, TD2N	27, 28	LVDS OUT	
TCLK2P, TCLK2N	29, 30	LVDS OUT	LVDS clock out
R17～R10	60, 59, 58, 57, 54, 53, 52, 51	IN	1st Pixel data input.
G17～G10	68, 67, 66, 65, 64, 63, 62, 61	IN	
B17～B10	78, 77, 76, 75, 74, 73, 70, 69	IN	
R27～R20	86, 85, 84, 83, 82, 81, 80, 79	IN	2st Pixel data inputs.
G27～G20	96, 95, 94, 93, 92, 91, 90, 89	IN	
B27～B20	6, 5, 2, 1, 100, 99, 98, 97	IN	
DE	9	IN	DATA-ENABLE input.
VSYNC	8	IN	VSYNC input.
HSYNC	7	IN	HSYNC input.
CLKIN	10	IN	Clock Input.
MAP	14	IN	LVDS mapping table select. See Table11-14 and Figure11-14.
XRST	19	IN	H : Normal operation, L : Power down (all outputs are Hi-Z)
FLIP	21	IN	LVDS output pin select. See Table10.

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>RS</td><td>12</td><td>IN</td><td>LVDS swing mode, RS select.
<table><tr><th>RS</th><th>LVDS Swing</th></tr><tr><td>VDD</td><td>350mV</td></tr><tr><td>GND</td><td>200mV</td></tr></table></td></tr>
<tr><td>MODE1, MODE0</td><td>15, 16</td><td>IN</td><td>Pixel Data Mode
<table><tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr><tr><td>L</td><td>L</td><td>Dual-in/Dual-out</td></tr><tr><td>L</td><td>H</td><td>Dual-in/Single-out</td></tr><tr><td>H</td><td>L</td><td>Single-in/Dual-out</td></tr><tr><td>H</td><td>H</td><td>Single-in/Single-out</td></tr></table></td></tr>
<tr><td>SEL_BIT</td><td>18</td><td>IN</td><td>6bit/8bit color select.
H : 6bit (TDxP/N*1 are Hi-Z), L : 8bit.</td></tr>
<tr><td>OE</td><td>17</td><td>IN</td><td>Outputs enable.
H : Outputs enable,
L : Output disable (all outputs are Hi-Z)</td></tr>
<tr><td>RF</td><td>11</td><td>IN</td><td>Input Clock Triggering Select
H : Rising edge,
L : Falling edge</td></tr>
<tr><td>N/C</td><td>22</td><td></td><td>Must be open</td></tr>
<tr><td>Reserved1</td><td>20</td><td>IN</td><td>Must be tied to GND</td></tr>
<tr><td>Reserved0</td><td>13</td><td>IN</td><td>Must be open</td></tr>
<tr><td>VDD</td><td>3, 55, 71, 87</td><td>Power</td><td>Power Supply Pins for CMOS inputs, output and digital circuitry.</td></tr>
<tr><td>GND</td><td>4, 56, 72, 88</td><td>Ground</td><td>Ground Pins for CMOS inputs, outputs and digital circuitry.</td></tr>
<tr><td>LVDS VDD</td><td>33, 45</td><td>Power</td><td>Power Supply Pins for LVDS Outputs.</td></tr>
<tr><td>LVDS GND</td><td>26, 38, 50</td><td>Ground</td><td>Ground Pins for LVDS Outputs.</td></tr>
<tr><td>PLL VDD</td><td>24</td><td>Power</td><td>Power Supply for PLL circuitry.</td></tr>
<tr><td>PLL GND</td><td>23, 25</td><td>Ground</td><td>Ground Pin for PLL circuitry.</td></tr>
</table>

*1: X=1,2

●Electrical characteristics

■Rating

Table 2 : Absolute Maximum Rating

Parameter	Symbol	Rating		Units
		Min	Max	
Supply Voltage	VDD	−0.3	4.0	V
Input Voltage	VIN	−0.3	VDD+0.3	V
Output Voltage	VOUT	−0.3	VDD+0.3	V
Storage Temperature Range	Tstg	−55	125	℃

Table 3 : Package Power

PACKAGE	Power Dissipation (mW)	De-rating (mW/℃)*1
TQFP100V	900	9.0
	1400*2	14.0*2

*1:At temperature Ta >25℃

*2:Package power when mounting on the PCB board.

The size of PCB board :70 × 70 × 1.6 (mm^3)

The material of PCB board : The FR4 glass epoxy board.(3% or less copper foil area)

(It is recommended to apply the above package power requirement to PCB board when the small swing input mode is used)

Table 4 : Recommended Operating Conditions

Parameter	Symbol	Rating			Units	Conditions
		Min	Typ	Max		
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	VDD,LVDSVDD,PLLVDD
Operating Temperature Range	Topr	−20	−	85	℃	Clock frequency from 8MHz up to 90MHz
		0	−	70	℃	Clock frequency from 90MHz up to 112MHz

■DC characteristics

Table 5 : CMOS DC Specifications（VDD=3.0V～3.6V, Ta=−20℃～+85℃）

Symbol	Parameter	Rating			Units	Conditions
		Min	Typ	Max		
V_{IH}	High Level Input Voltage	VDD×0.8	−	VDD	V	
V_{IL}	Low Level Input Voltage	GND	−	VDD×0.2	V	
I_{INC}	Input Leak Current	−10	−	+10	μA	0V≦V_{IN}≦VDD

Table 6 : LVDS Transmitter DC Specifications（VDD=3.0V～3.6V, Ta=−20℃～+85℃）

Symbol	Parameter	Rating			Units	Conditions	
		Min	Typ	Max			
VOD	Differential Output Voltage	250	350	450	mV	RL=100Ω	Normal swing RS=VDD
		120	200	300	mV		Reduced swing RS=GND
ΔVOD	Change in VOD between complementary output states	−	−	35	mV	RL=100Ω	
VOC	Common Mode Voltage	1.125	1.25	1.375	V		
ΔVOC	Change in VOC between complementary output states	−	−	35	mV		
I_{OS}	Output Short Circuit Current	−	−	−24	mA	V_{OUT}=0V, RL=100Ω	
I_{OZ}	Output TRI-STATE Current	−10	−	+10	μA	XRST=0V, V_{OUT}=0V to VDD	

■Supply Current

Table 7 : Supply Current (VDD=3.3V, Ta=25℃)

Symbol	Parameter	Rating			Units	Conditions		
		Min	Typ	Max				
I_{TCCG}	Transmitter Supply Current (Gray Scale Pattern)	–	TBD	–	mA	RS=H	MODE[1:0]=H H	f=112MHz RL=100Ω CL=5pF
		–	TBD	–			MODE[1:0]=H L	
		–	TBD	–			MODE[1:0]=L H	
		–	TBD	–			MODE[1:0]=L L	
		–	TBD	–	mA	RS=L	MODE[1:0]=H H	
		–	TBD	–			MODE[1:0]=H L	
		–	TBD	–			MODE[1:0]=L H	
		–	TBD	–			MODE[1:0]=L L	
I_{TCCW}	Transmitter Supply Current (Worst Case pattern)	–	TBD	–	mA	RS=H	MODE[1:0]=H H	f=112MHz RL=100Ω CL=5pF
		–	TBD	–			MODE[1:0]=H L	
		–	TBD	–			MODE[1:0]=L H	
		–	TBD	–			MODE[1:0]=L L	
		–	TBD	–	mA	RS=L	MODE[1:0]=H H	
		–	TBD	–			MODE[1:0]=H L	
		–	TBD	–			MODE[1:0]=L H	
		–	TBD	–			MODE[1:0]=L L	
I_{TCCS}	Transmitter Power Down Supply Current	–	–	10	μA	XRST=L		

Gray Scale Pattern

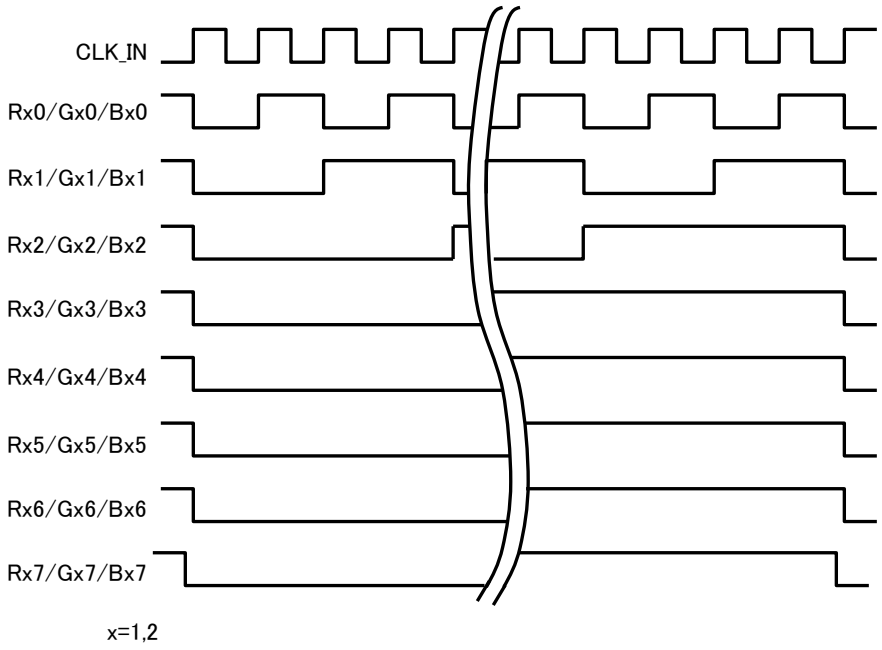


Figure-4　Gray scale pattern

Worst Case Pattern (Maximum Power condition)

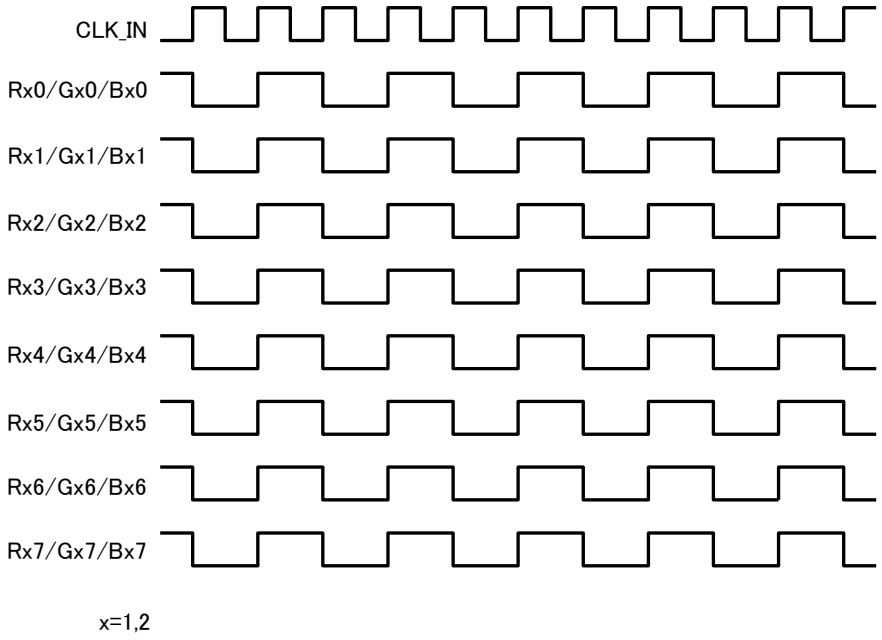


Figure-5　Worst Case Pattern

■AC characteristics

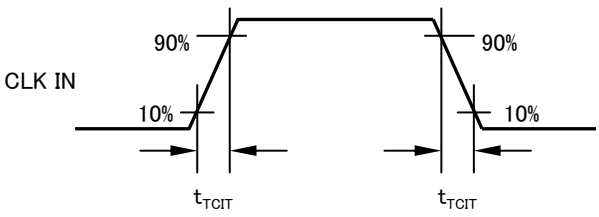
Table 8 : Switching Characteristics (VDD=3.3V, Ta=25℃)

Symbol	Parameter		Min	Typ	Max	Units
t_{TCIT}	CLK IN Transition time		–	–	5.0	ns
t_{TCP}	CLK IN Period	Dual In /Dual Out	8.9	–	125.0	ns
		Dual In / Single Out	17.8	–	62.5	
		Single In / Dual Out	6.7	–	250.0	
		Single In / Single Out	8.9		125.0	
t_{TCH}	CLK IN High Time		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCL}	CLK IN Low Time		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCD}	CLK IN to TCLK+/−Delay	Dual In /Dual Out Single In/Single Out	–	TBD	–	ns
		Dual In / Single Out	–	TBD	–	
		Single In / Dual Out	–	TBD	–	
t_{TS}	CMOS Data Setup to CLK IN		2.5	–	–	ns
t_{TH}	CMOS Data Hold from CLK IN		0	–	–	ns
t_{TCOP}	CLK OUT Period	Dual In /Dual Out	8.9	–	125.0	
		Dual In / Single Out	8.9	–	125.0	
		Single In / Dual Out	13.3	–	125.0	
		Single In / Single Out	8.9		125.0	
t_{LVT}	LVDS Transition Time		–	0.6	1.5	ns
t_{TOP1}	Output Data Position 0		−0.2	0.0	+0.2	ns
t_{TOP0}	Output Data Position 1		$\frac{t_{TCP}}{7}-0.2$	$\frac{t_{TCP}}{7}$	$\frac{t_{TCP}}{7}+0.2$	ns
t_{TOP6}	Output Data Position 2		$2\frac{t_{TCP}}{7}-0.2$	$2\frac{t_{TCP}}{7}$	$2\frac{t_{TCP}}{7}+0.2$	ns
t_{TOP5}	Output Data Position 3		$3\frac{t_{TCP}}{7}-0.2$	$3\frac{t_{TCP}}{7}$	$3\frac{t_{TCP}}{7}+0.2$	ns
t_{TOP4}	Output Data Position 4		$4\frac{t_{TCP}}{7}-0.2$	$4\frac{t_{TCP}}{7}$	$4\frac{t_{TCP}}{7}+0.2$	ns
t_{TOP3}	Output Data Position 5		$5\frac{t_{TCP}}{7}-0.2$	$5\frac{t_{TCP}}{7}$	$5\frac{t_{TCP}}{7}+0.2$	ns
t_{TOP2}	Output Data Position 6		$6\frac{t_{TCP}}{7}-0.2$	$6\frac{t_{TCP}}{7}$	$6\frac{t_{TCP}}{7}+0.2$	ns
T_{ck12}	Skew Time between TCLKXP and TCLKYP		–	–	0.5	ns
t_{TPLL}	Phase Lock Loop Set Time		–	–	10.0	ms

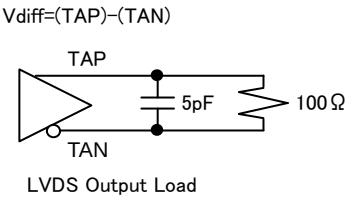
●AC Timing

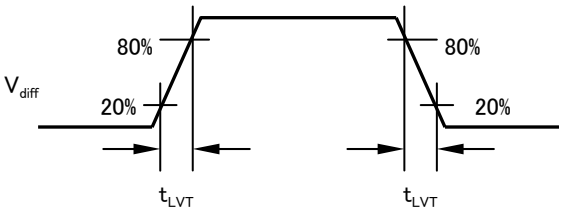
■AC Timing Diagrams

LVCMOS Input

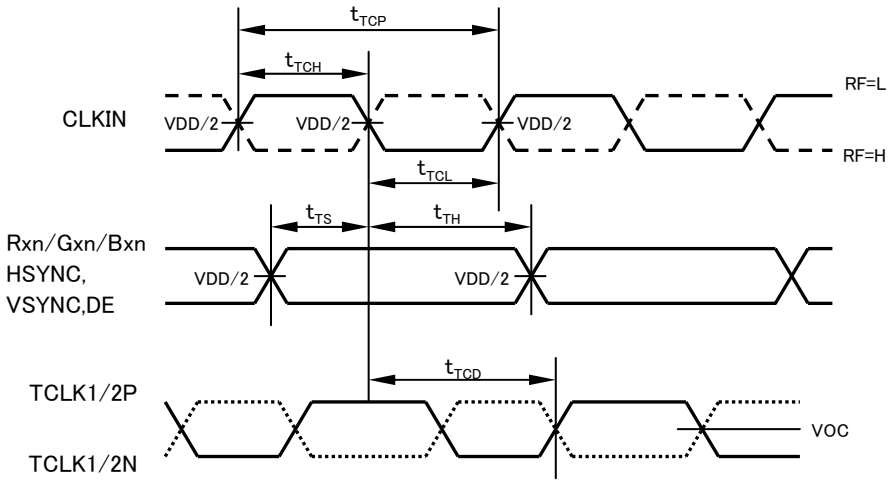


LVDS Output





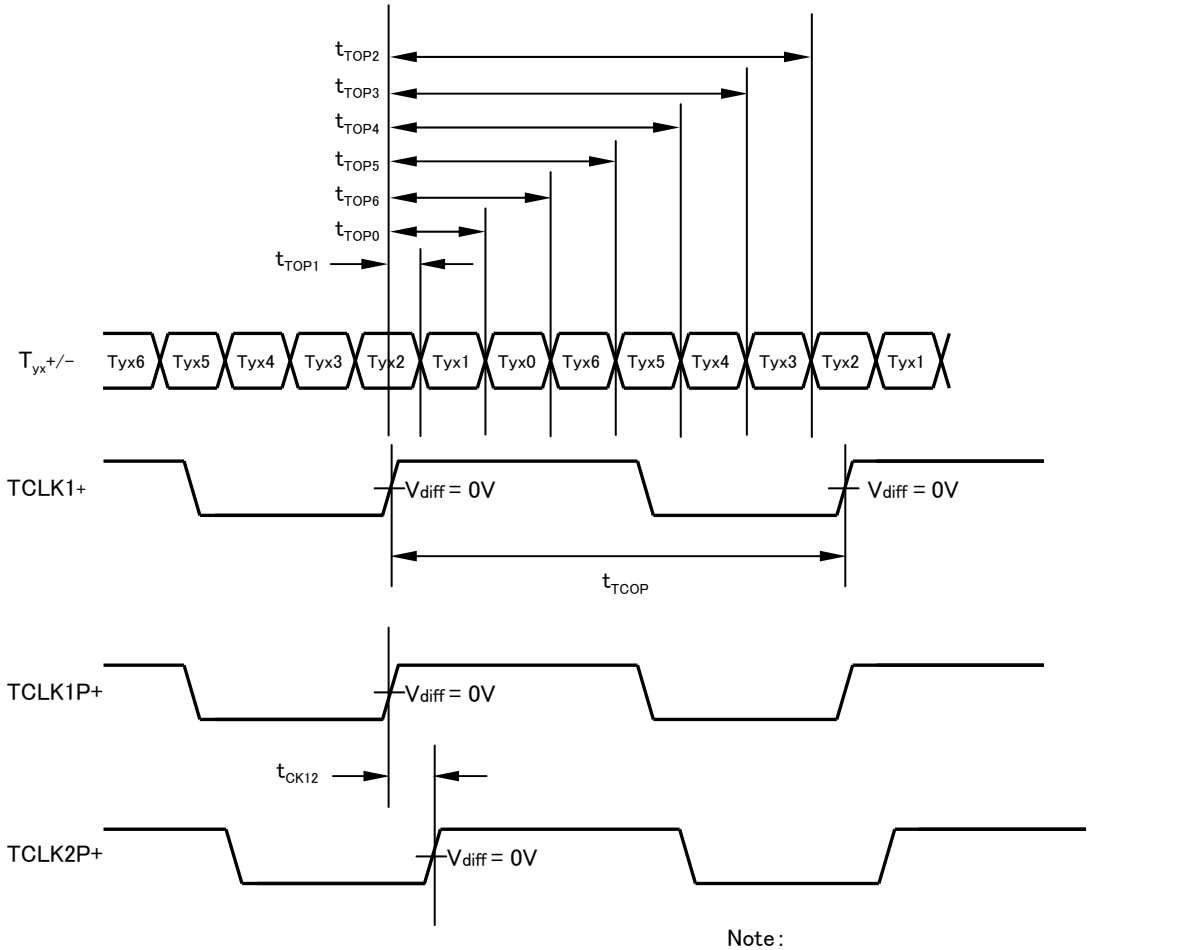
LVCMOS Input



x=1, 2
y=0-7

Figure-6　AC Timing Diagrams

■ AC Timing Diagrams



Note:
Vdiff = (T_{yx}+) − (T_{yx}−), (TCLK1P) − (TCLK1N)

Figure-7 AC Timing Diagrams

X=1.2
Y=A,B,C,D

■Phase Lock Loop Set Time

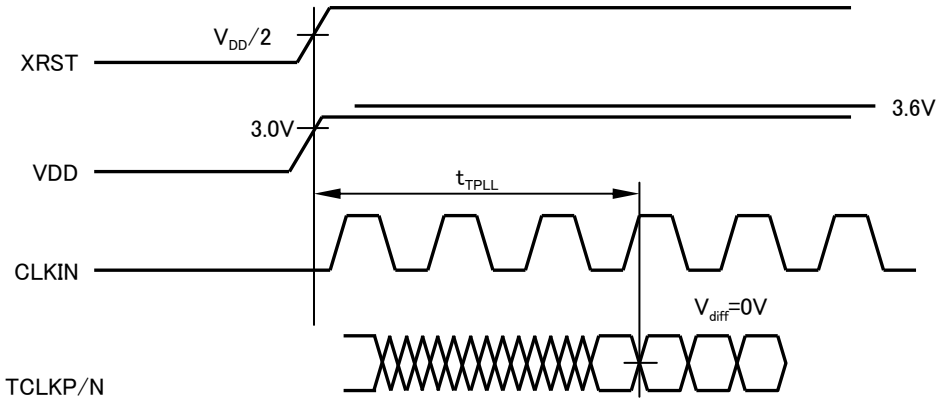


Figure-8 Phase Lock Loop Set Time

●Pixel Map Table for Dual Link

Table 9 : Pixel Map Table for Dual Link

1st Pixel Data				2nd Pixel Data			
TFT Panel Data			BU7988KVT Input	TFT Panel Data			BU7988KVT Input
	24Bit	18Bit			24Bit	18Bit	
LSB	R10	–	R10	LSB	R20	–	R20
	R11	–	R11		R21	–	R21
	R12	R10	R12		R22	R20	R22
	R13	R11	R13		R23	R21	R23
	R14	R12	R14		R24	R22	R24
	R15	R13	R15		R25	R23	R25
	R16	R14	R16		R26	R24	R26
MSB	R17	R15	R17	MSB	R27	R25	R27
LSB	G10	–	G10	LSB	G20	–	G20
	G11	–	G11		G21	–	G21
	G12	G10	G12		G22	G20	G22
	G13	G11	G13		G23	G21	G23
	G14	G12	G14		G24	G22	G24
	G15	G13	G15		G25	G23	G25
	G16	G14	G16		G26	G24	G26
MSB	G17	G15	G17	MSB	G27	G25	G27
LSB	B10	–	B10	LSB	B20	–	B20
	B11	–	B11		B21	–	B21
	B12	B10	B12		B22	B20	B22
	B13	B11	B13		B23	B21	B23
	B14	B12	B14		B24	B22	B24
	B15	B13	B15		B25	B23	B25
	B16	B14	B16		B26	B24	B26
MSB	B17	B15	B17	MSB	B27	B25	B27

●LVDS Data Output Table for Function of FLIP pin

Table 10 : LVDS Data Output Pin Name

Pin No	Output Pin Names	
	FLIP=L	FLIP=H
49	TA1N	TD2P
48	TA1P	TD2N
47	TB1N	TCLK2P
46	TB1P	TCLK2N
44	TC1N	TC2P
43	TC1P	TC2N
42	TCLK1N	TB2P
41	TCLK1P	TB2N
40	TD1N	TA2P
39	TD1P	TA2N
37	TA2N	TD1P
36	TA2P	TD1N
35	TB2N	TCLK1P
34	TB2P	TCLK1N
32	TC2N	TC1P
31	TC2P	TC1N
30	TCLK2N	TB1P
29	TCLK2P	TB1N
28	TD2N	TA1P
27	TD2P	TA1N

●LVCMOS Data Input Timing for Dual Link

Example : SXGA+(1400×1050)

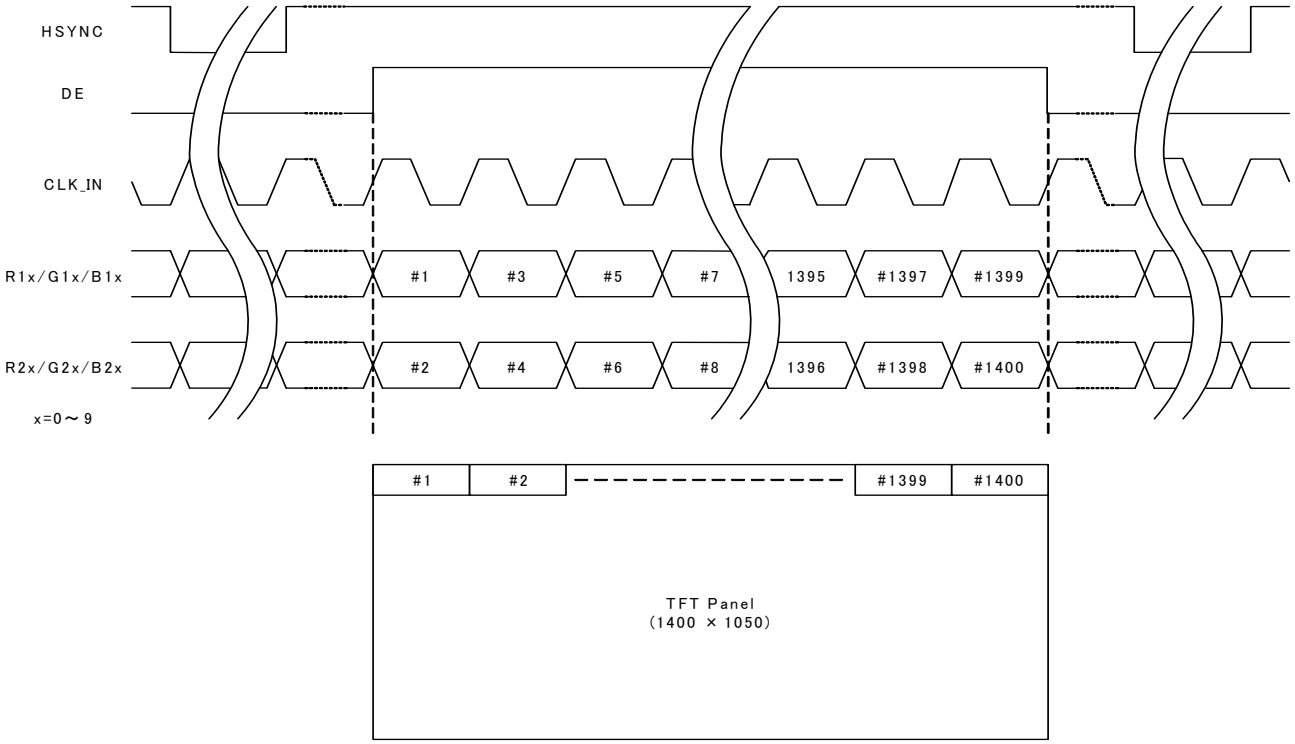


Figure-9　LVCMOS Data Input Timing for Dual Link

●LVCMOS Data Input Timing for Single Link

Example : SXGA+(1400×1050)

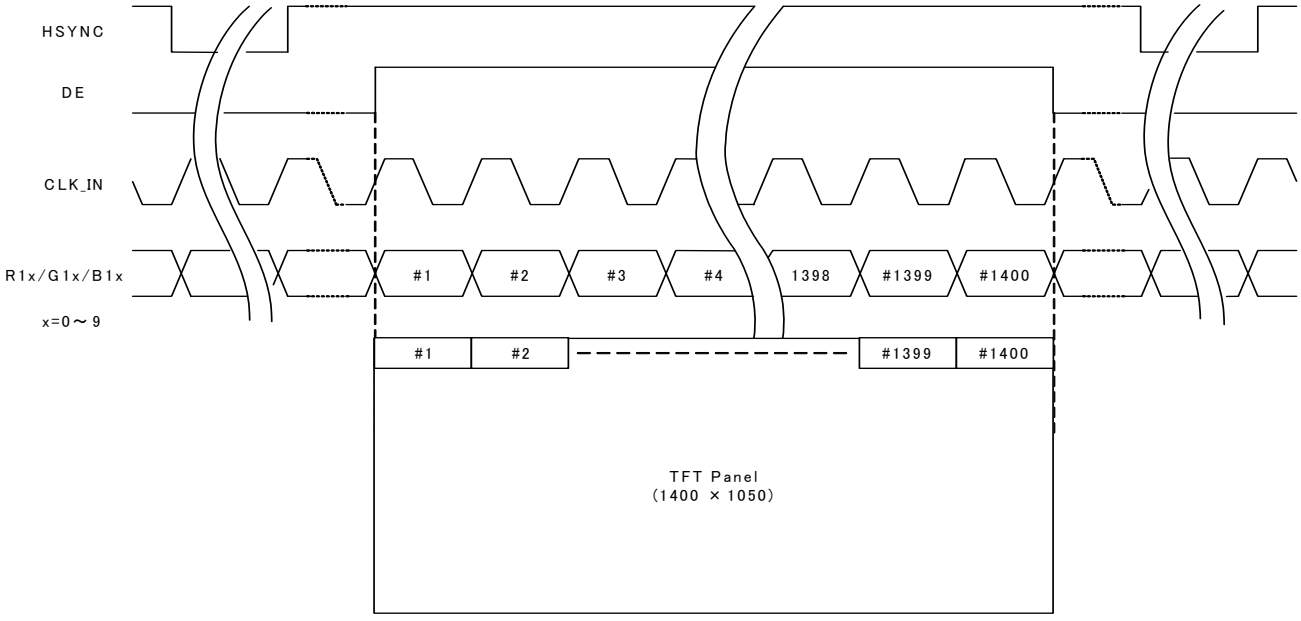
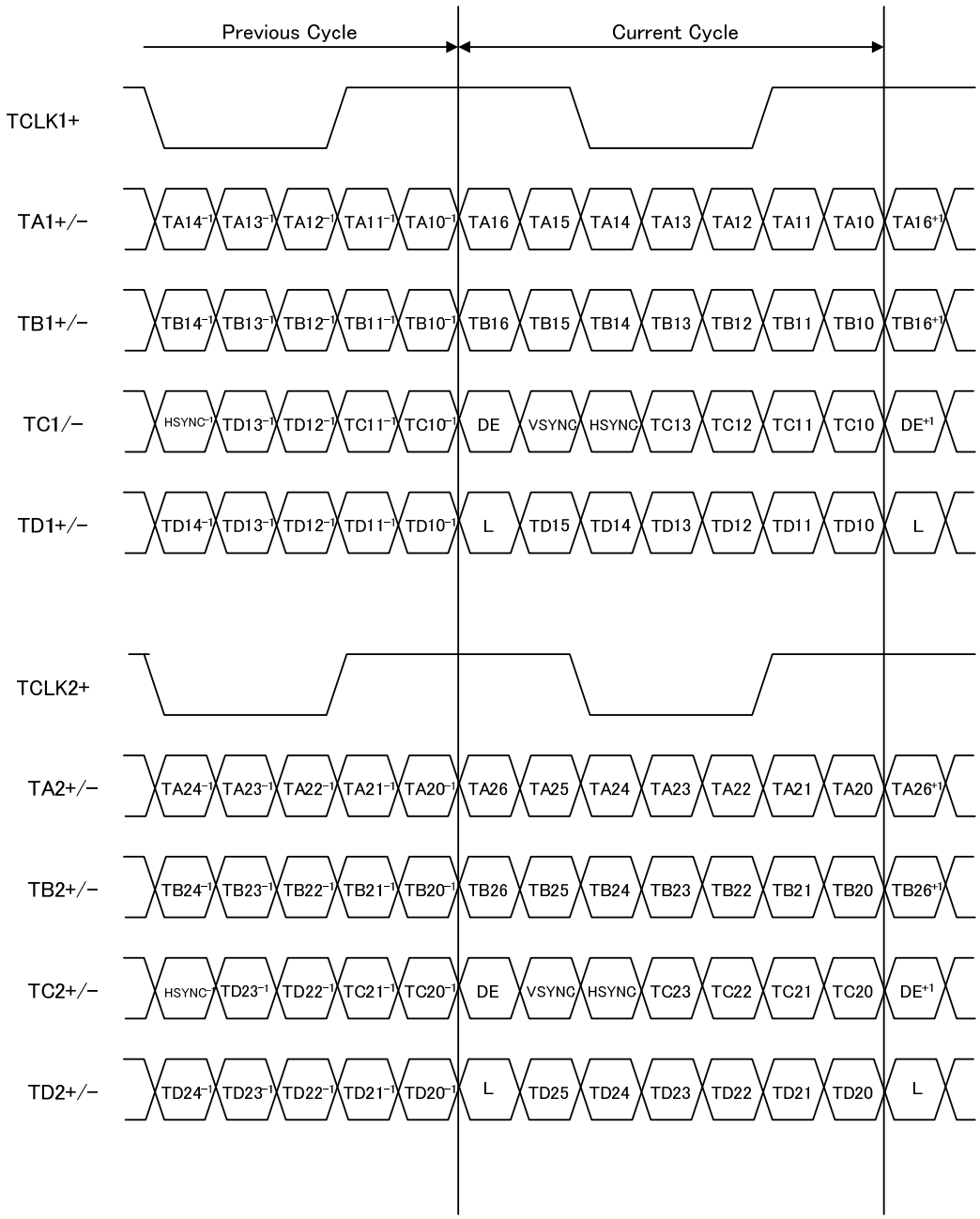
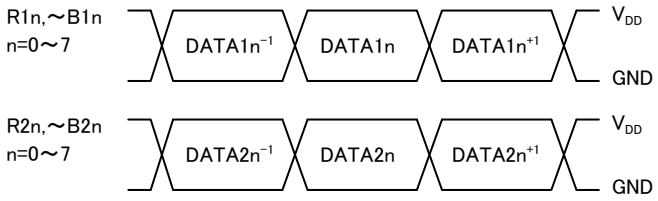


Figure-10 LVCMOS Data Input Timing for Single Link

●LVDS Output Data Mapping （Dual Link / Single Link）



LVDS Data Output



LVCMOS Data Input

Figure-11　LVDS Output Data Mapping

●LVCMOS Data Inputs Timing in Dual Link

Dual-in / Dual-out Mode (MODE<1:0>=LL , FLIP=L)

Table 11 : LVCMOS Data Inputs Timing Diagrams in Dual Link

1st Pixel Data			2nd Pixel Data		
LVDS Output Data (1st Pixel Data)	MAP=H Input Pin Name	MAP=L Input Pin Name	LVDS Output Data (2nd Pixel Data)	MAP=H Input Pin Name	MAP=L Input Pin Name
TA10	R12	R10	TA20	R22	R20
TA11	R13	R11	TA21	R23	R21
TA12	R14	R12	TA22	R24	R22
TA13	R15	R13	TA23	R25	R23
TA14	R16	R14	TA24	R26	R24
TA15	R17	R15	TA25	R27	R25
TA16	G12	G10	TA26	G22	G20
TB10	G13	G11	TB20	G23	G21
TB11	G14	G12	TB21	G24	G22
TB12	G15	G13	TB22	G25	G23
TB13	G16	G14	TB23	G26	G24
TB14	G17	G15	TB24	G27	G25
TB15	B12	B10	TB25	B22	B20
TB16	B13	B11	TB26	B23	B21
TC10	B14	B12	TC20	B24	B22
TC11	B15	B13	TC21	B25	B23
TC12	B16	B14	TC22	B26	B24
TC13	B17	B15	TC23	B27	B25
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R10	R16	TD20	R20	R26
TD11	R11	R17	TD21	R21	R27
TD12	G10	G16	TD22	G20	G26
TD13	G11	G17	TD23	G21	G27
TD14	B10	B16	TD24	B20	B26
TD15	B11	B17	TD25	B21	B27
TD16	L	L	TD26	L	L

●LVCMOS Data Inputs Timing Diagrams in Dual Link

Dual-in / Dual-out Mode　　(MODE<1:0>=LL, FLIP=L, MAP=H)

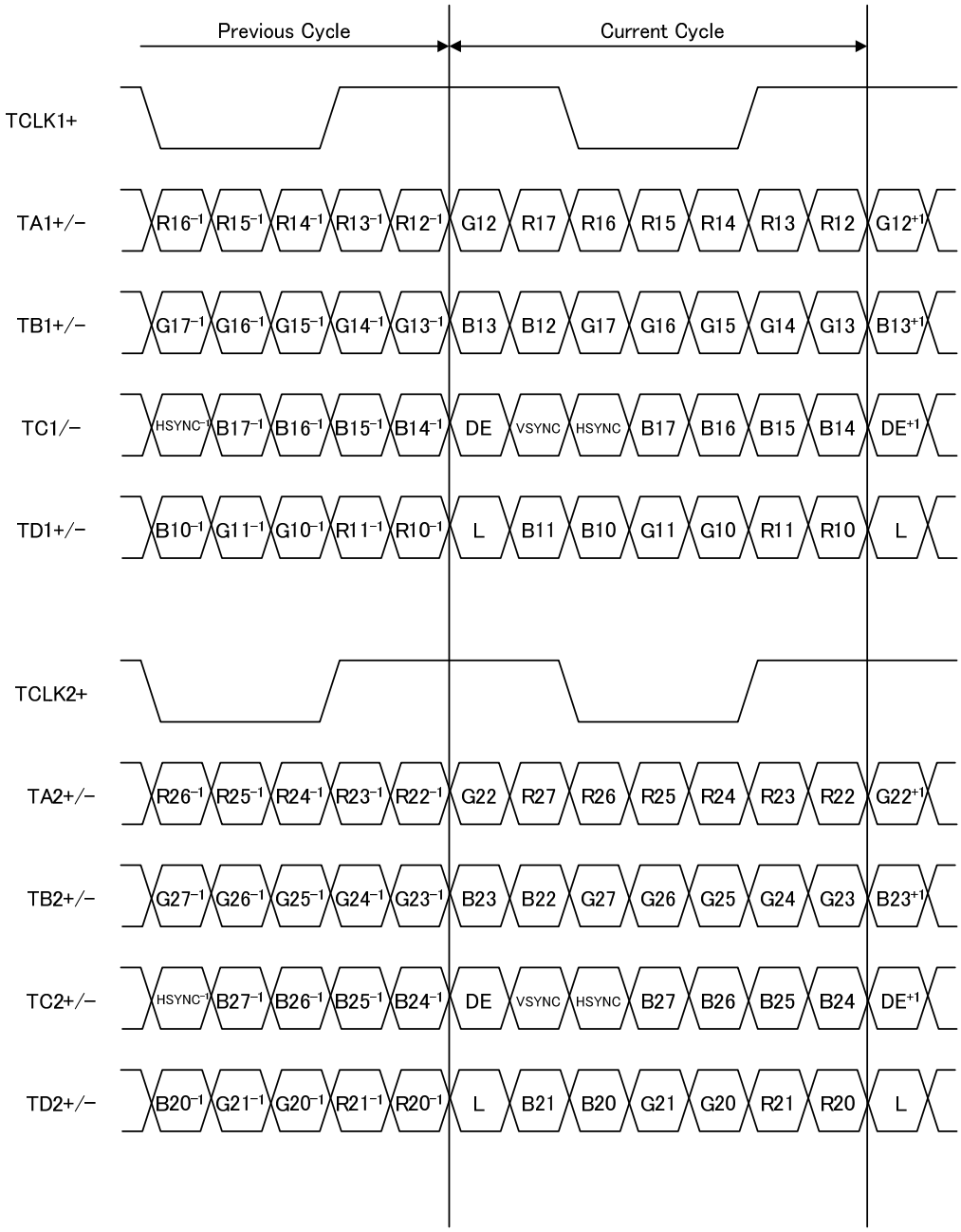


Figure-12　LVCMOS Data Inputs Timing Diagrams in Dual Link

●LVCMOS Data Inputs Timing in Single Link

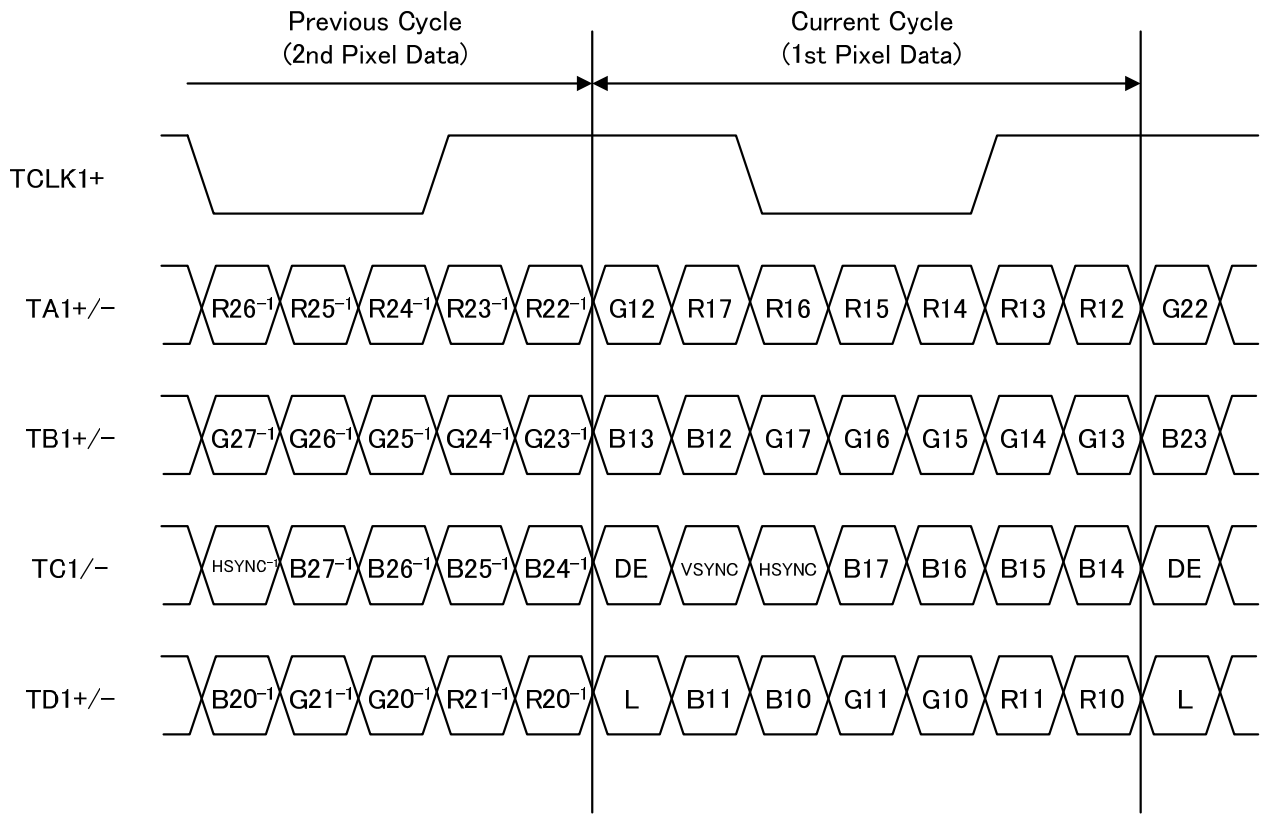
Dual-in / Single-out Mode (MODE<1:0>=LH, FLIP=L)

Table 12 : LVCMOS Data Inputs Timing Diagrams in Dual Link

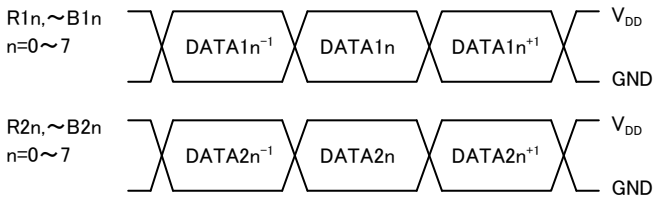
LVDS Output Data (1st Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10	R12/R22	R10/R20
TA11	R13/R23	R11/R21
TA12	R14/R24	R12/R22
TA13	R15/R25	R13/R23
TA14	R16/R26	R14/R24
TA15	R17/R27	R15/R25
TA16	G12/G22	G10/G20
TB10	G13/G23	G11/G21
TB11	G14/G24	G12/G22
TB12	G15/G25	G13/G23
TB13	G16/G26	G14/G24
TB14	G17/G27	G15/G25
TB15	B12/B22	B10/B20
TB16	B13/B23	B11/B21
TC10	B14/B24	B12/B22
TC11	B15/B25	B13/B23
TC12	B16/B26	B14/B24
TC13	B17/B27	B15/B25
TC14	HSYNC	HSYNC
TC15	VSYNC	VSYNC
TC16	DE	DE
TD10	R10/R20	R16/R26
TD11	R11/R21	R17/R27
TD12	G10/G20	G16/G26
TD13	G11/G21	G17/G27
TD14	B10/B20	B16/B26
TD15	B11/B21	B17/B27
TD16	L	L

●LVCMOS Data Inputs Timing Diagrams in Single Link

Dual-in / Single-out Mode　　(MODE<1:0>=LH, FLIP=L, MAP=H)



LVDS Data Output



LVCMOS Data Input

Figure-13　LVCMOS Data Inputs Timing Diagrams in Single Link

●LVCMOS Data Inputs Timing in Single Link

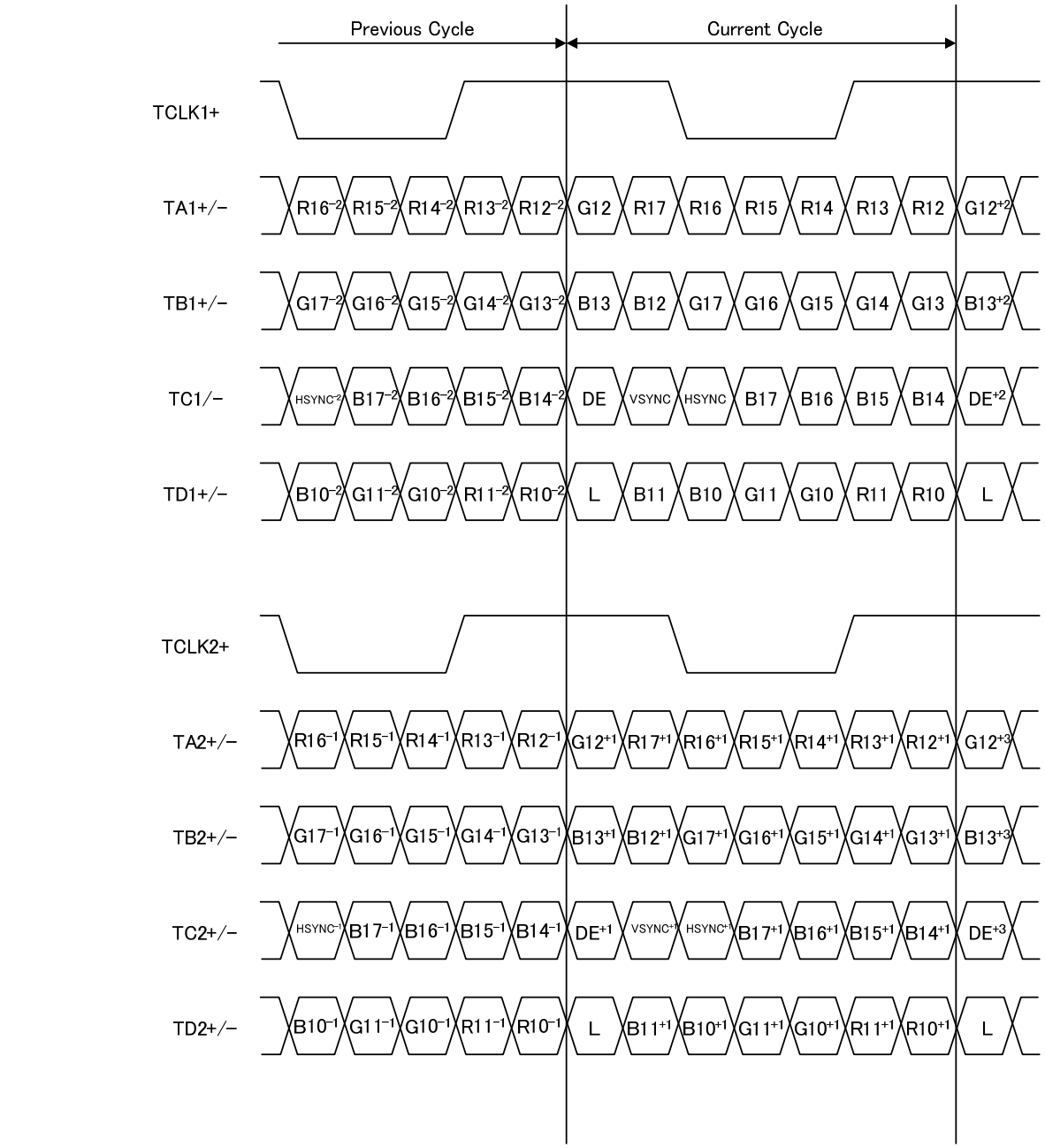
Single-in / Dual-out Mode (MODE<1:0>=HH, FLIP=L)

Table 13 : LVCMOS Data Inputs Timing Diagrams in Single Link

1st Pixel Data			2nd Pixel Data		
LVDS Output Data (1st Pixel Data)	MAP=H Input Pin Name	MAP=L Input Pin Name	LVDS Output Data (1st Pixel Data)	MAP=H Input Pin Name	MAP=L Input Pin Name
TA10	R12	R10	TA20	$R12^{+1}$	$R10^{+1}$
TA11	R13	R11	TA21	$R13^{+1}$	$R11^{+1}$
TA12	R14	R12	TA22	$R14^{+1}$	$R12^{+1}$
TA13	R15	R13	TA23	$R15^{+1}$	$R13^{+1}$
TA14	R16	R14	TA24	$R16^{+1}$	$R14^{+1}$
TA15	R17	R15	TA25	$R17^{+1}$	$R15^{+1}$
TA16	G12	G10	TA26	$G12^{+1}$	$G10^{+1}$
TB10	G13	G11	TB20	$G13^{+1}$	$G11^{+1}$
TB11	G14	G12	TB21	$G14^{+1}$	$G12^{+1}$
TB12	G15	G13	TB22	$G15^{+1}$	$G13^{+1}$
TB13	G16	G14	TB23	$G16^{+1}$	$G14^{+1}$
TB14	G17	G15	TB24	$G17^{+1}$	$G15^{+1}$
TB15	B12	B10	TB25	$B12^{+1}$	$B10^{+1}$
TB16	B13	B11	TB26	$B13^{+1}$	$B11^{+1}$
TC10	B14	B12	TC20	$B14^{+1}$	$B12^{+1}$
TC11	B15	B13	TC21	$B15^{+1}$	$B13^{+1}$
TC12	B16	B14	TC22	$B16^{+1}$	$B14^{+1}$
TC13	B17	B15	TC23	$B17^{+1}$	$B15^{+1}$
TC14	HSYNC	HSYNC	TC24	$HSYNC^{+1}$	$HSYNC^{+1}$
TC15	VSYNC	VSYNC	TC25	$VSYNC^{+1}$	$VSYNC^{+1}$
TC16	DE	DE	TC26	DE^{+1}	DE^{+1}
TD10	R10	R16	TD20	$R10^{+1}$	$R16^{+1}$
TD11	R11	R17	TD21	$R11^{+1}$	$R17^{+1}$
TD12	G10	G16	TD22	$G10^{+1}$	$G16^{+1}$
TD13	G11	G17	TD23	$G11^{+1}$	$G17^{+1}$
TD14	B10	B16	TD24	$B10^{+1}$	$B16^{+1}$
TD15	B11	B17	TD25	$B11^{+1}$	$B17^{+1}$
TD16	L	L	TD26	L	L

●LVCMOS Data Inputs Timing in Dual Link

Single-in / Dual-out Mode **(MODE<1:0>=HL, FLIP=L, MAP=H)**



LVDS Data Output



LVCMOS Data Input

Figure-14 LVCMOS Data Inputs Timing in Dual Link

●LVCMOS Data Inputs Timing in Single Link

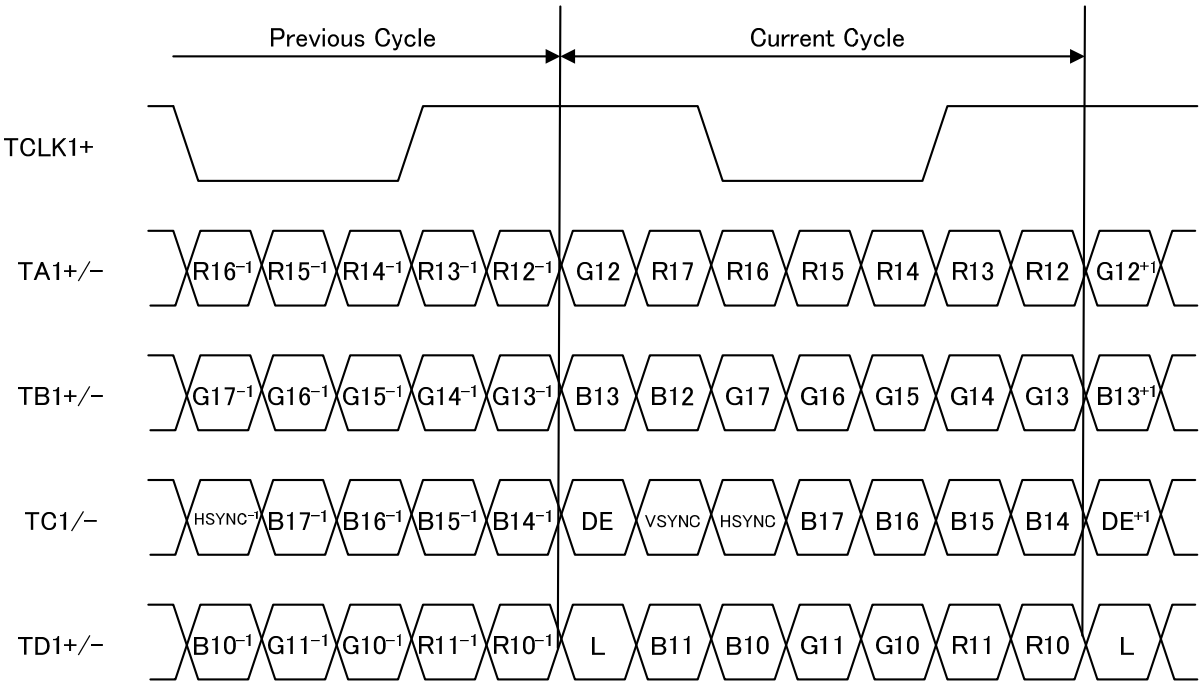
Single-in / Single-out Mode (MODE<1:0>=HH, FLIP=L)

Table 14 : LVCMOS Data Inputs Timing Diagrams in Single Link

LVDS Output Data (1st Pixel Data)	MAP=H Input Pin Name	MAP=L Input Pin Name
TA10	R12	R10
TA11	R13	R11
TA12	R14	R12
TA13	R15	R13
TA14	R16	R14
TA15	R17	R15
TA16	G12	G10
TB10	G13	G11
TB11	G14	G12
TB12	G15	G13
TB13	G16	G14
TB14	G17	G15
TB15	B12	B10
TB16	B13	B11
TC10	B14	B12
TC11	B15	B13
TC12	B16	B14
TC13	B17	B15
TC14	HSYNC	HSYNC
TC15	VSYNC	VSYNC
TC16	DE	DE
TD10	R10	R16
TD11	R11	R17
TD12	G10	G16
TD13	G11	G17
TD14	B10	B16
TD15	B11	B17
TD16	L	L

●LVCMOS Data Inputs Timing Diagrams in Single Link

Single-in / Single-out Mode　　(MODE<1:0>=HH, FLIP=L, MAP=H)



LVDS Data Output



LVCMOS Data Input

Figure-15 LVCMOS Data Inputs Timing Diagrams in Single Link

●About the Power On Reset

Power On Reset is not mandatory for this device.
(The PD pin should be set to high level when Power On Reset procedure is not used.)

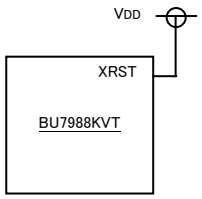


Figure-16 terminal connection when Power On Reset is not used

However, Power On Reset procedure is strongly recommend for internal logic initialization by following two methods.

① The method of using CR circuit.
② The method of using external specific IC.

It is recommend to do enough examination for target application.

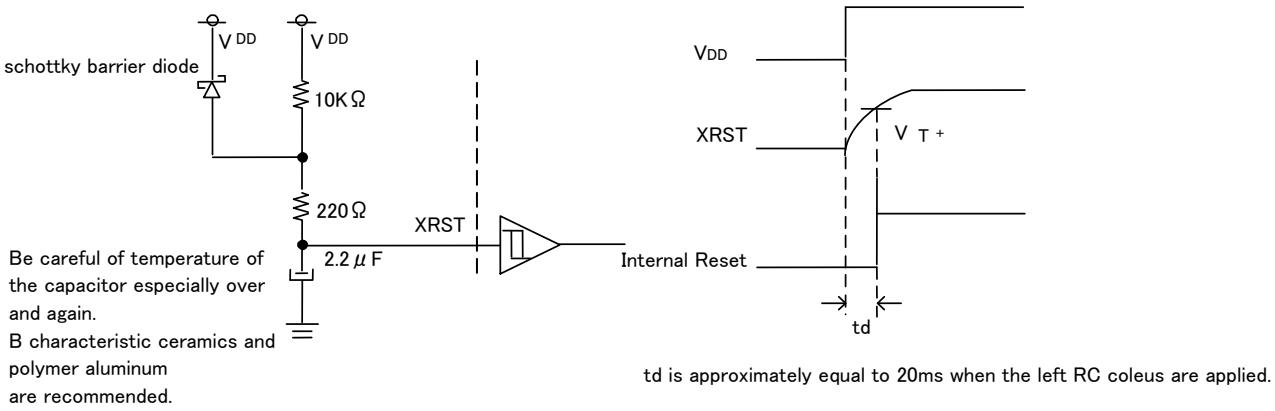


Figure-17 Power On Reset by external a CR circuit

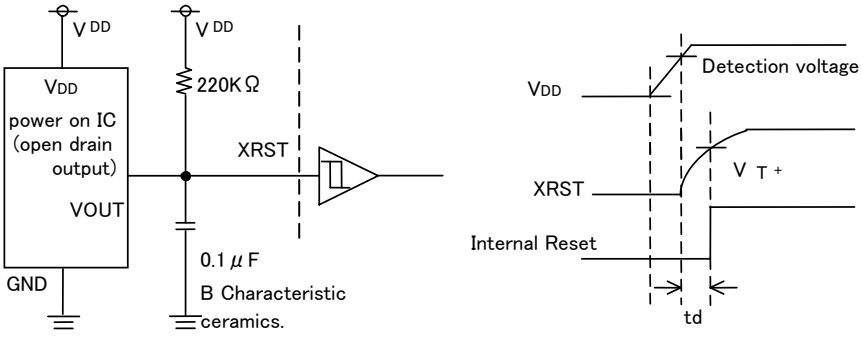
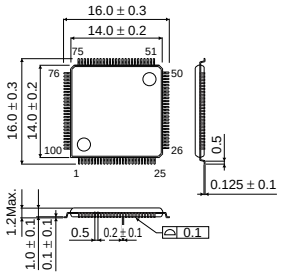


Figure-18 Power On Reset by specific IC

TQFP100V

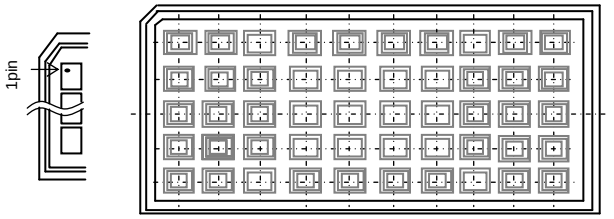
<Dimension>



(Unit:mm)

<Packing information>

Container	Tray(with dry pack)
Quantity	500pcs
Direction of feed	Direction of product is fixed in a tray.



※When you order , please order in times the amount of package quantity.

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