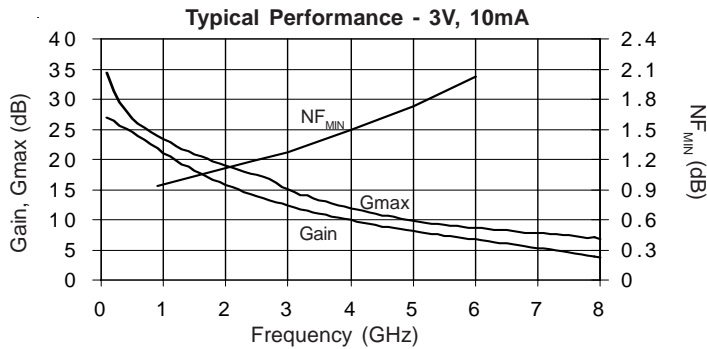




Product Description

Sirenza Microdevices' SGA-8343 is a high performance Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) designed for operation from DC to 6 GHz. The SGA-8343 is optimized for 3V operation but can be biased at 2V for low-voltage battery operated systems. The device provides high gain, low NF, and excellent linearity at a low cost. It can be operated at very low bias currents in applications where high linearity is not required.

The matte tin finish on Sirenza's lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.



SGA-8343

SGA-8343Z



Low Noise, High Gain SiGe HBT



Product Features

- Now Available in Lead Free, RoHS Compliant, & Green Packaging
- DC-6 GHz Operation
- 0.9 dB NF_{MIN} @ 0.9 GHz
- 24 dB G_{max} @ 0.9 GHz
- $|G_{OPT}|=0.10$ @ 0.9 GHz
- $OIP3 = +28$ dBm, $P1dB = +9$ dBm
- Low Cost, High Performance, Versatility

Applications

- Analog and Digital Wireless Systems
- 3G, Cellular, PCS, RFID
- Fixed Wireless, Pager Systems
- Driver Stage for Low Power Applications
- Oscillators

| Symbol | Device Characteristics | Test Conditions $V_{CE}=3V, I_{CE}=10mA, 25^{\circ}C$ (unless otherwise noted) | Test Frequency | Units | Min. | Typ. | Max. |
|------------|---|--|-------------------------------|---------------|------|----------------------|------|
| G_{MAX} | Maximum Available Gain | $Z_S=Z_S^*, Z_L=Z_L^*$ | 0.9 GHz 1.9 GHz 2.4 GHz | dB | | 23.9 19.3 17.7 | |
| NF | Minimum Noise Figure | $Z_S=Gamma_{OPT}, Z_L=Z_L^*$ | 0.9 GHz 1.9 GHz 2.4 GHz | dB | | 0.94 1.10 1.18 | |
| S_{21} | Insertion Gain ^[1] | $Z_S=Z_L= 50$ Ohms | 0.9 GHz | dB | 21.0 | 22.0 | 23.0 |
| NF | Noise Figure ^[2] | LNA Application Circuit Board | 1.9 GHz | dB | | 1.40 | 1.75 |
| Gain | Gain ^[2] | LNA Application Circuit Board | 1.9 GHz | dB | 15.5 | 16.5 | 17.5 |
| OIP_3 | Output Third Order Intercept Point ^[2] | LNA Application Circuit Board | 1.9 GHz | dBm | 25.8 | 27.8 | |
| P_{1dB} | Output 1dB Compression Point ^[2] | LNA Application Circuit Board | 1.9 GHz | dBm | 7.5 | 9.0 | |
| h_{FE} | DC Current Gain | | | | 120 | 180 | 300 |
| BV_{CEO} | Collector-Emitter Breakdown Voltage | | | V | 5.7 | 6.0 | |
| Rth | Thermal Resistance | junction-to-lead | | $^{\circ}C/W$ | | 200 | |
| V_{CE} | Operating Voltage | collector-emitter | | V | | | 4.0 |
| I_{CE} | Operating Current | collector-emitter | | mA | | | 50 |

[1] 100% tested - Insertion gain tested using a 50 ohm contact board (no matching circuitry) during final production test.

[2] Sample tested - Samples pulled from each wafer/package lot. Sample test specifications are based on statistical data from sample test measurements. The test fixture is an engineering application circuit board (parts are pressed down on the circuit board). The application circuit represents a trade-off between the optimal noise match and input return loss.

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Junction Temperature Calculation

MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the device operating conditions should also satisfy the following expression:

$$P_{DC} < (T_J - T_L) / R_{TH}$$

where:

$$P_{DC} = I_{CE} * V_{CE} \text{ (W)}$$

T_J = Junction Temperature (C)
 T_L = Lead Temperature (pin 2) (C)
 R_{TH} = Thermal Resistance (C/W)

Biasing Details

The SGA-8343 should be biased through a dropping resistor or with active bias circuitry to prevent thermal runaway and combat Beta variation. For passive biasing it is recommended that the voltage drop be at least 20% of V_{CE} . A voltage divider from collector-to-base is preferred over a simple series resistor. The effect of Beta variation can be minimized by bleeding $\sim 10 * I_B$ through the shunt resistor.

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--------------------------------|------------|-------------|------|
| Collector Current | I_{CE} | 72 | mA |
| Base Current | I_B | 1 | mA |
| Collector - Emitter Voltage | V_{CE} | 5 | V |
| Collector - Base Voltage | V_{CB} | 12 | V |
| Emitter - Base Voltage | V_{EB} | 4.5 | V |
| RF Input Power | P_{IN} | 5 | dBm |
| Storage Temperature Range | T_{stor} | -40 to +150 | C |
| Power Dissipation | P_{DISS} | 350 | mW |
| Operating Junction Temperature | T_J | +150 | C |

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

Typical Performance - Engineering Application Circuits (See App Note AN-044)

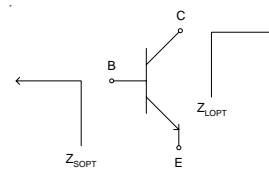
| Freq (GHz) | Vs (V) | V_{CE} (V) | I_{CQ} (mA) | NF (dB) | Gain (dB) | P1dB (dBm) | OIP3 ^[3] (dBm) | S11 (dB) | S22 (dB) | Comments |
|------------|--------|--------------|---------------|---------|-----------|------------|---------------------------|----------|----------|-----------------|
| 0.90 | 5.0 | 3.0 | 12 | 1.25 | 18.2 | 9 | 27.3 | -16 | -18 | series feedback |
| 1.575 | 3.3 | 2.7 | 10 | 1.25 | 15.7 | 6.8 | 26.5 | -10 | -25 | see AN-061 |
| 1.90 | 5.0 | 3.0 | 12 | 1.4 | 16.5 | 9 | 27.8 | -9 | -24 | |
| 2.40 | 3.3 | 2.7 | 10 | 1.6 | 14.4 | 9 | 27.5 | -13 | -24 | |

^[3] P_{OUT} = 0 dBm per tone, 1MHz tone spacing

Refer to the application note for additional RF data, PCB layouts, BOMs, biasing instructions, and other key issues to be considered. For the latest application note please visit our site at www.sirenza.com.

Peak RF Performance Under Optimum Matching Conditions

| Freq (GHz) | V_{CE} (V) | I_{CQ} (mA) | NF _{MIN} ^[4] (dB) | Gmax (dB) | P1dB ^[5] (dBm) | OIP3 ^[6] (dBm) |
|------------|--------------|---------------|---------------------------------------|-----------|---------------------------|---------------------------|
| 0.90 | 2 | 10 | 0.90 | 23.7 | 10 | 25 |
| | 3 | 10 | 0.94 | 23.9 | 13 | 29 |
| 1.90 | 2 | 10 | 1.05 | 19.1 | 10 | 25 |
| | 3 | 10 | 1.10 | 19.3 | 13 | 29 |
| 2.40 | 2 | 10 | 1.15 | 17.4 | 10 | 25 |
| | 3 | 10 | 1.18 | 17.7 | 13 | 29 |



^[4] $Z_S = \Gamma_{OPT}^*$, $Z_L = Z_L^*$, The input matching circuit losses have been de-embedded.

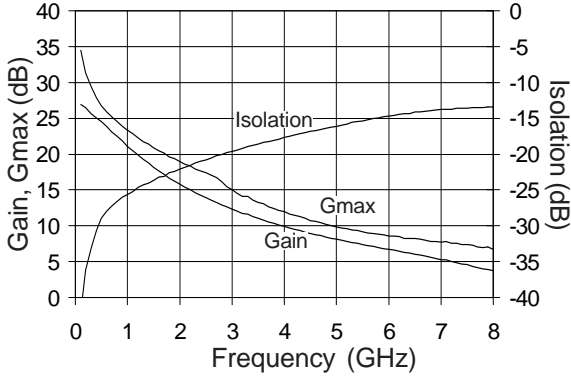
^[5] $Z_S = Z_{SOPT}$, $Z_L = Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max P1dB (current allowed to drive-up with constant V_{CE})

^[6] $Z_S = Z_{SOPT}$, $Z_L = Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max OIP3

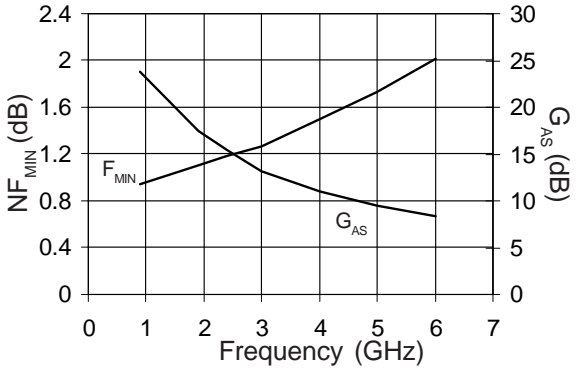
Note: Optimum NF, P1dB, and OIP3 performance cannot be achieved simultaneously.

Typical Performance - De-embedded S-Parameters

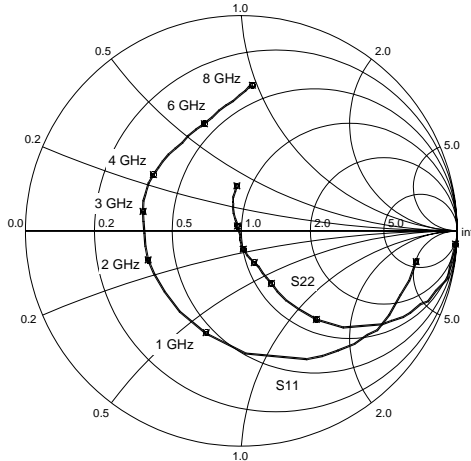
Gain vs Frequency (3V,10mA)



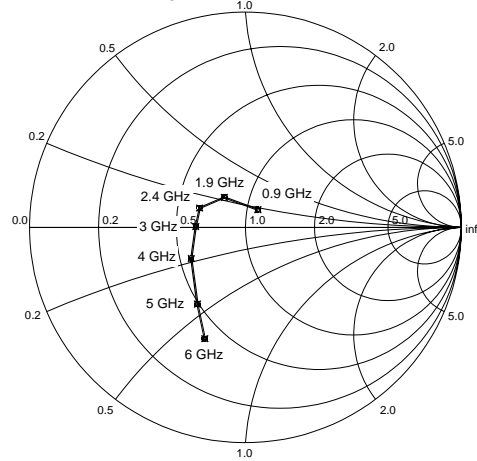
Minimum Noise Figure (3V,10mA)



S11,S22 vs Frequency (3V,10mA)



Γ_OPT (3V,10mA)



Note: S-parameters are de-embedded to the device leads with $Z_S=Z_L=50\Omega$. The device was mounted on a 0.010" PCB with plated-thru holes close to pins 2 and 4. De-embedded s-parameters can be downloaded from our website (www.sirenza.com).

Typical Performance - Noise Parameters - 3V,10mA

| Frequency (GHz) | NF _{MIN} ^[7] (dB) | Γ _{OPT} Mag ∠ Ang | r _n (Ω) | Gmax (dB) |
|-----------------|---------------------------------------|----------------------------|--------------------|-----------|
| 0.9 | 0.94 | 0.10 ∠ 55 | 0.11 | 23.88 |
| 1.9 | 1.1 | 0.17 ∠ 125 | 0.10 | 19.33 |
| 2.4 | 1.18 | 0.23 ∠ 157 | 0.09 | 17.66 |
| 3 | 1.27 | 0.23 ∠ 179 | 0.09 | 15.01 |
| 4 | 1.5 | 0.29 ∠ -150 | 0.12 | 11.94 |
| 5 | 1.73 | 0.42 ∠ -122 | 0.18 | 9.84 |
| 6 | 2.02 | 0.55 ∠ -110 | 0.24 | 8.62 |

^[7] $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$, NF_{MIN} is a noise parameter for which the input matching circuit losses have been de-embedded. The noise parameters were measured using a Maury Microwave Automated Tuner System. The device was mounted on a 0.010" PCB with plated-thru holes close to pins 2 and 4.



Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Pin Description

| Pin # | Function | Description |
|-------|-----------|--|
| 1 | Base | RF Input / Base Bias |
| 2 | Emitter | Connection to ground. Use multiple via holes to reduce emitter inductance. |
| 3 | Collector | RF Output / Collector Bias |
| 4 | Emitter | Same as Pin 2 |

Part Number Ordering Information

| Part Number | Reel Size | Devices/Reel |
|-------------|-----------|--------------|
| SGA-8343 | 7" | 3000 |
| SGA-8343Z | 7" | 3000 |

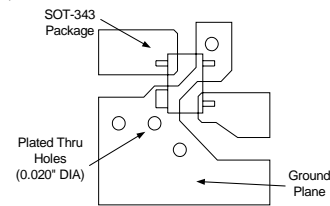
Part Symbolization

The part will be symbolized with the "A83" or "A83Z" designator and a dot signifying pin 1 on the top surface of the package.

MARKING

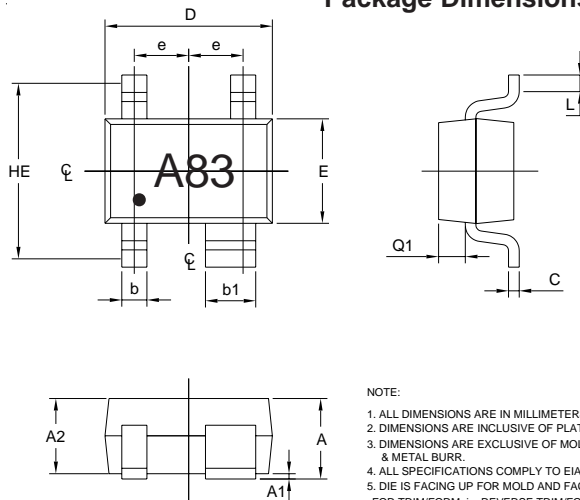


Recommended PCB Layout



Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.

Package Dimensions



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. DIMENSIONS ARE INCLUSIVE OF PLATING.
 3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
 4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
 5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM, ie :REVERSE TRIM/FORM.
 6. PACKAGE SURFACE TO BE MIRROR FINISH.

| SYMBOL | MIN | MAX |
|--------|----------|------|
| E | 1.15 | 1.35 |
| D | 1.85 | 2.25 |
| HE | 1.80 | 2.40 |
| A | 0.80 | 1.10 |
| A2 | 0.80 | 1.00 |
| A1 | 0.00 | 0.10 |
| Q1 | 0.10 | 0.40 |
| e | 0.65 BSC | |
| b | 0.25 | 0.40 |
| b1 | 0.55 | 0.70 |
| c | 0.10 | 0.18 |
| L | 0.10 | 0.30 |