TUSB542 USB Type-C 5 Gbps Redriver 2:1 MUX

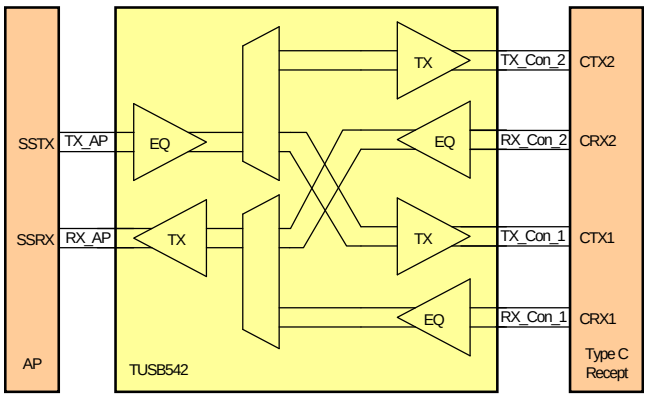
1 Features

- Provides USB 3.1 Gen-1 5 Gbps Super Speed (SS) 2:1 Mux for a USB Type-C Port
- Supports USB Type-C Cable and Connector Specifications
- Ultra Low-Power Architecture
  - Active 100 mA
  - U2/U3 1.3 mA
  - No Connection 300 µA
- Selectable Equalization, De-Emphasis, and Output Swing
- Automatic LFPS De-Emphasis Control for USB 3.1 Compliance
- Integrated Termination
- RX-detect Function
- Signal Monitoring for Power Management
- No Host/Device Side Requirement – Can Support USB-C DFP, UFP or DRP Port
- Single Supply Voltage 1.8 V ±10%
- Industrial Temperature Range of –40 – 85°C

2 Applications

- USB Type-C SS Application
  - Phones
  - Tablets, Phablets and Notebooks
  - Docking Stations

Simplified Schematic



3 Description

The TUSB542 is a dual channel USB 3.1 Gen1 (5 Gbps) re-driver supporting systems with USB Type-C connectors. The device offers signal conditioning plus the ability to switch the USB SS signals for the USB Type-C flippable connector. The TUSB542 can be controlled through the SEL pin by an external Configuration Channel Logic Controller to properly mux the signals.

The TUSB542 incorporates receiver equalization and transmitter de-emphasis to maintain signal integrity on both transmit and receive data paths. The receiver equalization offers multiple gain settings to overcome channel degradation from insertion loss and inter-symbol interference. To compensate for downstream transmission line losses, the output driver supports de-emphasis configuration. Additionally, automatic LFPS de-emphasis control allows for full compliance.

The TUSB542 offers low power consumption on a 1.8-V supply with its ultra-low power architecture. The re-driver supports low power modes, which further reduce the idle power consumption.

The Type-C USB redriver is available in a small ultra-thin package, which is suitable for many portable applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB542	X2QFN (18)	2.00 mm x 2.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Sample Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (January 2016) to Revision B	Page
• Changed the RX_AP+ (pin 18) and RX_AP- (pin 17) I/O Type and Description to Diff output	3
• Changed the TX_AP+ (pin 15) and RX_AP- (pin 14) I/O Type and Description to Diff input	3

Changes from Original (December 2015) to Revision A	Page
• Changed the TX_AP and RX_AP pins in the *Simplified Schematic*	1
• Changed the RX_AP+, RX_AP- and TX_AP+, TX_PA- pins in the RWQ Package	3
• Changed pin RX_AP+ number From: 15 To: 18	3
• Changed pin RX_AP- number From: 14 To: 17	3
• Changed pin TX_AP+ number From: 18 To: 15	3
• Changed pin TX_AP- number From: 17 To: 14	3
• Changed Table 1	11
• Changed Figure 13	11
• Changed the *Functional Block Diagram*	12
• Changed location of pins SSTXP, SSTXN and SSRXP, SSRXN in Figure 16	16

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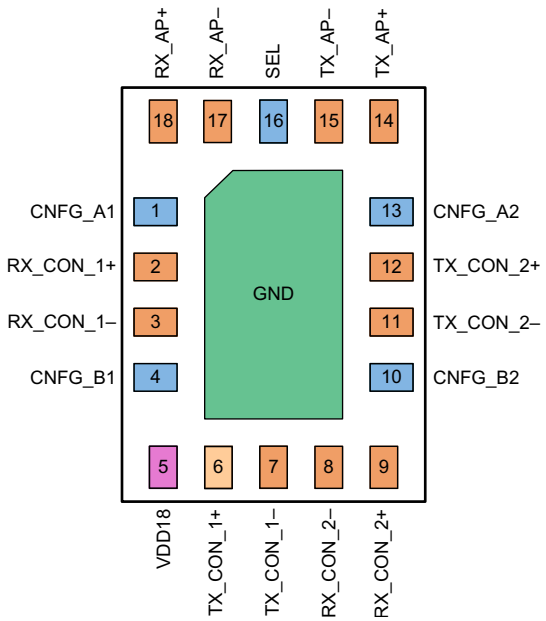
5 Pin Configuration and Functions

RWQ Package
18 Pins (X2QFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD18	5	P	1.8 V Power Supply
GND	PAD	G	Reference Ground Thermal Pad. Must connect to GND on the board.
SEL	16	Input	2:1 SS MUX control. See Table 1 for signal path settings.210KΩ internal pullup resistor. H: AP SS signals are connected to Type-C position 1 signals. L: AP SS signals are connected to Type-C position 2 signals
CNFG_A1	1	Tri-level Input	Tri-level configuration input pin A1 (for Ch 1): sets channel 1 (AP to redriver) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105 kΩ. Refer to Table 2 for configuration settings.
CNFG_B1	4	Tri-level Input	Tri-level configuration input pin B1 (for Ch 1): sets channel 1 (AP to redriver) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105 kΩ. Refer to Table 2 for configuration settings.
CNFG_A2	13	Tri-level Input	Tri-level configuration input pin A2 (for Ch 2): sets channel 2 (redriver to device) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 10 5kΩ. Refer to Table 2 for configuration settings.
CNFG_B2	10	Tri-level Input	Tri-level configuration input pin B2 (for Ch 2): sets channel 2 (redriver to device) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105 kΩ.refer to Table 2 for configuration settings.
RX_AP+	18	Diff output	Differential output to Application Processor (AP), 5 Gbps SS positive signal
RX_AP-	17	Diff output	Differential output to AP, 5 Gbps SS negative signal
TX_AP+	15	Diff input	Differential input from AP, 5 Gbps SS positive signal
TX_AP-	14	Diff input	Differential input from AP, 5 Gbps SS negative signal
Rx_Con_1+	2	Diff input	Differential input from Type-C Connector, Position 1, SS positive signal
Rx_Con_1-	3	Diff input	Differential input from Type-C Connector, Position 1, SS negative signal
Tx_Con_1+	6	Diff output	Differential output to Type-C Connector, Position 1, SS positive signal
Tx_Con_1-	7	Diff output	Differential output to Type-C Connector, Position 1, SS negative signal
Rx_Con_2-	8	Diff input	Differential input from Type-C Connector, Position 2, SS negative signal

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
Rx_Con_2+	9	Diff input	Differential input from Type-C Connector, Position 2, SS positive signal
Tx_Con_2+	12	Diff output	Differential output to Type-C Connector, Position 2, SS positive signal
Tx_Con_2-	11	Diff output	Differential output to Type-C Connector, Position 2, SS negative signal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		–0.3	2.3	V
Voltage range at any input or output terminal	Differential I/O	–0.3	1.5	V
	CMOS Inputs	–0.3	2.3	V
Junction temperature, T_J		65	150	°C
Storage temperature, T_{stg}			105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	1.62	1.8	1.98	V
T_A	Operating free-air temperature	–40		85	°C
$C_{(AC)}$	AC coupling capacitor required for TX pins	75		200	nF
$V_{(PSN)}$	AC coupling capacitor required for TX pins			100	mV
$t_{(VCC_RAMP)}$	V_{CC} supply ramp requirement	0.2		40	ms
$R_{(pullup\text{-}down)}$	Pull-up/down resistor to control CNF pins			2.2	kΩ

6.4 Thermal Information

THERMAL METRIC[(1)]		TUSB542 X2QFN (RWQ) 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics, Power Supply Currents

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
ICC(ACTIVE)	Average active current; link in U0 with SuperSpeed data transmission; OS = 0.9 V; DE = 0 dB		100	130	mA
ICC(U2/U3)	Average current in U2/U3		1.3		mA
ICC(NC)	Average current with no connection No SuperSpeed device is connected to TXP/TXN		0.3		mA

6.6 Electrical Characteristics, DC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRI-STATE CMOS INPUTS (CNFG_A1, CNFG_B1, CNFG_A2 and CNFG_B2)						
V_{IH}	High-level input voltage		V_{CC} x 0.75			V
V_{IM}	Mid-level input voltage			V_{CC} / 2		V
V_{IL}	Mid-level input voltage				V_{CC} x 0.25	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
$R_{(PU)}$	Internal pull-up resistance			105		kΩ
$R_{(PD)}$	Internal pull-down resistance			105		kΩ
I_{IH}	High-level input current	V_{IN} = 1.98 V			26	µA
I_{IL}	Low-level input current	V_{IN} = GND	–26			µA
I_{lkg}	External leakage current (from application board + Application Processor pin high impedance) tolerance	V_{IN} = GND or V_{IN} = 1.98 V	–1		1	µA
CMOS INPUT – SEL						
V_{IH}	High-level input voltage		V_{CC} x 0.7			V
V_{IL}	Mid-level input voltage				V_{CC} x 0.3	V
I_{IH}	High-level input current	V_{IN} = 1.98 V			5	µA
I_{IL}	Low-level input current	V_{IN} = GND	–16			µA

6.7 Electrical Characteristics, Dynamic

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Receiver						
$V_{(RX-DC-CM)}$	RX DC common mode voltage		0		2	V
$R_{(RX-CM-DC)}$	Receiver DC common mode impedance	Measured at connector. Present when SuperSpeed USB device detected on TX pins.	18		30	Ω
$R_{(RX-DIFF-DC)}$	Receiver DC differential impedance	Measured at connector. Present when SuperSpeed USB device detected on TX pins.	72		120	Ω
$Z_{(RX-HIGH-IMP-DC-POS)}$	DC input CM input impedance when termination is disabled.	Measured at connector. Present when no SuperSpeed USB device detected on TX pins or while V_{CC} is ramping.	25			KΩ
$V_{(RX-LFPS-DET-DIFF-P-P)}$	LFPS Detect threshold. Below min is noise.	Measured at connector. Below min is squelched.	0.1		0.3	V
$V_{(RX-CM-AC-P)}$	Peak RX AC common mode voltage	Measured at package pin.			150	mV
$C_{(RX-PARASITIC)}$	Rx Input capacitance for return loss	At package pin to AC GND.			1.1	pF
Differential Transmitter						
$V_{(TX-DIFF-PP)}$	Differential peak-to-peak TX voltage swing	OS Low, 0 dB DE		0.9		V
		OS High, 0 dB DE		1.1		V
$V_{(TX-DIFF-PP-LFPS)}$	LFPS differential voltage swing	OS Low, High	0.8		1.2	V
$V_{(TX-DE-RATIO)}$	Transmitter de-emphasis	Low		0		dB
		Mid		3.5		dB
		High		6		dB
$V_{(TX-RCV-DETECT)}$	The amount of voltage change allowed during Receiver Detection.				0.6	V
$V_{(TX-DC-CM)}$	TX DC common mode voltage	The instantaneous allowed DC common-mode voltage at connector side of AC coupling capacitor.	0		2	V
$V_{(TX-IDLE-DIFF-AC-PP)}$	AC Electrical Idle differential peak-to-peak output voltage	At package pin.	0		10	mV
$V_{(TX-IDLE-DIFF_DC)}$	DC Electrical Idle differential output voltage	At package pin. After low pass filter to remove AC component.	0		10	nV
$V_{(TX-CM-DC-ACTIVE-IDLE-DELTA)}$	Absolute DC common mode voltage between U1 and U0.	At package pin.			0.2	V
$I_{(TX-SHORT)}$	TX short-circuit current limit				60	mA
$R_{(TX-DC)}$	TX DC common mode impedance	At package pins	18		30	Ω
$R_{(TX-DIFF-DC)}$	TX DC differential impedance		72		120	Ω
$C_{(TX-PARASTIC)}$	TX input capacitance for return loss	At package pins to AC GND			1.25	pF
$T_{(jitter)}$	Total Residual Jitter (peak to peak)			12		ps

6.8 Electrical Characteristics, AC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Xtalk	Differential Cross talk between TX and RX Signal Pairs	at 2.5 Ghz, TX to RX		–45		dB

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6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{IDLEEntry}$	Delay from U0 to electrical idle.	See Figure 2		6		ns
$t_{IDLEExit_U1}$	U1 exit time: break in electrical idle to the transmission of LFPS	See Figure 2		6		ns
$t_{IDLEExit_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	From the time when the far end terminations detected for both ports		1		µs
$t_{IDLEExit_DISC}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	From the time when the far end terminations detected for both ports		2		µs
$t_{DIFF-DLY}$	Differential propagation delay.	See Figure 1		225		ps
$t_{PWRUPACTIVE}$	Time when V_{CC} reach 80% to device active				30	ms

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TX-RISE-FALL}$	Transmitter rise/fall time (see Figure 3)	20% to 80% of differential output. At device pins.		80		ps
$t_{RF-MISMATCH}$	Transmitter rise/fall mismatch	20% to 80% of differential output. At device pins			2.3	ps

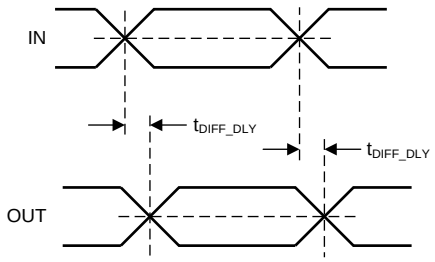


Figure 1. Propagation Delay Timing

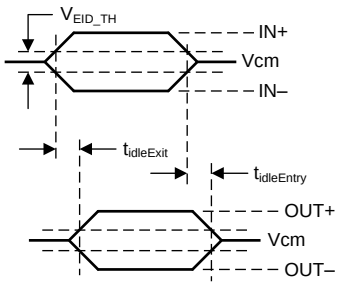


Figure 2. Electrical Idle Mode Exit and Entry Delay Timing

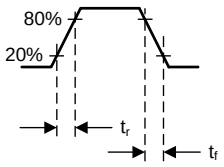
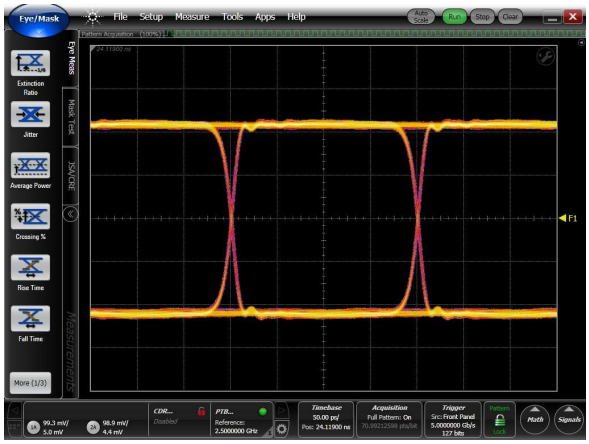


Figure 3. Output Rise and Fall Times

6.11 Typical Characteristics

6.11.1 1-Inch Pre Channel



880 mV 5 Gbps

Figure 4. Input Signal: 1-Inch Input Trace

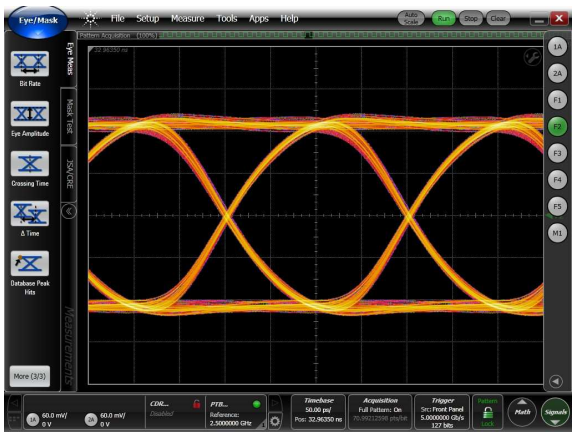


Figure 5. Output Signal: 12-Inches Output Trace

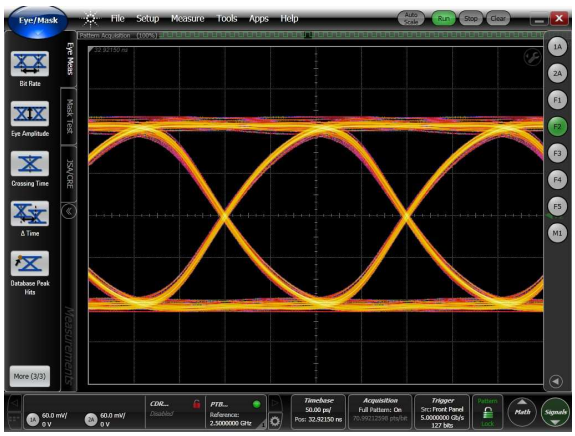


Figure 6. Output Signal: 16-Inches Output Trace

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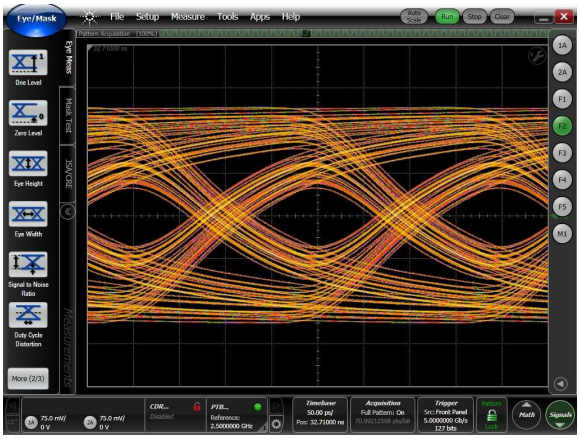
6.11.2 24-Inch Pre Channel



880 mV 5 Gbps

Figure 7. Input Signal: 24-Inch Input Trace

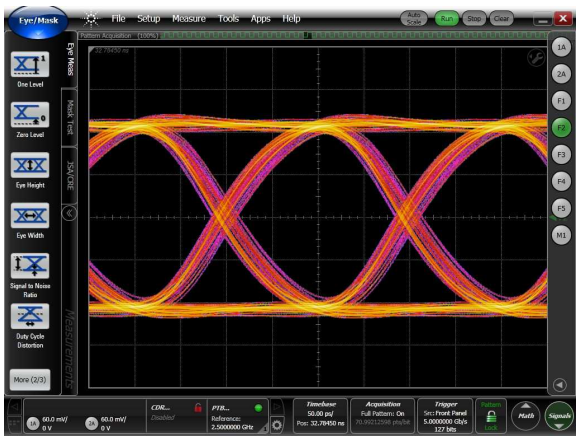


Figure 8. Output Signal: 12-Inches Output Trace

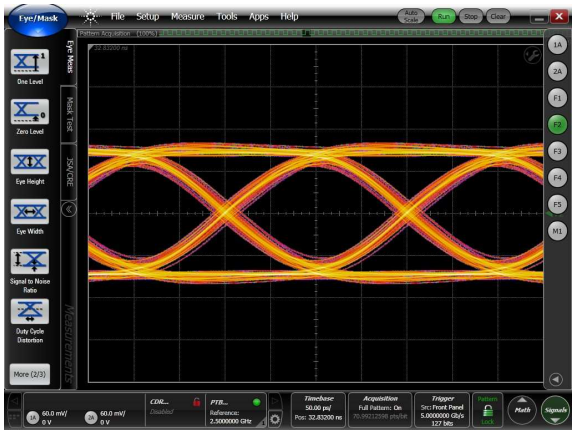
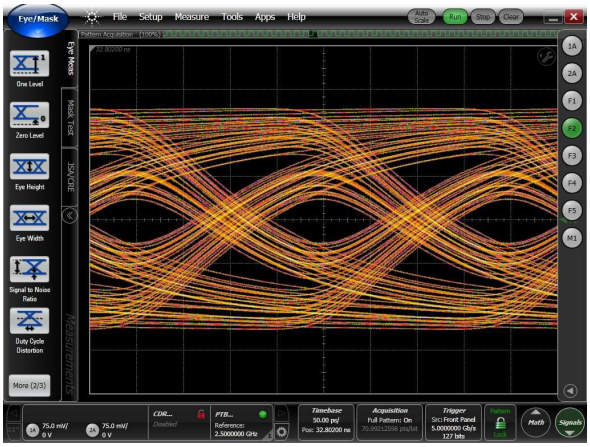


Figure 9. Output Signal: 24-Inches Output Trace

6.11.3 32-Inch Pre Channel



880 mV 5 Gbps

Figure 10. Input Signal: 32-Inch Input Trace

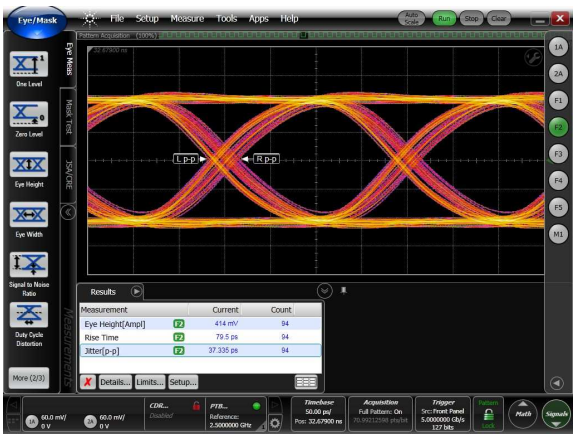


Figure 11. Output Signal: 12-Inches Output Trace

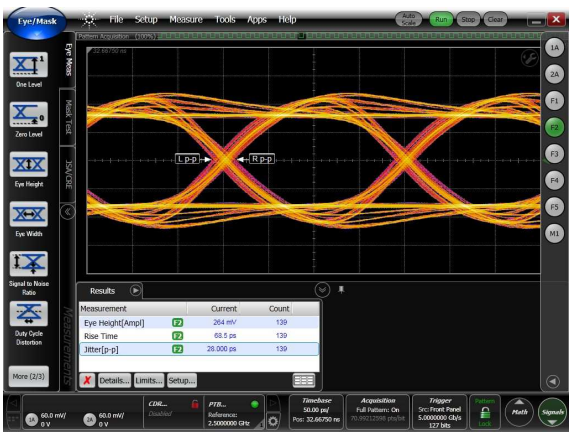


Figure 12. Output Signal: 24-Inches Output Trace

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7 Detailed Description

7.1 Overview

TUSB542 is an active redriver USB Type-C Mux that provides signal conditioning and switching according to plug orientation. The device is a dual channel USB 3.1 Gen1 (5 Gbps) redriver supporting systems with USB Type-C connectors. The TUSB542 can be controlled through the SEL pin by an external Configuration Channel Logic Controller to properly mux the signals.

When 5 Gbps Super Speed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The TUSB542 recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.1 compliance.

The TUSB542 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB542 periodically performs receiver detection on the TX pair. If it detects a SS USB receiver, the RX termination is enabled, and the TUSB542 is ready to re-drive.

The TUSB542 operates over the industrial temperature range of -40ºC to 85ºC in the 2 mm x 2.4 mm X2QFN package. The device ultra-low power architecture operates at a 1.8-V power supply. The automatic LFPS De-Emphasis control further enables the system to be USB 3.0 compliant. An advanced state machine inside the device monitors the USB SS traffic to perform enhanced power management to operate in no-connect, U2, U3 and active modes.

The USB Type-C connector is designed to allow insertion either upside-up or downside-up. The TUSB542 supports this feature by routing the AP signals to one of two output channels. The SEL input control defines the way that the AP side signals is routed on the redriver device side. Table 1 lists the active MUX configurations based on the SEL input.

Table 1. USB SS MUX Control

SEL	Tx_Con_1	Rx_Con_1	Tx_Con_2	Rx_Con_2
H	TX_AP	RX_AP	GND	GND (1)
L	GND	GND (1)	TX_AP	RX_AP

(1) Terminated through 50 K (minimum) resistors

The TUSB542 has flexible configurations to optimize the device using GPIO control pins. Figure 13 shows a typical signal chain for mobile applications. Channel 1 is between Application Processor (AP) and TUSB542, Channel 2 is between the TUSB542 redriver and the downstream device. The CNFG_A1 and CNFG_B1 pins provide signal integrity configuration settings for channel 1, while CNFG_A2 and CNFG_B2 pins control the operation of Channel 2. as depicted in Table 2.

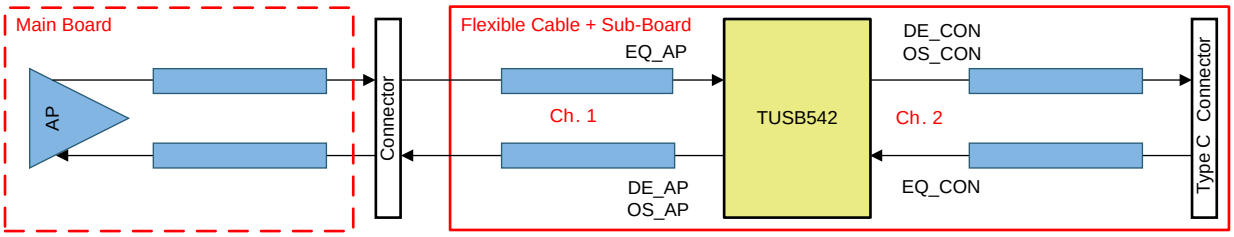


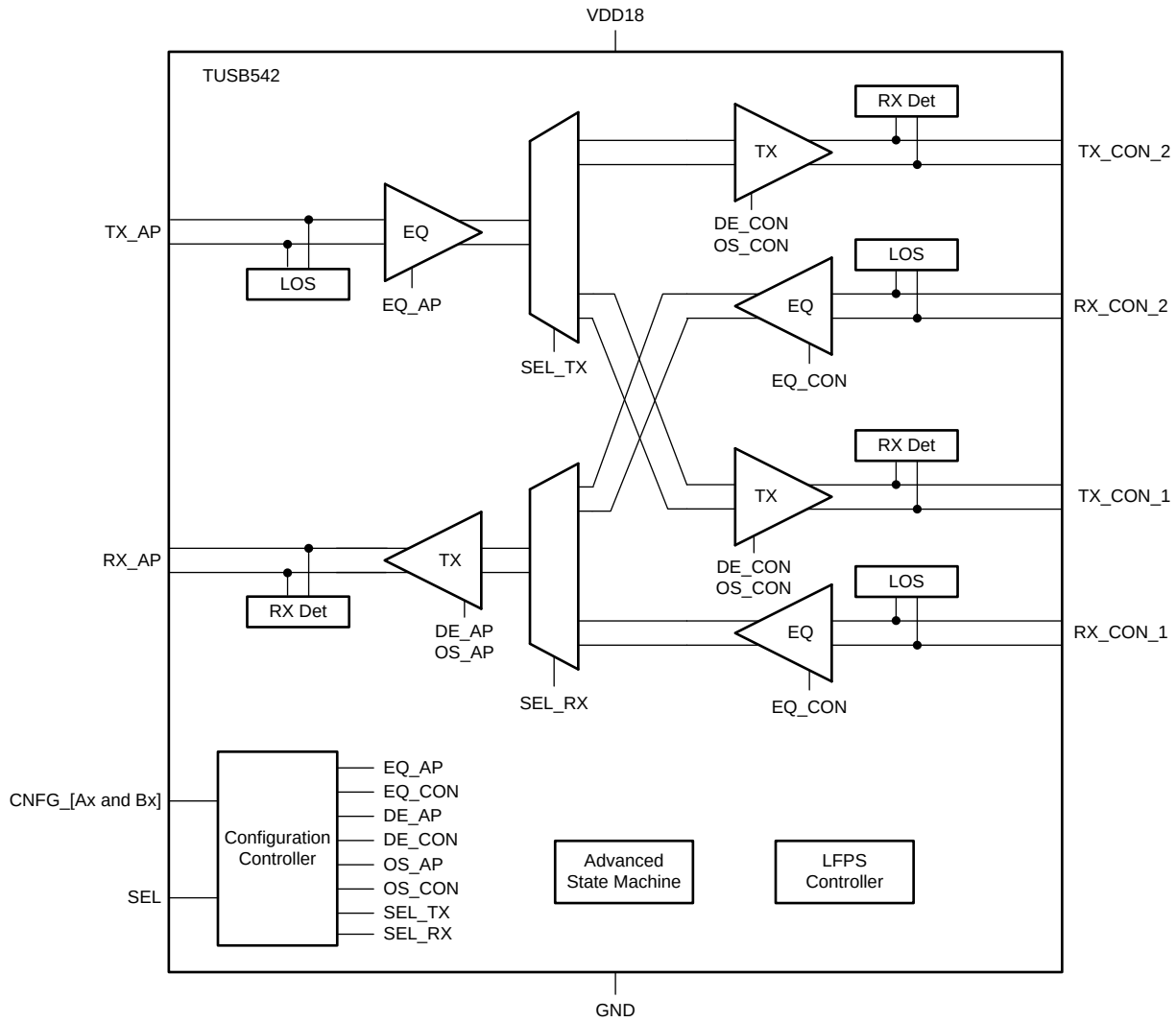
Figure 13. Typical Channels

The receiver (RX) of the device provides the flexibility of 0, 3, 6 and 9 dB of equalization, while the transmitter (TX) provides the options of 0, 3.5 or 6 dB De-Emphasis. The transmitter also supports output swing settings of 900 mV and 1.1 V.

Table 2. Device Signal Conditioning Configuration Settings for TUSB542

Ch1 (AP-Redriver)		DE_AP (dB)	OS_AP (V)	EQ_AP (dB)	Ch2 (Redriver-Conn)		DE_Conn (dB)	OS_Conn (V)	EQ_Conn (dB)
CNFG_A1	CNFG_B1				CNFG_A2	CNFG_B2			
Low	Low	3.5	1.1	3	Low	Low	6	1.1	0
	Float	3.5	0.9	3		Float	3.5	1.1	0
	High	0	1.1	3		High	3.5	0.9	0
Float	Low	0	0.9	3	Float	Low	6	0.9	0
	Float	3.5	1.1	0		Float	3.5	1.1	6
	High	.35	0.9	0		High	3.5	0.9	6
High	Low	0	1.1	0	High	Low	6	1.1	6
	Float	0	0.9	0		Float	6	0.9	6
	High	6	1.1	6		High	6	1.1	9

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Receiver Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB542 receiver. The receiver overcomes these losses by providing gain to the high frequency components of the signals with respect to the low frequency components. The proper gain setting should be selected to match the channel insertion loss before the receiver input of the TUSB542.

7.3.2 De-Emphasis Control and Output Swing

The output differential drivers of the TUSB542 provide selectable De-Emphasis and output swing in order to achieve USB3.1 compliance, these options are configurable by means of 3-state control pins, and its available settings are listed on the Table 2. The level of de-emphasis required in the system depends on the channel length after the output of the re-driver. Figure 14 shows transmit bits with De-Emphasis.

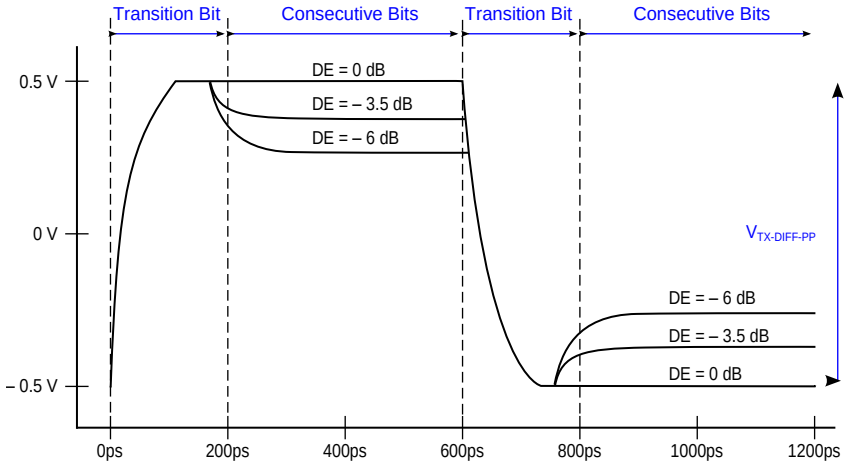

Figure 14. Transmitter Differential Voltage in Presence of De-Emphasis

7.3.3 Automatic LFPS Detection

The TUSB542 features an intelligent low frequency periodic signaling (LFPS) controller. The controller senses the low frequency signals and automatically disables the driver de-emphasis, for full USB3.1 compliance.

7.3.4 Automatic Power Management

The TUSB542 deploys RX detect, LFPS signal detection and signal monitoring to implement an automatic power management scheme to provide active, U2/U3 and disconnect modes. The automatic power management is driven by an advanced state machine, which is implemented to manage the device such that the re-driver operates smoothly in the links.

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7.4 Device Functional Modes

7.4.1 Disconnect Mode

The Disconnect mode is the lowest power state of the TUSB542. In this state, the TUSB542 periodically checks for far-end receiver termination on both TX. Upon detection of the far-end receiver's termination on both ports, the TUSB542 will transition to U0 mode.

7.4.2 U Modes

7.4.2.1 U0 Mode

The U0 mode is the highest power state of the TUSB542. Anytime super-speed traffic is being received, the TUSB542 remains in this mode.

7.4.2.2 U2/U3 Mode

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB542 periodically performs far-end receiver detection.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TUSB542 is a USB 3.1 G1 5 Gbps super speed 1:2 or 2:1 redriver de-multiplexer/multiplexer for RX and TX differential pairs. The device is host/device side agnostic and can be used for host or device switching.

8.2 Typical Applications, USB Type-C Port SS MUX

TUSB542 is optimized for USB Type-C port. The device provide multiplexing to select appropriate super speed RX and TX signal pairs resulting from Type-C plug orientation flipping. A companion USB PD or CC controller provides the MUX selection. The device can be used part of UFP, DFP or DRP Type-C port. Figure 7 illustrates typical Type-C applications.

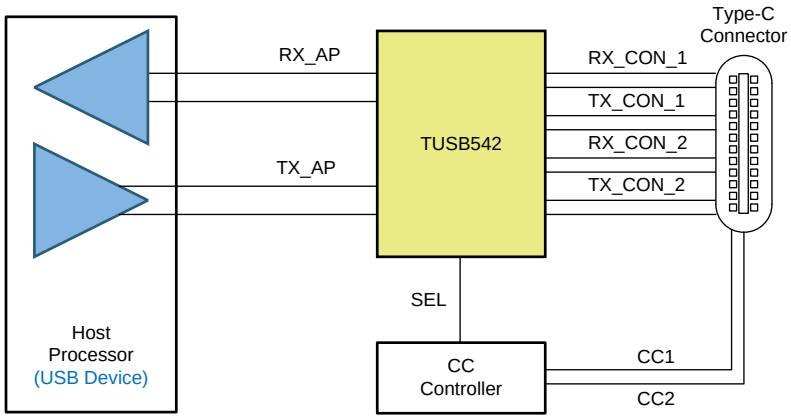

Figure 15. USB Type-C Host (Device) Application

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE	COMMENT
VDD18	1.8 V	
AC Coupling Capacitors for SS signals	100 nF	75-200nF range allowed. TUSB542 biases both input and output common mode voltage, hence ac-coupling caps as required on both sides. Note: TX pairs need to be biased at the connector.
Pull-up/down resistor to control CNF pins	4.7 kΩ	

8.2.2 Detailed Design Procedure

Figure 16 shows an example implementation of a USB Type-C DRP port using TUSB542. Texas Instruments TUSB322 is shown here as channel configuration (CC) controller. Note connections for CNFG pins of TUSB542 is example only. The connection of the CNFG pins is application dependent; refer to theTable 2, where the user can find the available settings.

It is recommended to run an overall system signal integrity analysis, in order to estimate the channel loss and configure the re-driver. It is also recommended to have pull-up and pull-down option on the configuration pins for debug and testing purposes.

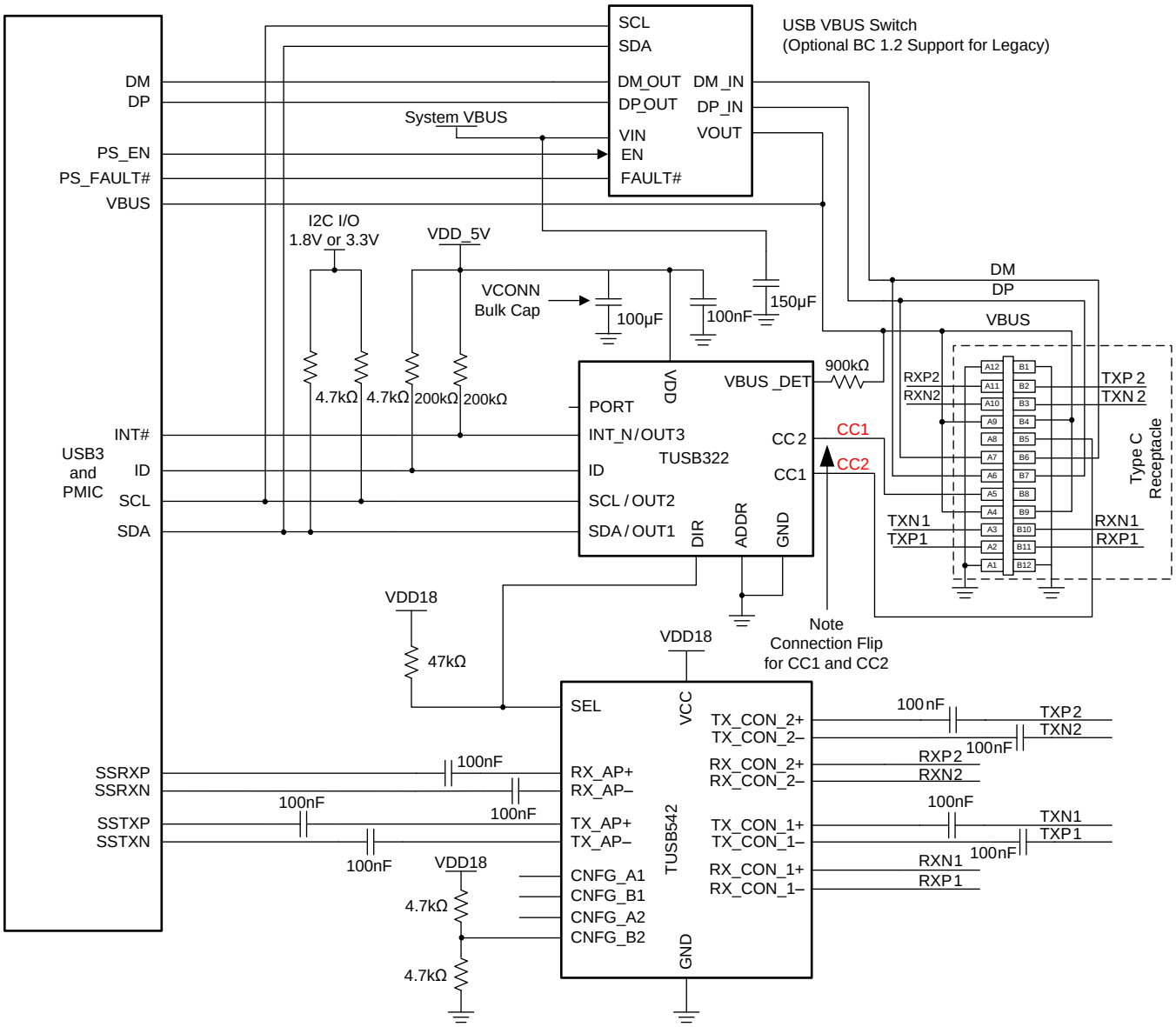

Figure 16. USB-C DRP Implementation Using TUSB542 and TUSB322/TUSB321

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8.2.3 Application Curves

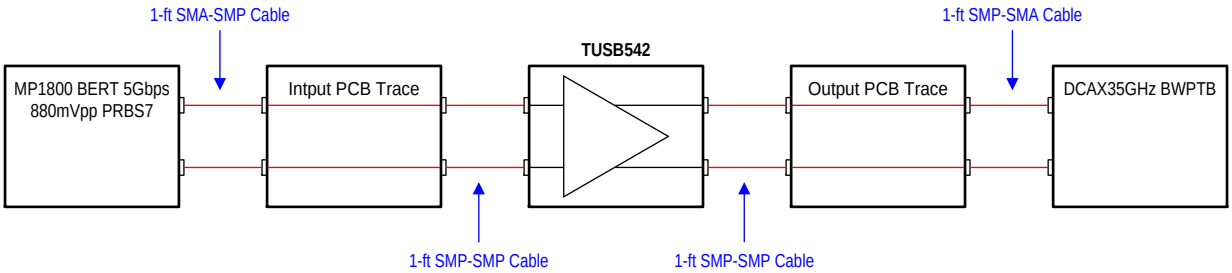

Figure 17. Measurement Setup

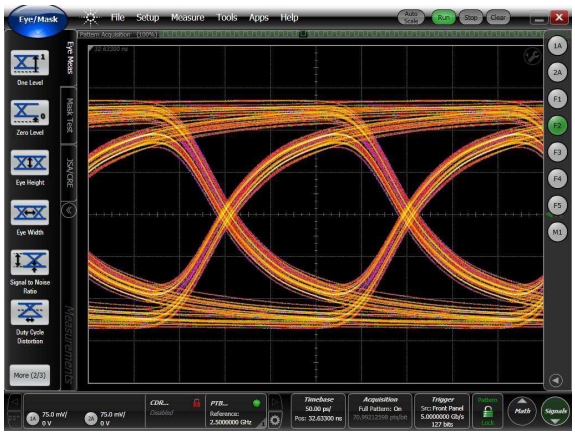

Figure 18. Input Signal: 12 Inch Input Trace (Eye Diagram at the Re-driver input)

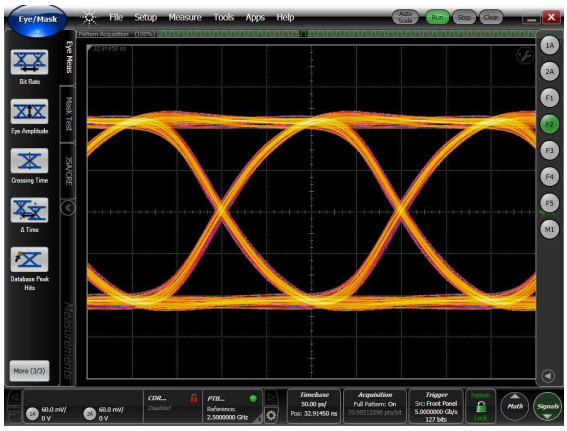

Figure 19. Output Signal: 12 Inch Output Trace (Eye Diagram at the DCAX)

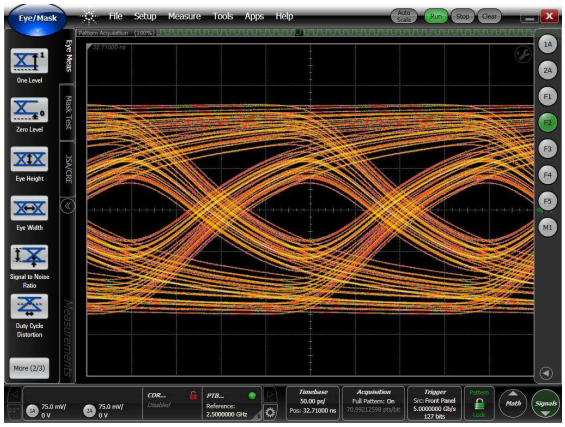

Figure 20. Input Signal: 24 Inch Input Trace (Eye Diagram at the Re-driver input)

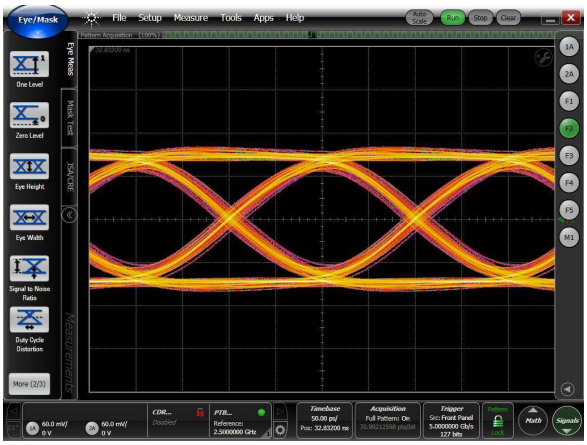

Figure 21. Output Signal: 24 Inch Output Trace (Eye Diagram at the DCAX)

8.2.4 Typical Application: Switching USB SS Host or Device Ports

TUSB542, being USB SS mux/demux, can be used for host or device switching. Figure 8 illustrates how the device can be used:

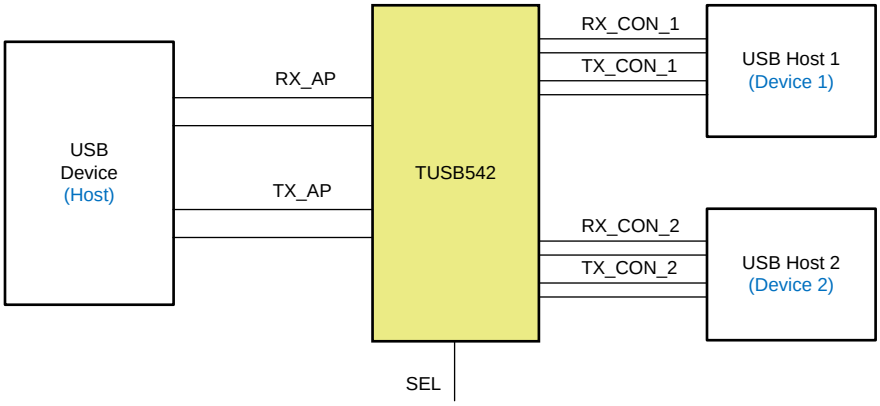

Figure 22. Muxing Two Host (Device) Port

8.2.4.1 Design Requirements

For this design example, use the design requirements shown in *Design Requirements*.

8.2.4.2 Detailed Design Procedure

For this design example, use the detailed design procedure shown in *Detailed Design Procedure*.

8.2.4.3 Application Curves

For this design example, use the application curves shown in *Application Curves*.

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9 Power Supply Recommendations

TUSB542 has internal power on reset circuit to provide clean reset for state machine provided supply ramp and level recommendations are met.

10 Layout

10.1 Layout Guidelines

- RXP/N and TXP/N pairs should be routed with controlled 90-Ohm differential impedance (±15%).
- Keep away from other high speed signals.
- Intra-pair routing should be kept to within 2 mils.
- Length matching should be near the location of mismatch.
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity, and therefore; negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

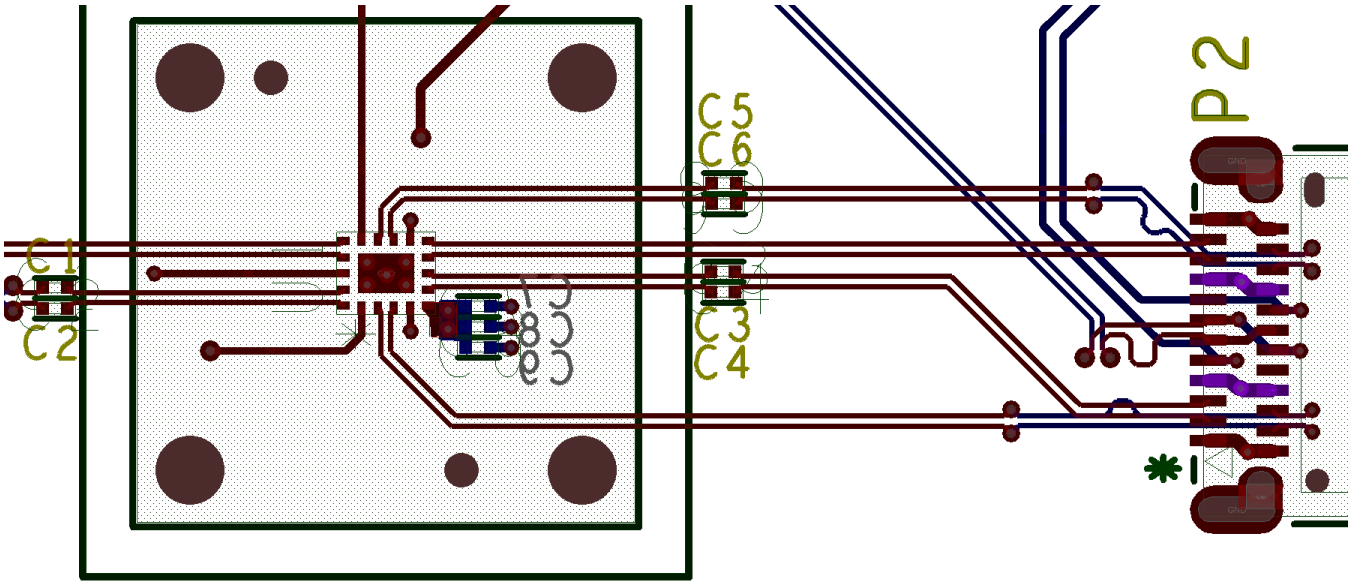

Figure 23. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB542RWQR	PREVIEW	X2QFN	RWQ	18	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	54	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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