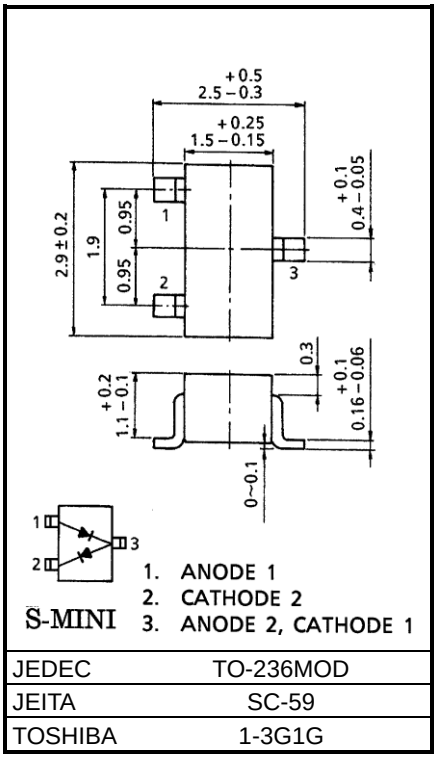
TOSHIBA Diode Silicon Epitaxial Planar Diode

1SS398

High-Voltage, High-Speed Switching Applications

Unit: mm



JEDEC	TO-236MOD
JEITA	SC-59
TOSHIBA	1-3G1G

Weight: 0.012 g (typ.)

- Small package : SC-59
- Low forward voltage : V_F = 1.0 V (typ.) @ I_F = 100 mA
- Fast reverse recovery time : t_{rr} = 0.5 μs (typ.)
- Small total capacitance : C_T = 2.5 pF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	V_{RM}	420	V
Reverse voltage	V_R	400	V
Maximum (peak) forward current	I_{FM}	300 *	mA
Average forward current	I_O	100 *	mA
Surge current (10ms)	I_{FSM}	2 *	A
Power dissipation	P	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

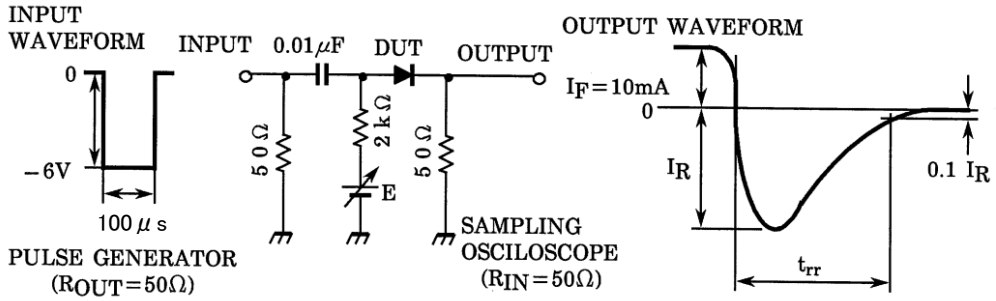
*: Unit rating. Total rating = unit rating × 0.7

Electrical Characteristics (Ta = 25°C)

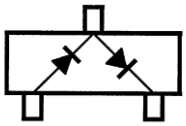
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_{F\ (1)}$	I_F = 10 mA	—	0.8	—	V
	$V_{F\ (2)}$	I_F = 100 mA	—	1.0	1.3	
Reverse current	$I_{R\ (1)}$	V_R = 300 V	—	—	0.05	μA
	$I_{R\ (2)}$	V_R = 400 V	—	—	0.1	
Total capacitance	C_T	V_R = 0 V, f = 1 MHz	—	2.5	5.0	pF
Reverse recovery time	t_{rr}	I_F = 10 mA (Fig.1)	—	0.5	—	μs

Start of commercial production
1995-10

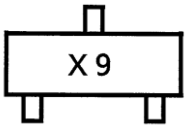
Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit



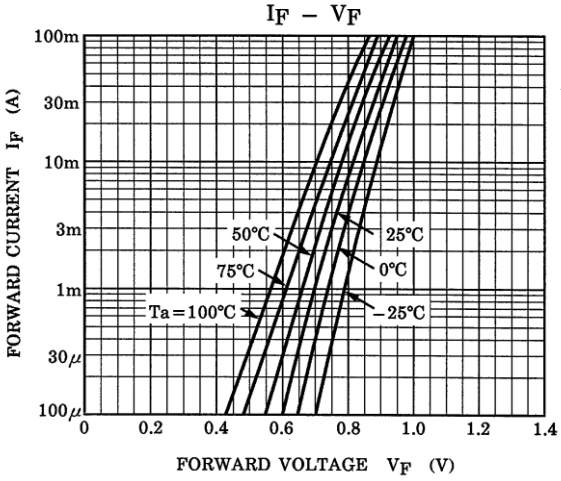
Equivalent Circuit (Top View)



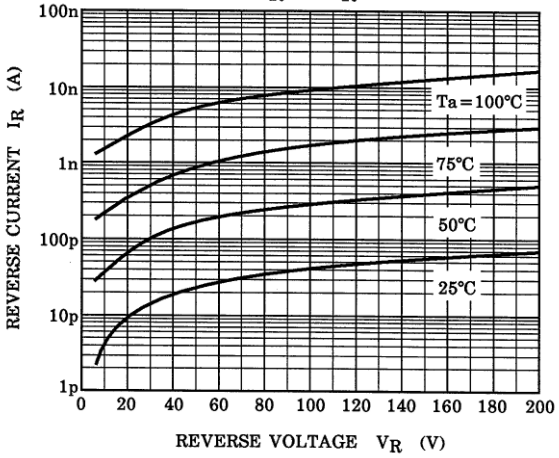
Marking



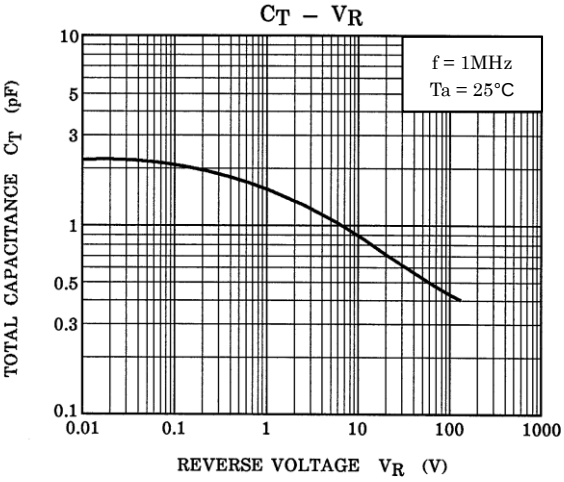
$I_F - V_F$



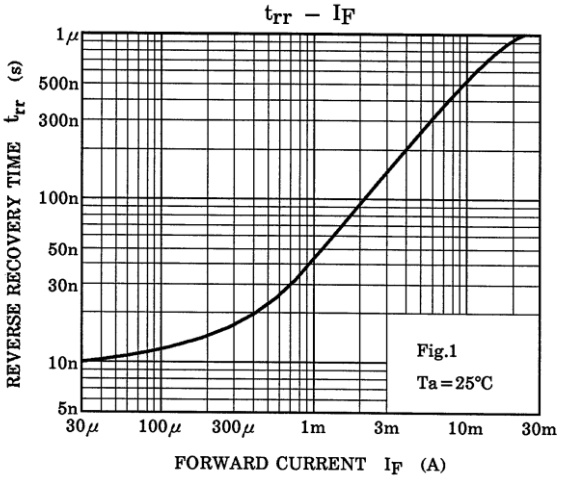
$I_R - V_R$



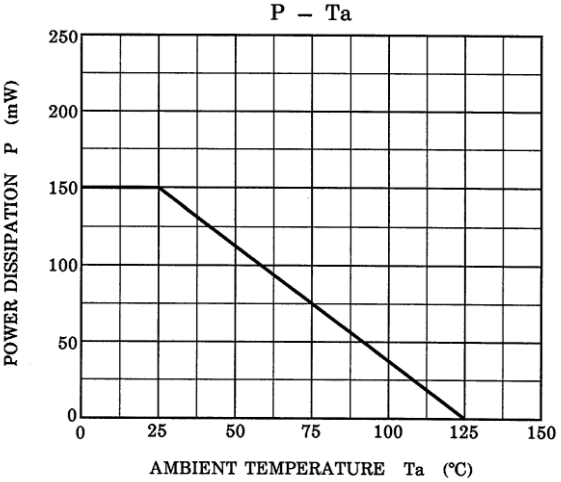
$C_T - V_R$



$t_{rr} - I_F$



P – Ta



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