HCMOS Oscillator

Platinum Series CAM

- *TTL Compatible (3.3v)*
- *2 Packaging Styles*
- *Ultra Low Jitter*
- *Low Phase Noise*
- *Immediate Delivery*

Part Numbering Example: CAM C 7 L Z - A5 B6 - XXX.XXXX TS

CAM	C	7	L	Z	A5	B6	XXX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	PACKAGING OPTIONS	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CAM	C=HCMOS	1 = Full Size 4 = Half Size 5 = 5 X 3.2 Ceramic 7 = 5 X 7 Ceramic	L = 3.3 V S = 2.5 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.000~200.000 MHz	TS = Tri-State

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.000		200.000	MHz
Available Stability Options:	-100 -50 -25		100 50 25	ppm ppm ppm
Supply Voltage Options:				
(1–133 MHz) (1–200 MHz)	2.25 3.0	2.5 3.3	2.75 3.6	V V
Operating Temperature Range Options:	0 -20 -40		+70 +70 +85	°C °C °C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V/2.5V			±5	
Output Level:	HCMOS			
Packaging:	Tape and Reel (1K per Reel) Tube			

Operating Conditions:

	Description	Min	Max	Unit
Vdd	Supply Voltage	2.25	3.6	V
Vdd	Rise Time	100		µS
HCMOS	Max Capacitive Load on outputs for CMOS levels Frequency: < 40 MHz Frequency: 40–200 MHz		 30 15	 pF pF

Cardinal Components, Inc., 155 Rt. 46 W, Wayne, NJ. 07470 TEL: (973)785-1333 FAX: (973)785-0053
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Electrical Characteristics

Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1): V_{IL}, Low–Level Input Voltage TO DISABLE OUTPUT	 3.0–3.6V Vdd			 0.2Vdd	 V
V_{IH}, High–Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT	3.0–3.6V Vdd	0.7Vdd			V
I_{IL}, Input Low Current I_{IH}, Input High Current	V_{IN} = 0V V_{IN} =Vdd			80 10	µA µA
Output Characteristics: V_{OL}, Low–Level Output Voltage	3.0V–3.6V Vdd, 8 mA I_{OL}			0.4	V
V_{OHCMOS}, High-level HCMOS Voltage	 2.25V–3.6V Vdd, -8 mA I_{OL}	 Vdd-0.4			V V
Power Supply Current: (unloaded)	2.25–3.6 Vdd, Output Freq ≤ 200 MHz			35	mA
Input Pull-Up Resistor:	2.25–3.6V Vdd, V_{IN} = 0.7V	50	70	90	KΩ
Tri-State Leakage Current:	3.6V Vdd		20		µA
Output Enable Mode:	Output is Tri-Stated				

Output Clock Switching Characteristics

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle: HCMOS @ Vdd/2	2.25 V – 3.6V Vdd	45		55	%
Output Clock Rise/Fall:	0.2–0.8Vdd, 2.25–3.6 Vdd, C_L = 30 0.2–0.8Vdd, 2.25–3.6 Vdd, C_L = 15			4.0 2.4	nS nS
Start Up Time:	From power on		3	10	mS
RMS Period Jitter:			10		pS
RMS Integrated Jitter:	12kHz to 20MHz		15		pS
Phase Noise:	@ 10kHz			-100	dBc/Hz

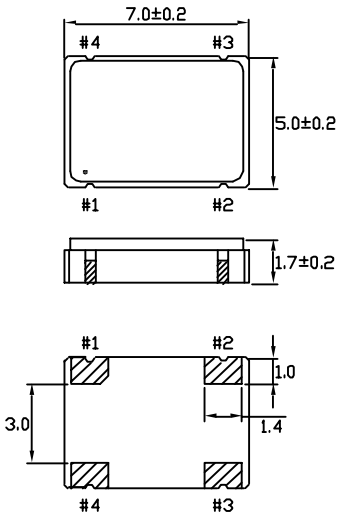
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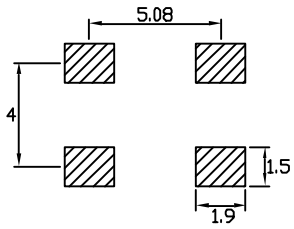
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Style 7 5x7 Ceramic SMD

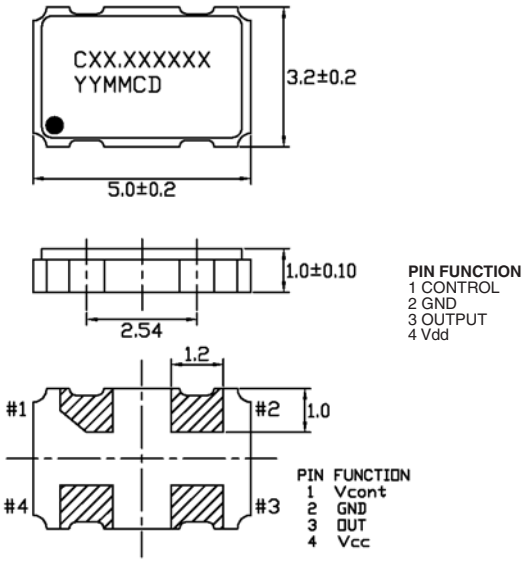


PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Recommended Solder Pad Layout



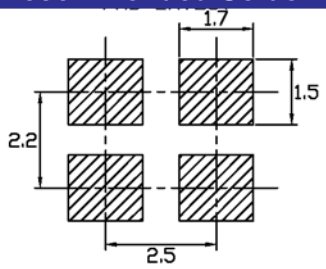
Style 5 5x3.2 Ceramic SMD



PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

PIN FUNCTION
1 Vcont
2 GND
3 OUT
4 Vcc

Recommended Solder Pad Layout



Note: *Bypass Vdd to GND with a 0.01µF capacitor*

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