

DM74ALS373

Octal D-Type TRI-STATE® Transparent Latch

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance

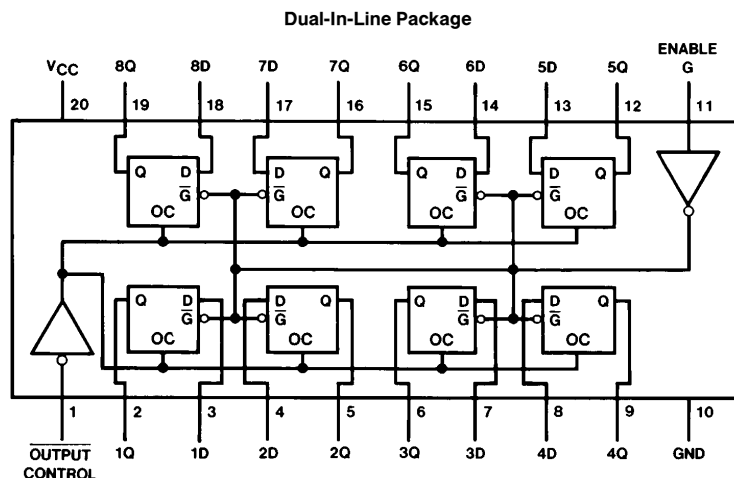
state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram



TL/F/6220-1

Order Number DM74ALS373WM, DM74ALS373N or DM74ALS373SJ
See NS Package Number M20B, M20D or N20A

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Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	57.0°C/W
M Package	76.0°C/W

Note: This product meets application requirements of 500 temperature cycles from −65°C to +150°C.

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.5	5	5.5	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			−2.6	mA
I _{OL}	Low Level Output Current			24	mA
t _W	Width of Enable Pulse, High or Low	10			ns
t _{SU}	Data Setup Time	10 ↓			ns
t _H	Data Hold Time	7 ↓			ns
T _A	Free Air Operating Temperature	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V _{IK}	Input Clamp Voltage	V _{CC} = 4.5V, I _I = −18 mA				−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = 4.5V	I _{OH} = −2.6 mA	2.4	3.3		V
		V _{CC} = 4.5V to 5.5V I _{OH} = −400 μA		V _{CC} − 2			V
V _{OL}	Low Level Output Voltage	V _{CC} = 4.5V	I _{OL} = 24 mA		0.35	0.5	V
I _I	Input Current at Max Input Voltage	V _{CC} = 5.5V, V _{IH} = 7V				0.1	mA
I _{IH}	High Level Input Current	V _{CC} = 5.5V, V _{IH} = 2.7V				20	μA
I _{IL}	Low Level Input Current	V _{CC} = 5.5V, V _{IL} = 0.4V				−0.1	mA
I _O	Output Drive Current	V _{CC} = 5.5V	V _O = 2.25V	−30		−112	mA
I _{OZH}	Off-State Output Current High Level Voltage Applied	V _{CC} = 5.5V V _O = 2.7V				20	μA
I _{OZL}	Off-State Output Current Low Level Voltage Applied	V _{CC} = 5.5V V _O = 0.4V				−20	μA
I _{CC}	Supply Current	V _{CC} = 5.5V Outputs Open	Outputs High		9	16	mA
			Outputs Low		16	25	mA
			Outputs Disabled		17	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\Omega$ $C_L = 50$ pF	Data	Any Q	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	4	16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	7	23	ns
t_{pZH}	Output Enable Time to High Level Output		Output Control	Any Q	6	18	ns
t_{pZL}	Output Enable Time to Low Level Output		Output Control	Any Q	5	20	ns
t_{pHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	10	ns
t_{pLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	12	ns

Note 1: See Section 5 for test waveforms and output load.

Function Table

Output Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram

The logic diagram illustrates the internal structure of the TL/F/6220-2 device, which consists of eight D-type flip-flops arranged in a vertical column. Each flip-flop has a D input, a $\bar{G}$ (clock) input, and a $\bar{Q}$ output. The inputs and outputs are numbered as follows:

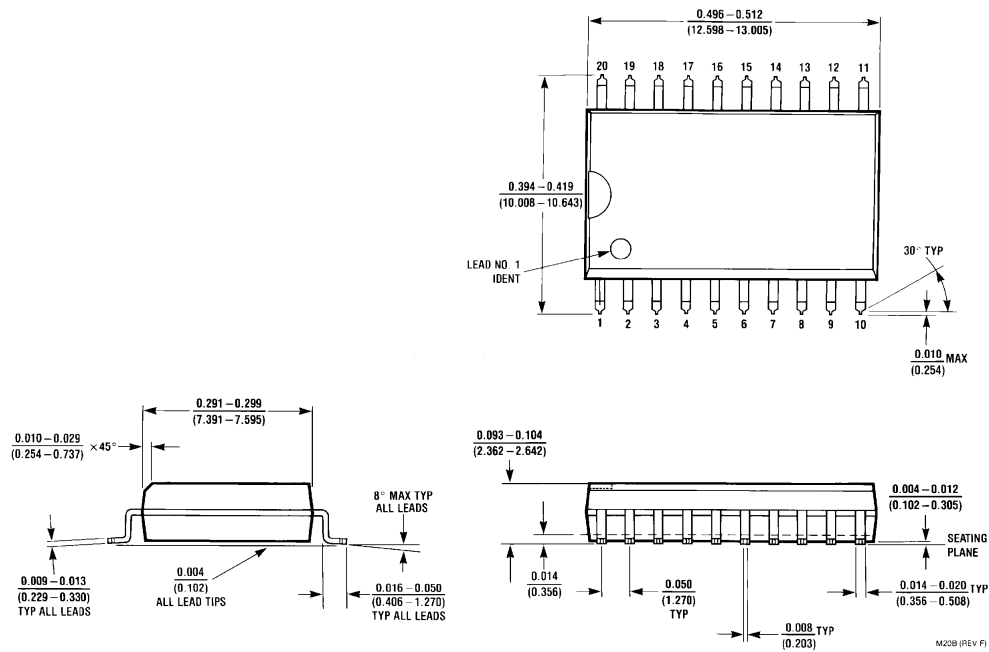
- Inputs:**
 - 1: OUTPUT CONTROL (connected to the $\bar{Q}$ output of the first flip-flop and the D input of the eighth flip-flop).
 - 3: D input of the first flip-flop.
 - 4: D input of the second flip-flop.
 - 7: D input of the third flip-flop.
 - 8: D input of the fourth flip-flop.
 - 13: D input of the fifth flip-flop.
 - 14: D input of the sixth flip-flop.
 - 17: D input of the seventh flip-flop.
 - 18: D input of the eighth flip-flop.
 - 11: ENABLE G (connected to the $\bar{G}$ input of the eighth flip-flop).
- Outputs:**
 - 2: $\bar{Q}$ output of the first flip-flop.
 - 5: $\bar{Q}$ output of the second flip-flop.
 - 6: $\bar{Q}$ output of the third flip-flop.
 - 9: $\bar{Q}$ output of the fourth flip-flop.
 - 12: $\bar{Q}$ output of the fifth flip-flop.
 - 15: $\bar{Q}$ output of the sixth flip-flop.
 - 16: $\bar{Q}$ output of the seventh flip-flop.
 - 19: $\bar{Q}$ output of the eighth flip-flop.

The diagram shows that the $\bar{Q}$ output of each flip-flop is inverted to produce the final output. The ENABLE G input is active-low, as indicated by the bubble on the input symbol.

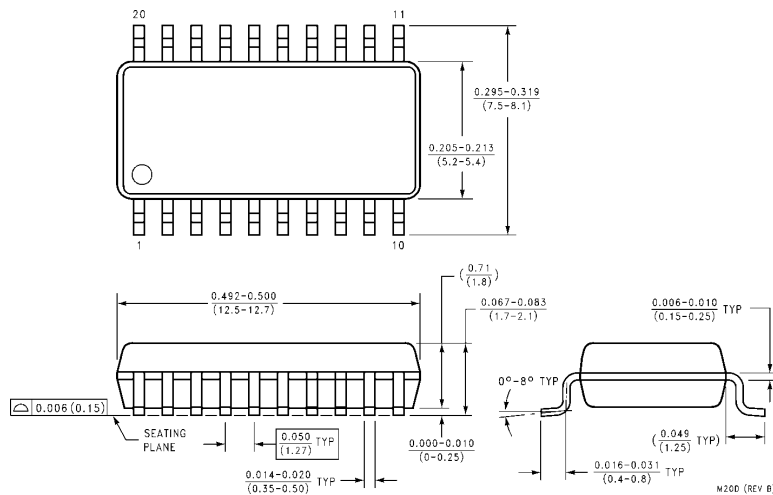
TL/F/6220-2



Physical Dimensions inches (millimeters)

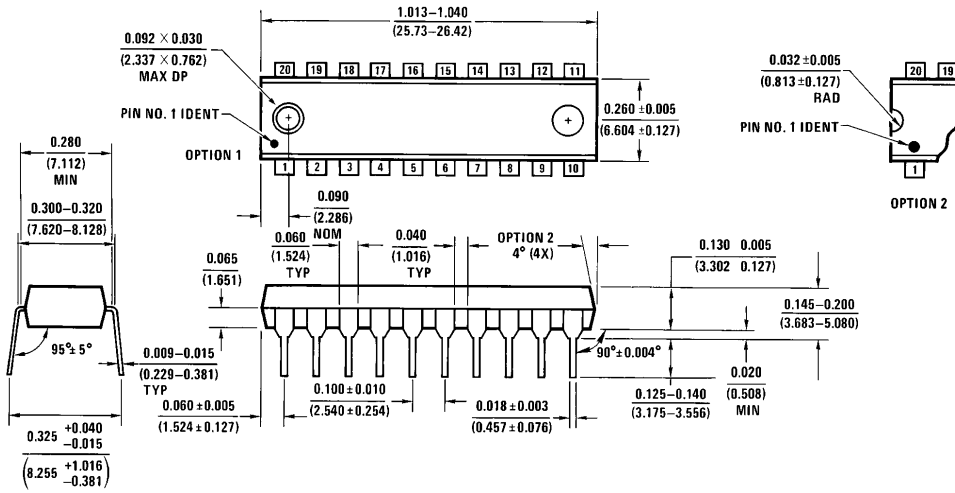


S.O. Package (M)
Order Number DM74ALS373WM
NS Package Number M20B



Small Outline Package (SJ)
Order Number DM74ALS373SJ
NS Package Number M20D

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number DM74ALS373N
NS Package Number N20A

N20A (REV G)

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