TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET DESYNCHRONIZER

OCTOBER 2003 *REV. P1.0.1*

GENERAL DESCRIPTION

The XRT75R12D is a twelve channel fully integrated Line Interface Unit (LIU) featuring EXAR's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers, Transmitters and Jitter Attenuators in a single 420 Lead TBGA package.

Each channel of the XRT75R12D can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R12D's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75R12D incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also, the jitter attenuators can be used for clock smoothing in SONET STS-1 to DS-3 de-mapping.

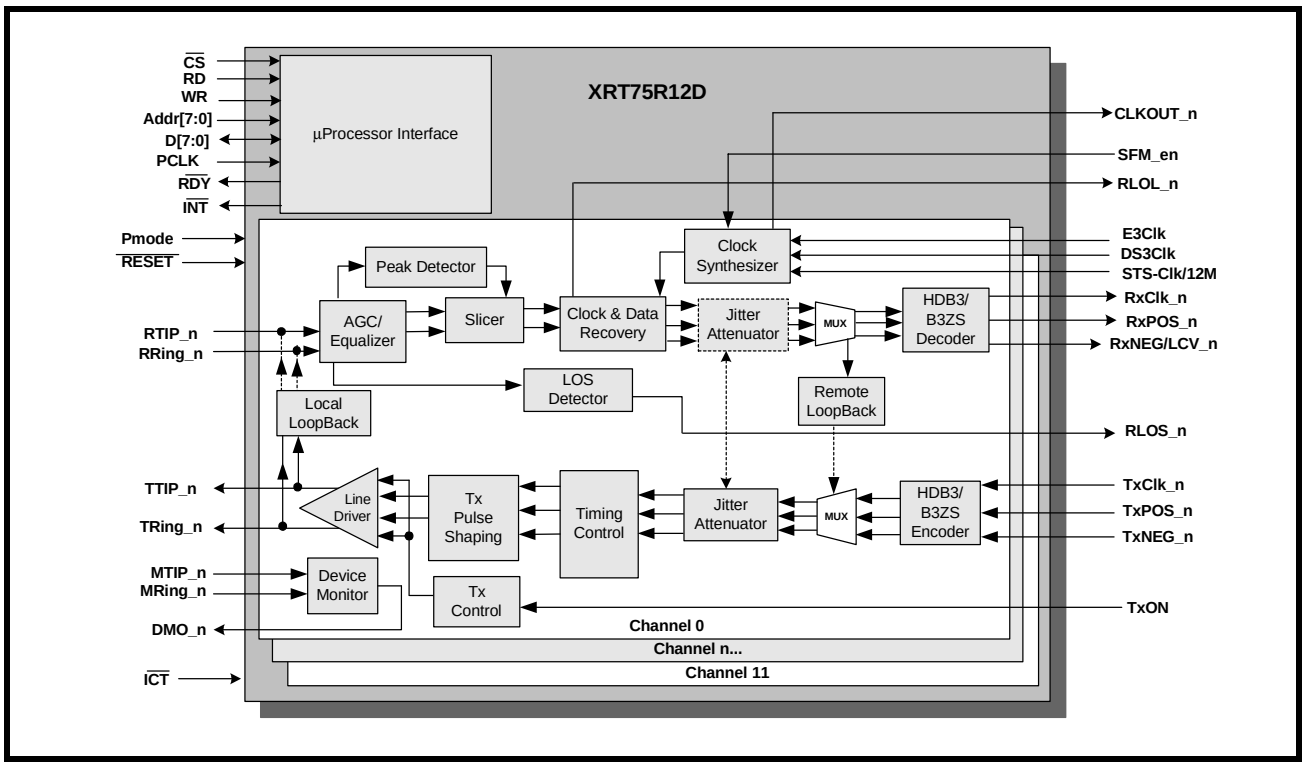
The XRT75R12D provides a Parallel Microprocessor Interface for programming and control.

The XRT75R12D supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R12D



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R12DIB	420 Lead TBGA	-40°C to +85°C

FEATURES

RECEIVER

- R^3 Technology (Reconfigurable, Relayless Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- R^3 Technology (Reconfigurable, Relayless Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be turned on or off
- Transmitters provide Current Output Drive

JITTER ATTENUATOR

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive, Transmit path, or disabled
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 420 pin TBGA Thermally enhanced Package
- - 40°C to 85°C Industrial Temperature Range

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

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PIN DESCRIPTIONS (BY FUNCTION)

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
P4	TxON	I	**Transmit On/Off Input** Upon power up, the transmitters are powered on. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 12 transmitters are powered off. ***NOTE:*** *TxON is ideal for redundancy applications. See the R³ Technology section of this datasheet for more details. Internally pulled "High".*
F22 AA22 H22 Y23 G26 AA25 G1 AA2 H5 Y4 F5 AA5	TxCLK0 TxCLK1 TxCLK2 TxCLK3 TxCLK4 TxCLK5 TxCLK6 TxCLK7 TxCLK8 TxCLK9 TxCLK10 TxCLK11	I	**Transmit Clock Input** These input pins have three functions: • They function as the timing source for the Transmit Section of the corresponding channel within the XRT75R12D. • They are used by the Transmit Section of the LIU IC to sample the corresponding TxPOS_n and TxNEG_n input pins. • They are used to clock the PRBS generator ***NOTE:*** *The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20 ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E or better applications).*
E23 AB24 J22 AA23 G25 AA26 G2 AA1 J5 AA4 E4 AB3	TxPOS0 TxPOS1 TxPOS2 TxPOS3 TxPOS4 TxPOS5 TxPOS6 TxPOS7 TxPOS8 TxPOS9 TxPOS10 TxPOS11	I	**Transmit Positive Data Input** The function of these digitial input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Single Rail Mode - Transmit Data Input** Operating in the Single-Rail Mode; all transmit input data will be serially applied to this input pin. This signal will be latched into the Transmit Section circuitry on the active edge of the TxCLK_n signal. The Transmit Section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). **Dual Rail Mode - Transmit Positive Data Input** In the Dual-Rail Mode, the user should apply a pulse to this input pin when a positive-polarity pulse is to be transmitted onto the line. This signal will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal,. The Transmit Section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, B3ZS/HDB3 encoding must have already been done prior to this input.

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
C25 AB25 H23 W23 H24 Y26 H3 Y1 H4 W4 C2 AB2	TxNEG0 TxNEG1 TxNEG2 TxNEG3 TxNEG4 TxNEG5 TxNEG6 TxNEG7 TxNEG8 TxNEG9 TxNEG10 TxNEG11	I	**Transmit Negative Data Input** When a Channel has been configured to operate in the Dual-Rail Mode, the user should apply a pulse to this input pin anytime the Transmit Section of the LIU IC to generate a negative-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal. ***NOTE:*** *In the Single-Rail Mode, this input pin has no function, and should be tied to GND.*
B24 AE24 C20 AD20 C16 AD16 C11 AD11 C7 AD7 C3 AD3	TTip0 TTip1 TTip2 TTip3 TTip4 TTip5 TTip6 TTip7 TTip8 TTip9 TTip10 TTip11	O	**Transmit TTIP Output - Positive Polarity Signal** These output pins along with the corresponding TRING_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel of the XRT75R12D. Connect this signal and the corresponding TRING_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a high ervoltage than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TRING_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".*
C24 AD24 B20 AE20 B16 AE16 B11 AE11 B7 AE7 B3 AE3	TRing0 TRing1 TRing2 TRing3 TRing4 TRing5 TRing6 TRing7 TRing8 TRing9 TRing10 TRing11	O	**Transmit Ring Output - Negative Polarity Signal** These output pins along with the corresponding TTIP_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, within the XRT75R12D. Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TTIP_n output pin. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a higher voltage than its corresponding TTIP_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
C23 AD23 D19 AC19 D15 AC15 E11 AB11 E8 AB8 C4 AD4	MTip0 MTip1 MTip2 MTip3 MTip4 MTip5 MTip6 MTip7 MTip8 MTip9 MTip10 MTip11	I	**Monitor Tip Input - Positive Polarity Signal** These input pins along with MRing_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. (1) To monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this pin MUST be connected to the corresponding TTIP_n output pin via a 270Ω series resistor. Similarly, the MRING_n input pin MUST also be connected to its corresponding TRING_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTE:*** *These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.*
D23 AC23 E19 AB19 E16 AB16 D10 AC10 D8 AC8 D4 AC4	MRing0 MRing1 MRing2 MRing3 MRing4 MRing5 MRing6 MRing7 MRing8 MRing9 MRing10 MRing11	I	**Monitor Ring Input** These input pins along with MTIP_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. (1) To monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this input pin MUST be connected to the corresponding TRING_n output pin via a 270Ω series resistor. Similarly, the MTIP_n input pin MUST be connected to its corresponding TTIP_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" to indicate a possible fault condition in the Transmit Output Line signal path. ***NOTE:*** *These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.*
N3 N4 N5 N1 M1 L2 M2 M3 M4 M5 K2 J1	DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7 DMO8 DMO9 DMO10 DMO11	O	**Drive Monitor Output** These output signals are used to indicate a fault condition within the Transmit Output signal path. This output pin will toggle "High" anytime the Transmit Drive Monitor circuitry either, via the corresponding MTIP and MRING input pins or internally, detects no bipolar pulses via the Transmit Output line signal (e.g., via the TTIP_m and TRING_m output pins) for 128 bit-periods. This output pin will be driven "Low" anytime the Transmit Drive Monitor circuitry has detected at least one bipolar pulse via the Transmit Output line signal within the last 128 bit periods.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
D25 AD25 G23 AA24 J24 U24 J3 U3 G4 AA3 D2 AD2	RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7 RLOS8 RLOS9 RLOS10 RLOS11	O	**Receive Loss of Signal Output Indicator** This output pin indicates Loss of Signal (LOS) Defect condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding Channel is currently declaring the LOS defect condition.
G22 AB26 K22 U22 L24 W25 L3 W2 K5 U5 G5 AB1	RLOL0 RLOL1 RLOL2 RLOL3 RLOL4 RLOL5 RLOL6 RLOL7 RLOL8 RLOL9 RLOL10 RLOL11	O	**Receive Loss of Lock Output Indicator** This output pin indicates Loss of Lock (LOL) condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding Channel is currently declaring the LOL condition. ***NOTE:*** *The Receive Section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the reference clock programmed for that channel by 0.5% or more.*
E25 AD26 G24 Y24 L22 T22 L5 T5 G3 Y3 E2 AD1	RxPOS0 RxPOS1 RxPOS2 RxPOS3 RxPOS4 RxPOS5 RxPOS6 RxPOS7 RxPOS8 RxPOS9 RxPOS10 RxPOS11	O	**Receive Positive Data Output** The function of these output pins depends upon whether the channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Dual-Rail Mode - Receive Positive Polarity Data Output** If the channel has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this pin. The negative-polarity data will be output via the corresponding RxNEG_n pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP/RRING input pins. The data output via this pin is updated upon the active edge of RxCLK_n output clock signal. **Single-Rail Mode - Receive Data Output** In the Single-Rail Mode, all Receive (or Recovered) data will be output via this pin. The data output via this pin is updated upon the active edge of the RCLK_n output clock signal.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
F23 AC26 F24 U23 L23 T24 L4 T3 F3 U4 F4 AC1	RxNEG/LCV0 RxNEG/LCV1 RxNEG/LCV2 RxNEG/LCV3 RxNEG/LCV4 RxNEG/LCV5 RxNEG/LCV6 RxNEG/LCV7 RxNEG/LCV8 RxNEG/LCV9 RxNEG/LCV10 RxNEG/LCV11	O	**Receive Negative Data Output/Line Code Violation** The function of these pins depends on whether the XRT75R12D is configured in Single Rail or Dual Rail mode. **Dual-Rail Mode - Receive Negative Polarity Data Output** In the Dual-Rail Mode, all negative-polarity data will be output via this pin. The positive-polarity data will be output via the corresponding RxPOS_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RxCLK_n anytime it receives a negative-polarity pulse via the RTIP/RRING input pins. The data output via this pin is updated upon the active edge of the RCLK_n output clock signal. **Single-Rail Mode - Line Code Violation Indicator Output** In the Single-Rail Mode, this output pin will function as the Line Code Violation indicator output. In this configuration, the Receive Section of the Channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event). The data that is output via this pin is updated upon the active edge of the RCLK_n output clock signal.
E24 AC25 J23 V23 K24 T23 K3 T4 J4 V4 E3 AC2	RxCLK0 RxCLK1 RxCLK2 RxCLK3 RxCLK4 RxCLK5 RxCLK6 RxCLK7 RxCLK8 RxCLK9 RxCLK10 RxCLK11	O	**Receive Clock Output** This output pin functions as the Receive or recovered clock signal. All Receive (or recovered) data will output via the RxPOS_n and RxNEG_n outputs upon the active edge of this clock signal. Additionally, if the device/channel has been configured to operate in the Single-Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the active edge of this clock signal.

RECEIVE LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
B22 AE22 B18 AE18 A14 AF14 D13 AC13 B9 AE9 B5 AE5	RTip0 RTip1 RTip2 RTip3 RTip4 RTip5 RTip6 RTip7 RTip8 RTip9 RTip10 RTip11	I	**Receive TIP Input** These input pins along with the corresponding RRing_n input pin function as the Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12D. Cconnect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a higher voltage than its corresponding RRING_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a lower voltage than its corresponding RRING_n input pin.
C22 AD22 C18 AD18 B14 AE14 C13 AD13 C9 AD9 C5 AD5	RRing0 RRing1 RRing2 RRing3 RRing4 RRing5 RRing6 RRing7 RRing8 RRing9 RRing10 RRing11	I	**Receive Ring Input** These input pins along with the corresponding RTIP_n input pin function as the Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12D. Connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. (See Figure 6) Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a lower voltage than its corresponding RTIP_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a higher voltage than its corresponding RTIP_n input pin.

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
R5	SFM_EN	I	**Single Frequency Mode Enable** This input pin is used to configure the XRT75R12D to operate in the SFM (Single Frequency Mode). When this feature is invoked, the SFM Synthesizer will become active. By applying a 12.288MHz clock signal to the STS-1Clk/12M pin, the XRT75R12D will generate all of the appropriate clock signals (e.g., 34.368MHz, 44.736MHz or 51.84). The XRT75R12D internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding channels in the XRT75R12D. "Low" - Disables the Single Frequency Mode. In this setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. ***NOTE:*** *This input pin is internally pulled low.*
R1	E3Clk	I	**E3 Clock Input (34.368 MHz ± 20 ppm)** If any one of the channels is configured in E3 mode, a reference clock of 34.368 MHz ± 20 ppm is applied to this input pin. If the LIU is used in E3 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. ***NOTE:*** *SFM mode negates the need for this clock*
T1	DS3Clk	I	**DS3 Clock Input (44.736 MHz ± 20 ppm)** If any one of the channels is configured in DS3 mode, a reference clock of 44.736 MHz ± 20 ppm is applied to this input pin. ***NOTE:*** *SFM mode negates the need for this clock*
U1	STS-1Clk/12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm)** If any one of the channels is configured in STS-1 mode, a reference clock of 51.84MHz ± 20 ppm is applied to this input pin. If the LIU is used in STS-1 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. **Single Frequency Mode Clock (12.288MHz) Input** In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3, DS3 or STS-1).
C26 W22 K23 W24 J25 V25 J2 V2 K4 W3 C1 W5	CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6 CLKOUT7 CLKOUT8 CLKOUT9 CLKOUT10 CLKOUT11	O	**Reference clock out** A reference clock pin is provided for each channel that will supply a precise data rate frequency derived from either the Clock input pin (E3Clk, DS3Clk, or STS-1Clk) or the 12.288MHz input in SFM mode. This frequency will be as stable as the original source. It is designed to provide the attached framer with its appropriate reference clock.

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
P3	TEST	****	**Factory Test Mode Input Pin** This pin must be connected to GND for normal operation. ***NOTE:*** *This input pin is internally pulled "Low".*
AE25	TRST	I	**Test Reset** Test Boundary Scan
AB23	TMS	I	**Test Mose Select** Test Boundary Scan
AB5	TCK	I	**Test Clock** Test Boundary Scan
AB4	TDI	I	**Test Data Input** Test Boundary Scan
AE2	TDO	O	**Test Data Output** Test Boundary Scan

MICROPROCESSOR PARALLEL INTERFACE -

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
J26	Pmode	I	This pin controls the Microprocessor Parallel Interface mode. "High" sets a Synchronous clocked interface mode with a clock from the Host. "Low" sets an Asynchronous mode where a clock internal to the XRT75R12D will time the operations.
P24	PCLK	I	High speed clock supplied by the Host to provide timing in the Synchronous Interface mode. This signal must be a square-wave.
N24	$\overline{CS}$	I	**Chip select input (active low)** Initiates a read or write operation. When "High", no parallel communication is active between the LIU and the Host.
N22	$\overline{WR}$	I	**Write input (active low)** Enables the Host to write data D[7:0] into the LIU register space at address Addr[7:0].
N23	$\overline{RD}$	I	**Read input (active low)** Commands the LIU to transfer the contents of a register specified by Addr[7:0] to the Host.
N25	$\overline{RDY}$	O	**Ready line output (active low)** Provides a handshake between the LIU and the Host that communicates when an operation has been completed. *This pin must be pulled "High" with a 3kΩ ± 1% resistor.*

MICROPROCESSOR PARALLEL INTERFACE -

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
K25 M22 M23 M24 K26 L26 M26 N26	Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7	I	An eight bit direct address bus that specifies the source/destination register for a Read or Write operation.
P22 R26 T26 U26 R25 R24 R23 R22	D0 D1 D2 D3 D4 D5 D6 D7	I/O	An eight bit bi-directional data bus that provides the data into the LIU for a Write operation or the data out to the Host for a Read operation.
P26	$\overline{INT}$	O	**Interrupt active Output (active low)** Normally, this output pin will be pulled "High". However, if the user enables interrupts within the LIU, and if those conditions occur, the XRT75R12D will signal an interrupt from the Microprocessor by pulling this output pin "Low". The Host Microprocessor must ascertain the source of the interrupt and service it. Reading the source of the interupt will clear the flag and the $\overline{INT}$ pin will go back high unless another interrupt has gone active. ***NOTES:*** *1. This pin will remain "Low" until the Interrupt has been serviced.* *2. This pin must be pulled "High" with a 3kΩ ± 1% resistor.*
N2	$\overline{RESET}$	I	**RESET Input** Pulsing this input "Low" causes the XRT75R12D to reset the contents of the on-chip Command Registers to their default values. As a consequence, the XRT75R12D will then also be operating in its default condition. For normal operation this input pin should be at a logic "High". ***NOTE:*** *This input pin is internally pulled high.*

POWER SUPPLY PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RVDD0 RVDD1 RVDD2 RVDD3 RVDD4 RVDD5 RVDD6 RVDD7 RVDD8 RVDD9 RVDD10 RVDD11	D22 AC22 D18 AC18 E15 AB15 E12 AB12 A9 AF9 D5 AC5	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
TVDD0 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 TVDD8 TVDD9 TVDD10 TVDD11	B23 AE23 B19 AE19 B15 AE15 B10 AE10 A6 AF6 B4 AE4	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
AVDD	M25, T25, AB21, AB18, AF13, AF12, AB9, AB6, R4, K1, E6, E9, A12, A13, E18, E21,	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1µF capacitor.
DVDD	D26, F25, H25, P25, W26, V24, Y22, AF21, AF20, AF17, AF16, AD14, AD12, AF11, AF8, AF7, AF24, AD6, AF3, Y5, V3, W1, P5, P2, H2, F2, D1, C6, A7, A3, A8, A11, C12, C14, A16, A17, A20, A21, A24	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor.

GROUND PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RGND0 RGND1 RGND2 RGND3 RGND4 RGND5 RGND6 RGND7 RGND8 RGND9 RGND10 RGND11	A22 AF22 A18 AF18 E14 AB14 E13 AB13 D9 AC9 A5 AF5	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9 TGND10 TGND11	A23 AF23 A19 AF19 A15 AF15 A10 AF10 B6 AE6 A4 AF4	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
AGND	A1, A2, A25, A26, B1, B2, B25, B26, C8, C10, C17, C19, C21, D17, D21, E5, E22, L25, U25, AB22, AB20, AB17, AB10, AB7, R3, L1, E7, E10, B12, B13, E17, E20, T2, U2, AC17, AC21, AD8, AD10, AD15, AD17, AD19, AD21, AE1, AE26, AE12, AE13, AF1, AF2, AF25, AF26, C15	**Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND	E26, F26, H26, P23, , V26, Y25, V22, AC24, AC20, AC16, AC14, AC12, AC11, AE8, AE17, AE21, AC7, AC6, AC3, V5, Y2, V1, R2, P1, H1, F1, E1, D3, D7, B8, D6, D11, D12, D14, D16, B17, D20, B21, D24	**Digital Ground** It's recommended that all ground pins of this device be tied together.

TABLE 1: LIST BY PIN NUMBER

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A1	AGND	B6	TGND8	C13	RRing6	D20	DGND
A2	AGND	B7	TRing8	C14	DVDD	D21	AGND
A3	DVDD	B8	DGND	C15	AGND	D22	RVDD0
A4	TGND10	B9	RTip8	C16	TTip4	D23	MRing0
A5	RGND10	B10	TVDD6	C17	AGND	D24	DGND
A6	TVDD8	B11	TRing6	C18	RRing2	D25	RLOS0
A7	DVDD	B12	AGND	C19	AGND	D26	DVDD
A8	DVDD	B13	AGND	C20	TTip2	E1	DGND
A9	RVDD8	B14	RRing4	C21	AGND	E2	RxPOS10
A10	TGND6	B15	TVDD4	C22	RRing0	E3	RxCLK10
A11	DVDD	B16	TRing4	C23	MTip0	E4	TxPOS10
A12	AVDD	B17	DGND	C24	TRing0	E5	AGND
A13	AVDD	B18	RTip2	C25	TxNEG0	E6	AVDD
A14	RTip4	B19	TVDD2	C26	CLKOUT0	E7	AGND
A15	TGND4	B20	TRing2	D1	DVDD	E8	MTip8
A16	DVDD	B21	DGND	D2	RLOS10	E9	AVDD
A17	DVDD	B22	RTip0	D3	DGND	E10	AGND
A18	RGND2	B23	TVDD0	D4	MRing10	E11	MTip6
A19	TGND2	B24	TTip0	D5	RVDD10	E12	RVDD6
A20	DVDD	B25	AGND	D6	DGND	E13	RGND6
A21	DVDD	B26	AGND	D7	DGND	E14	RGND4
A22	RGND0	C1	CLKOUT10	D8	MRing8	E15	RVDD4
A23	TGND0	C2	TxNEG10	D9	RGND8	E16	MRing4
A24	DVDD	C3	TTip10	D10	MRing6	E17	AGND
A25	AGND	C4	MTip10	D11	DGND	E18	AVDD
A26	AGND	C5	RRing10	D12	DGND	E19	MRing2
B1	AGND	C6	DVDD	D13	RTip6	E20	AGND
B2	AGND	C7	TTip8	D14	DGND	E21	AVDD
B3	TRing10	C8	AGND	D15	MTip4	E22	AGND
B4	TVDD10	C9	RRing8	D16	DGND	E23	TxPOS0
B5	RTip10	C10	AGND	D17	AGND	E24	RxCLK0
		C11	TTip6	D18	RVDD2	E25	RxPOS0
		C12	DVDD	D19	MTip2	E26	DGND

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
F1	DGND	J4	RxCLK8	M23	Addr2	R26	D1
F2	DVDD	J5	TxPOS8	M24	Addr3	T1	DS3Clk
F3	RxNEG/LCV8	J22	TxPOS2	M25	AVDD	T2	AGND
F4	RxNEG/LCV10	J23	RxCLK2	M26	Addr6	T3	RxNEG/LCV7
F5	TxCLK10	J24	RLOS4	N1	DMO3	T4	RxCLK7
F22	TxCLK0	J25	CLKOUT4	N2	$\overline{\text{RESET}}$	T5	RxPOS7
F23	RxNEG/LCV0	J26	Pmode	N3	DMO0	T22	RxPOS5
F24	RxNEG/LCV2	K1	AVDD	N4	DMO1	T23	RxCLK5
F25	DVDD	K2	DMO10	N5	DMO2	T24	RxNEG/LCV5
F26	DGND	K3	RxCLK6	N22	$\overline{\text{WR}}$	T25	AVDD
G1	TxCLK6	K4	CLKOUT8	N23	$\overline{\text{RD}}$	T26	D2
G2	TxPOS6	K5	RLOL8	N24	$\overline{\text{CS}}$	U1	STS-1Clk/12M
G3	RxPOS8	K22	RLOL2	N25	$\overline{\text{RDY}}$	U2	AGND
G4	RLOS8	K23	CLKOUT2	N26	Addr7	U3	RLOS7
G5	RLOL10	K24	RxCLK4	P1	DGND	U4	RxNEG/LCV9
G22	RLOL0	K25	Addr0	P2	DVDD	U5	RLOL9
G23	RLOS2	K26	Addr4	P3	TEST	U22	RLOL3
G24	RxPOS2	L1	AGND	P4	TxON	U23	RxNEG/LCV3
G25	TxPOS4	L2	DMO5	P5	DVDD	U24	RLOS5
G26	TxCLK4	L3	RLOL6	P22	D0	U25	AGND
H1	DGND	L4	RxNEG/LCV6	P23	DGND	U26	D3
H2	DVDD	L5	RxPOS6	P24	PCLK	V1	DGND
H3	TxNEG6	L22	RxPOS4	P25	DVDD	V2	CLKOUT7
H4	TxNEG8	L23	RxNEG/LCV4	P26	$\overline{\text{INT}}$	V3	DVDD
H5	TxCLK8	L24	RLOL4	R1	E3Clk	V4	RxCLK9
H22	TxCLK2	L25	AGND	R2	DGND	V5	DGND
H23	TxNEG2	L26	Addr5	R3	AGND	V22	DGND
H24	TxNEG4	M1	DMO4	R4	AVDD	V23	RxCLK3
H25	DVDD	M2	DMO6	R5	SFM_EN	V24	DVDD
H26	DGND	M3	DMO7	R22	D7	V25	CLKOUT5
J1	DMO11	M4	DMO8	R23	D6	V26	DGND
J2	CLKOUT6	M5	DMO9	R24	D5	W1	DVDD
J3	RLOS6	M22	Addr1	R25	D4	W2	RLOL7

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
W3	CLKOUT9	AB6	AVDD	AC13	RTip7	AD20	TTip3
W4	TxNEG9	AB7	AGND	AC14	DGND	AD21	AGND
W5	CLKOUT11	AB8	MTip9	AC15	MTip5	AD22	RRing1
W22	CLKOUT1	AB9	AVDD	AC16	DGND	AD23	MTip1
W23	TxNEG3	AB10	AGND	AC17	AGND	AD24	TRing1
W24	CLKOUT3	AB11	MTip7	AC18	RVDD3	AD25	RLOS1
W25	RLOL5	AB12	RVDD7	AC19	MTip3	AD26	RxPOS1
W26	DVDD	AB13	RGND7	AC20	DGND	AE1	AGND
Y1	TxNEG7	AB14	RGND5	AC21	AGND	AE2	TDO
Y2	DGND	AB15	RVDD5	AC22	RVDD1	AE3	TRing11
Y3	RxPOS9	AB16	MRing5	AC23	MRing1	AE4	TVDD11
Y4	TxCLK9	AB17	AGND	AC24	DGND	AE5	RTip11
Y5	DVDD	AB18	AVDD	AC25	RxCLK1	AE6	TGND9
Y22	DVDD	AB19	MRing3	AC26	RxNEG/LCV1	AE7	TRing9
Y23	TxCLK3	AB20	AGND	AD1	RxPOS11	AE8	DGND
Y24	RxPOS3	AB21	AVDD	AD2	RLOS11	AE9	RTip9
Y25	DGND	AB22	AGND	AD3	TTip11	AE10	TVDD7
Y26	TxNEG5	AB23	TMS	AD4	MTip11	AE11	TRing7
AA1	TxPOS7	AB24	TxPOS1	AD5	RRing11	AE12	AGND
AA2	TxCLK7	AB25	TxNEG1	AD6	DVDD	AE13	AGND
AA3	RLOS9	AB26	RLOL1	AD7	TTip9	AE14	RRing5
AA4	TxPOS9	AC1	RxNEG/LCV11	AD8	AGND	AE15	TVDD5
AA5	TxCLK11	AC2	RxCLK11	AD9	RRing9	AE16	TRing5
AA22	TxCLK1	AC3	DGND	AD10	AGND	AE17	DGND
AA23	TxPOS3	AC4	MRing11	AD11	TTip7	AE18	RTip3
AA24	RLOS3	AC5	RVDD11	AD12	DVDD	AE19	TVDD3
AA25	TxCLK5	AC6	DGND	AD13	RRing7	AE20	TRing3
AA26	TxPOS5	AC7	DGND	AD14	DVDD	AE21	DGND
AB1	RLOL11	AC8	MRing9	AD15	AGND	AE22	RTip1
AB2	TxNEG11	AC9	RGND9	AD16	TTip5	AE23	TVDD1
AB3	TxPOS11	AC10	MRing7	AD17	AGND	AE24	TTip1
AB4	TDI	AC11	DGND	AD18	RRing3	AE25	TRST
AB5	TCK	AC12	DGND	AD19	AGND	AE26	AGND

PIN	PIN NAME
AF1	AGND
AF2	AGND
AF3	DVDD
AF4	TGND11
AF5	RGND11
AF6	TVDD9
AF7	DVDD
AF8	DVDD
AF9	RVDD9
AF10	TGND7
AF11	DVDD
AF12	AVDD
AF13	AVDD
AF14	RTip5
AF15	TGND5
AF16	DVDD
AF17	DVDD
AF18	RGND3
AF19	TGND3
AF20	DVDD
AF21	DVDD
AF22	RGND1
AF23	TGND1
AF24	DVDD
AF25	AGND
AF26	AGND

FUNCTIONAL DESCRIPTION

The XRT75R12D is a twelve channel fully integrated Line Interface Unit featuring EXAR's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers, Transmitters and Jitter Attenuators in a single 420 Lead TBGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for provding the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS). EXAR's proven expertise in providing redundany solutions has paved the way for R^3 Technology.

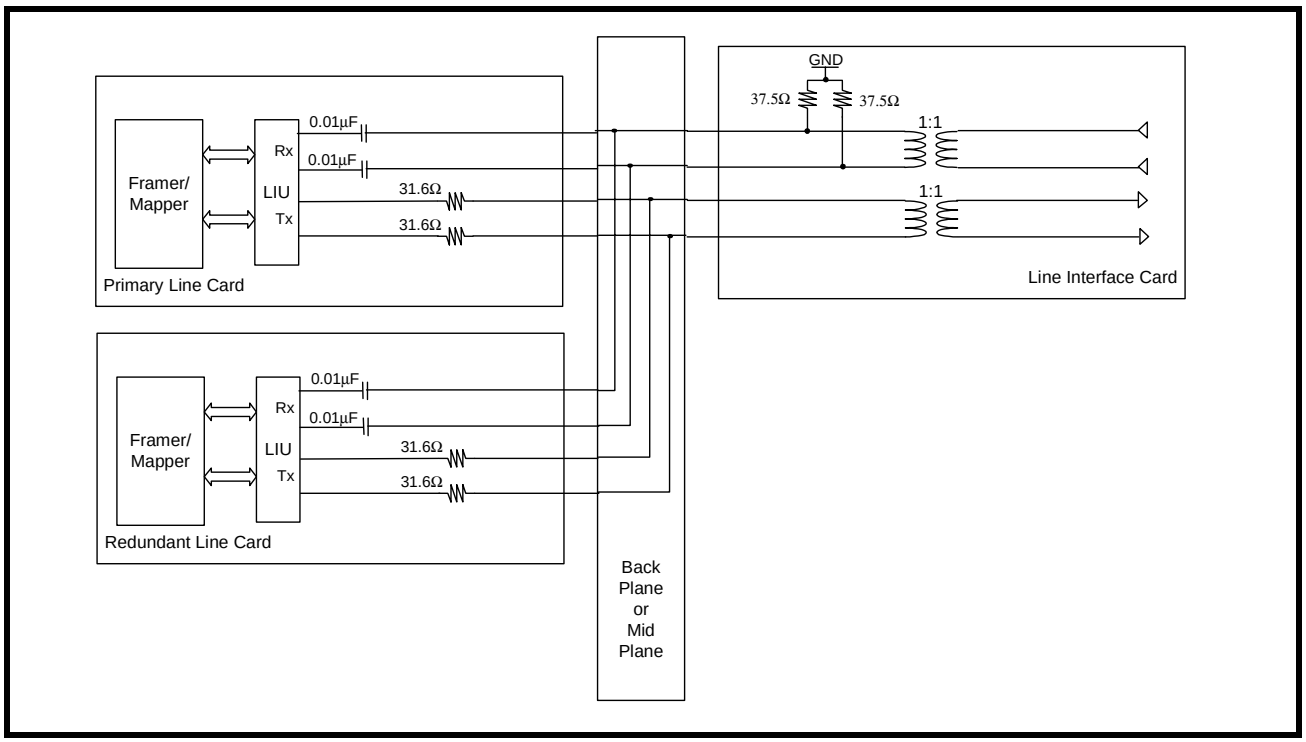
1.0 R^3 TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR's R^3 technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R^3 Technology with EXAR's world leading line interface units.

1.1 Network Architecture

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. Wtih this design, the bill of materials is reduced to the fewest amount of components. See Figure 2. for a simplified block diagram of a typical redundancy design.

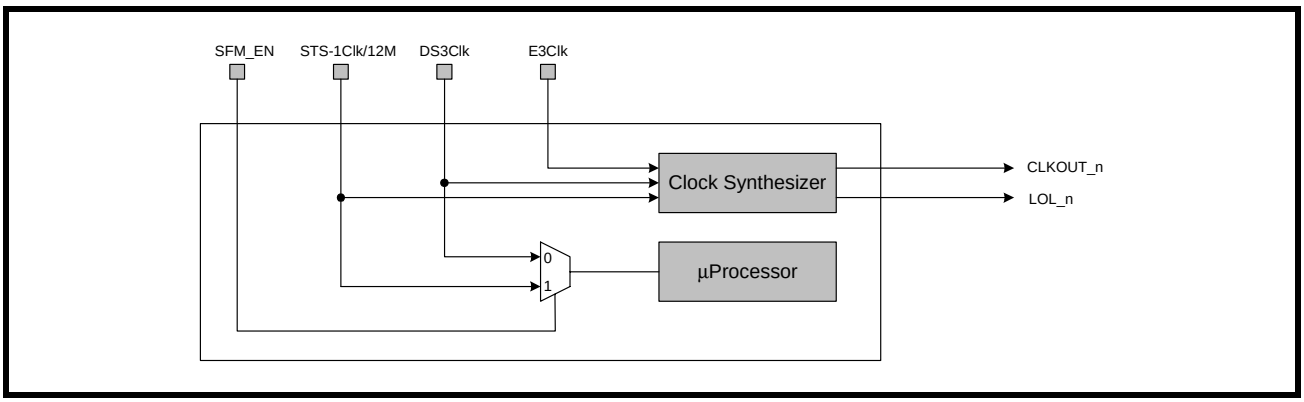
FIGURE 2. NETWORK REDUNDANCY ARCHITECTURE



2.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 3

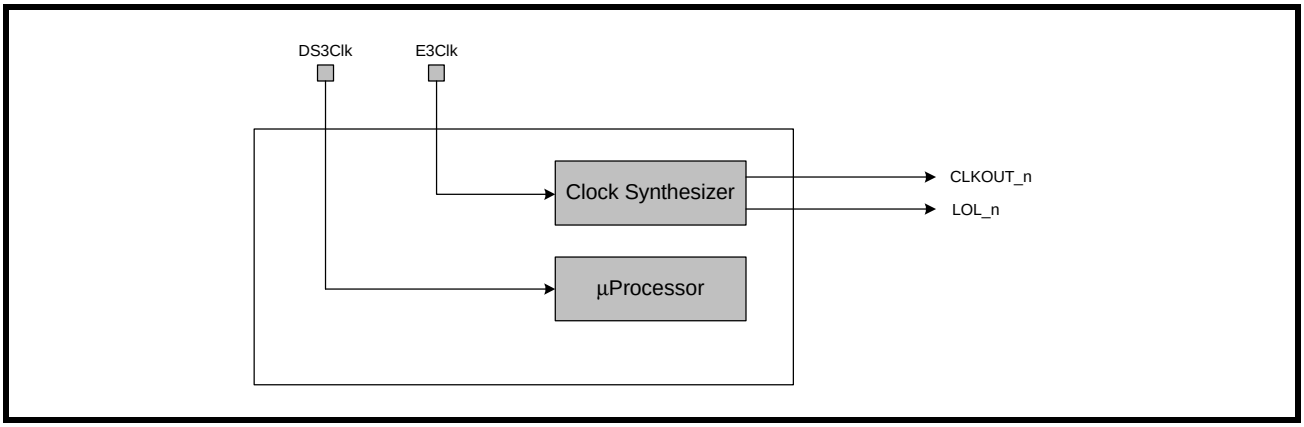
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR



2.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 4. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM

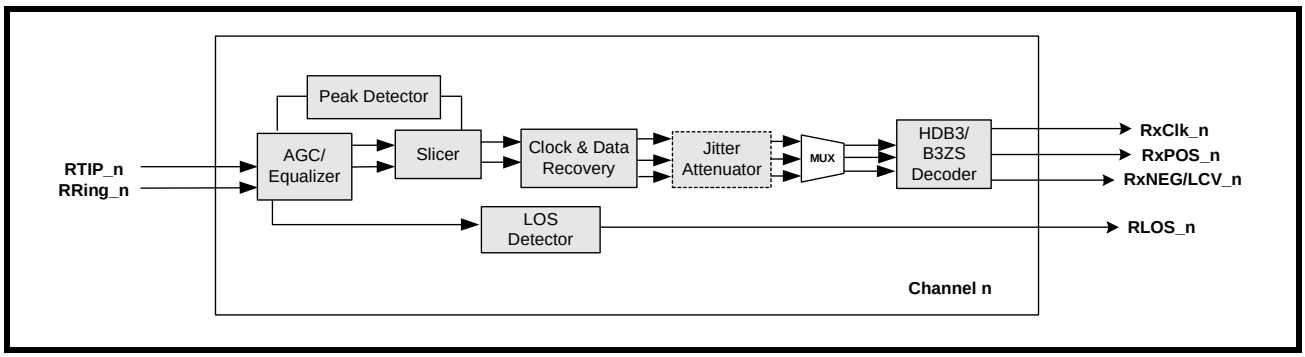


NOTE: *For one input clock reference, the single frequency mode should be used.*

3.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 5.

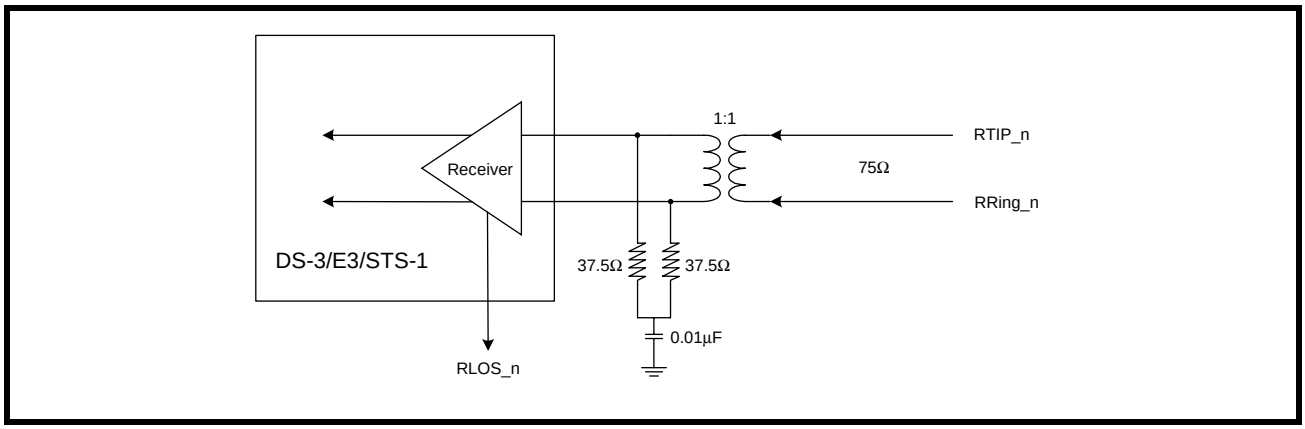
FIGURE 5. RECEIVE PATH BLOCK DIAGRAM



3.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 6.

FIGURE 6. RECEIVE LINE INTERFACECONNECTION



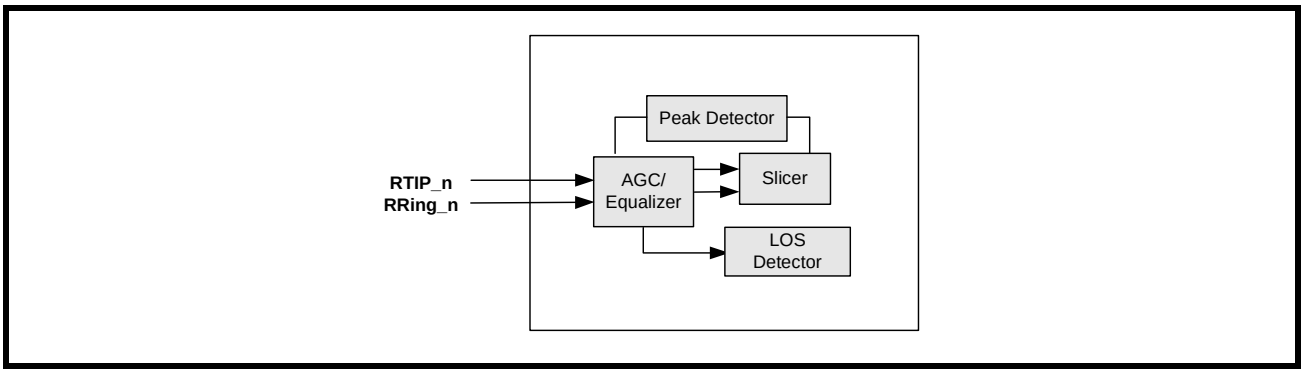
3.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

3.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 7. ACG/EQUALIZER BLCOK DIAGRAM



3.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. The equalizer gain mode can be enabled by programming the appropriate register.

NOTE: *The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.*

3.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

3.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

3.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” or setting the RLOL_n bit to “1” in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

3.5 LOS (Loss of Signal) Detector

3.5.1 DS3/STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to "1" in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 2.The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled "High" and the RLOS_n bit is set to "1" in the status control register.

TABLE 2: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS DEFECT	SIGNAL LEVEL TO CLEAR ALOS DEFECT
DS3	0	0	< 75mVpk	> 130mVpk
	1	0	< 45mVpk	> 60mVpk
	0	1	< 120mVpk	> 45mVpk
	1	1	< 55mVpk	> 180mVpk
STS-1	0	0	< 120mVpk	> 170mVpk
	1	0	< 50mVpk	> 75mVpk
	0	1	< 125mVpk	> 205mVpk
	1	1	< 55mVpk	> 90mVpk

3.5.2 Disabling ALOS/DLOS Detection

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a "1" to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

3.5.3 E3 LOS Condition:

If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35 dB below the normal. This is illustrated in Figure 8. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 9 shows the LOS declaration and clearance conditions.

FIGURE 8. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775

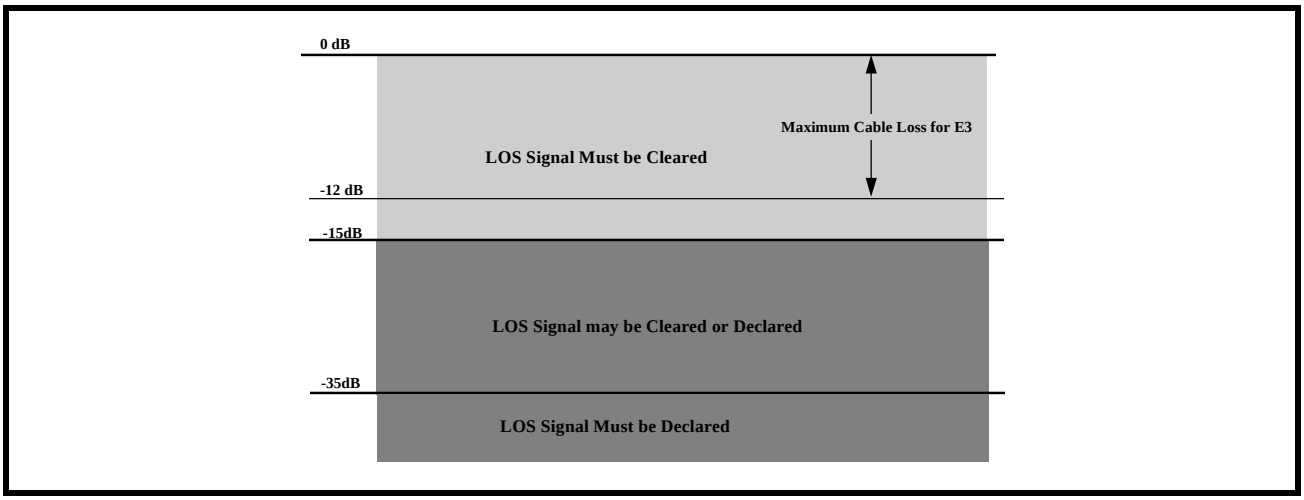
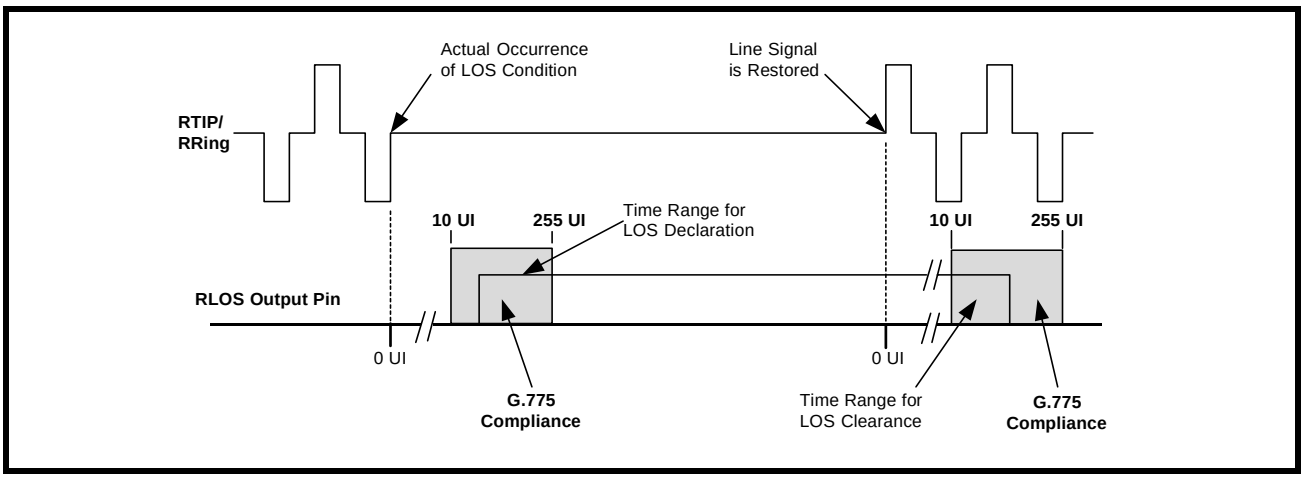


FIGURE 9. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



3.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 10 shows the configuration to test the interference margin for DS3/ STS1. Figure 11 shows the set up for E3.

FIGURE 10. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

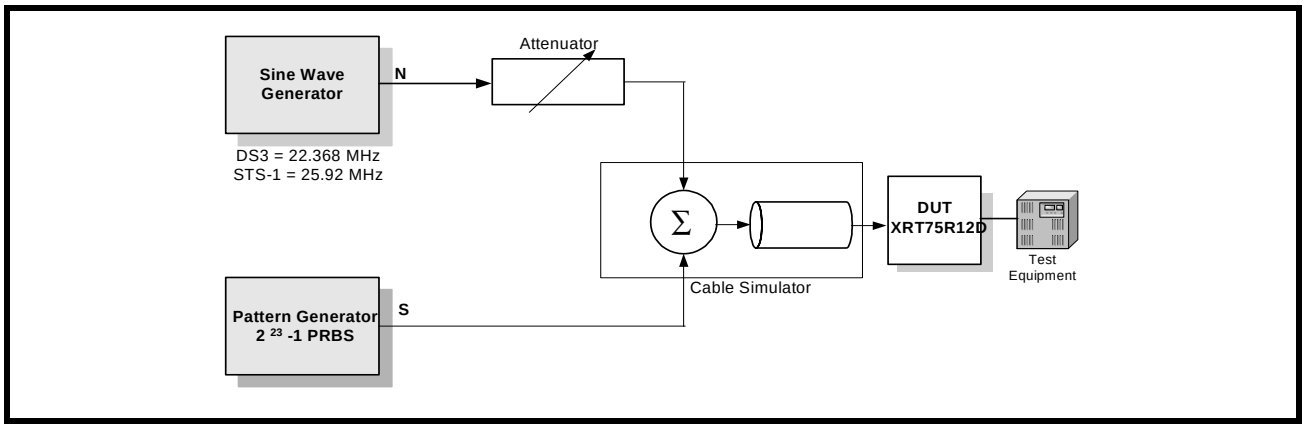


FIGURE 11. INTERFERENCE MARGIN TEST SET UP FOR E3.

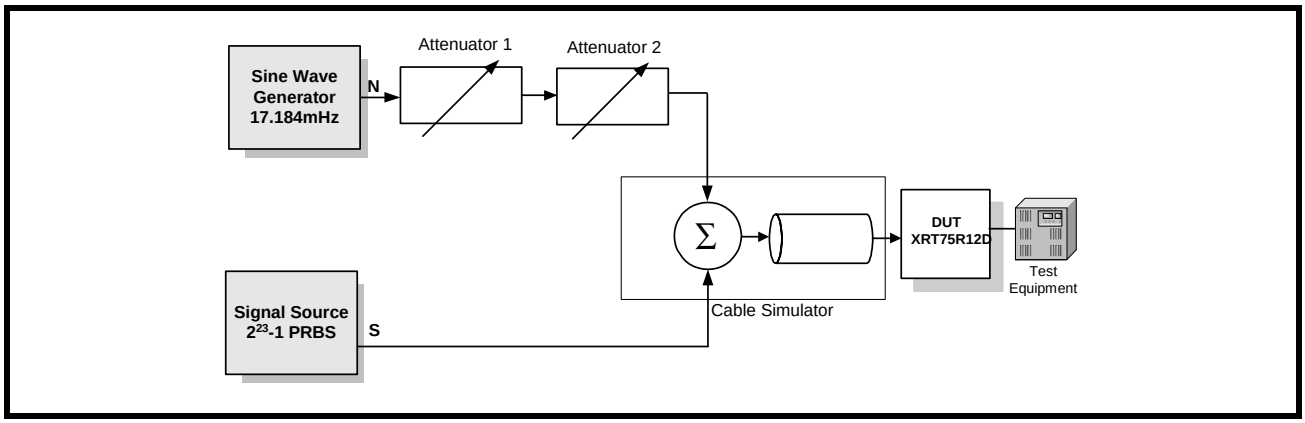


TABLE 3: INTERFERENCE MARGIN TEST RESULTS

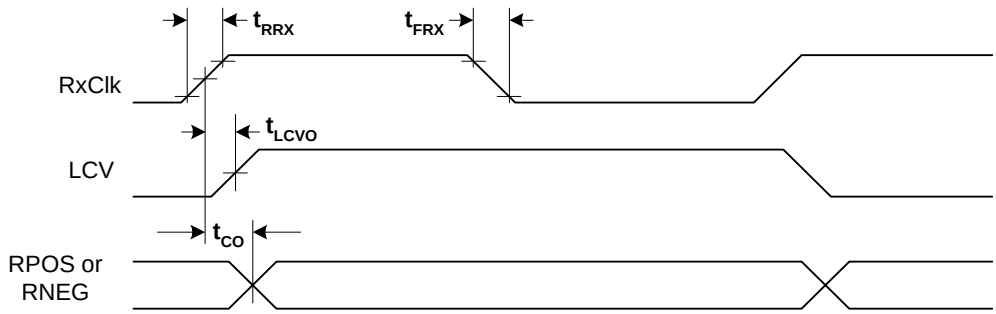
MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	Equalizer “IN”
		-17 dB
	12 dB	-14 dB
DS3	0 feet	-15 dB
	225 feet	-15 dB
	450 feet	-14 dB
STS-1	0 feet	-15 dB
	225 feet	-14 dB
	450 feet	-14 dB

3.5.5 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the internal master clock outputs this clock onto the RxClk_n output pin. The data on the RxPOS_n and RxNEG_n pins can be forced to zero by setting the LOSMUT_n bits in the individual channel control register to "1".

NOTE: *When the LOS condition is cleared, the recovered data is output on RxPOS_n and RxNEG_n pins.*

FIGURE 12. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle	45	50	55	%
	RxClk Frequency E3 DS-3 STS-1		 34.368 44.736 51.84		 MHz MHz MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

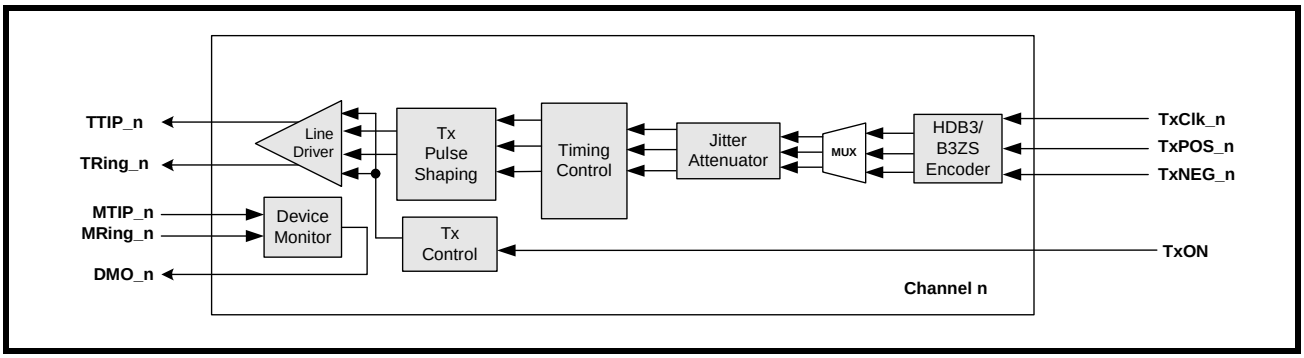
3.6 B3ZS/HDB3 Decoder

The decoder block takes the output from the clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream. Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active "High" pulse is generated on the RLCV_n output pins to indicate line code violation.

4.0 THE TRANSMITTER SECTION

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 13.

FIGURE 13. TRANSMIT PATH BLOCK DIAGRAM



4.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a Framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 14.

FIGURE 14. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75R12D (DUAL-RAIL DATA)

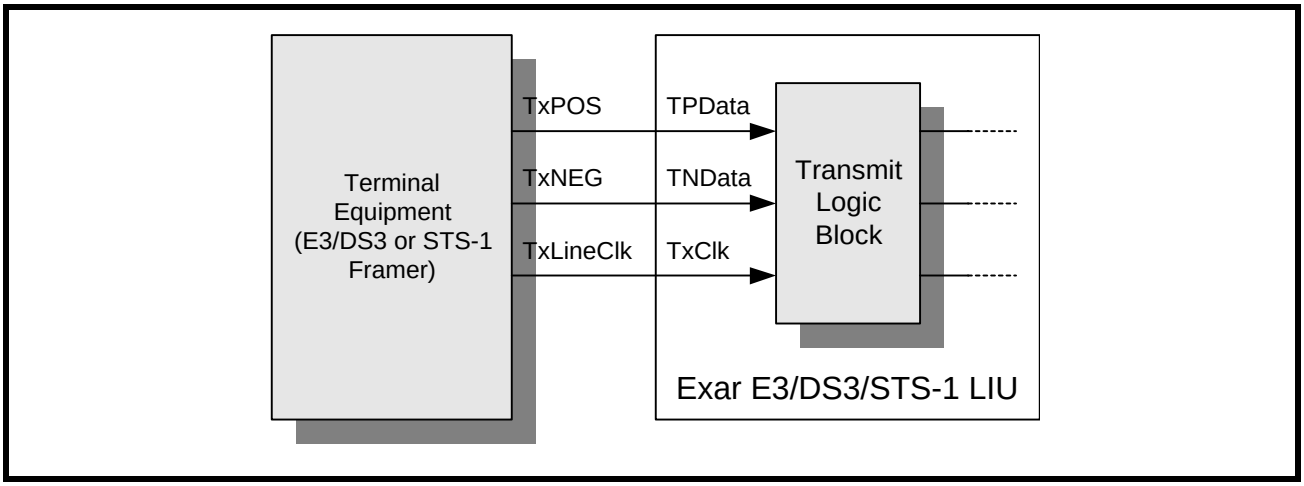
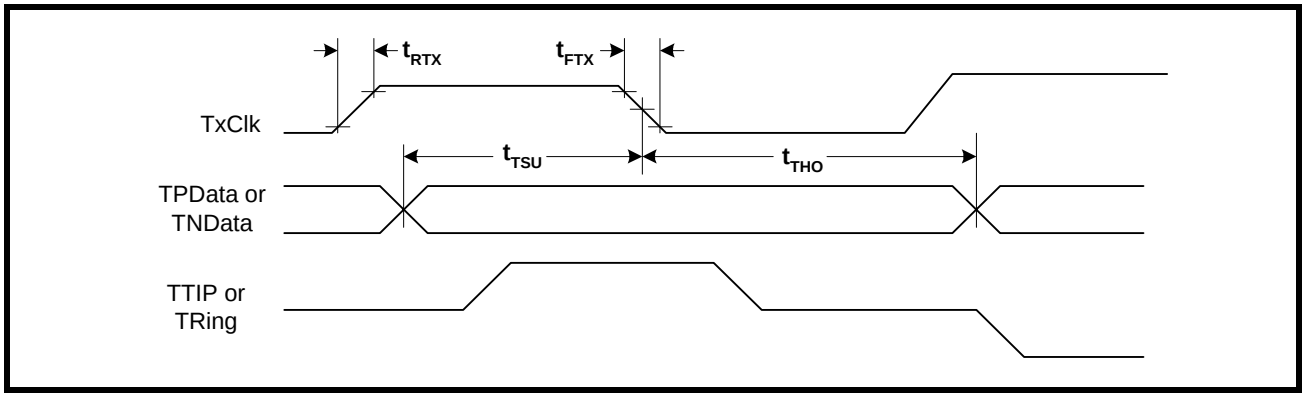


FIGURE 15. TRANSMITTER TERMINAL INPUT TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle	30	50	70	%
	TxClk Frequency				
	E3		34.368		MHz
	DS-3		44.736		MHz
	STS-1		51.84		MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns

FIGURE 16. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)

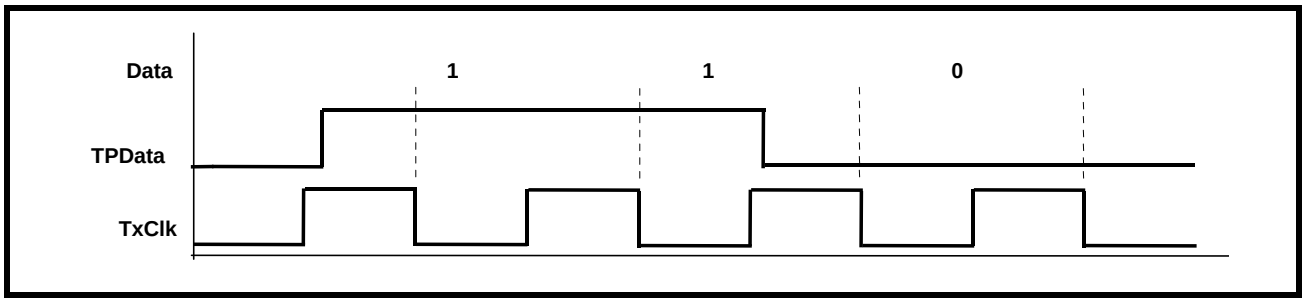
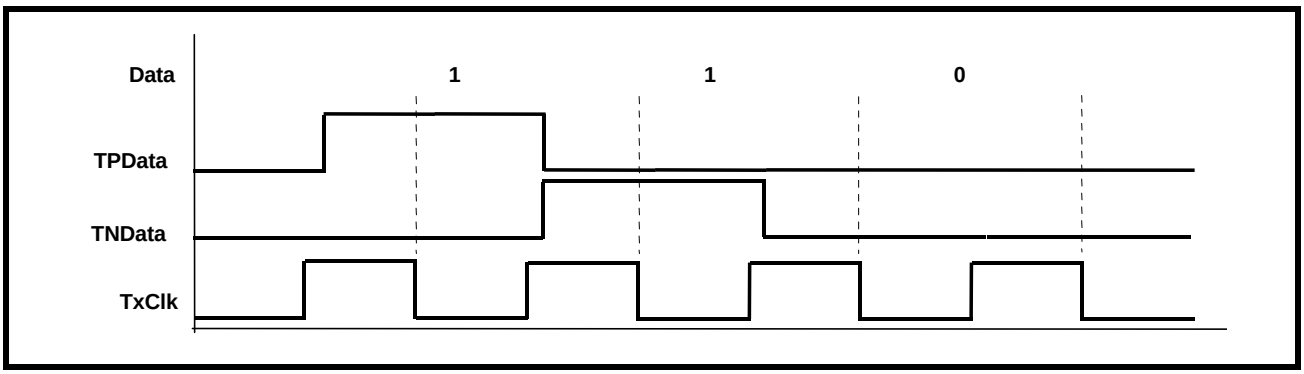


FIGURE 17. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.2 Transmit Clock

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

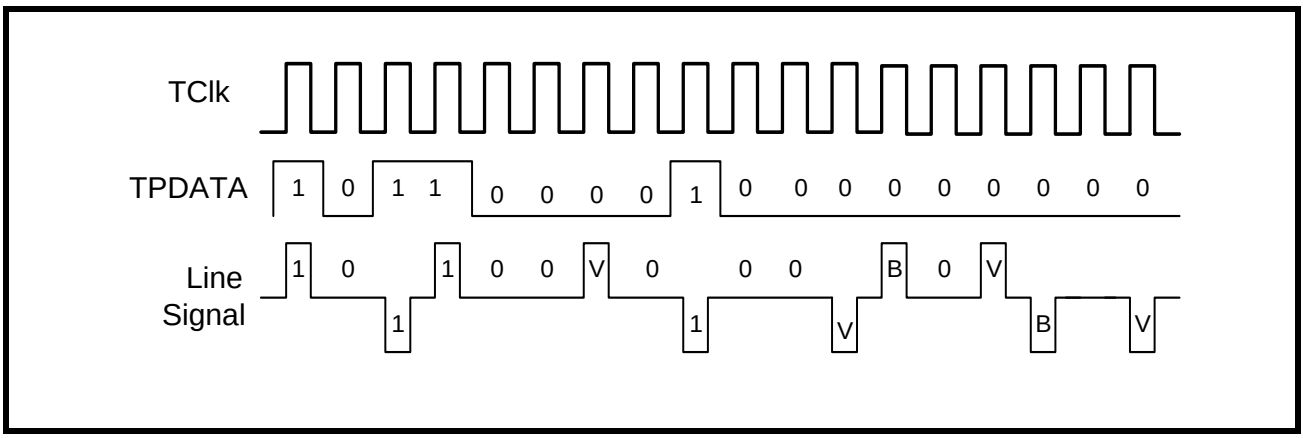
4.3 B3ZS/HDB3 ENCODER

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.3.1 B3ZS Encoding

An example of B3ZS encoding is shown in Figure 18. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

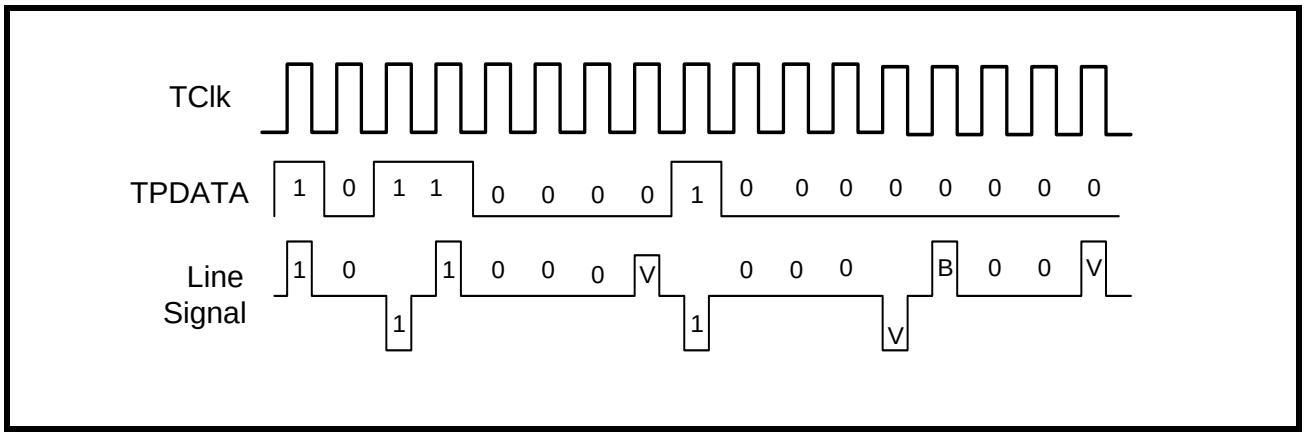
FIGURE 18. B3ZS ENCODING FORMAT



4.3.2 HDB3 Encoding

An example of the HDB3 encoding is shown in Figure 19. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

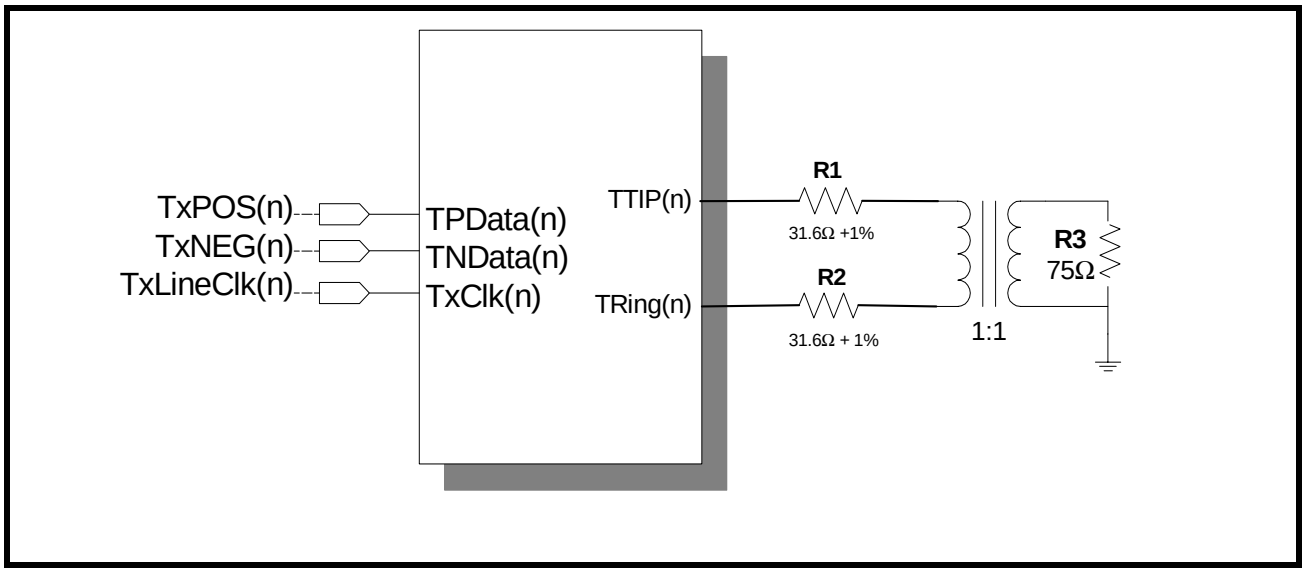
FIGURE 19. HDB3 ENCODING FORMAT



4.4 TRANSMIT PULSE SHAPER

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n bit to "1" or "0" in the control register. For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 20.

FIGURE 20. TRANSMIT PULSE SHAPE TEST CIRCUIT



4.4.1 Guidelines for using Transmit Build Out Circuit

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n control bit to "0". If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.5 E3 line side parameters

The XRT75R12D line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 21. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

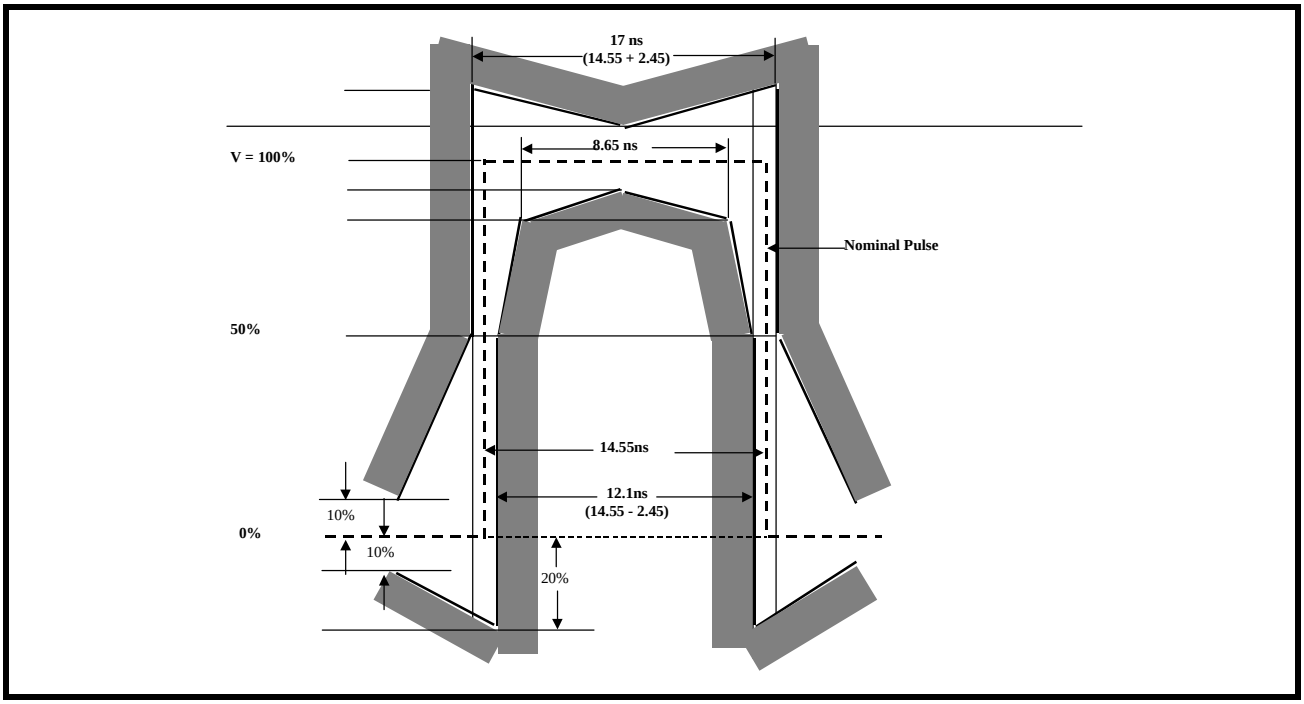


TABLE 4: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Transmit Intrinsic Jitter		0.02	0.05	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1200		feet
Interference Margin	-20	-14		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3 V± 5%.*

FIGURE 22. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

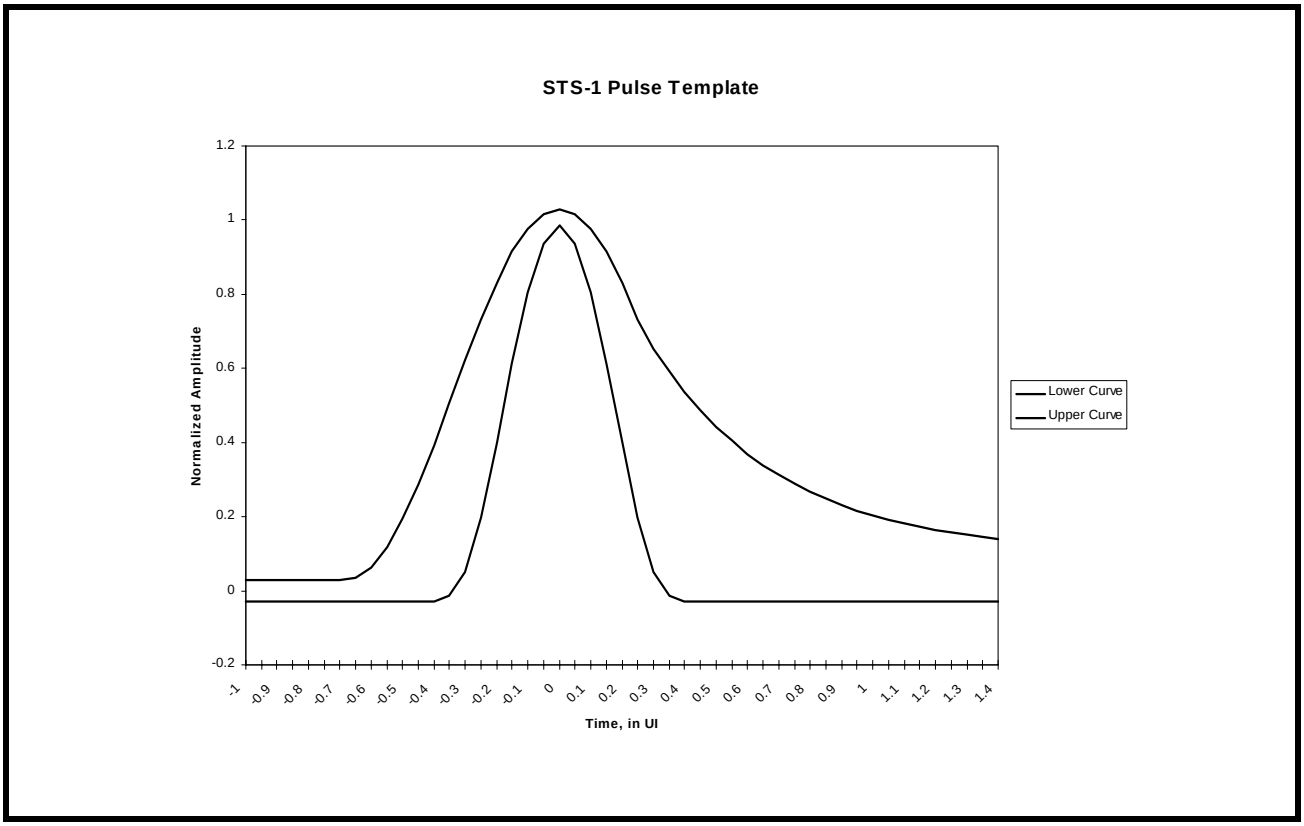


TABLE 5: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 6: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Transmit Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3 V ± 5%.*

FIGURE 23. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

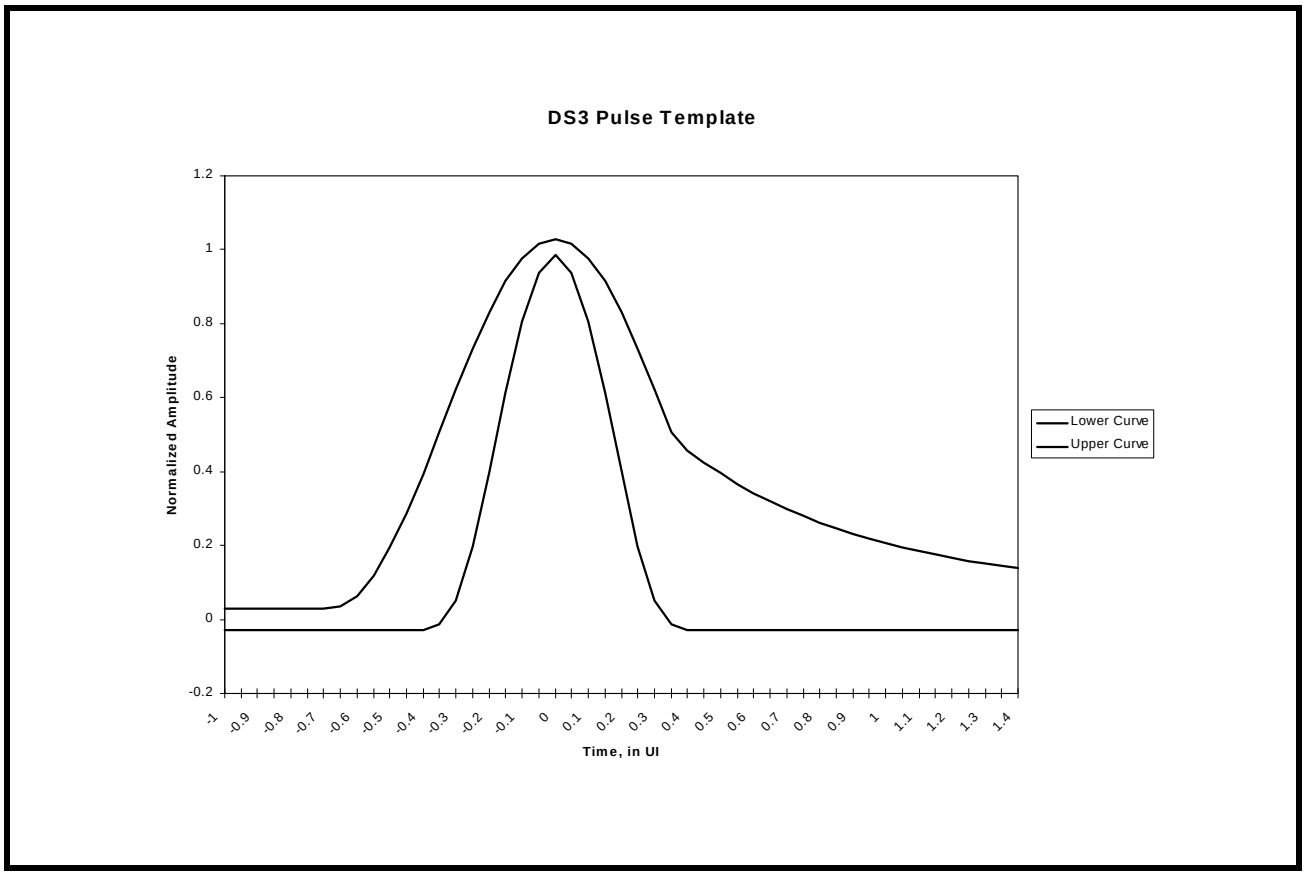


TABLE 7: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 8: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

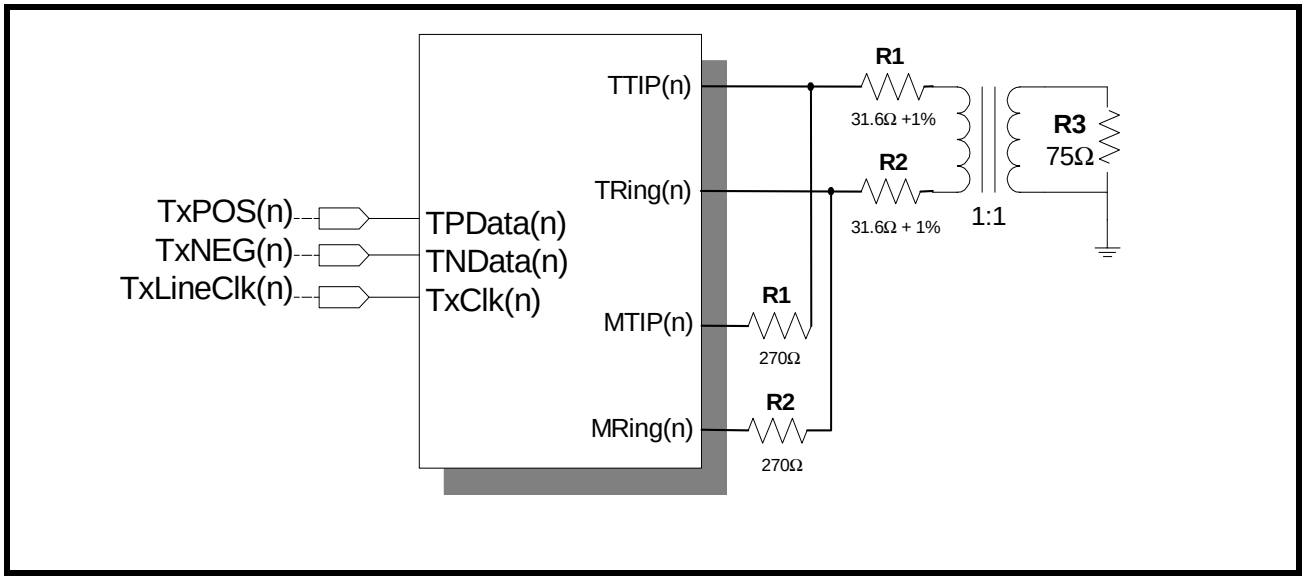
PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Transmit Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3V ± 5%.*

4.6 Transmit Drive Monitor

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver. To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270Ω resistor and MRing_n pins to TRing_n lines via 270Ω resistor as shown in Figure 24.

FIGURE 24. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the drive monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted "Low" as long as the transitions on the line are detected via MTIP_n and MRing_n. If no transitions on the line are detected for 128 ± 32 TxClk_n periods, the DMO_n output toggles "High" and when the transitions are detected again, DMO_n toggles "Low".

NOTE: *The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.*

4.7 Transmitter Section On/Off

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON to "High" and write a "1" to the TxON_n control bit. When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *If the XRT75R12D is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a "1" to the TxON_n control bits transfers the control to TxON pin.*

5.0 JITTER

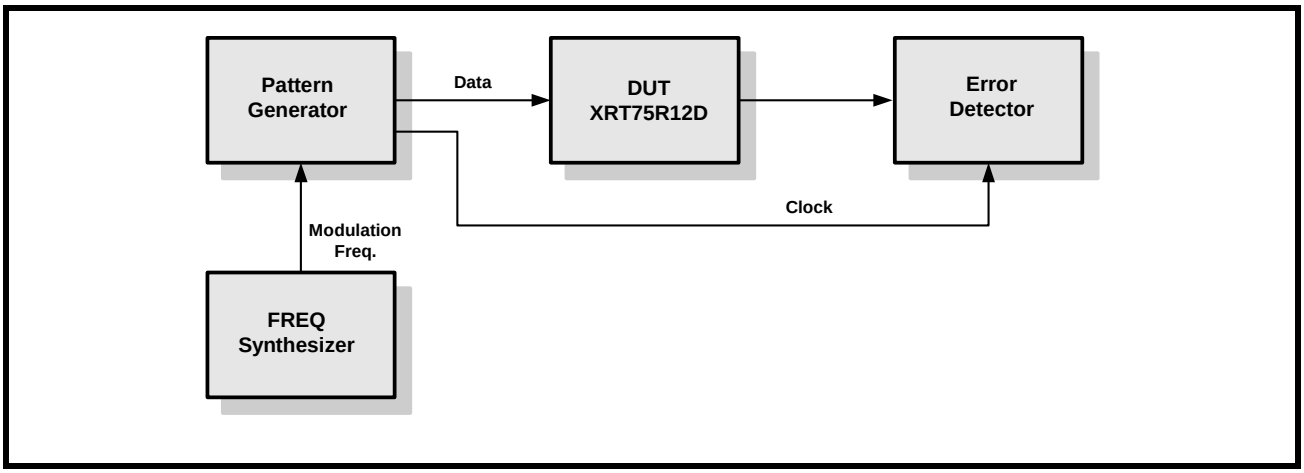
There are three fundamental parameters that describe circuit performance relative to jitter

- **Jitter Tolerance**
- **Jitter Transfer**
- **Jitter Generation**

5.1 JITTER TOLERANCE

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 25, jitter is introduced by the sinusoidal modulation of the serial data bit sequence. Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

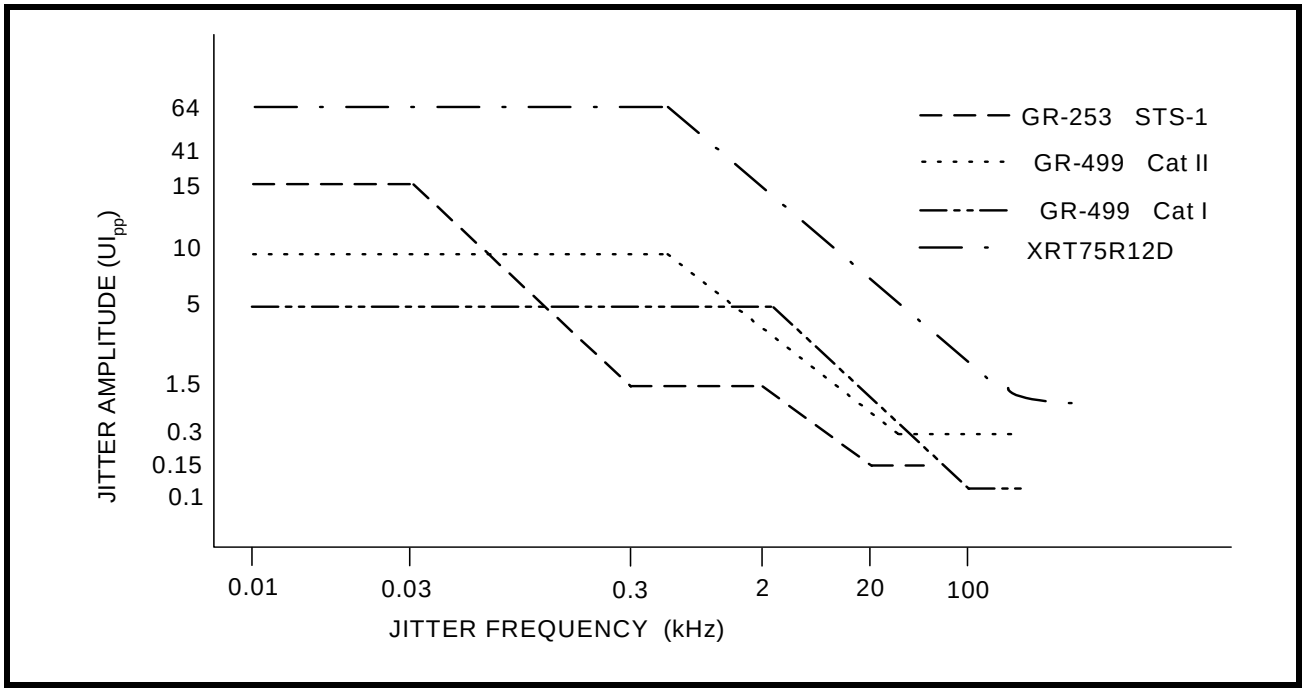
FIGURE 25. JITTER TOLERANCE MEASUREMENTS



5.1.1 DS3/STS-1 Jitter Tolerance Requirements

Bellcore GR-499 CORE specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 26 shows the jitter tolerance curve as per GR-499 specification.

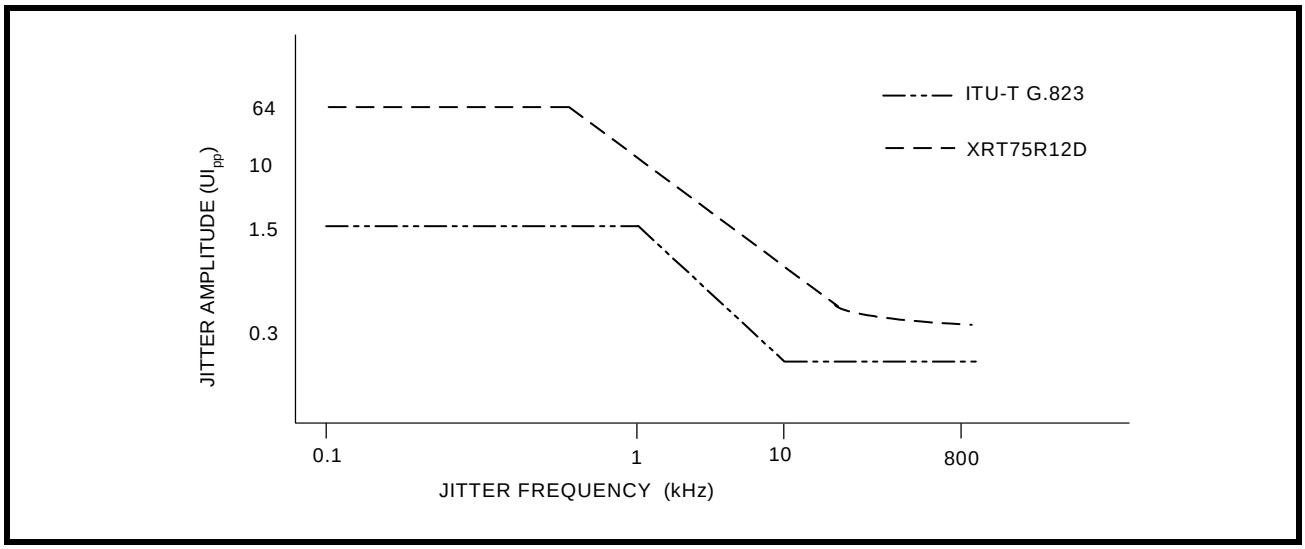
FIGURE 26. INPUT JITTER TOLERANCE FOR DS3/STS-1



5.1.2 E3 Jitter Tolerance Requirements

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to tolerate jitter up to certain specified limits. Figure 27 shows the tolerance curve.

FIGURE 27. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate. Table 9 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 9: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI_{P-P})			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

5.2 JITTER TRANSFER

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. There are two distinct characteristics in jitter transfer, jitter gain (jitter peaking) defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controlled crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. Table 10 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 10: JITTER TRANSFER SPECIFICATION/REFERENCES

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

NOTE: *The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.*

5.3 Jitter Attenuator

An advanced crystal-less jitter attenuator per channel is included in the XRT75R12D. The jitter attenuator requires no external crystal nor high-frequency reference clock. By clearing or setting the JATx/Rx_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. The FIFO size can be either 16-bit or 32-bit. The bits JA0_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL_n is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

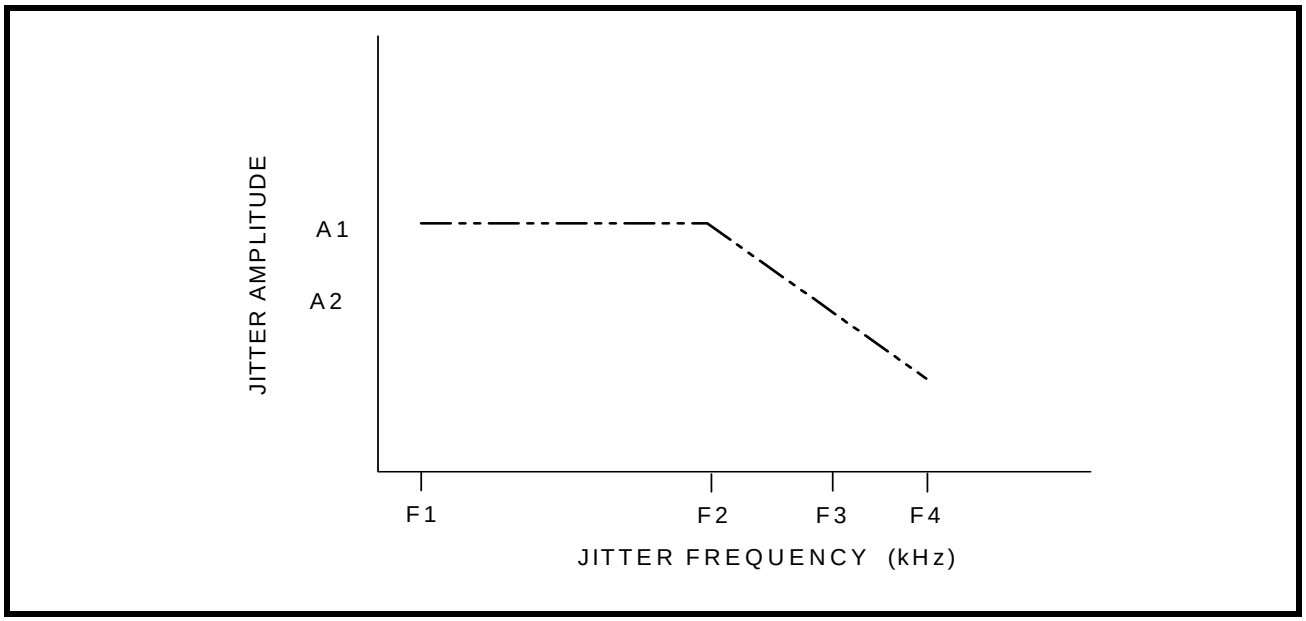
NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 11 specifies the jitter transfer mask requirements for various data rates:*

TABLE 11: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75R12D meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 28.

FIGURE 28. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



5.3.1 JITTER GENERATION

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.0 DIAGNOSTIC FEATURES

6.1 PRBS Generator and Detector

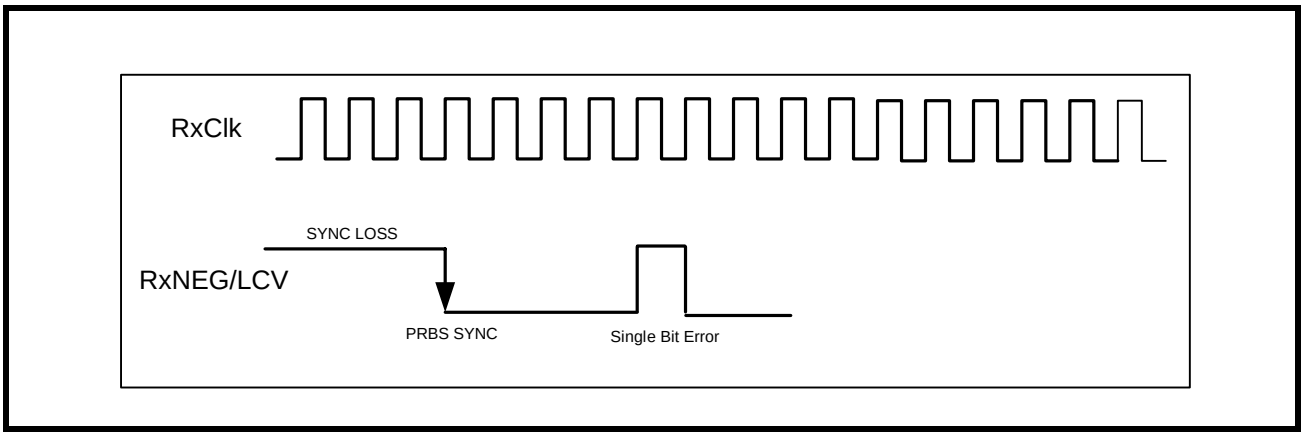
The XRT75R12D contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 29 shows the status of RNEG/LCV pin when the XRT75R12D is configured in PRBS mode.

NOTE: *In PRBS mode, the device is forced to operate in Single-Rail Mode.*

FIGURE 29. PRBS MODE



6.2 LOOPBACKS

The XRT75R12D offers three loopback modes for diagnostic purposes. The loopback modes are selected via the RLB_n and LLB_n bits n the Channel control registers select the loopback modes.

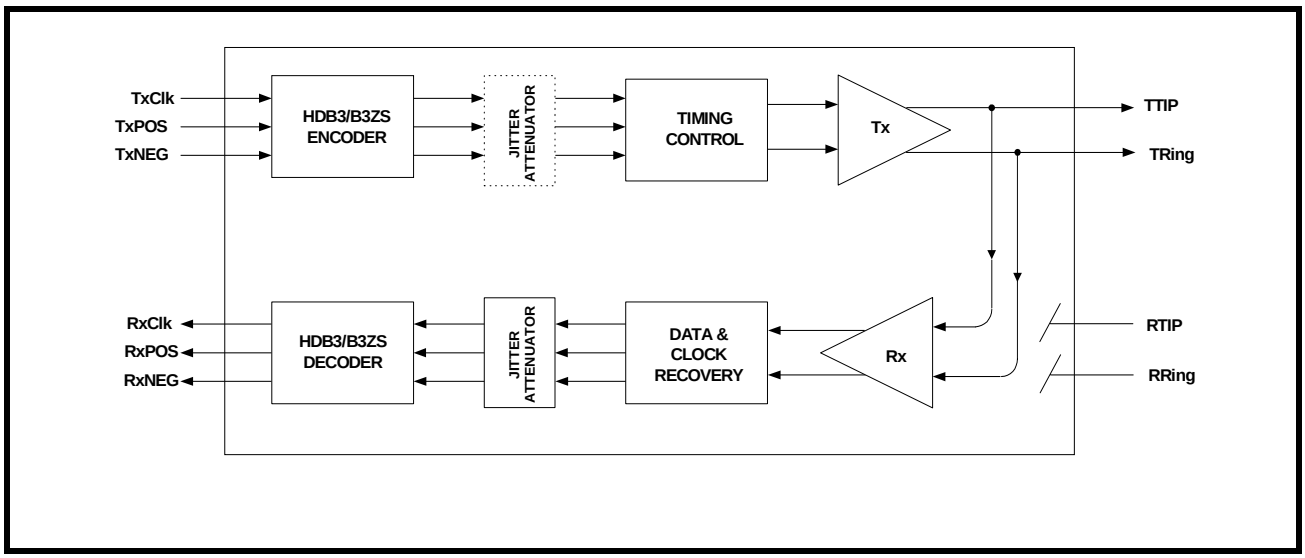
6.2.1 ANALOG LOOPBACK

In this mode, the transmitter outputs TTIP_n and TRing_n are internally connected to the receiver inputs RTIP_n and RRing_n as shown in Figure 30. Data and clock are output at RxClk_n, RxPOS_n and RxNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP_n and TRing_n pins.*
2. *Signals on the RTIP_n and RRing_n pins are ignored during analog loopback.*

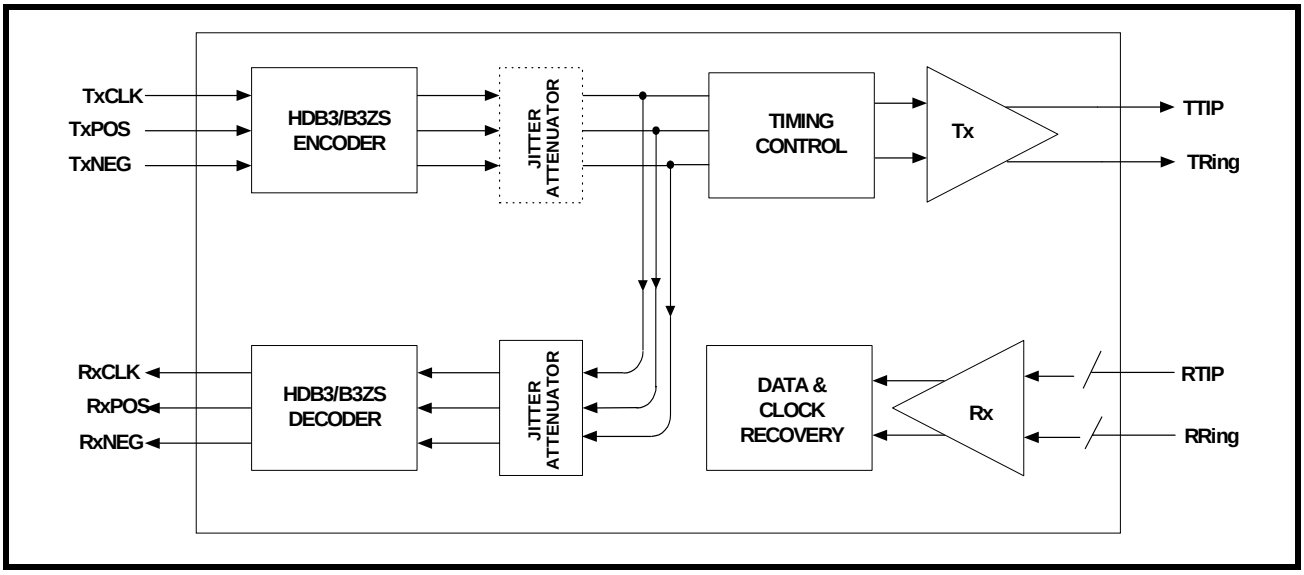
FIGURE 30. ANALOG LOOPBACK



6.2.2 DIGITAL LOOPBACK

When the Digital Loopback is selected, the transmit clock TxClk_n and transmit data inputs (TxPOS_n & TxNEG_n are looped back and output onto the RxClk_n, RxPOS_n and RxNEG_n pins as shown in Figure 31.

FIGURE 31. DIGITAL LOOPBACK

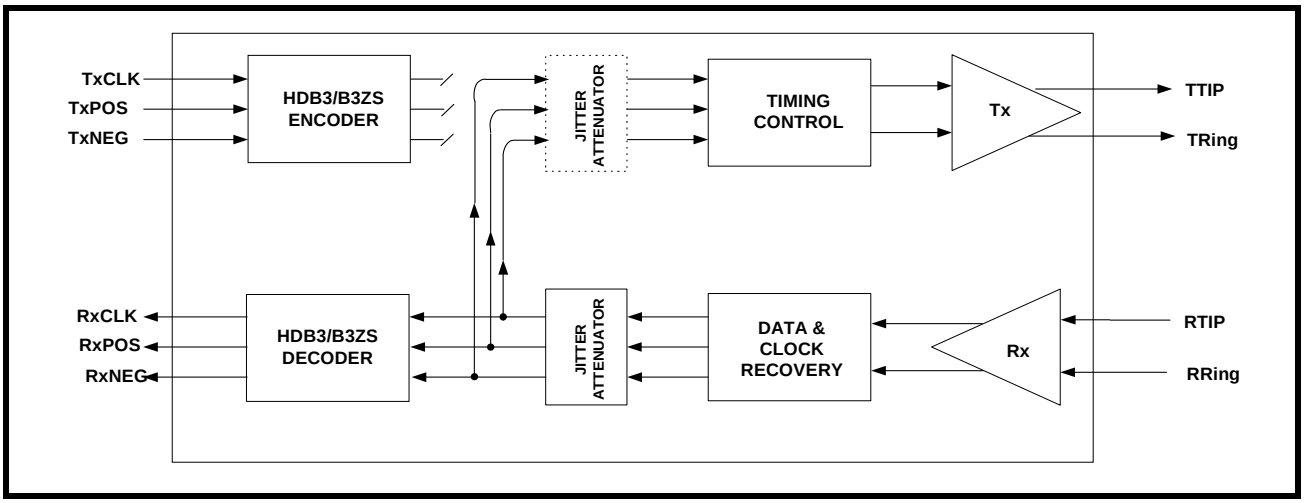


6.2.3 REMOTE LOOPBACK

With Remote loopback activated as shown in Figure 32, the receive data on RTIP and RRing is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RxPOS and RxNEG pins.

NOTE: *Input signals on TxClk, TxPOS and TxNEG are ignored during Remote loopback.*

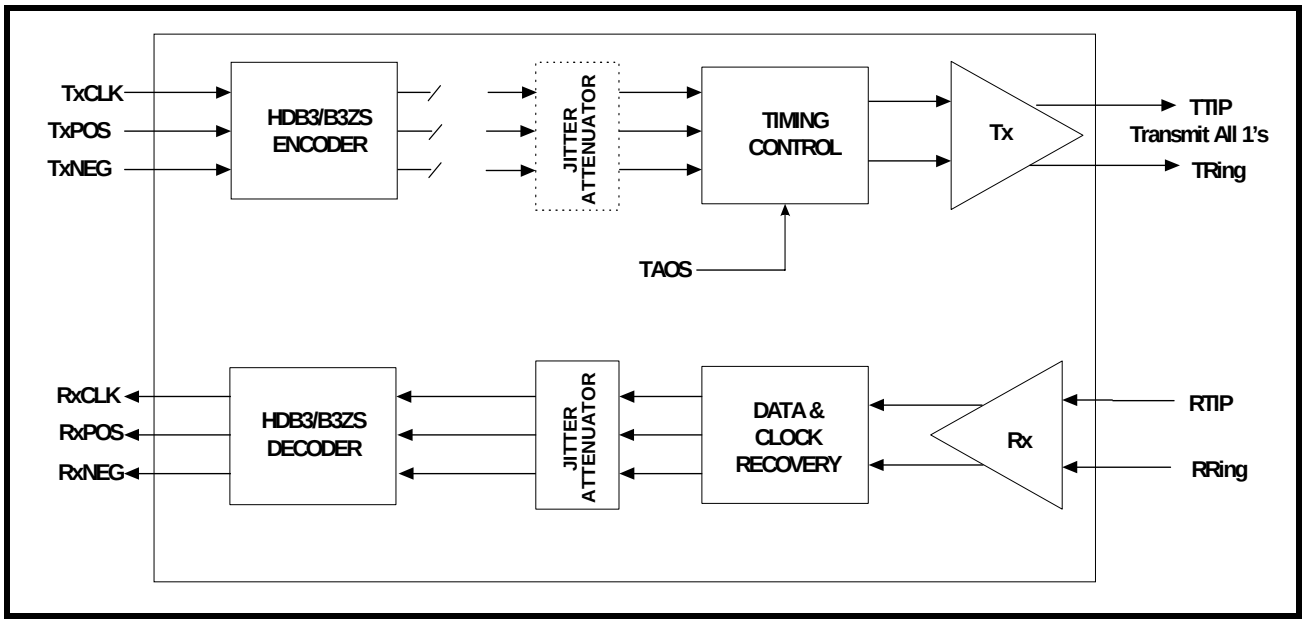
FIGURE 32. REMOTE LOOPBACK



6.3 TRANSMIT ALL ONES (TAOS)

Transmit All Ones (TAOS) can be set by setting the TAOS_n control bits to "1" in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all "1's" pattern on TTIP_n and TRing_n pins. The frequency of this ones pattern is determined by TxClk_n. the TAOS data path is shown in Figure 33. TAOS does not operate in Analog loopback or Remote loopback modes, however will function in Digital loopback mode.

FIGURE 33. TRANSMIT ALL ONES (TAOS)



7.0 MICROPROCESSOR INTERFACE BLOCK

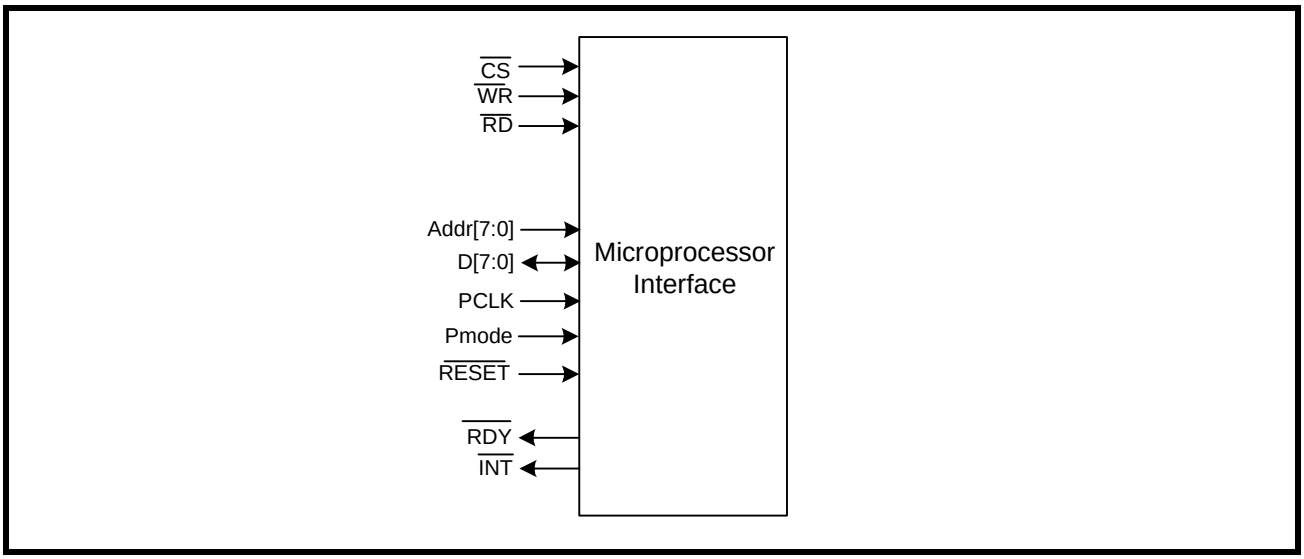
The Microprocessor Interface section supports communication between the local microprocessor (µP) and the LIU. The XRT75R12D supports a parallel interface asynchronously or synchronously timed to the LIU. The microprocessor interface is selected by the state of the Pmode input pin. Selecting the microprocessor interface mode is shown in Table 12.

TABLE 12: SELECTING THE MICROPROCESSOR INTERFACE MODE

PMODE	MICROPROCESSOR MODE
"Low"	Asynchronous Mode
"High"	Synchronous Mode

The local µP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The µP provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The µP also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 34.

FIGURE 34. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



7.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNALS

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 13. The microprocessor interface can be configured to operate in Asynchronous mode or Synchronous mode.

TABLE 13: XRT75R12D MICROPROCESSOR INTERFACE SIGNALS

PIN NAME	TYPE	DESCRIPTION
Pmode	I	**Microprocessor Interface Mode Select Input pin** This pin is used to specify the microprocessor interface mode.
D[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
Addr[7:0]	I	**Eight-Bit Address Bus Inputs** The XRT75R12D LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT75R12D LIU and enables Read/Write operations with the on-chip register locations.
$\overline{RD}$	I	**Read Signal** This active low input functions as the read signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$	I	**Write Signal** This active low input functions as the write signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$	O	**Ready Output** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.
$\overline{INT}$	O	**Interrupt Output** This active low signal is provided by the LIU to alert the local mP that a change in alarm status has occured. This pin is Reset Upon Read (RUR) once the alarm status registers have been cleared.
$\overline{RESET}$	I	**Reset Input** This active low input pin is used to Reset the LIU.

7.2 ASYNCHRONOUS AND SYNCHRONOUS DESCRIPTION

Whether the LIU is configured for Asynchronous or Synchronous mode, the following descriptions apply. The synchronous mode requires an input clock (PCLK) to be used as the microprocessor timing reference. Read and Write operations are described below.

Read Cycle (For Pmode = "0" or "1")

Whenever the local µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
4. After the µP toggles the Read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
5. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

Write Cycle (For Pmode = "0" or "1")

Whenever a local µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus D[7:0].
4. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action enables the bi-directional data bus input drivers of the LIU.
5. After the µP toggles the Write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

FIGURE 35. ASYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

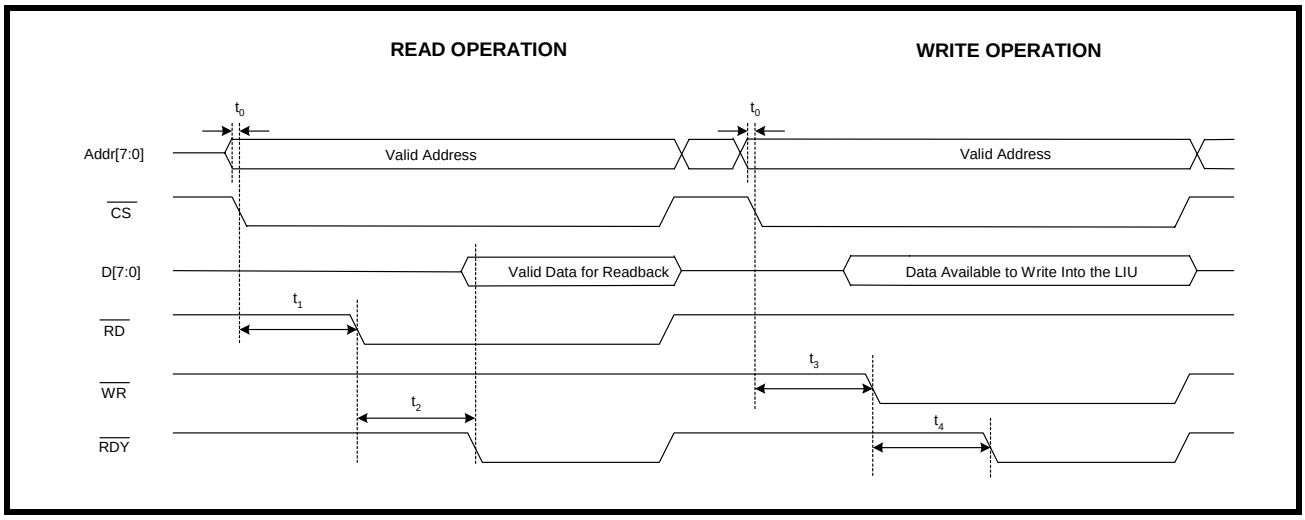


TABLE 14: ASYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	65	ns
NA	$\overline{RD}$ Pulse Width (t_2)	70	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	65	ns
NA	$\overline{WR}$ Pulse Width (t_4)	70	-	ns

FIGURE 36. SYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

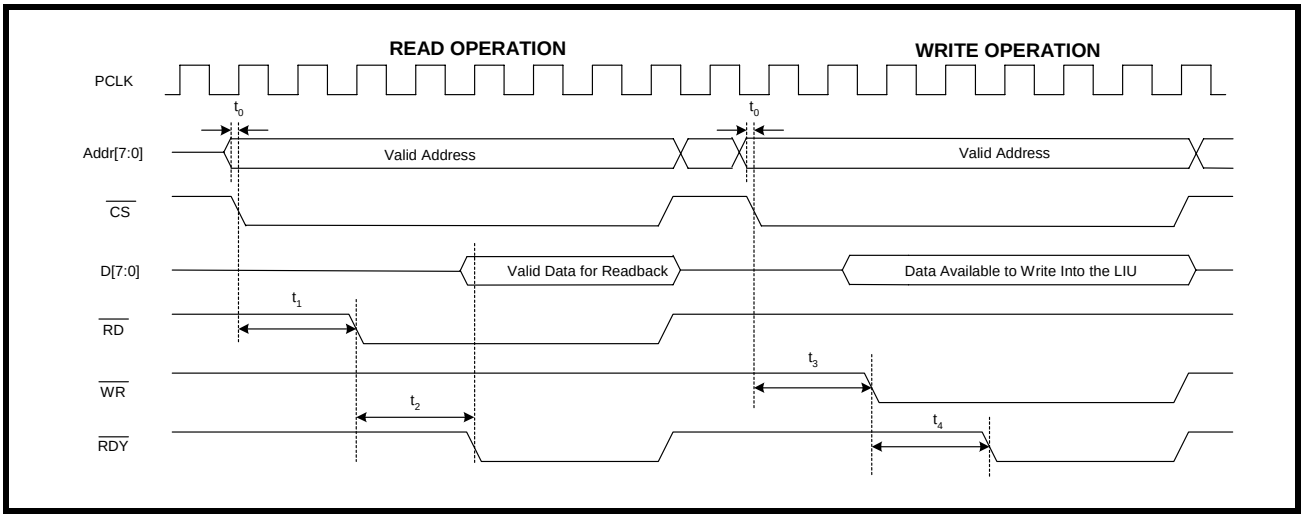


TABLE 15: SYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	35	ns, see note 1
NA	$\overline{RD}$ Pulse Width (t_2)	40	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	35	ns, see note 1
NA	$\overline{WR}$ Pulse Width (t_4)	40	-	ns
	PCLK Period	15		ns
	PCLK Duty Cycle			
	PCLK "High/Low" time			

NOTE: *1. This timing parameter is based on the frequency of the synchronous clock (PCLK). To determine the access time, use the following formula: ($PCLK_{period}$ * 2) + 5ns*

7.3 Register Map

TABLE 16: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75R12D

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x00	CR0	APST	R/W	APS Transmit Redundancy Control Register 0-5
CHANNEL 0 CONTROL REGISTERS				
0x01	CR1	IER0	R/W	Source Level Interrupt Enable Register - Ch 0
0x02	CR2	ISR0	RUR	Source Level Interrupt Status Register Ch 0
0x03	CR3	AS0	R/O	Alarm Status Register - Ch 0
0x04	CR4	TC0	R/W	Transmit Control Register - Ch 0
0x05	CR5	RC0	R/W	Receive Control Register - Ch 0
0x06	CR6	CC0	R/W	Channel Control Register - Ch 0
0x07	CR7	JA0	R/W	Jitter Attenuator Control Register - Ch 0
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x09				
0x0A	CR10	EM0	R/W	Error counter MS Byte Ch 0
0x0B	CR11	EL0	R/W	Error counter LS Byte
0x0C	CR12	EH0	R/W	Error counter Holding register
0x0D				
0x0E				
0x0F				
0x10				
CHANNEL 1 CONTROL REGISTERS				
0x11	CR17	IER1	R/W	Source Level Interrupt Enable Register - Ch 1
0x12	CR18	ISR1	RUR	Source Level Interrupt Status Register - Ch 1
0x13	CR19	AS1	R/O	Alarm Status Register - Ch 1
0x14	CR20	TC0	R/W	Transmit Control Register - Ch 1
0x15	CR21	RC1	R/W	Receive Control Register - Ch 1
0x16	CR22	CC1	R/W	Channel Control Register - Ch 1
0x17	CR23	JA1	R/W	Jitter Attenuator Control Register - Ch 1
0x18				
0x19				
0x1A	CR26	EM1	R/W	Error counter MSByte Ch 1
0x1B	CR27	EL1	R/W	Error counter LSbyte
0x1C	CR28	EH1	R/W	Error counter Holding register

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x1D				
0x1E				
0x1F				
0x20				
CHANNEL 2 CONTROL REGISTERS				
0x21	CR33	IER2	R/W	Source Level Interrupt Enable Register - Ch 2
0x22	CR34	ISR2	RUR	Source Level Interrupt Status Register - Ch 2
0x23	CR35	AS2	R/O	Alarm Status Register - Ch 2
0x24	CR36	TC2	R/W	Transmit Control Register - Ch 2
0x25	CR37	RC2	R/W	Receive Control Register - Ch 2
0x26	CR38	CC2	R/W	Channel Control Register - Ch 2
0x27	CR39	JA2	R/W	Jitter Attenuator Control Register - Ch 2
0x28				
0x29				
0x2A	CR42	EM2	R/W	Error counter MSByte Ch 2
0x2B	CR43	EL2	R/W	Error counter LSbyte
0x2C	CR44	EH2	R/W	Error counter Holding register
0x2D				
0x2E				
0x2F				
0x30				
CHANNEL 3 CONTROL REGISTERS				
0x31	CR49	IER3	R/W	Source Level Interrupt Enable Register - Ch 3
0x32	CR50	ISR3	RUR	Source Level Interrupt Status Register - Ch 3
0x33	CR51	AS3	R/O	Alarm Status Register - Ch 3
0x34	CR52	TC3	R/W	Transmit Control Register - Ch 3
0x35	CR53	RC3	R/W	Receive Control Register - Ch 3
0x36	CR54	CC3	R/W	Channel Control Register - Ch 3
0x37	CR55	JA3	R/W	Jitter Attenuator Control Register - Ch 3
0x38				
0x39				
0x3A	CR58	EM3	R/W	Error counter MSByte Ch 3
0x3B	CR59	EL3	R/W	Error counter LSbyte

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x3C	CR60	EH3	R/W	Error counter Holding register
0x3D				
0x3E				
0x3F				
0x40				
CHANNEL 4 CONTROL REGISTERS				
0x41	CR65	IER4	R/W	Source Level Interrupt Enable Register - Ch 4
0x42	CR66	ISR4	RUR	Source Level Interrupt Status Register - Ch 4
0x43	CR67	AS4	R/O	Alarm Status Register - Ch 4
0x44	CR68	TC4	R/W	Transmit Control Register - Ch 4
0x45	CR69	RC4	R/W	Receive Control Register - Ch 4
0x46	CR70	CC4	R/W	Channel Control Register - Ch 4
0x47	CR71	JA4	R/W	Jitter Attenuator Control Register - Ch 4
0x48				
0x49				
0x4A	CR74	EM4	R/W	Error counter MSByte Ch 4
0x4B	CR75	EL4	R/W	Error counter LSbyte
0x4C	CR76	EH4	R/W	Error counter Holding register
0x4D				
0x4E				
0x4F				
0x50				
CHANNEL 5 CONTROL REGISTERS				
0x51	CR81	IER5	R/W	Source Level Interrupt Enable Register - Ch 5
0x52	CR82	ISR5	RUR	Source Level Interrupt Status Register - Ch 5
0x53	CR83	AS5	R/O	Alarm Status Register - Ch 5
0x54	CR84	TC5	R/W	Transmit Control Register - Ch 5
0x55	CR85	RC5	R/W	Receive Control Register - Ch 5
0x56	CR86	CC5	R/W	Channel Control Register - Ch 5
0x57	CR87	JA5	R/W	Jitter Attenuator Control Register - Ch 5
0x58				
0x59				
0x5A	CR90	EM5	R/W	Error counter MSByte Ch 5

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x5B	CR91	EL5	R/W	Error counter LSbyte
0x5C	CR92	EH5	R/W	Error counter Holding register
0x5D				
0x5E				
0x5F				
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt status flags
0x62				
0x63				
0x64				
0x65				
0x66				
0x67				
0x68				
0x65				
0x69				
0x6A				
0x6B				
0x6C				
0x6D				
0x6E	CR110	PN	R/O	Device Part Number Register
0x6F	CR111	VN	R/O	Chip Revision Number Register
0x70				
0x71				
0x72				
0x73				
0x74				
0x75				
0x76				
0x77				
0x78				
0x75				
0x79				

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x7A				
0x7B				
0x7C				
0x7D				
0x7E				
0x7F				
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11
CHANNEL 6 CONTROL REGISTERS				
0x81	CR129	IER6	R/W	Source Level Interrupt Enable Register - Ch 6
0x82	CR130	ISR6	RUR	Source Level Interrupt Status Register - Ch 6
0x83	CR131	AS6	R/O	Alarm Status Register - Ch 6
0x84	CR132	TC6	R/W	Transmit Control Register - Ch 6
0x85	CR133	RC6	R/W	Receive Control Register - Ch 6
0x86	CR134	CC6	R/W	Channel Control Register - Ch 6
0x87	CR135	JA6	R/W	Jitter Attenuator Control Register - Ch 6
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11
0x89				
0x8A	CR138	EM6	R/W	Error counter MSByte Ch 6
0x8B	CR139	EL6	R/W	Error counter LSbyte
0x8C	CR140	EH6	R/W	Error counter Holding register
0x8D				
0x8E				
0x8F				
0x90				
CHANNEL 7 CONTROL REGISTERS				
0x91	CR145	IER7	R/W	Source Level Interrupt Enable Register - Ch 7
0x92	CR146	ISR7	RUR	Source Level Interrupt Status Register - Ch 7
0x93	CR147	AS7	R/O	Alarm Status Register - Ch 7
0x94	CR148	TC7	R/W	Transmit Control Register - Ch 7
0x95	CR149	RC7	R/W	Receive Control Register - Ch 7
0x96	CR150	CC7	R/W	Channel Control Register - Ch 7
0x97	CR151	JA7	R/W	Jitter Attenuator Control Register - Ch 7
0x98				

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0x99				
0x9A	CR154	EM7	R/W	Error counter MSByte Ch 7
0x9B	CR155	EL7	R/W	Error counter LSbyte
0x9C	CR156	EH7	R/W	Error counter Holding register
0x9D				
0x9E				
0x9F				
0xA0				
CHANNEL 8 CONTROL REGISTERS				
0xA1	CR161	IER8	R/W	Source Level Interrupt Enable Register - Ch 8
0xA2	CR162	ISR8	RUR	Source Level Interrupt Status Register - Ch 8
0xA3	CR163	AS8	R/O	Alarm Status Register - Ch 8
0xA4	CR164	TC8	R/W	Transmit Control Register - Ch 8
0xA5	CR165	RC8	R/W	Receive Control Register - Ch 8
0xA6	CR166	CC8	R/W	Channel Control Register - Ch 8
0xA7	CR167	JA8	R/W	Jitter Attenuator Control Register - Ch 8
0xA8				
0xA9				
0xAA	CR170	EM8	R/W	Error counter MSByte Ch 8
0xAB	CR171	EL8	R/W	Error counter LSbyte
0xAC	CR172	EH8	R/W	Error counter Holding register
0xAD				
0xAE				
0xAF				
0xB0				
CHANNEL 9 CONTROL REGISTERS				
0xB1	CR177	IER9	R/W	Source Level Interrupt Enable Register - Ch 9
0xB2	CR178	ISR9	RUR	Source Level Interrupt Status Register - Ch 9
0xB3	CR179	AS9	R/O	Alarm Status Register - Ch 9
0xB4	CR180	TC9	R/W	Transmit Control Register - Ch 9
0xB5	CR181	RC9	R/W	Receive Control Register - Ch 9
0xB6	CR182	CC9	R/W	Channel Control Register - Ch 9
0xB7	CR183	JA9	R/W	Jitter Attenuator Control Register - Ch 9

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0xB8				
0xB9				
0xBA	CR186	EM9	R/W	Error counter MSByte Ch 9
0xBB	CR187	EL9	R/W	Error counter LSbyte
0xBC	CR188	EH9	R/W	Error counter Holding register
0xBD				
0xBE				
0xBF				
0xC0				
CHANNEL 10 CONTROL REGISTERS				
0xC1	CR193	IER10	R/W	Source Level Interrupt Enable Register - Ch 10
0xC2	CR194	ISR10	RUR	Source Level Interrupt Status Register - Ch 10
0xC3	CR195	AS10	R/O	Alarm Status Register - Ch 10
0xC4	CR196	TC10	R/W	Transmit Control Register - Ch 10
0xC5	CR197	RC10	R/W	Receive Control Register - Ch 10
0xC6	CR198	CC10	R/W	Channel Control Register - Ch 10
0xC7	CR199	JA10	R/W	Jitter Attenuator Control Register - Ch 10
0xC8				
0xC9				
0xCA	CR202	EM10	R/W	Error counter MSByte Ch 10
0xCB	CR203	EL10	R/W	Error counter LSbyte
0xCC	CR204	EH10	R/W	Error counter Holding register
0xCD				
0xCE				
0xCF				
0xD0				
CHANNEL 11 CONTROL REGISTERS				
0xD1	CR209	IER11	R/W	Source Level Interrupt Enable Register - Ch 11
0xD2	CR210	ISR11	RUR	Source Level Interrupt Status Register - Ch 11
0xD3	CR211	AS11	R/O	Alarm Status Register - Ch 11
0xD4	CR212	TC11	R/W	Transmit Control Register - Ch 11
0xD5	CR213	RC11	R/W	Receive Control Register - Ch 11
0xD6	CR214	CC11	R/W	Channel Control Register - Ch 11

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0xD7	CR215	JA11	R/W	Jitter Attenuator Control Register - Ch 11
0xD8				
0xD9				
0xDA	CR218	EM11	R/W	Error counter MSByte Ch 11
0xDB	CR219	EL11	R/W	Error counter LSbyte
0xDC	CR229	EH11	R/W	Error counter Holding register
0xDD				
0xDE				
0xDF				
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt enable flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt status flags
0xE2				
0xE3				
0xE4				
0xE5				
0xE6				
0xE7				
0xE8				
0xE5				
0xE9				
0xEA				
0xEB				
0xEC				
0xED				
0xEE				
0xEF				
0xF0				
0xF1				
0xF2				
0xF3				
0xF4				
0xF5				
0xF6				

ADDRESS (HEX)	COMMAND REGISTER (DECIMAL)	LABEL	TYPE	REGISTER NAME
0xF7				
0xF8				
0xF5				
0xF9				
0xFA				
0xFB				
0xFC				
0xFD				
0xFE				
0xFF				

THE GLOBAL/CHIP-LEVEL REGISTERS

The register set, within the XRT75R12D contains ten global or chip-level registers. These registers control operations in more than one channel or apply to the complete chip. This section will present detailed information on the Global Registers.

TABLE 17: LIST AND ADDRESS LOCATIONS OF GLOBAL REGISTERS

ADDRESS	COMMAND REGISTER	LABEL	TYPE	REGISTER NAME
0x00	CR0	APST	R/W	APS Transmit Redundancy Control Register 0-5
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt status flags
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt enable flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt status flags
0x6E	CR110	PN	ROM	Device Part Number Register
0x6F	CR111	VN	ROM	Chip Revision/Version Number Register

REGISTER DESCRIPTION - GLOBAL REGISTERS

TABLE 18: APS/REDUNDANCY TRANSMIT CONTROL REGISTER - CR0 (ADDRESS LOCATION = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	TxON Ch 5	TxON Ch 4	TxON Ch 3	TxON Ch 2	TxON Ch 1	TxON Ch 0
		R/W	R/W	R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	TxON Ch 5 TxON Ch 4 TxON Ch 3 TxON Ch 2 TxON Ch 1 TxON Ch 0	R/W	Transmit Section ON - Channel n This READ/WRITE bit-field is used to turn on or turn off the Transmit Driver associated with Channel n. If the user turns on the Transmit Driver, then Channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_ n output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_n and TRING_n output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel n and tri-states the TTIP_n and TRING_ n output pins. 1 - Turns on the Transmit Driver associated with Channel n. ***NOTE:*** The master TxON control pin(pin # P4) **must** be in a high state (logic 1) for this operation to turn on any channel.

TABLE 19: APS/REDUNDANCY TRANSMIT CONTROL REGISTER - CR8 (ADDRESS LOCATION = 0X08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	TxON Ch 11	TxON Ch 10	TxON Ch 9	TxON Ch 8	TxON Ch 7	TxON Ch 6
		R/W	R/W	R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	TxON Ch 11 TxON Ch 10 TxON Ch 9 TxON Ch 8 TxON Ch 7 TxON Ch 6	R/W	Transmit Section ON - Channel n This READ/WRITE bit-field is used to turn on or turn off the Transmit Driver associated with Channel n on a per channel basis. If the user turns on the Transmit Driver, then Channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_ n output pins. Conversely, if the user turns off the Transmit Driver (for channel n), the TTIP_n and TRING_n output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel n and tri-states the TTIP_n and TRING_ n output pins. 1 - Turns on the Transmit Driver associated with Channel n. ***NOTE:*** The master TxON control (pin # P4) **must** be in a high state (logic 1) for this operation to turn on any channel.

TABLE 20: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR96 (ADDRESS LOCATION = 0X60)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	Channel 5 Interrupt Enable	Channel 4 Interrupt Enable	Channel 3 Interrupt Enable	Channel 2 Interrupt Enable	Channel 1 Interrupt Enable	Channel 0 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7,6	Unused		
5 4 3 2 1 0	Channel 5 Interrupt Enable Channel 4 Interrupt Enable Channel 3 Interrupt Enable Channel 2 Interrupt Enable Channel 1 Interrupt Enable Channel 0 Interrupt Enable	R/W	**Channel n Interrupt Enable Bit:** This READ/WRITE bit is used to: • To enable Channel n for Interrupt Generation at the Channel Level • To disable all Interrupts associated with Channel n within the XRT75R12D This is a "master" enable bit for ***each*** channel. This bit allows control on a per channel basis to signal the Host of selected error conditions. If a bit is cleared, no interrupts from that channel will be sent to the Host via the $\overline{INT}$. If the bit is set (logic 1), any generated interrupt in channel n that has been enabled in the Interrupt Enable register (IERn) for the channel will activate the $\overline{INT}$ pin to the Host. 0 - Disables all Channel n related Interrupts. 1 - Enables Channel n-related Interrupts. The user **must enable** individual Channel n related Interrupts at the source level, before they are can generate an interrupt.

TABLE 21: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR224 (ADDRESS LOCATION = 0XE0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	Channel 11 Interrupt Enable	Channel 10 Interrupt Enable	Channel 9 Interrupt Enable	Channel 8 Interrupt Enable	Channel 7 Interrupt Enable	Channel 6 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	Channel 11 Interrupt Enable Channel 10 Interrupt Enable Channel 9 Interrupt Enable Channel 8 Interrupt Enable Channel 7 Interrupt Enable Channel 6 Interrupt Enable	R/W	**Channel n Interrupt Enable Bit:** This READ/WRITE bit is used to: • To enable Channel n for Interrupt Generation at the Channel Level • To disable all Interrupts associated with Channel n within the XRT75R12D This is a "master" enable bit for ***each*** channel. This bit allows control on a per channel basis to signal the Host of selected error conditions. If a bit is cleared, no interrupts from that channel will be sent to the Host via the $\overline{INT}$ pin. If the bit is set (logic 1), any generated interrupt in channel n that has been enabled in the Interrupt Enable register (IERn) for the channel will activate the $\overline{INT}$ pin to the Host. 0 - Disables all Channel n related Interrupts. 1 - Enables Channel n-related Interrupts. The user **must enable** individual Channel n related Interrupts at the source level, before they are can generate an interrupt.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	Channel 5 Interrupt Status	Channel 4 Interrupt Status	Channel 3 Interrupt Status	Channel 2 Interrupt Status	Channel 1 Interrupt Status	Channel 0 Interrupt Status
		R/O	R/O	R/O	R/O	R/O	R/O

BIT NUMBER	NAME	TYPE	DESCRIPTION
7, 6	Reserved		
5 4 3 2 1 0	Channel 5 Interrupt Status Channel 4 Interrupt Status Channel 3 Interrupt Status Channel 2 Interrupt Status Channel 1 Interrupt Status Channel 0 Interrupt Status	R/O	**Channel n Interrupt Status Bit:** This READ-ONLY bit-field indicates whether the XRT75R12D has a pending Channel n-related interrupt that is awaiting service. The first six channels are serviced through this location and the other six at address 0xE1. These two registers are used by the Host to identify the source channel of an active interrupt. 0 - Indicates that there is NO Channel n-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel n-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel n (Address Locations = 0xn2) to determine the exact source of the interrupt request. ***NOTE:*** *Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds to the interrupt request channel.*

TABLE 22: The above is: **CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR97 (ADDRESS LOCATION = 0X61)**

TABLE 23: CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR225 (ADDRESS LOCATION = 0XE1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	Channel 11 Interrupt Status	Channel 10 Interrupt Status	Channel 9 Interrupt Status	Channel 8 Interrupt Status	Channel 7 Interrupt Status	Channel 6 Interrupt Status
		R/O	R/O	R/O	R/O	R/O	R/O

BIT NUMBER	NAME	TYPE	DESCRIPTION
7, 6	Reserved		
5 4 3 2 1 0	Channel 11 Interrupt Status Channel 10 Interrupt Status Channel 9 Interrupt Status Channel 8 Interrupt Status Channel 7 Interrupt Status Channel 6 Interrupt Status	R/O	**Channel n Interrupt Status Bit:** This READ-ONLY bit-field indicates whether the XRT75R12D has a pending Channel n-related interrupt that is awaiting service. The last six channels are serviced through this location and the other six at address 0x61. These two registers are used by the Host to identify the source channel of an active interrupt. 0 - Indicates that there is NO Channel n-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel n-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel n (Address Locations = 0xn2) to determine the exact source of the interrupt request. ***NOTE:*** *Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds to the interrupt request channel.*

TABLE 24: DEVICE/PART NUMBER REGISTER - CR110 (ADDRESS LOCATION = 0X6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Part Number ID Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	0	1	1	1

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 0	Part Number ID Value	R/O	0x77	**Part Number ID Value:** This READ-ONLY register contains a unique value for the XRT75R12D. This value will always be 0x77.

TABLE 25: CHIP REVISION NUMBER REGISTER - CR111 (ADDRESS LOCATION = 0X6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Chip Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	X	X	X	X

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 0	Chip Revision Number Value	R/O	0x0#	**Chip Revision Number Value:** This READ-ONLY register contains a value that represents the current revision of this XRT75R12D. This revision number will always be in the form of "0x0#", where "#" is a hexadecimal value that specifies the current revision of the chip. For example, the very first revision of this chip will contain the value "0x01".

THE PER-CHANNEL REGISTERS

The XRT75R12D consists of 120 per-Channel Registers (12 channels and 10 registers per channel). Table 9 presents the overall Register Map with the Per-Channel Registers unshaded.

REGISTER DESCRIPTION - PER CHANNEL REGISTERS

TABLE 26: XRT75R12D REGISTER MAP SHOWING INTERRUPT ENABLE REGISTERS (IER_N)

ADDRESS LOCATION	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	**IER0**	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		**IER1**	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		**IER2**	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		**IER3**	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		**IER4**	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		**IER5**	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	**IER6**	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		**IER7**	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		**IER8**	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		**IER9**	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		**IER10**	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		**IER11**	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 27: SOURCE LEVEL INTERRUPT ENABLE REGISTER - CHANNEL N ADDRESS LOCATION = 0XM1 (m= 0-5 & 8-D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Change of FL Condition Interrupt Enable Ch n	Change of LOL Condition Interrupt Enable Ch n	Change of LOS Condition Interrupt Enable Ch n	Change of DMO Condition Interrupt Enable Ch n
				R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Reserved	R/O	
3	Change of FL Condition Interrupt Enable - Ch n	R/W	**Change of FL (FIFO Limit Alarm) Condition Interrupt Enable - Ch n:** This READ/WRITE bit-field is used to enable or disable the Change of FIFO Limit Alarm Condition Interrupt. If the user enables this interrupt, the XRT75R12D will generate an interrupt if any of the following events occur. • Whenever the Jitter Attenuator (within Channel n) declares the FL (FIFO Limit Alarm) condition. • Whenever the Jitter Attenuator (within Channel n) clears the FL (FIFO Limit Alarm) condition. 0 - Disables the Change in FL Condition Interrupt. 1 - Enables the Change in FL Condition Interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	**Change of Receive LOL (Loss of Lock) Condition Interrupt Enable - Channel n:** This READ/WRITE bit-field is used to enable or disable the Change of Receive LOL Condition Interrupt. If the user enables this interrupt, then the XRT75R12D will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel n) declares the Loss of Lock Condition. • Whenever the Receive Section (within Channel n) clears the Loss of Lock Condition. 0 - Disables the Change in Receive LOL Condition Interrupt. 1 - Enables the Change in Receive LOL Condition Interrupt.
1	Change of LOS Condition Interrupt Enable	R/W	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable - Ch 0:** This READ/WRITE bit-field is used to enable or disable the Change of the Receive LOS Defect Condition Interrupt. If the user enables this interrupt, then the XRT75R12D will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel n) declares the LOS Defect Condition. • Whenever the Receive Section (within Channel n) clears the LOS Defect condition. 0 - Disables the Change in the LOS Defect Condition Interrupt. 1 - Enables the Change in the LOS Defect Condition Interrupt.
0	Change of DMO Condition Interrupt Enable	R/W	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable - Ch n:** This READ/WRITE bit-field is used to enable or disable the Change of Transmit DMO Condition Interrupt. If the user enables this interrupt, then the XRT75R12D will generate an interrupt any time any of the following events occur. • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "1". • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the Change in the DMO Condition Interrupt. 1 - Enables the Change in the DMO Condition Interrupt.

TABLE 28: XRT75R12D REGISTER MAP SHOWING INTERRUPT STATUS REGISTERS (ISR_N)

TABLE 29: SOURCE LEVEL INTERRUPT STATUS REGISTER - CHANNEL N ADDRESS LOCATION = 0XM2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Change of FL Condition Interrupt Status Ch_n	Change of LOL Condition Interrupt Status Ch_n	Change of LOS Condition nterrupt Status Ch_n	Change of DMO Condition Interrupt Status Ch_n
				RUR	RUR	RUR	RUR

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Reserved		
3	Change of FL Condition Interrupt Status	RUR	**Change of FL (FIFO Limit Alarm) Condition Interrupt Status - Ch n:** This RESET-upon-READ bit-field indicates whether or not the Change of FL Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of FL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of FL Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the FIFO Alarm condition by reading out the contents of Bit 3 (FL Alarm Declared) within the Alarm Status Register.(n)*
2	Change of LOL Condition Interrupt Status	RUR	**Change of Receive LOL (Loss of Lock) Condition Interrupt Status - Ch n:** This RESET-upon-READ bit-field indicates whether or not the Change of Receive LOL Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of Receive LOL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of Receive LOL Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOL Defect condition by reading out the contents of Bit 2 (Receive LOL Defect Declared) within the Alarm Status Register.(n)*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Change of LOS Condition Interrupt Status	RUR	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of the Receive LOS Defect Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOS Defect condition by reading out the contents of Bit 1 (Receive LOS Defect Declared) within the Alarm Status Register.(n)*
0	Change of DMO Condition Interrupt Status	RUR	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status - Ch n:** This RESET-upon-READ bit-field indicates whether or not the Change of the Transmit DMO Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of the Transmit DMO Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Transmit DMO Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Transmit DMO Condition by reading out the contents of Bit 0 (Transmit DMO Condition) within the Alarm Status Register.(n)*

TABLE 30: XRT75R12D REGISTER MAP SHOWING ALARM STATUS REGISTERS (AS_N)

TABLE 31: ALARM STATUS REGISTER - CHANNEL N ADDRESS LOCATION = 0XM3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Loss of PRBS Pattern Sync	Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
	R/O	R/O	R/O	R/O	R/O	R/O	R/O

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Reserved		
6	Loss of PRBS Pattern Lock	R/O	**Loss of PRBS Pattern Lock Indicator:** This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Receive Section of Channel n) is declaring PRBS Lock within the incoming PRBS pattern. If the PRBS Receiver detects a very large number of bit-errors within its incoming data-stream, then it will declare the Loss of PRBS Lock Condition. Conversely, if the PRBS Receiver were to detect its pre-determined PRBS pattern with the incoming DS3, E3 or STS-1 data-stream, (with little or no bit errors) then the PRBS Receiver will clear the Loss of PRBS Lock condition. 0 - Indicates that the PRBS Receiver is currently declaring the PRBS Lock condition within the incoming DS3, E3 or STS-1 data-stream. 1 - Indicates that the PRBS Receiver is currently declaring the Loss of PRBS Lock condition within the incoming DS3, E3 or STs-1 data-stream. ***NOTE:*** *This register bit is only valid if all of the following are true.* **a.** The PRBS Generator block (within the Transmit Section of the Chip is enabled). **b.** The PRBS Receiver is enabled. **c.** The PRBS Pattern (that is generated by the PRBS Generator) is somehow looped back into the Receive Path (via the Line-Side) and in-turn routed to the receive input of the PRBS Receiver.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	Digital LOS Defect Declared	R/O	**Digital LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Digital LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Digital LOS Detector will declare the LOS Defect condition whenever it detects an absence of pulses (within the incoming DS3 or STS-1 data-stream) for 160 consecutive bit-periods. Further, (again for DS3 and STS-1 applications) the Digital LOS Detector will clear the LOS Defect condition whenever it determines that the pulse density (within the incoming DS3 or STS-1 signal) is at least 33%. 0 - Indicates that the Digital LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Digital LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT75R12D) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*
4	Analog LOS Defect Declared	R/O	**Analog LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Analog LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Analog LOS Detector will declare the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) drops below a certain Analog LOS Defect Declaration threshold level. Conversely, (again for DS3 and STS-1 applications) the Analog LOS Detector will clear the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) has risen above a certain Analog LOS Defect Clearance threshold level. It should be noted that, in order to prevent "chattering" within the Analog LOS Detector output, there is some built-in hysteresis between the Analog LOS Defect Declaration and the Analog LOS Defect Clearance threshold levels. 0 - Indicates that the Analog LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Analog LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT75R12D) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	FL Alarm Declared	R/O	**FL (FIFO Limit) Alarm Declared:** This READ-ONLY bit-field indicates whether or not the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm. The Jitter Attenuator block will declare the FIFO Limit Alarm anytime the Jitter Attenuator FIFO comes within two bit-periods of either over-flowing or under-running. Conversely, the Jitter Attenuator block will clear the FIFO Limit Alarm anytime the Jitter Attenuator FIFO is NO longer within two bit-periods of either overflowing or under-running. Typically, this Alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. 0 - Indicates that the Jitter Attenuator block (within Channel_n) is NOT currently declaring the FIFO Limit Alarm condition. 1 - Indicates that the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm condition. ***NOTE:*** *This bit-field is only active if the Jitter Attenuator (within Channel_n) has been enabled.*
2	Receive LOL Condition Declared	R/O	**Receive LOL (Loss of Lock) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOL (Loss of Lock) condition. The Receive Section (of Channel_n) will declare the LOL Condition, if the frequency of the Recovered Clock signal differs from that of the reference clock programmed for that channel (from the appropriate oscillator or the SFM clock synthesizer if in that mode) by 0.5% (or 5000ppm) or more . 0 - Indicates that the Receive Section of Channel_n is NOT currently declaring the LOL Condition. 1 - Indicates that the Receive Section of Channel_n is currently declaring the LOL Condition and the recovered clock differs by more than 0.5%..

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Receive LOS Defect Condition Declared	R/O	**Receive LOS (Loss of Signal) Defect Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOS defect condition. The Receive Section (of Channel_n) will declare the LOS defect condition, if any one of the following conditions is met. • If the Digital LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) • If the Analog LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) • If the ITU-T G.775 LOS Detector declares the LOS defect condition (for E3 applications). 0 - Indicates that the Receive Section of Channel_n is NOT currently declaring the LOS Defect Condition. 1 - Indicates that the Receive Section of Channel_n is currently declaring the LOS Defect condition.
0	Transmit DMO Condition Declared	R/O	**Transmit DMO (Drive Monitor Output) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Transmit Section of Channel_n is currently declaring the DMO Alarm condition. As configured, the Transmit Section will either internally (via the TTIP_n and TRING_n) or externally (via the MTIP_n and MRING_n) check the Transmit Output DS3/E3/STS-1 Line signal for bipolar pulses. If the Transmit Section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition upon detecting bipolar activity on the Transmit Output Line signal. 0 - Indicates that the Transmit Section of Channel_n is NOT currently declaring the Transmit DMO Alarm condition. 1 - Indicates that the Transmit Section of Channel_n is currently declaring the Transmit DMO Alarm condition.

TABLE 32: XRT75R12D REGISTER MAP SHOWING TRANSMIT CONTROL REGISTERS (TC_N)

TABLE 33: TRANSMIT CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM4

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Internal Transmit Drive Monitor	Insert PRBS Error	Reserved	TAOS	TxCLKINV	TxLEV
		R/W	R/W		R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Reserved		
5	Internal Transmit Drive Monitor Enable	R/W	**Internal Transmit Drive Monitor Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Transmit Section of Channel_n to either internally or externally monitor the TTIP_n and TRING_n output pins for bipolar pulses, in order to determine whether to declare the Transmit DMO Alarm condition. If the user configures the Transmit Section to externally monitor the TTIP_n and TRING_n output pins (for bipolar pulses) then the user must connect the MTIP_n and MRING_n input pins to their corresponding TTIP_n and TRING_n output pins (via a 270 ohm series resistor). If the user configures the Transmit Section to internally monitor the TTIP_n and TRING_n output pins (for bipolar pulses), the user does NOT need to conect the MTIP_n and MRING_n input pins. This monitoring will be performed internally at the TTIP_n and TRING_n pads. 0 - Configures the Transmit Drive Monitor to externally monitor the TTIP_n and TRING_n output pins for bipolar pulses. 1 - Configures the Transmit Drive Monitor to internally monitor the TTIP_n and TRING_n output pins for bipolar pulses.
4	Insert PRBS Error	R/W	**Insert PRBS Error - Channel_n:** A "0 to 1" transition within this bit-field causes the PRBS Generator (within the Transmit Section of Channel_n) to generate a single bit error within the outbound PRBS pattern-stream. ***NOTES:*** *1. This bit-field is only active if the PRBS Generator and Receiver have been enabled within the corresponding Channel.* *2. After writing the "1" into this register, the user must execute a write operation to clear this particular register bit to "0" in order to facilitate the next "0 to 1" transition in this bit-field.*
3	Reserved		

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	TAOS	R/W	**Transmit All OneS Pattern - Channel_n:** This READ/WRITE bit-field is used to command the Transmit Section of Channel_n to generate and transmit an unframed, All Ones pattern via the DS3, E3 or STS-1 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting, the Transmit Section will ignore the data that it is accepting from the System-side equipment and output the "All Ones" Pattern. 0 - Configures the Transmit Section to transmit the data that it accepts from the System-side Interface. 1 - Configures the Transmit Section to generate and transmit the Unframed, All Ones pattern.
1	TxCLKINV	R/W	**Transmit Clock Invert Select - Channel_n:** This READ/WRITE bit-field is used to select the edge of the TxCLK_n input that the Transmit Section of Channel_n will use to sample the TxPOS_n and TxNEG_n input pins, as described below. 0 - Configures the Transmit Section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the falling edge of TxCLK_n. 1 - Configures the Transmit Section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the rising edge of TxCLK_n. ***NOTE:*** *This is done on a per-channel basis.*
0	TxLEV	R/W	**Transmit Line Build-Out Select - Channel_n:** This READ/WRITE bit-field is used to enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set this bit-field to either "0" or to "1" based upon the following guidelines. 0 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or less. 1 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is more than 225 feet . The user must follow these guidelines in order to insure that the Transmit Section (of Channel_n) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE. ***NOTE:*** *This bit-field is ignored if the channel has been configured to operate in the E3 Mode.*

TABLE 34: XRT75R12D REGISTER MAP SHOWING RECEIVE CONTROL REGISTERS (RC_N)

TABLE 35: RECEIVE CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Disable DLOS Detector	Disable ALOS Detector	RxCLKINV	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
		R/W	R/W	R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Reserved		
5	Disable DLOS Detector	R/W	**Disable Digital LOS Detector - Channel_n:** This READ/WRITE bit-field is used to enable or disable the Digital LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Digital LOS Detector within Channel_n. 1 - Disables the Digital LOS Detector within Channel_n. ***NOTE:*** *This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.*
4	Disable ALOS Detector	R/W	**Disable Analog LOS Detector - Channel_n:** This READ/WRITE bit-field is used to either enable or disable the Analog LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Analog LOS Detector within Channel_n. 1 - Disables the Analog LOS Detector within Channel_n. ***NOTE:*** *This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.*
3	RxCLKINV	R/W	**Receive Clock Invert Select - Channel_n:** This READ/WRITE bit-field is used to select the edge of the RxCLK_n output that the Receive Section of Channel_n will use to output the recovered data via the RxPOS_n and RxNEG_n output pins, as described below. 0 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the rising edge of RCLK_n. 1 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the falling edge of RCLK_n.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	LOSMUT Enable	R/W	**Muting upon LOS Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Receive Section (within Channel_n) to automatically pull their corresponding Recovered Data Output pins (e.g., RxPOS_n and RxNEG_n) to GND for the duration that the Receive Section declares the LOS defect condition. In other words, this feature (if enabled) will cause the Receive Channel to automatically mute the Recovered data anytime the Receive Section declares the LOS defect condition. 0 - Disables the Muting upon LOS feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. 1 - Enables the Muting upon LOS feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition.
1	Receive Monitor Mode Enable	R/W	**Receive Monitor Mode Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Receive Section of Channel_n to operate in the Receive Monitor Mode. If the user configures the Receive Section to operate in the Receive Monitor Mode, then it will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuator by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. 0 - Configures the corresponding channel to operate in the Normal Mode. 1 - Configure the corresponding channel to operate in the Receive Monitor Mode.
0	Receive Equalizer Enable	R/W	**Receive Equalizer Enable - Channel_n:** This READ/WRITE register bit is used to enable or disable the Receive Equalizer block within the Receive Section of Channel_n, as listed below. 0 - Disables the Receive Equalizer within the corresponding channel. 1 - Enables the Receive Equalizer within the corresponding channel. ***NOTE:*** *For virtually all applications, we recommend that the user set this bit-field to "1" (for all channels) and enable the Receive Equalizer.*

TABLE 36: XRT75R12D REGISTER MAP SHOWING CHANNEL CONTROL REGISTERS (CC_N)

TABLE 37: CHANNEL CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM6

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
		R/W	R/W	R/W	R/W	R/W	R/W

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>7 - 6</td><td>Reserved</td><td></td><td></td></tr>
<tr><td>5</td><td>PRBS Enable</td><td>R/W</td><td>PRBS Generator and Receiver Enable - Channel_n:
This READ/WRITE bit-field is used to enable or disable the PRBS Generator and Receiver within a given Channel of the XRT75R12D.
If the user enables the PRBS Generator and Receiver, then the following will happen.
1. The PRBS Generator (which resides within the Transmit Section of the Channel) will begin to generate an unframed, 2^15-1 PRBS Pattern (for DS3 and STS-1 applications) and an unframed, 2^23-1 PRBS Pattern (for E3 applications).
2. The PRBS Receiver (which resides within the Receive Section of the Channel) will now be enabled and will begin to search the incoming data for the above-mentioned PRBS patterns.
0 - Disables both the PRBS Generator and PRBS Receiver within the corresponding channel.
1 - Enables both the PRBS Generator and PRBS Receiver within the corresponding channel.
NOTES:
1. To check and monitor PRBS Bit Errors, DR (Dual Rail) mode will be over-ridden and Single Rail mode forced for the duration of this mode. This will configure the RNEG/LCV_n output pin to function as a PRBS Error Indicator. All errors will be flagged on this pin. The errors will also be accumulated in the 16 bit Error counter for the channel.
2. If the user enables the PRBS Generator and PRBS Receiver, the Channel will ignore the data that is being accepted from the System-side Equipment (via the TxPOS_n and TxNEG_n input pins) and will overwrite this outbound data with the PRBS Pattern.
3. The system must provide an accurate and stable data-rate clock to the TxClk_n pin during this operation.</td></tr>
<tr><td>4</td><td>RLB_n</td><td>R/W</td><td>Loop-Back Select - RLB Bit - Channel_n:
This READ/WRITE bit-field along with the corresponding LLB_n bit-field is used to configure a given channel into various loop-back modes ass shown by the following table.
<table><tr><th>LLB_n</th><th>RLB_n</th><th>Loop-back Mode</th></tr><tr><td>0</td><td>0</td><td>Normal (No Loop-back) Mode</td></tr><tr><td>0</td><td>1</td><td>Remote Loop-back Mode</td></tr><tr><td>1</td><td>0</td><td>Analog Local Loop-back Mode</td></tr><tr><td>1</td><td>1</td><td>Digital Local Loop-back Mode</td></tr></table></td></tr>
<tr><td>3</td><td>LLB_n</td><td>R/W</td><td>Loop-Back Select - LLB Bit-field - Channel_n:
See the table (above) for RLB_n.</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	E3_n	R/W	**E3 Mode Select - Channel_n:** This READ/WRITE bit-field, along with Bit 1 (STS-1/$\overline{DS3}$_n) within this register, is used to configure a given channel into either the DS3, E3 or STS-1 Modes. 0 - Configures Channel_n to operate in either the DS3 or STS-1 Modes, depending upon the state of Bit 1 (STS-1/$\overline{DS3}$_n) within this same register. 1- Configures Channel_n to operate in the E3 Mode.
1	STS-1/$\overline{DS3}$_n	R/W	**STS-1/DS3 Mode Select - Channel_n:** This READ/WRITE bit-field, along with Bit 2 (E3_n) is used to configure a given channel into either the DS3, E3 or STS-1 Modes. This bit-field is ignored if Bit 2 (E3_n) has been set to "1". If Bit 2 (E3_n) is a 0: 0 - Configures Channel_n to operate in the DS3 Mode. 1 - Configures Channel_n to operate in the STS-1 Mode .
0	SR/$\overline{DR}$_n	R/W	**Single-Rail/Dual-Rail Select - Channel_n:** This READ/WRITE bit-field is used to configure Channel_n to operate in either the Single-Rail or Dual-Rail Mode. If the user configures the Channel to operate in the Single-Rail Mode, the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks (within Channel_n) will be enabled. • The Transmit Section of Channel_n will accept **all** of the outbound data (from the System-side Equipment) via the TxPOS_n input pin. • The Receive Section of each channel will output all of the recovered data (to the System-side Equipment) via the RxPOS_n output pin. • The corresponding RNEG/LCV_n output pin will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin for Channel_n. If the user configures Channel_n to operate in the Dual-Rail Mode, the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks of Channel_n will be disabled. • The Transmit Section of Channel_n will be configured to accept positive-polarity data via the TxPOS_n input pin and negative-polarity data via the TxNEG_n input pin. • The Receive Section of Channel_n will pulse the RxPOS_n output pin "High" (for one period of RCLK_n) for each time a positive-polarity pulse is received via the RTIP_n/RRING_n input pins. Likewise, the Receive Section of each channel will pulse the RxNEG_n output pin "High" (for one period of RxCLK_n) for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. 0 - Configures Channel_n to operate in the Dual-Rail Mode. 1 - Configures Channel_n to operate in the Single-Rail Mode.

TABLE 38: XRT75R12D REGISTER MAP SHOWING JITTER ATTENUATOR CONTROL REGISTERS (JA_N)

TABLE 39: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
				R/W	R/W	R/W	R/W

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Reserved		
3	JA RESET Ch_n	R/W	**Jitter Attenuator RESET - Channel_n:** Writing a "0 to 1" transition within this bit-field will configure the Jitter Attenuator (within Channel_n) to execute a RESET operation. Whenever the user executes a RESET operation, then following will occur. • The READ and WRITE pointers (within the Jitter Attenuator FIFO) will be reset to their default values. • The contents of the Jitter Attenuator FIFO will be flushed. ***NOTE:*** *The user must follow up any "0 to 1" transition with the appropriate write operate to set this bit-field back to "0", in order to resume normal operation with the Jitter Attenuator.*
2	JA1 Ch_n	R/W	**Jitter Attenuator Configuration Select Input - Bit 1:** This READ/WRITE bit-field, along with Bit 0 (JA0 Ch_n) is used to do any of the following. • To enable or disable the Jitter Attenuator corresponding to Channel_n. • To select the FIFO Depth for the Jitter Attenuator within Channel_n. The relationship between the settings of these two bit-fields and the Enable/Disable States, and FIFO Depths is presented below.

JA0	JA1	Jitter Attenuator Mode
0	0	FIFO Depth = 16 bits
0	1	FIFO Depth = 32 bits
1	0	Disabled
1	1	Disabled

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	JA in Tx Path Ch_n	R/W	**Jitter Attenuator in Transmit/Receive Path Select Bit:** This input pin is used to configure the Jitter Attenuator (within Channel_n) to operate in either the Transmit or Receive path, as described below. 0 - Configures the Jitter Attenuator (within Channel_n) to operate in the Receive Path. 1 - Configures the Jitter Attenuator (within Channel_n) to operate in the Transmit Path.
0	JA0 Ch_n	R/W	**Jitter Attenuator Configuration Select Input - Bit 0:** See the description for Bit 2 (JA1 Ch_n).

TABLE 40: XRT75R12D REGISTER MAP SHOWING ERROR COUNTER MSBYTE REGISTERS (EM_N)

ADDRESS LOCATION	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 41: ERROR COUNTER MSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0XMA

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Msb							9th bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TABLE 42: XRT75R12D REGISTER MAP SHOWING ERROR COUNTER LSBYTE REGISTERS (EL_N)

ADDRESS LOCATION	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 43: ERROR COUNTER LSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0XMB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
8th bit							Ls bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TABLE 44: XRT75R12D REGISTER MAP SHOWING ERROR COUNTER HOLDING REGISTERS (EH_N)

ADDRESS LOCATION	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN

ADDRESS LOCATION	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 45: ERROR COUNTER HOLDING REGISTER - CHANNEL N ADDRESS LOCATION = 0XMC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Msb							Ls bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each channel contains a dedicated 16 bit PRBS error counter. When enabled this counter will accumulate PRBS errors (as well as excess zeros and LCVs). The LS byte will "carry" a one over to the MS byte each time it rolls over from 255 to zero until the MS byte also reaches 255. When both counters reach 255, no further errors will be accumulated and "all ones" will signify an overflow condition.

The counter can be read while in the active count mode. Either register may be read "on the fly" and the other byte will be simultaneously transferred into the channel's Error Holding register. The holding register may then be read to supply the Host with a correct 16 bit count (as of the instant of reading). With this mechanism, the Host could rapidly cycle thru reading all twelve counters in order (storing the read byte in scratch RAM) and then come back and read the second byte from each holding register to form the 16 bit accumulation in the Host system.

8.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE LIU

The LIU with D-SYNC is very similar to the non D-SYNC LIU in that they both contain Jitter Attenuator blocks within each channel. They are also pin to pin compatible with each other. However, the Jitter Attenuators within the D-SYNC have some enhancements over and above those within the non D-SYNC device. The Jitter Attenuator blocks will support all of the modes and features that exist in the non D-SYNC device and in addition they also support a SONET/SDH De-Sync Mode.

NOTE: *The "D" suffix within the part number stands for "De-Sync".*

The SONET/SDH De-Sync feature of the Jitter Attenuator blocks permits the user to design a SONET/SDH PTE (Path Terminating Equipment) that will comply with all of the following Intrinsic Jitter and Wander requirements.

- **For SONET Applications**
  - Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 Applications)
  - ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement
- **For SDH Applications**
  - Jitter and Wander Generation Requirements per ITU-T G.783 (for DS3 and E3 Applications)

Specifically, if the user designs in the LIU along with a SONET/SDH Mapper IC (which can be realized as either a standard product or as a custom logic solution, in an ASIC or FPGA), then the following can be accomplished.

- The Mapper can receive an STS-N or an STM-M signal (which is carrying asynchronously-mapped DS3 and/or E3 signals) and byte de-interleave this data into N STS-1 or 3*M VC-3 signals
- The Mapper will then terminate these STS-1 or VC-3 signals and will de-map out this DS3 or E3 data from the incoming STS-1 SPEs or VC-3s, and output this DS3 or E3 to the DS3/E3 Facility-side towards the LIU
- This DS3 or E3 signal (as it is output from these Mapper devices) will contain a large amount of intrinsic jitter and wander due to (1) the process of asynchronously mapping a DS3 or E3 signal into a SONET or SDH signal, (2) the occurrence of Pointer Adjustments within the SONET or SDH signal (transporting these DS3 or E3 signals) as it traverses the SONET/SDH network, and (3) clock gapping.
- When the LIU has been configured to operate in the "SONET/SDH De-Sync" Mode, then it will (1) accept this jittery DS3 or E3 clock and data signal from the Mapper device (via the Transmit System-side interface) and (2) through the Jitter Attenuator, the LIU will reduce the Jitter and Wander amplitude within these DS3 or E3 signals such that they (when output onto the line) will comply with the above-mentioned intrinsic jitter and wander specifications.

8.1 *BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS*

This section provides an in-depth discussion on the mechanisms that will cause Jitter and Wander within a DS3 or E3 signal that is being transported across a SONET or SDH Network. A lot of this material is introductory, and can be skipped by the engineer that is already experienced in SONET/SDH designs.

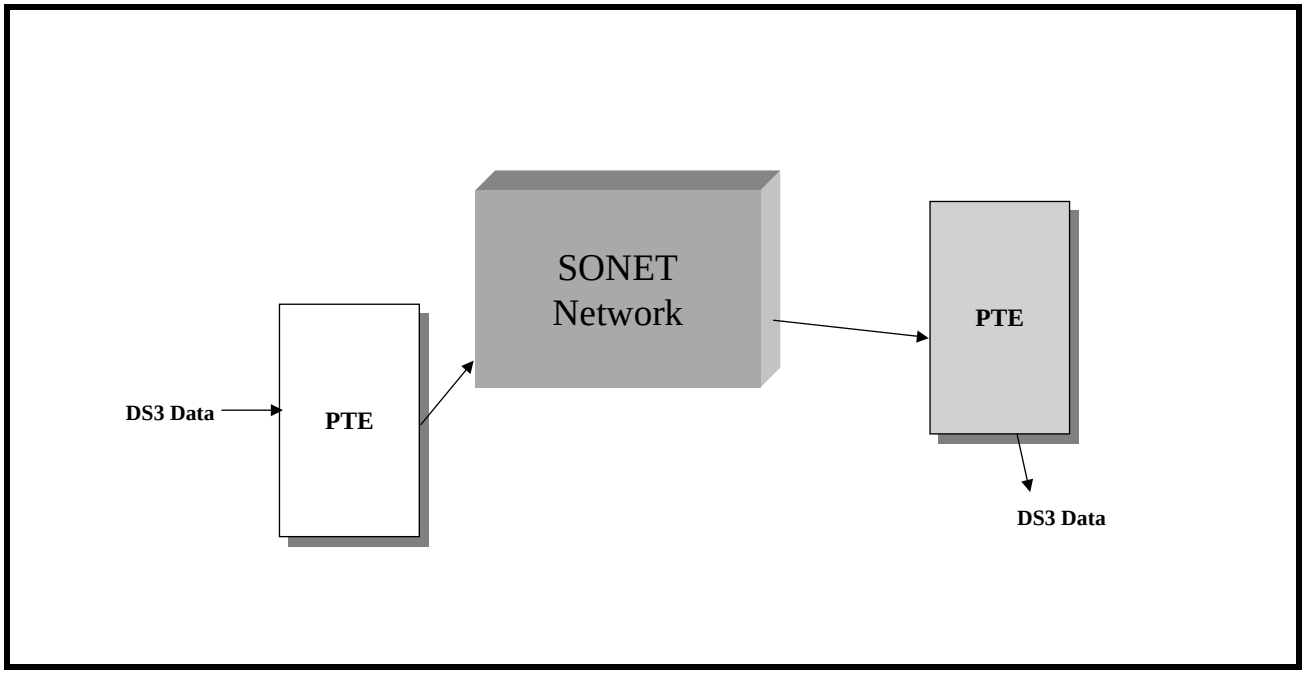
In the wide-area network (WAN) in North America it is often necessary to transport a DS3 signal over a long distance (perhaps over a thousand miles) in order to support a particular service. Now rather than realizing this transport of DS3 data, by using over a thousand miles of coaxial cable (interspaced by a large number of DS3 repeaters) a common thing to do is to route this DS3 signal to a piece of equipment (such as a Terminal MUX, which in the "SONET Community" is known as a PTE or Path Terminating Equipment). This Terminal MUX will asynchronously map the DS3 signal into a SONET signal. At this point, the SONET network will now transport this asynchronously mapped DS3 signal from one PTE to another PTE (which is located at the other end of the SONET network). Once this SONET signal arrives at the remote PTE, this DS3 signal will then be extracted from the SONET signal, and will be output to some other DS3 Terminal Equipment for further processing.

Similar things are done outside of North America. In this case, this DS3 or E3 signal is routed to a PTE, where it is asynchronously mapped into an SDH signal. This asynchronously mapped DS3 or E3 signal is then transported across the SDH network (from one PTE to the PTE at the other end of the SDH network). Once

this SDH signal arrives at the remote PTE, this DS3 or E3 signal will then be extracted from the SDH signal, and will be output to some other DS3/E3 Terminal Equipment for further processing.

Figure 37 presents an illustration of this approach to transporting DS3 data over a SONET Network

FIGURE 37. A SIMPLE ILLUSTRATION OF A DS3 SIGNAL BEING MAPPED INTO AND TRANSPORTED OVER THE SONET NETWORK



As mentioned above a DS3 or E3 signal will be asynchronously mapped into a SONET or SDH signal and then transported over the SONET or SDH network. At the remote PTE this DS3 or E3 signal will be extracted (or de-mapped) from this SONET or SDH signal, where it will then be routed to DS3 or E3 terminal equipment for further processing.

In order to insure that this "de-mapped" DS3 or E3 signal can be routed to any industry-standard DS3 or E3 terminal equipment, without any complications or adverse effect on the network, the Telcordia and ITU-T standard committees have specified some limits on both the Intrinsic Jitter and Wander that may exist within these DS3 or E3 signals as they are de-mapped from SONET/SDH. As a consequence, all PTEs that maps and de-mapped DS3/E3 signals into/from SONET/SDH must be designed such that the DS3 or E3 data that is de-mapped from SONET/SDH by these PTEs must meet these Intrinsic Jitter and Wander requirements.

As mentioned above, the LIU can assist the System Designer (of SONET/SDH PTE) by ensuring that their design will meet these Intrinsic Jitter and Wander requirements.

This section of the data sheet will present the following information to the user.

- Some background information on Mapping DS3/E3 signals into SONET/SDH and de-mapping DS3/E3 signals from SONET/SDH.
- A brief discussion on the causes of jitter and wander within a DS3 or E3 signal that mapped into a SONET/SDH signal, and is transported across the SONET/SDH Network.
- A brief review of these Intrinsic Jitter and Wander requirements in both SONET and SDH applications.
- A brief review on the Intrinsic Jitter and Wander measurement results (of a de-mapped DS3 or E3 signal) whenever the LIU device is used in a system design.
- A detailed discussion on how to design with and configure the LIU device such that the end-system will meet these Intrinsic Jitter and Wander requirements.

In a SONET system, the relevant specification requirements for Intrinsic Jitter and Wander (within a DS3 signal that is mapped into and then de-mapped from SONET) are listed below.

- Telcordia GR-253-CORE Category I Intrinsic Jitter Requirements for DS3 Applications (Section 5.6), and
- ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement

In general, there are three (3) sources of Jitter and Wander within an asynchronously-mapped DS3 signal that the system designer must be aware of. These sources are listed below.

- Mapping/De-Mapping Jitter
- Pointer Adjustments
- Clock Gapping

Each of these sources of jitter/wander will be defined and discussed in considerable detail within this Section. In order to accomplish all of this, this particular section will discuss all of the following topics in details.

- How DS3 data is mapped into SONET, and how this mapping operation contributes to Jitter and Wander within this "eventually de-mapped" DS3 signal.
- How this asynchronously-mapped DS3 data is transported throughout the SONET Network, and how occurrences on the SONET network (such as pointer adjustments) will further contributes to Jitter and Wander within the "eventually de-mapped" DS3 signal.
- A review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications
- A review of the DS3 Wander requirements per ANSI T1.105.03b-1997
- A review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application
- An in-depth discussion on how to design with and configure the LIU to permit the system to the meet the above-mentioned Intrinsic Jitter and Wander requirements

NOTE: *An in-depth discussion on SDH De-Sync Applications will be presented in the next revision of this data sheet.*

8.2 *MAPPING/DE-MAPPING JITTER/WANDER*

Mapping/De-Mapping Jitter (or Wander) is defined as that intrinsic jitter (or wander) that is induced into a DS3 signal by the "Asynchronous Mapping" process. This section will discuss all of the following aspects of Mapping/De-Mapping Jitter.

- How DS3 data is mapped into an STS-1 SPE
- How frequency offsets within either the DS3 signal (being mapped into SONET) or within the STS-1 signal itself contributes to intrinsic jitter/wander within the DS3 signal (being transported via the SONET network).

8.2.1 HOW DS3 DATA IS MAPPED INTO SONET

Whenever a DS3 signal is asynchronously mapped into SONET, this mapping is typically accomplished by a PTE accepting DS3 data (from some remote terminal) and then loading this data into certain bit-fields within a given STS-1 SPE (or Synchronous Payload Envelope). At this point, this DS3 signal has now been asynchronously mapped into an STS-1 signal. In most applications, the SONET Network will then take this particular STS-1 signal and will map it into "higher-speed" SONET signals (e.g., STS-3, STS-12, STS-48, etc.) and will then transport this asynchronously mapped DS3 signal across the SONET network, in this manner. As this "asynchronously-mapped" DS3 signal approaches its "destination" PTE, this STS-1 signal will eventually be de-mapped from this STS-N signal. Finally, once this STS-1 signal reaches the "destination" PTE, then this asynchronously-mapped DS3 signal will be extracted from this STS-1 signal.

8.2.1.1 *A Brief Description of an STS-1 Frame*

In order to be able to describe how a DS3 signal is asynchronously mapped into an STS-1 SPE, it is important to define and understand all of the following.

- The STS-1 frame structure
- The STS-1 SPE (Synchronous Payload Envelope)

- Telcordia GR-253-CORE's recommendation on mapping DS3 data into an STS-1 SPE

An STS-1 frame is a data-structure that consists of 810 bytes (or 6480 bits). A given STS-1 frame can be viewed as being a 9 row by 90 byte column array (making up the 810 bytes). The frame-repetition rate (for an STS-1 frame) is 8000 frames/second. Therefore, the bit-rate for an STS-1 signal is (6480 bits/frame * 8000 frames/sec =) 51.84Mbps.

A simple illustration of this SONET STS-1 frame is presented below in Figure 38.

FIGURE 38. A SIMPLE ILLUSTRATION OF THE SONET STS-1 FRAME

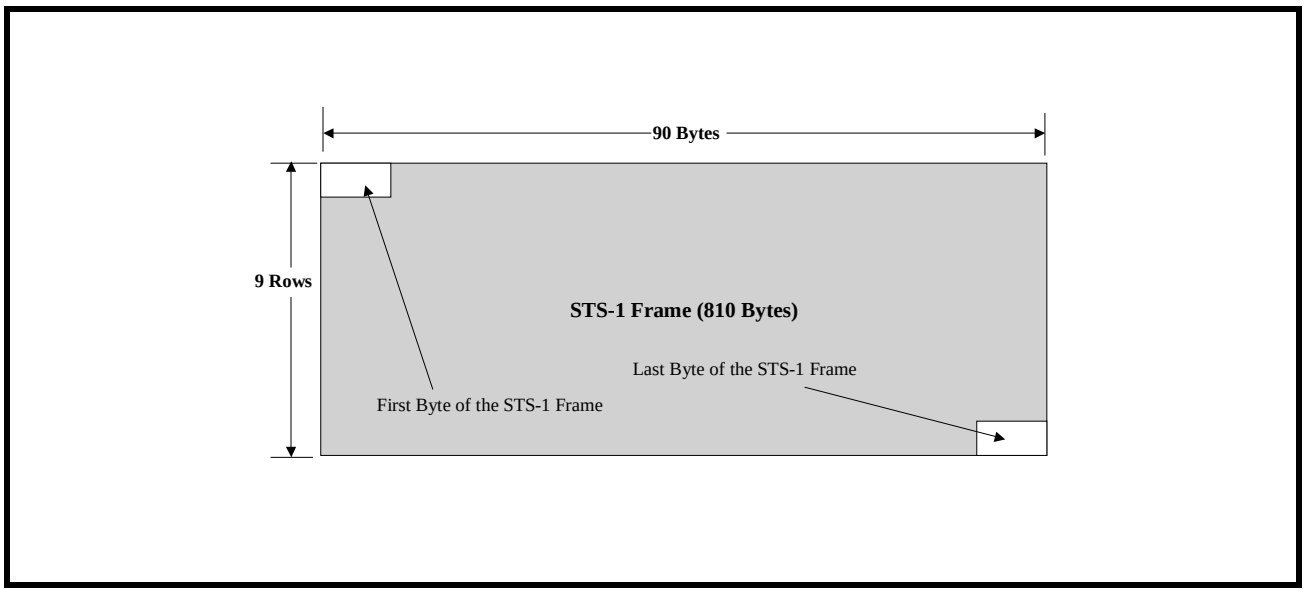


Figure 38 indicates that the very first byte of a given STS-1 frame (to be transmitted or received) is located in the extreme upper left hand corner of the 90 column by 9 row array, and that the very last byte of a given STS-1 frame is located in the extreme lower right-hand corner of the frame structure. Whenever a Network Element transmits a SONET STS-1 frame, it starts by transmitting all of the data, residing within the top row of the STS-1 frame structure (beginning with the left-most byte, and then transmitting the very next byte, to the right). After the Network Equipment has completed its transmission of the top or first row, it will then proceed to transmit the second row of data (again starting with the left-most byte, first). Once the Network Equipment has transmitted the last byte of a given STS-1 frame, it will proceed to start transmitting the very next STS-1 frame.

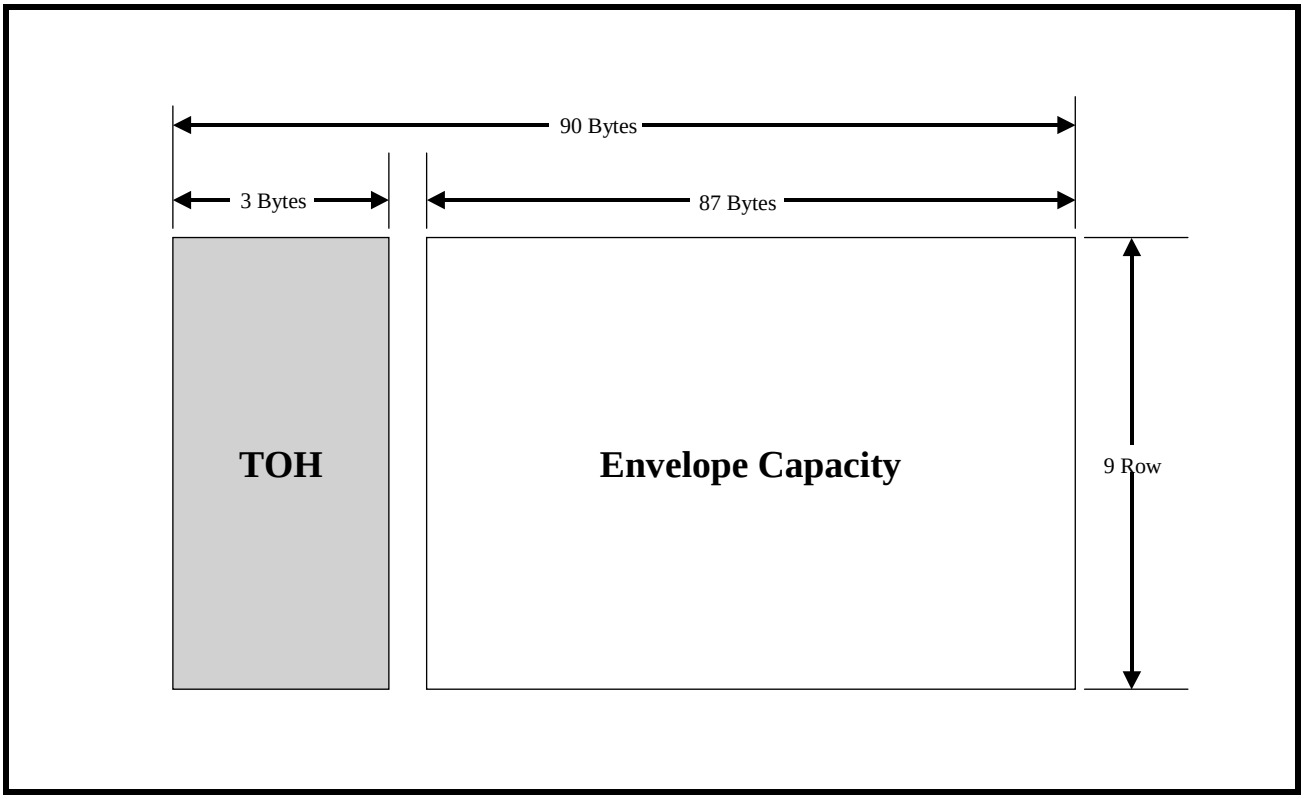
The illustration of the STS-1 frame (in Figure 38) is very simplistic, for multiple reasons. One major reason is that the STS-1 frame consists of numerous types of bytes. For the sake of discussion within this data sheet, the STS-1 frame will be described as consisting of the following types (or groups) of bytes.

- The Transport Overheads (or TOH) Bytes
- The Envelope Capacity Bytes

8.2.1.1.1 The Transport Overhead (TOH) Bytes

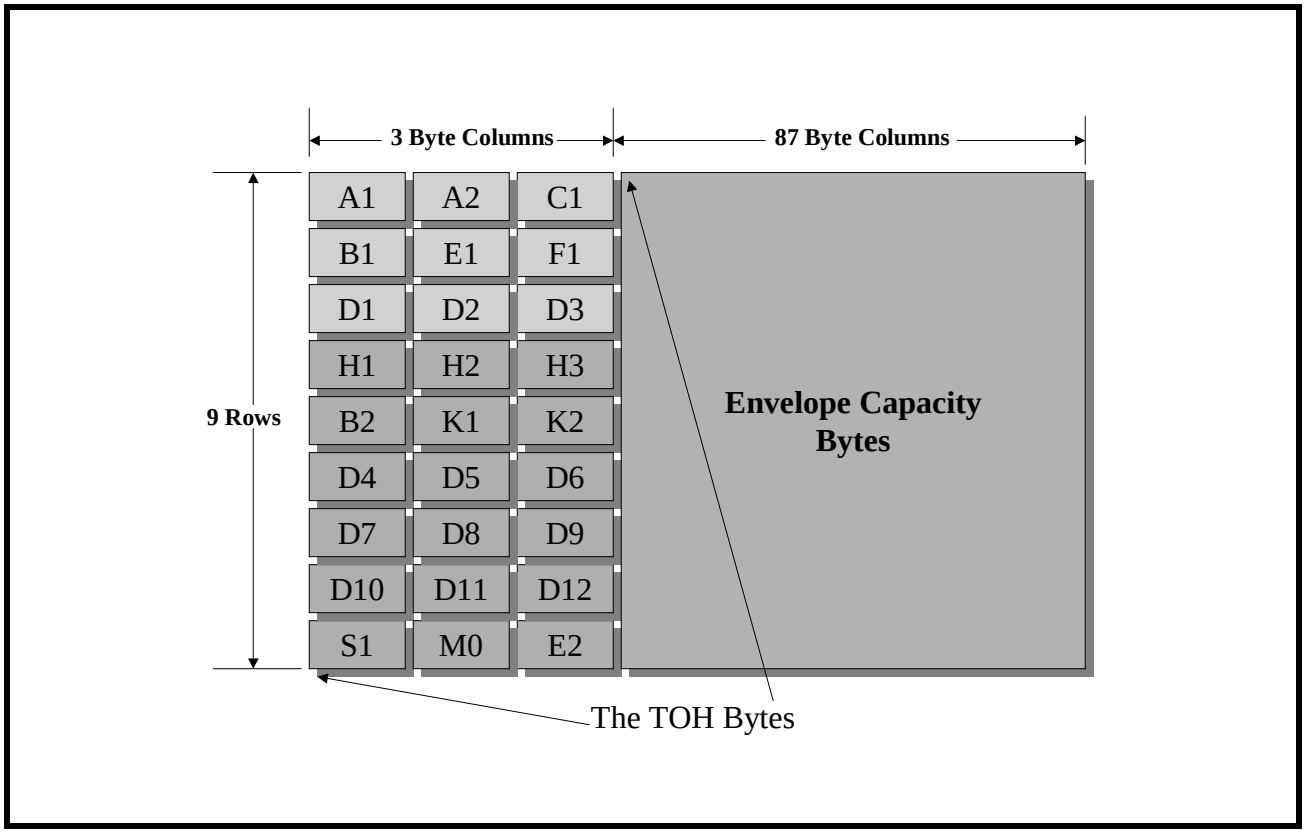
The Transport Overhead or TOH bytes occupy the very first three (3) byte columns within each STS-1 frame. Figure 39 presents another simple illustration of an STS-1 frame structure. However, in this case, both the TOH and the Envelope Capacity bytes are designated in this Figure.

FIGURE 39. A SIMPLE ILLUSTRATION OF THE STS-1 FRAME STRUCTURE WITH THE TOH AND THE ENVELOPE CAPACITY BYTES DESIGNATED



Since the TOH bytes occupy the first three byte columns of each STS-1 frame, and since each STS-1 frame consists of nine (9) rows, then we can state that the TOH (within each STS-1 frame) consists of 3 byte columns x 9 rows = 27 bytes. The byte format of the TOH is presented below in Figure 40.

FIGURE 40. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



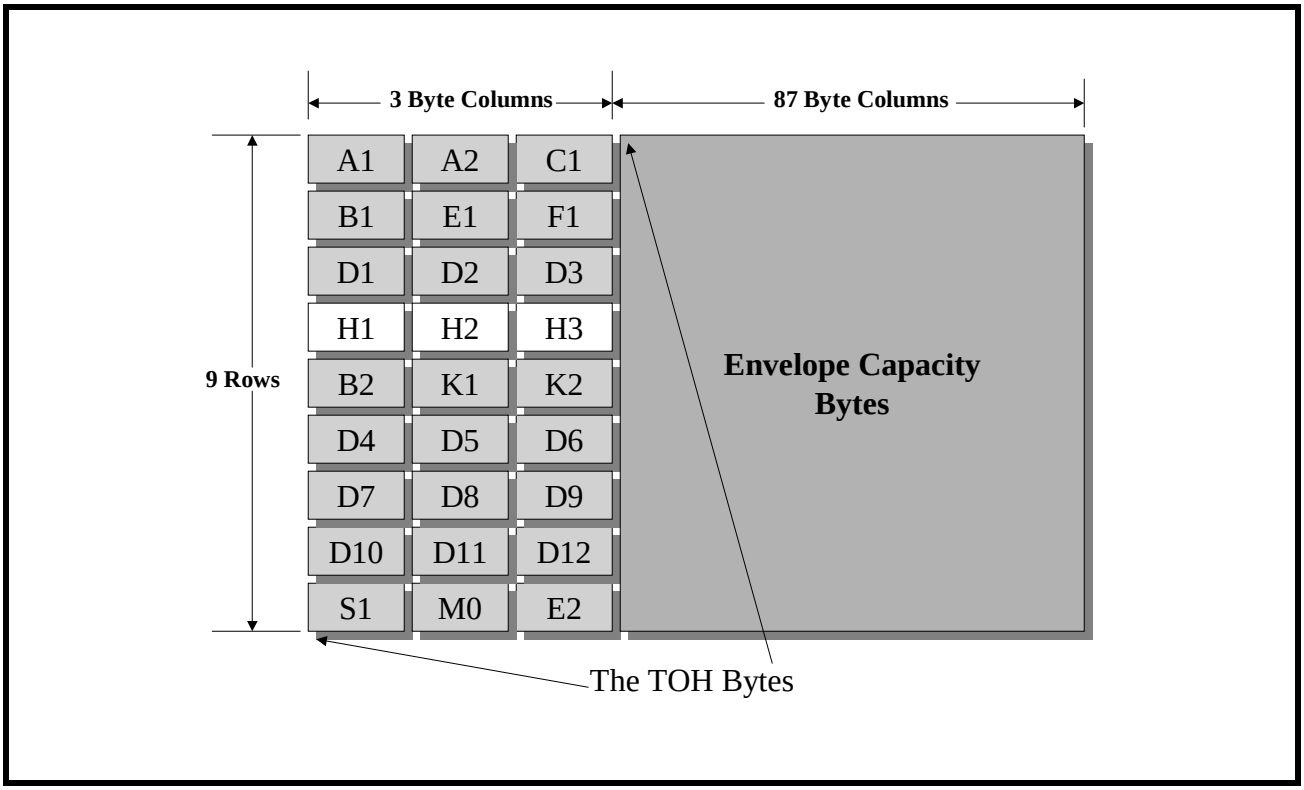
In general, the role/purpose of the TOH bytes is to fulfill the following functions.

- To support STS-1 Frame Synchronization
- To support Error Detection within the STS-1 frame
- To support the transmission of various alarm conditions such as RDI-L (Line - Remote Defect Indicator) and REI-L (Line - Remote Error Indicator)
- To support the Transmission and Reception of "Section Trace" Messages
- To support the Transmission and Reception of OAM&P Messages via the DCC Bytes (Data Communication Channel bytes - D1 through D12 byte)

The roles of most of the TOH bytes is beyond the scope of this Data Sheet and will not be discussed any further. However, there are a three TOH bytes that are important from the stand-point of this data sheet, and will discussed in considerable detail throughout this document. These are the H1 and H2 (e.g., the SPE Pointer) bytes and the H3 (e.g., the Pointer Action) byte.

Figure 41 presents an illustration of the Byte-Format of the TOH within an STS-1 Frame, with the H1, H2 and H3 bytes highlighted.

FIGURE 41. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



Although the role of the H1, H2 and H3 bytes will be discussed in much greater detail in “Section 8.3, Jitter/ Wander due to Pointer Adjustments” on page 98. For now, we will simply state that the role of these bytes is two-fold.

- To permit a given PTE (Path Terminating Equipment) that is receiving an STS-1 data to be able to locate the STS-1 SPE (Synchronous Payload Envelope) within the Envelope Capacity of this incoming STS-1 data stream and,
- To inform a given PTE whenever Pointer Adjustment and NDF (New Data Flag) events occur within the incoming STS-1 data-stream.

8.2.1.1.2 The Envelope Capacity Bytes within an STS-1 Frame

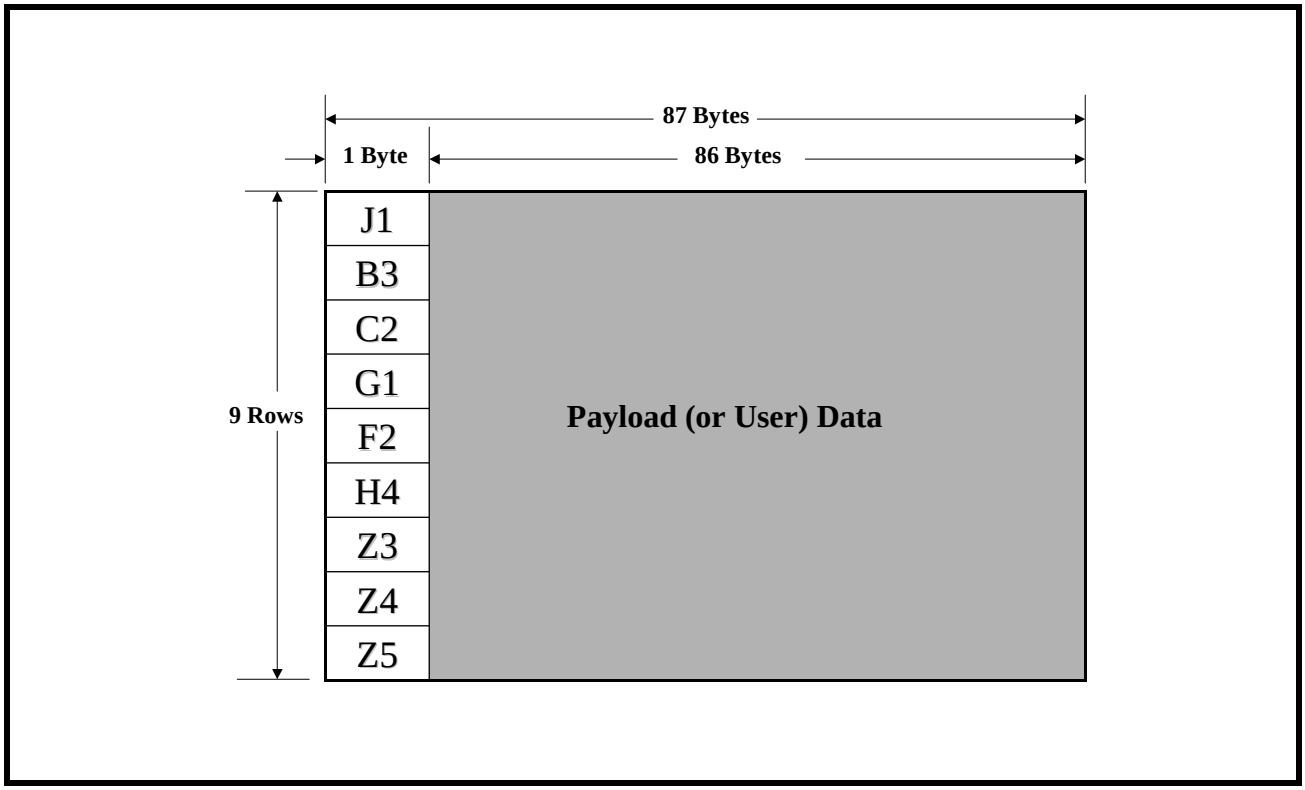
In general, the Envelope Capacity Bytes are any bytes (within an STS-1 frame) that exist outside of the TOH bytes. In short, the Envelope Capacity contains the STS-1 SPE (Synchronous Payload Envelope). In fact, every single byte that exists within the Envelope Capacity also exists within the STS-1 SPE. The only difference that exists between the "Envelope Capacity" as defined in Figure 40 and Figure 41 above and the STS-1 SPE is that the Envelope Capacity is aligned with the STS-1 framing boundaries and the TOH bytes; whereas the STS-1 SPE is NOT aligned with the STS-1 framing boundaries, nor the TOH bytes.

The STS-1 SPE is an "87 byte column x 9 row" data-structure (which is the exact same size as is the Envelope Capacity) that is permitted to "float" within the "Envelope Capacity". As a consequence, the STS-1 SPE (within an STS-1 data-stream) will typically straddle across an STS-1 frame boundary.

8.2.1.1.3 The Byte Structure of the STS-1 SPE

As mentioned above, the STS-1 SPE is an 87 byte column x 9 row structure. The very first column within the STS-1 SPE consists of some overhead bytes which are known as the "Path Overhead" (or POH) bytes. The remaining portions of the STS-1 SPE is available for "user" data. The Byte Structure of the STS-1 SPE is presented below in Figure 42.

FIGURE 42. ILLUSTRATION OF THE BYTE STRUCTURE OF THE STS-1 SPE



In general, the role/purpose of the POH bytes is to fulfill the following functions.

- To support error detection within the STS-1 SPE
- To support the transmission of various alarm conditions such as RDI-P (Path - Remote Defect Indicator) and REI-P (Path - Remote Error Indicator)
- To support the transmission and reception of "Path Trace" Messages

The role of the POH bytes is beyond the scope of this data sheet and will not be discussed any further.

8.2.1.2 *Mapping DS3 data into an STS-1 SPE*

Now that we have defined the STS-1 SPE, we can now describe how a DS3 signal is mapped into an STS-1 SPE. As mentioned above, the STS-1 SPE is basically an 87 byte column x 9 row structure of data. The very first byte column (e.g., in all 9 bytes) consists of the POH (Path Overhead) bytes. All of the remaining bytes within the STS-1 SPE is simply referred to as "user" or "payload" data because this is the portion of the STS-1 signal that is used to transport "user data" from one end of the SONET network to the other. Telcordia GR-253-CORE specifies the approach that one must use to asynchronously map DS3 data into an STS-1 SPE. In short, this approach is presented below in Figure 43.

FIGURE 43. AN ILLUSTRATION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW MAP DS3 DATA INTO AN STS-1 SPE

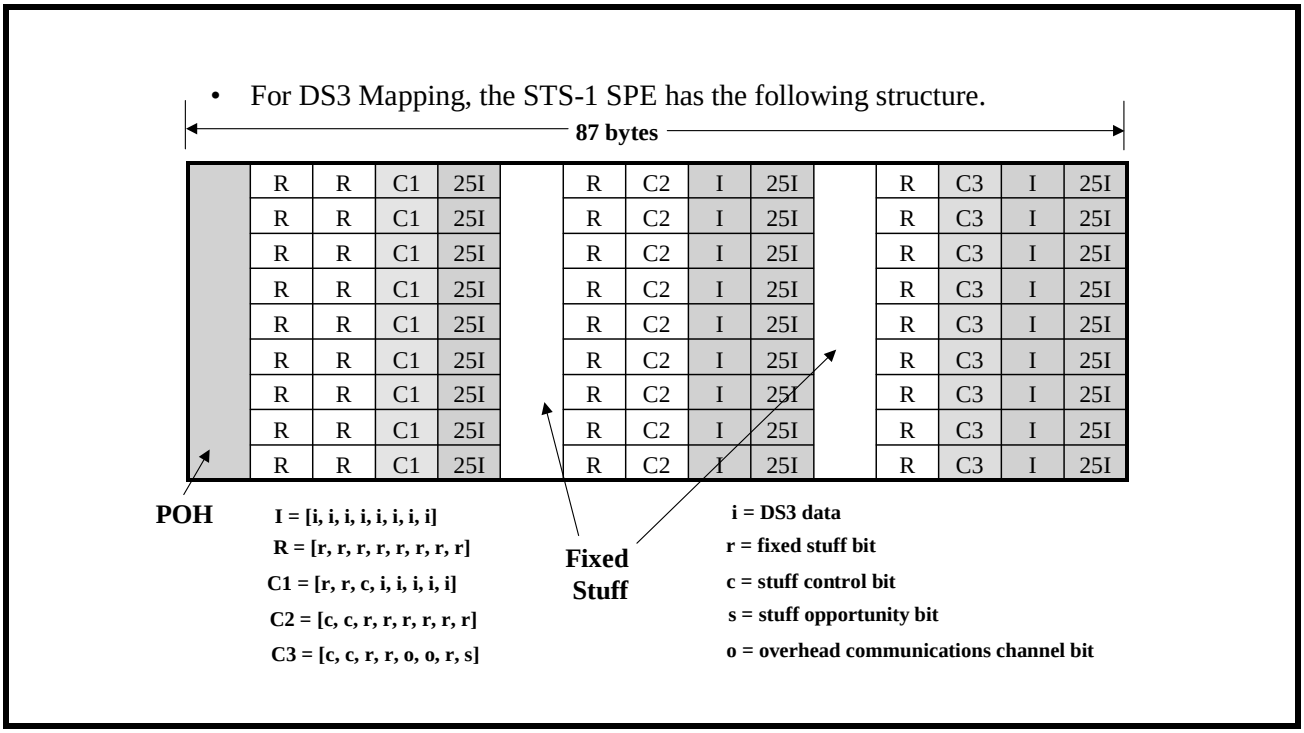


Figure 43 was copied directly out of Telcordia GR-253-CORE. However, this figure can be simplified and redrawn as depicted below in Figure 44.

FIGURE 44. A SIMPLIFIED "BIT-ORIENTED" VERSION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW TO MAP DS3 DATA INTO AN STS-1 SPE

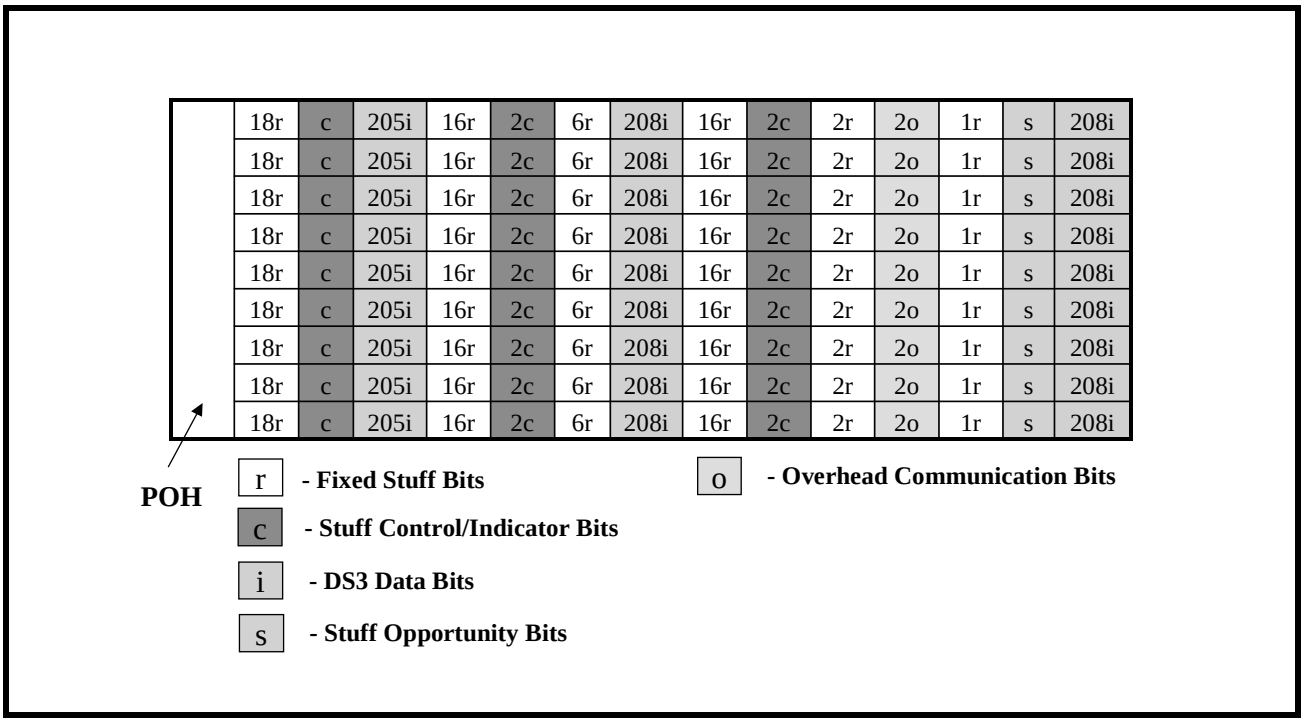


Figure 44 presents an alternative illustration of Telcordia GR-253-CORE's recommendation on how to asynchronously map DS3 data into an STS-1 SPE. In this case, the STS-1 SPE bit-format is expressed purely in the form of "bit-types" and "numbers of bits within each of these types of bits". If one studies this figure closely he/she will notice that this is the same "87 byte column x 9 row" structure that we have been talking about when defining the STS-1 SPE. However, in this figure, the "user-data" field is now defined and is said to consist of five (5) different types of bits. Each of these bit-types play a role when asynchronously mapping a DS3 signal into an STS-1 SPE. Each of these types of bits are listed and described below.

Fixed Stuff Bits

Fixed Stuff bits are simply "space-filler" bits that simply occupy space within the STS-1 SPE. These bit-fields have no functional role other than "space occupation". Telcordia GR-253-CORE does not define any particular value that these bits should be set to. Each of the 9 rows, within the STS-1 SPE will contain 59 of these "fixed stuff" bits.

DS3 Data Bits

The DS3 Data-Bits are (as its name implies) used to transport the DS3 data-bits within the STS-1 SPE. If the STS-1 SPE is transporting a framed DS3 data-stream, then these DS3 Data bits will carry both the "DS3 payload data" and the "DS3 overhead bits". Each of the 9 rows, within the STS-1 SPE will contain 621 of these "DS3 Data bits". This means that each STS-1 SPE contains 5,589 of these DS3 Data bit-fields.

Stuff Opportunity Bits

The "Stuff" Opportunity bits will function as either a "stuff" (or junk) bit, or it will carry a DS3 data-bit. The decision as to whether to have a "Stuff Opportunity" bit transport a "DS3 data-bit" or a "stuff" bit depends upon the "timing differences" between the DS3 data that is being mapped into the STS-1 SPE and the timing source that is driving the STS-1 circuitry within the PTE.

As will be described later on, these "Stuff Opportunity" Bits play a very important role in "frequency-justifying" the DS3 data that is being mapped into the STS-1 SPE. These "Stuff Opportunity" bits also play a critical role in inducing Intrinsic Jitter and Wander within the DS3 signal (as it is de-mapped by the remote PTE).

Each of the 9 rows, within the STS-1 SPE consists of one (1) Stuff Opportunity bit. Hence, there are a total of nine "Stuff Opportunity" bits within each STS-1 SPE.

Stuff Control/Indicator Bits

Each of the nine (9) rows within the STS-1 SPE contains five (5) Stuff Control/Indicator bits. The purpose of these "Stuff Control/Indicator" bits is to indicate (to the de-mapping PTE) whether the "Stuff Opportunity" bits (that resides in the same row) is a "Stuff" bit or is carrying a DS3 data bit.

If all five of these "Stuff Control/Indicator" bits, within a given row are set to "0", then this means that the corresponding "Stuff Opportunity" bit (e.g., the "Stuff Opportunity" bit within the same row) is carrying a DS3 data bit.

Conversely, if all five of these "Stuff Control/Indicator" bits, within a given row are set to "1" then this means that the corresponding "Stuff Opportunity" bit is carrying a "stuff" bit.

Overhead Communication Bits

Telcordia GR-253-CORE permits the user to use these two bits (for each row) as some sort of "Communications" bit. Some Mapper devices, such as the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-1 Mapper and the XRT94L33 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper IC (both from Exar Corporation) do permit the user to have access to these bit-fields.

However, in general, these particular bits can also be thought of as "Fixed Stuff" bits, that mostly have a "space occupation" function.

8.2.2 DS3 Frequency Offsets and the Use of the "Stuff Opportunity" Bits

In order to fully convey the role that the "stuff-opportunity" bits play, when mapping DS3 data into SONET, we will present a detailed discussion of each of the following "Mapping DS3 into STS-1" scenarios.

- The Ideal Case (e.g., with no frequency offsets)
- The 44.736Mbps + 1 ppm Case

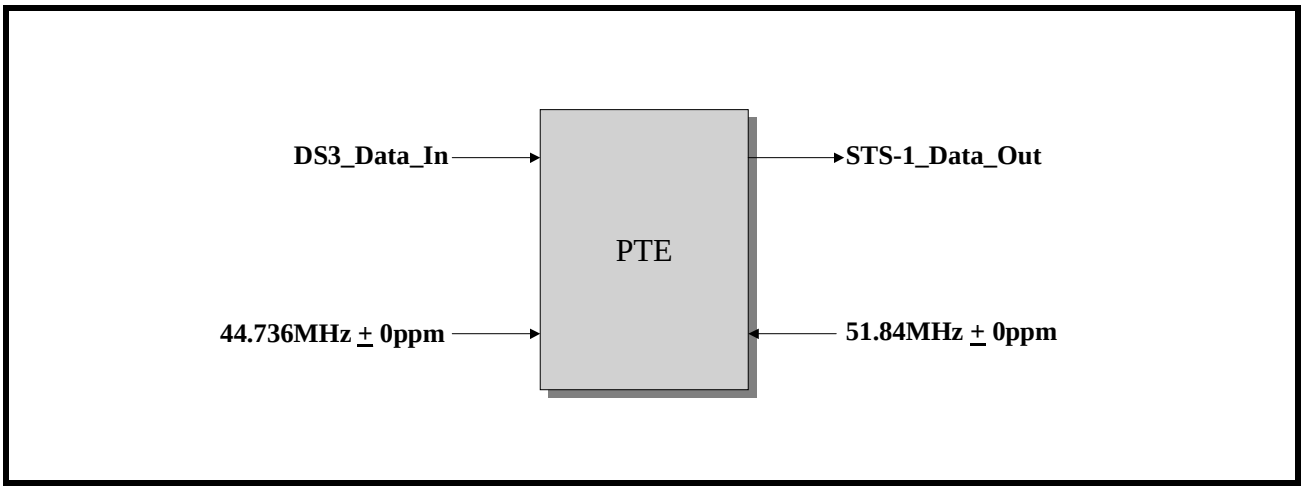
- The 44.736MHz - 1ppm Case

Throughout each of these cases, we will discuss how the resulting "bit-stuffing" (that was done when mapping the DS3 signal into SONET) affects the amount of intrinsic jitter and wander that will be present in the DS3 signal, once it is ultimately de-mapped from SONET.

8.2.2.1 *The Ideal Case for Mapping DS3 data into an STS-1 Signal (e.g., with no Frequency Offsets)*

Let us assume that we are mapping a DS3 signal, which has a bit rate of exactly 44.736Mbps (with no frequency offset) into SONET. Further, let us assume that the SONET circuitry within the PTE is clocked at exactly 51.84MHz (also with no frequency offset), as depicted below.

FIGURE 45. A SIMPLE ILLUSTRATION OF A DS3 DATA-STREAM BEING MAPPED INTO AN STS-1 SPE, VIA A PTE



Given the above-mentioned assumptions, we can state the following.

- The DS3 data-stream has a bit-rate of exactly 44.736Mbps
- The PTE will create 8000 STS-1 SPE's per second
- In order to properly map a DS3 data-stream into an STS-1 data-stream, then each STS-1 SPE must carry (44.736Mbps/8000 =) 5592 DS3 data bits.

Is there a Problem?

According to Figure 44, each STS-1 SPE only contains 5589 bits that are specifically designated for "DS3 data bits". In this case, each STS-1 SPE appears to be three bits "short".

No there is a Simple Solution

No, earlier we mentioned that each STS-1 SPE consists of nine (9) "Stuff Opportunity" bits. Therefore, these three additional bits (for DS3 data) are obtained by using three of these "Stuff Opportunity" bits. As a consequence, three (3) of these nine (9) "Stuff Opportunity" bits, within each STS-1 SPE, will carry DS3 data-bits. The remaining six (6) "Stuff Opportunity" bits will typically function as "stuff" bits.

In summary, for the "Ideal Case"; where there is no frequency offset between the DS3 and the STS-1 bit-rates, once this DS3 data-stream has been mapped into the STS-1 data-stream, then each and every STS-1 SPE will have the following "Stuff Opportunity" bit utilization.

3 "Stuff Opportunity" bits will carry DS3 data bits.

6 "Stuff Opportunity" bits will function as "stuff" bits

In this case, this DS3 signal (which has now been mapped into STS-1) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination PTE", this PTE will extract (or de-map) this DS3 data-stream from each incoming STS-1 SPE. Now since each and every STS-1 SPE contains exactly 5592 DS3 data bits; then the bit rate of this DS3 signal will be exactly 44.736Mbps (such as it was when it was mapped into SONET, at the "Source" PTE).

As a consequence, no "Mapping/De-Mapping" Jitter or Wander is induced in the "Ideal Case".

8.2.2.2 *The 44.736Mbps + 1ppm Case*

The "above example" was a very ideal case. In reality, there are going to be frequency offsets in both the DS3 and STS-1 signals. For instance Bellcore GR-499-CORE mandates that a DS3 signal have a bit rate of 44.736Mbps ± 20ppm. Hence, the bit-rate of a "Bellcore" compliant DS3 signal can vary from the exact correct frequency for DS3 by as much of 20ppm in either direction. Similarly, many SONET applications mandate that SONET equipment use at least a "Stratum 3" level clock as its timing source. This requirement mandates that an STS-1 signal must have a bit rate that is in the range of 51.84 ± 4.6ppm. To make matters worse, there are also provisions for SONET equipment to use (what is referred to as) a "SONET Minimum Clock" (SMC) as its timing source. In this case, an STS-1 signal can have a bit-rate in the range of 51.84Mbps ± 20ppm.

In order to convey the impact that frequency offsets (in either the DS3 or STS-1 signal) will impose on the bit-stuffing behavior, and the resulting bit-rate, intrinsic jitter and wander within the DS3 signal that is being transported across the SONET network; let us assume that a DS3 signal, with a bit-rate of 44.736Mbps + 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following things will occur.

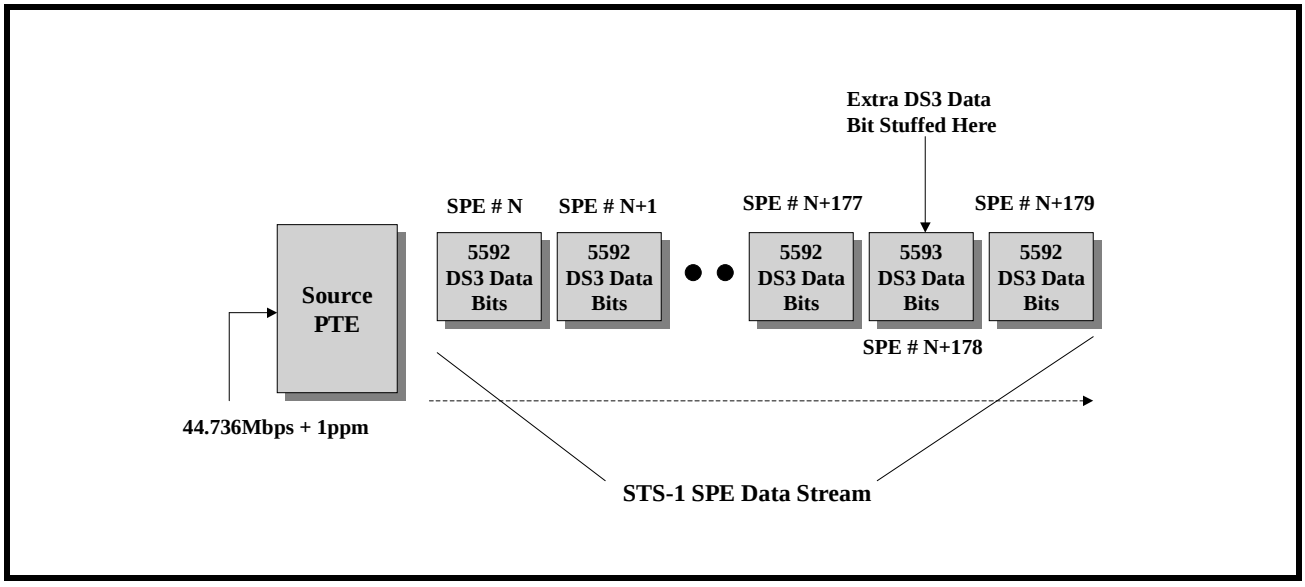
- In general, most of the STS-1 SPE's will each transport 5592 DS3 data bits.
- However, within a "one-second" period, a DS3 signal that has a bit-rate of 44.736Mbps + 1 ppm will deliver approximately 44.7 additional bits (over and above that of a DS3 signal with a bit-rate of 44.736Mbps + 0 ppm). This means that this particular signal will need to "negative-stuff" or map in an additional DS3 data bit every (1/44.736 =) 22.35ms. In other words, this additional DS3 data bit will need to be mapped into about one in every (22.35ms · 8000 =) 178.8 STS-1 SPEs in order to avoid dropping any DS3 data-bits.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps + 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits, as in the "Ideal" case). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need to insert an additional DS3 data bit within this STS-1 SPE. Whenever this occurs, then (for these particular STS-1 SPEs) the SPE will be carrying 5593 DS3 data bits (e.g., 4 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 5 Stuff Opportunity bits are "stuff" bits).

Figure 46 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 46. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE "SOURCE" PTE, WHEN MAPPING IN A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS + 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the "Destination" PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry 5593 DS3 data-bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is greater than 44.736Mbps. These "excursion" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of "mapping/de-mapping" jitter. Since each of these "bit-stuffing" events involve the insertion of one DS3 data bit, we can say that the amplitude of this "mapping/de-mapping" jitter is approximately 1UI-pp. From this point on, we will be referring to this type of jitter (e.g., that which is induced by the mapping and de-mapping process) as "de-mapping" jitter.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

8.2.2.3 *The 44.736Mbps - 1ppm Case*

In this case, let us assume that a DS3 signal, with a bit-rate of 44.736Mbps - 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following this will occur.

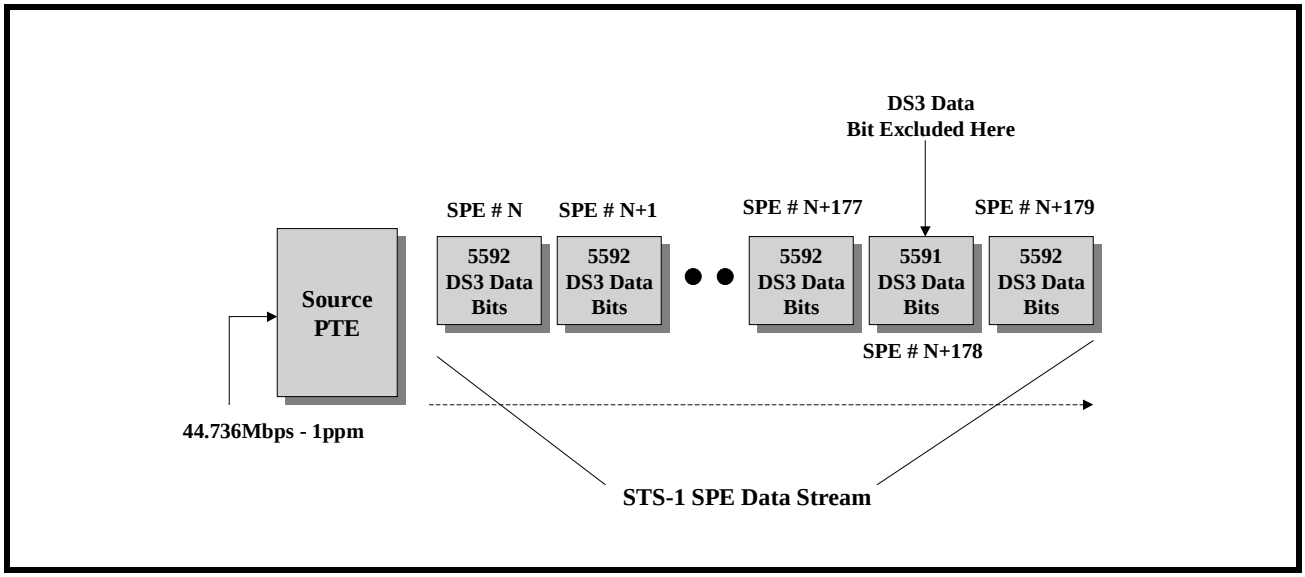
- In general, most of the STS-1 SPEs will each transport 5592 DS3 data bits.
- However, within a "one-second" period a DS3 signal that has a bit-rate of 44.736Mbps - 1ppm will deliver approximately 45 too few bits below that of a DS3 signal with a bit-rate of 44.736Mbps + 0ppm. This means that this particular signal will need to "positive-stuff" or exclude a DS3 data bit from mapping every (1/44.736) = 22.35ms. In other words, we will need to avoid mapping this DS3 data-bit about one in every (22.35ms*8000) = 178.8 STS-1 SPEs.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps - 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need for a "positive-stuffing" event. Whenever these "positive-stuffing" events occur then (for these particular STS-1 SPEs) the SPE will carry only 5591 DS3 data bits (e.g., in this case, only 2 Stuff Opportunity bits will be carrying DS3 data-bits, and the remaining 7 Stuff Opportunity bits are "stuff" bits).

Figure 47 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 47. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE SOURCE PTE, WHEN MAPPING A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS - 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the Destination PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case, most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry only 5591 DS3 data bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is less than 44.736Mbps. These "excursions" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of mapping/de-mapping jitter with an amplitude of approximately 1UI-pp.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

We talked about De-Mapping Jitter, What about De-Mapping Wander?

The Telcordia and Bellcore specifications define "Wander" as "Jitter with a frequency of less than 10Hz". Based upon this definition, the DS3 signal (that is being transported by SONET) will cease to contain jitter and will now contain "Wander", whenever the frequency offset of the DS3 signal being mapped into SONET is less than 0.2ppm.

8.3 *Jitter/Wander due to Pointer Adjustments*

In the previous section, we described how a DS3 signal is asynchronously-mapped into SONET, and we also defined "Mapping/De-mapping" jitter. In this section, we will describe how occurrences within the SONET network will induce jitter/wander within the DS3 signal that is being transported across the SONET network.

In order to accomplish this, we will discuss the following topics in detail.

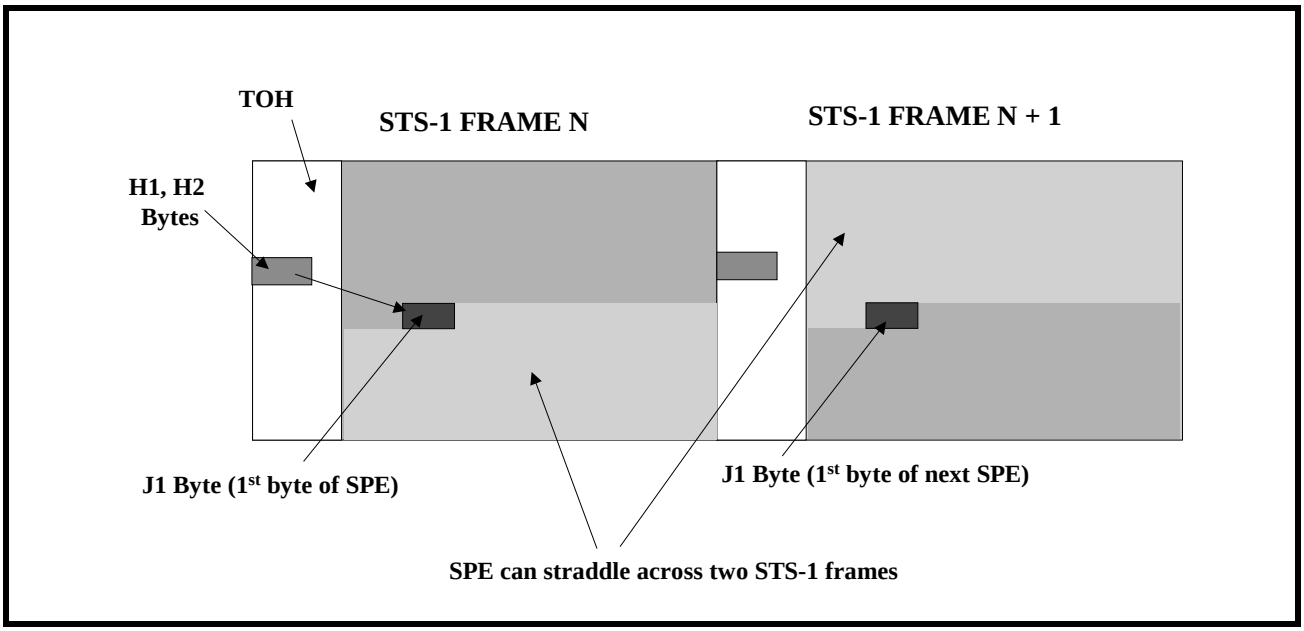
- The concept of an STS-1 SPE pointer
- The concept of Pointer Adjustments
- The causes of Pointer Adjustments
- How Pointer Adjustments induce jitter/wander within a DS3 signal being transported by that SONET network.

8.3.1 The Concept of an STS-1 SPE Pointer

As mentioned earlier, the STS-1 SPE is not aligned to the STS-1 frame boundaries and is permitted to "float" within the Envelope Capacity. As a consequence, the STS-1 SPE will often times "straddle" across two

consecutive STS-1 frames. Figure 48 presents an illustration of an STS-1 SPE straddling across two consecutive STS-1 frames.

FIGURE 48. AN ILLUSTRATION OF AN STS-1 SPE STRADDLING ACROSS TWO CONSECUTIVE STS-1 FRAMES



A PTE that is receiving and terminating an STS-1 data-stream will perform the following tasks.

- It will acquire and maintain STS-1 frame synchronization with the incoming STS-1 data-stream.
- Once the PTE has acquired STS-1 frame synchronization, then it will locate the J1 byte (e.g., the very byte within the very next STS-1 SPE) within the Envelope Capacity by reading out the contents of the H1 and H2 bytes.

The H1 and H2 bytes are referred to (in the SONET standards) as the SPE Pointer Bytes. When these two bytes are concatenated together in order to form a 16-bit word (with the H1 byte functioning as the "Most Significant Byte") then the contents of the "lower" 10 bit-fields (within this 16-bit word) reflects the location of the J1 byte within the Envelope Capacity of the incoming STS-1 data-stream. Figure 49 presents an illustration of the bit format of the H1 and H2 bytes, and indicates which bit-fields are used to reflect the location of the J1 byte.

FIGURE 49. THE BIT-FORMAT OF THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE 10 BITS, REFLECTING THE LOCATION OF THE J1 BYTE, DESIGNATED

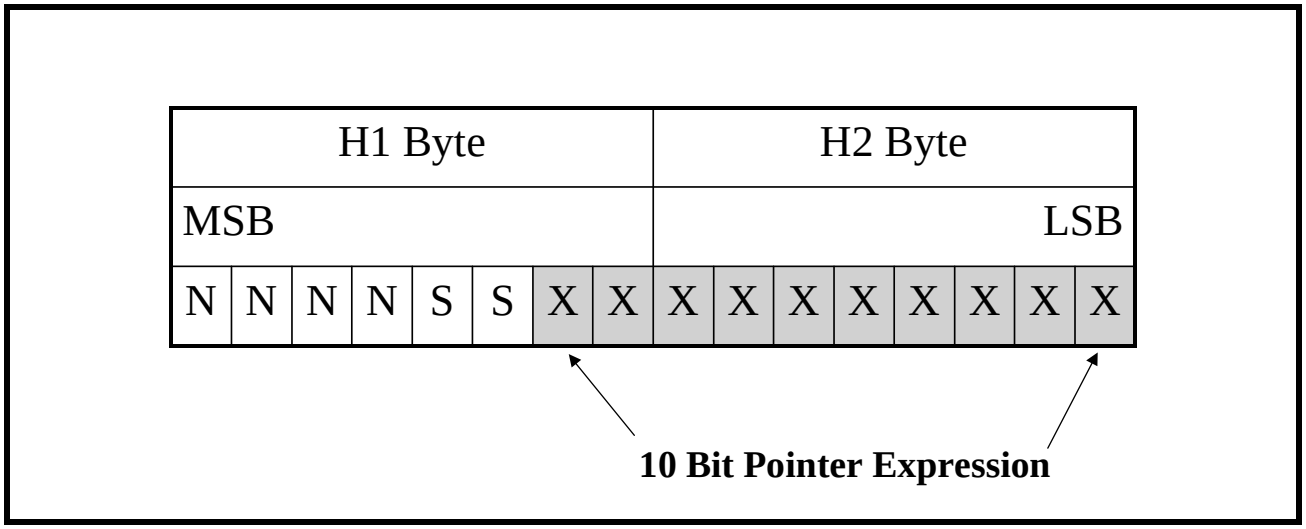
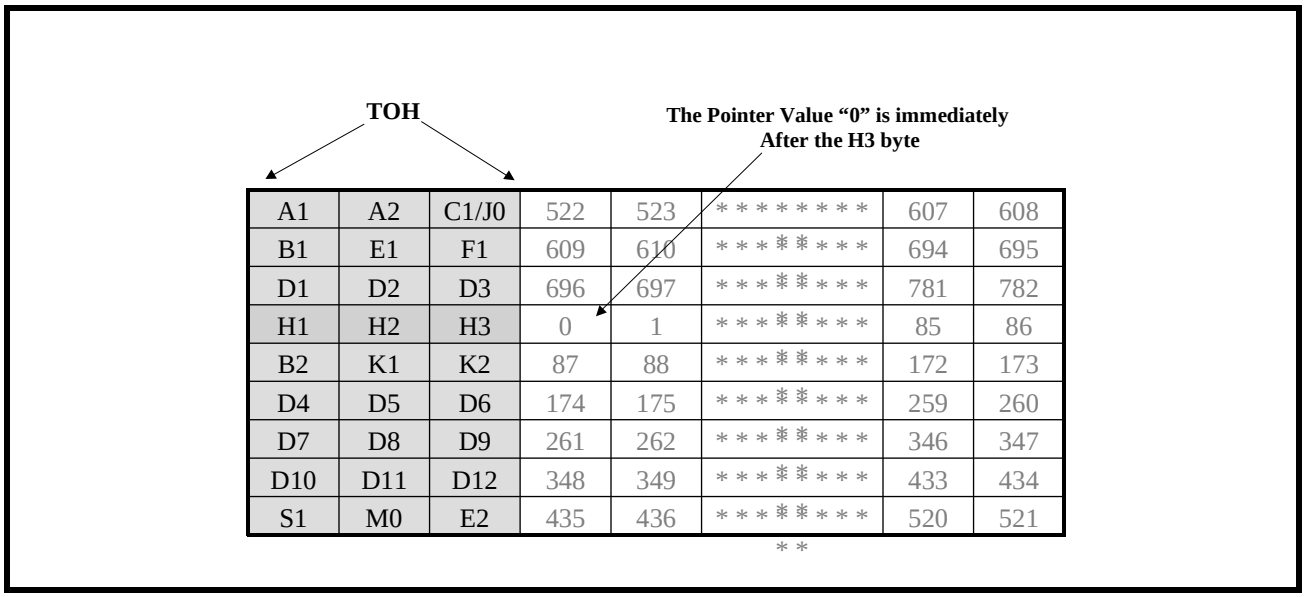


Figure 50 relates the contents within these 10 bits (within the H1 and H2 bytes) to the location of the J1 byte (e.g., the very first byte of the STS-1 SPE) within the Envelope Capacity.

FIGURE 50. THE RELATIONSHIP BETWEEN THE CONTENTS OF THE "POINTER BITS" (E.G., THE 10-BIT EXPRESSION WITHIN THE H1 AND H2 BYTES) AND THE LOCATION OF THE J1 BYTE WITHIN THE ENVELOPE CAPACITY OF AN STS-1 FRAME



NOTES:

1. *If the content of the "Pointer Bits" is "0x00" then the J1 byte is located immediately after the H3 byte, within the Envelope Capacity.*
2. *If the contents of the 10-bit expression exceed the value of 0x30F (or 782, in decimal format) then it does not contain a valid pointer value.*

8.3.2 Pointer Adjustments within the SONET Network

The word SONET stands for "Synchronous Optical NETwork. This name implies that the entire SONET network is synchronized to a single clock source. However, because the SONET (and SDH) Networks can

span thousands of miles, traverse many different pieces of equipments, and even cross International boundaries; in practice, the SONET/SDH network is NOT synchronized to a single clock source.

In practice, the SONET/SDH network can be thought of as being divided into numerous "Synchronization Islands". Each of these "Synchronization Islands" will consist of numerous pieces of SONET Terminal Equipment. Each of these pieces of SONET Terminal Equipment will all be synchronized to a single Stratum-1 clock source which is the most accurate clock source within the Synchronization Island. Typically a "Synchronization Island" will consist of a single "Timing Master" equipment along with multiple "Timing Slave" pieces of equipment. This "Timing Master" equipment will be directly connected to the Stratum-1 clock source and will have the responsibility of distributing a very accurate clock signal (that has been derived from the Stratum 1 clock source) to each of the "Timing Slave" pieces of equipment within the "Synchronization Island". The purpose of this is to permit each of the "Timing Slave" pieces of equipment to be "synchronized" with the "Timing Master" equipment, as well as the Stratum 1 Clock source. Typically this "clock distribution" is performed in the form of a BITS (Building Integrated Timing Supply) clock, in which a very precise clock signal is provided to the other pieces of equipment via a T1 or E1 line signal.

Many of these "Synchronization Islands" will use a Stratum-1" clock source that is derived from GPS pulses that are received from Satellites that operate at Geo-synchronous orbit. Other "Synchronization Islands" will use a Stratum-1" clock source that is derived from a very precise local atomic clock. As a consequence, different "Synchronization Islands" will use different Stratum 1 clock sources. The up-shot of having these "Synchronization Islands" that use different "Stratum-1 clock" sources, is that the Stratum 1 Clock frequencies, between these "Synchronization Islands" are likely to be slightly different from each other. These "frequency-differences" within Stratum 1 clock sources will result in "clock-domain changes" as a SONET signal (that is traversing the SONET network) passes from one "Synchronization Island" to another.

The following section will describe how these "frequency differences" will cause a phenomenon called "pointer adjustments" to occur in the SONET Network.

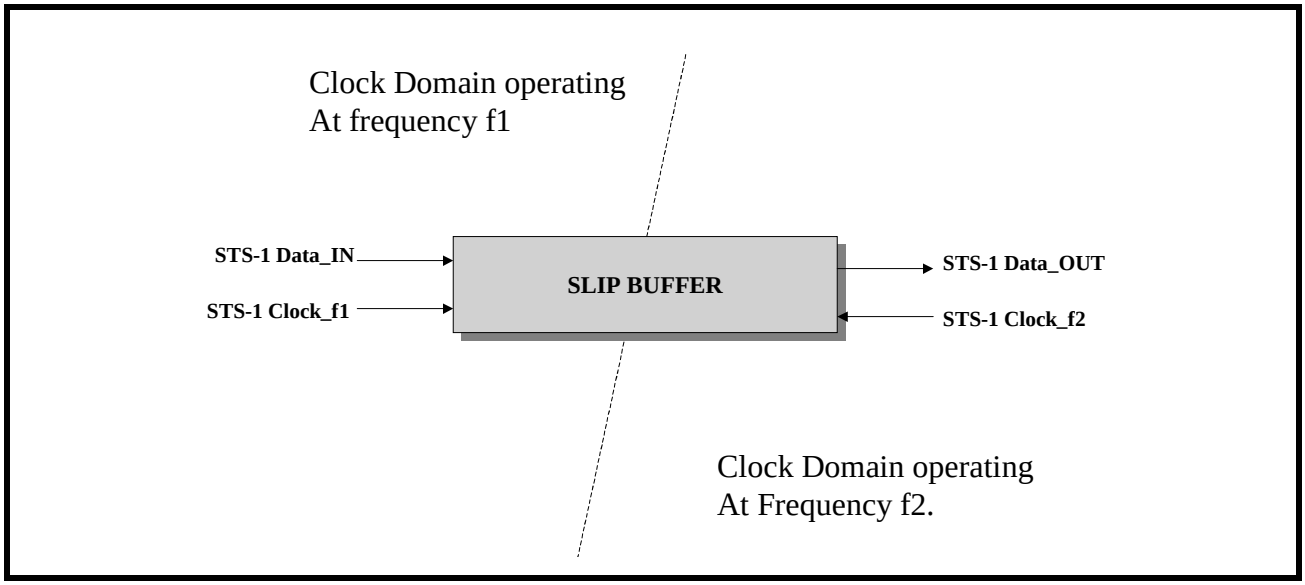
8.3.3 Causes of Pointer Adjustments

The best way to discuss how pointer adjustment events occur is to consider an STS-1 signal, which is driven by a timing reference of frequency f1; and that this STS-1 signal is being routed to a network equipment (that resides within a different "Synchronization Island") and processes STS-1 data at a frequency of f2.

NOTE: *Clearly, both frequencies f1 and f2 are at the STS-1 rate (e.g., 51.84MHz). However, these two frequencies are likely to be slightly different from each other.*

Now, since the STS-1 signal (which is of frequency f1) is being routed to the network element (which is operating at frequency f2), the typical design approach for handling "clock-domain" differences is to route this STS-1 signal through a "Slip Buffer" as illustrated below.

FIGURE 51. AN ILLUSTRATION OF AN STS-1 SIGNAL BEING PROCESSED VIA A SLIP BUFFER



In the "Slip Buffer, the "input" STS-1 data (labeled "STS-1 Data_IN") is latched into the FIFO, upon a given edge of the corresponding "STS-1 Clock_f1" input clock signal. The STS-1 Data (labeled "STS-1 Data_OUT") is clocked out of the Slip Buffer upon a given edge of the "STS-1 Clock_f2" input clock signal.

The behavior of the data, passing through the "Slip Buffer" is now described for each possible relationship between frequencies f1 and f2.

If f1 = f2

If both frequencies, f1 and f2 are exactly equal, then the STS-1 data will be "clocked" into the "Slip Buffer" at exactly the same rate that it is "clocked out". In this case, the "Slip Buffer" will neither fill-up nor become depleted. As a consequence, no pointer-adjustments will occur in this STS-1 data stream. In other words, the STS-1 SPE will remain at a constant location (or offset) within each STS-1 envelope capacity for the duration that this STS-1 signal is supporting this particular service.

If f1 < f2

If frequency f1 is less than f2, then this means that the STS-1 data is being "clocked out" of the "Slip Buffer" at a faster rate than it is being clocked in. In this case, the "Slip Buffer" will eventually become depleted. Whenever this occurs, a typical strategy is to "stuff" (or insert) a "dummy byte" into the data stream. The purpose of stuffing this "dummy byte" is to compensate for the frequency differences between f1 and f2, and attempt to keep the "Slip Buffer, at a somewhat constant fill level.

NOTE: *This "dummy byte" does not carry any valuable information (not for the user, nor for the system).*

Since this "dummy byte" carries no useful information, it is important that the "Receiving PTE" be notified anytime this "dummy byte" stuffing occurs. This way, the Receiving Terminal can "know" not to treat this "dummy byte" as user data.

Byte-Stuffing and Pointer Incrementing in a SONET Network

Whenever this "byte-stuffing" occurs then the following other things occur within the STS-1 data stream.

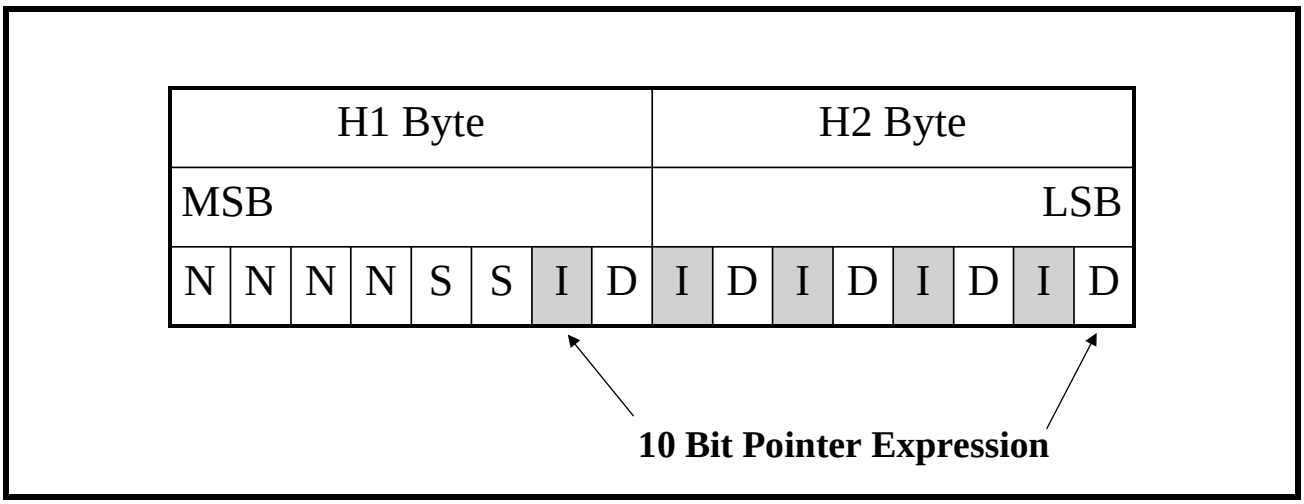
During the STS-1 frame that contains the "Byte-Stuffing" event

a. The "stuff-byte" will be inserted into the byte position immediately after the H3 byte. This insertion of the "dummy byte" immediately after the H3 byte position will cause the J1 byte (and in-turn, the rest of the SPE) to be "byte-shifted" away from the H3 byte. As a consequence, the offset between the H3 byte position and the STS-1 SPE will now have been increased by 1 byte.

b. The "Transmitting" Network Equipment will notify the remote terminal of this byte-stuffing event, by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "I" bits.

Figure 52 presents an illustration of the bit-format within the 16-bit word (consist of the H1 and H2 bytes) with the "I" bits designated.

FIGURE 52. AN ILLUSTRATION OF THE BIT FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "I" BITS DESIGNATED



NOTE: *At this time the "I" bits are inverted in order to denote that an "incrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Byte-Stuffing" event

The "I" bits (within the "pointer-word") will be set back to their normal value; and the contents of the H1 and H2 bytes will be incremented by "1".

If f1 > f2

If frequency f1 is greater than f2, then this means that the STS-1 data is being clocked into the "Slip Buffer" at a faster rate than is being clocked out. In this case, the "Slip Buffer" will start to fill up. Whenever this occurs, a typical strategy is to delete (e.g., negative-stuff) a byte from the Slip Buffer. The purpose of this "negative-stuffing" is to compensate for the frequency differences between f1 and f2; and to attempt to keep the "Slip Buffer" at a somewhat constant fill-level.

NOTE: *This byte, which is being "un-stuffed" does carry valuable information for the user (e.g., this byte is typically a payload byte). Therefore, whenever this negative stuffing occurs, two things must happen.*

a. The "negative-stuffed" byte must not be simply discarded. In other words, it must somehow also be transmitted to the remote PTE with the remainder of the SPE data.

b. The remote PTE must be notified of the occurrence of these "negative-stuffing" events. Further, the remote PTE must know where to obtain this "negative-stuffed" byte.

Negative-Stuffing and Pointer-Decrementing in a SONET Network

Whenever this "byte negative-stuffing" occurs then the following other things occur within the STS-1 data-stream.

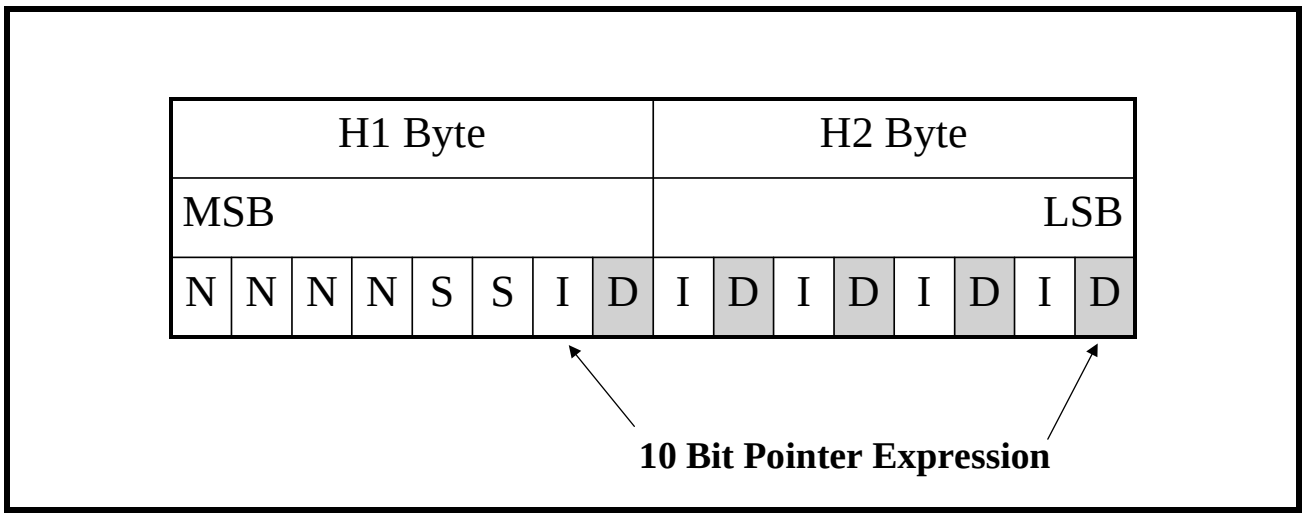
During the STS-1 frame that contains the "Negative Byte-Stuffing" Event

a. The "Negative-Stuffed" byte will be inserted into the H3 byte position. Whenever an SPE data byte is inserted into the H3 byte position (which is ordinarily an unused byte), the number of bytes that will exist between the H3 byte and the J1 byte within the very next SPE will be reduced by 1 byte. As a consequence, in this case, the J1 byte (and in-turn, the rest of the SPE) will now be "byte-shifted" towards the H3 byte position.

b. The "Transmitting" Network Element will notify the remote terminal of this "negative-stuff" event by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "D" bits.

Figure 53 presents an illustration of the bit format within the 16-bit word (consisting of the H1 and H2 bytes) with the "D" bits designated.

FIGURE 53. AN ILLUSTRATION OF THE BIT-FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "D" BITS DESIGNATED



NOTE: *At this time the "D" bits are inverted in order to denote that a "decrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Negative Byte-Stuffing" Event

The "D" bits (within the pointer-word) will be set back to their normal value; and the contents of the H1 and H2 bytes will be decremented by one.

8.3.4 Why are we talking about Pointer Adjustments?

The overall SONET network consists of numerous "Synchronization Islands". As a consequence, whenever a SONET signal is being transmitted from one "Synchronization Island" to another; that SONET signal will undergo a "clock domain" change as it traverses the network. This clock domain change will result in periodic pointer-adjustments occurring within this SONET signal. Depending upon the direction of this "clock-domain" shift that the SONET signal experiences, there will either be periodic "incrementing" pointer-adjustment events or periodic "decrementing" pointer-adjustment events within this SONET signal.

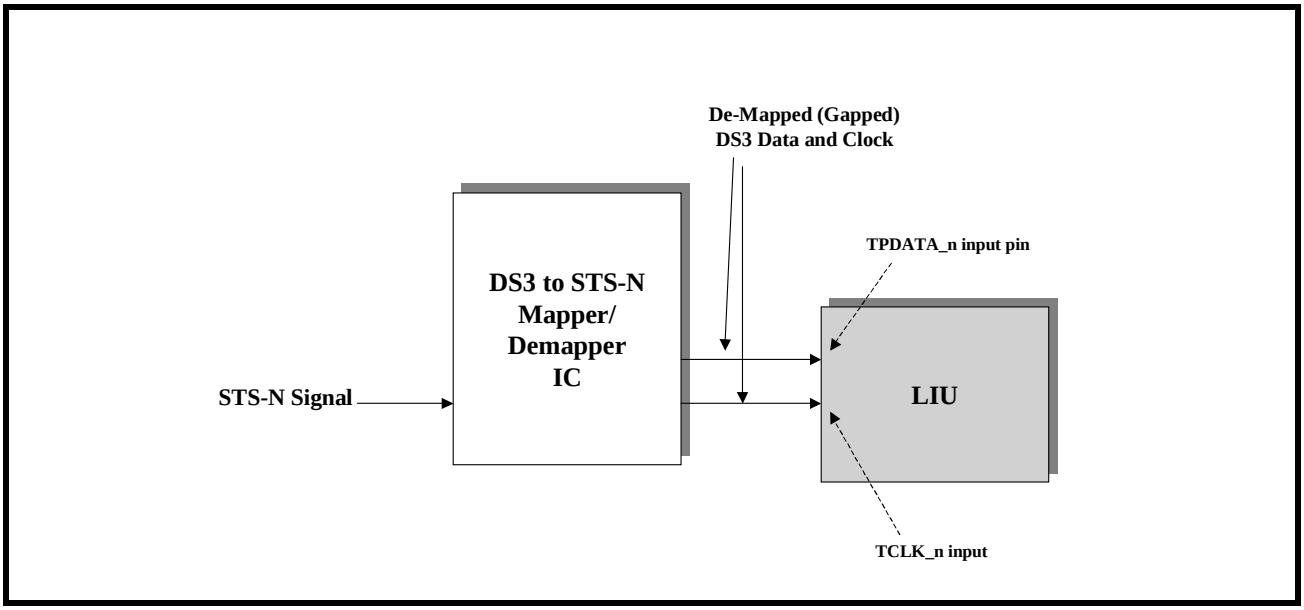
Regardless of whether a given SONET signal is experiencing incrementing or decrementing pointer adjustment events, each pointer adjustment event will result in an abrupt 8-bit shift in the position of the SPE within the STS-1 data-stream. If this STS-1 signal is transporting an "asynchronously-mapped" DS3 signal; then this 8-bit shift in the location of the SPE (within the STS-1 signal) will result in approximately 8UIpp of jitter within the asynchronously-mapped DS3 signal, as it is de-mapped from SONET. In “Section 8.5, A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications” on page 106 we will discuss the "Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE. However, for now we will simply state that this 8UIpp of intrinsic jitter far exceeds these "intrinsic jitter" requirements.

In summary, pointer-adjustments events are a "fact of life" within the SONET/SDH network. Further, pointer-adjustment events, within a SONET signal that is transporting an asynchronously-mapped DS3 signal, will impose a significant impact on the Intrinsic Jitter and Wander within that DS3 signal as it is de-mapped from SONET.

8.4 *Clock Gapping Jitter*

In most applications (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper Device in the manner as presented below in Figure 54.

FIGURE 54. ILLUSTRATION OF THE TYPICAL APPLICATIONS FOR THE LIU IN A SONET DE-SYNC APPLICATION



In this application, the Mapper IC will have the responsibility of receiving an STS-N signal (from the SONET Network) and performing all of the following operations on this STS-N signal.

- Byte-de-interleaving this incoming STS-N signal into N STS-1 signals
- Terminating each of these STS-1 signals
- Extracting (or de-mapping) the DS3 signal(s) from the SPEs within each of these terminated STS-1 signals.

In this application, these Mapper devices can be thought of as multi-channel devices. For example, an STS-3 Mapper can be viewed as a 3-Channel DS3/STS-1 to STS-3 Mapper IC. Similarly, an STS-12 Mapper can be

viewed as a 12-Channel DS3/STS-1 to STS-12 Mapper IC. Continuing on with this line of thought, if a Mapper IC is configured to receive an STS-N signal, and (from this STS-N signal) de-map and output N DS3 signals (towards the DS3 facility), then it will typically do so in the following manner.

- In many cases, the Mapper IC will output this DS3 signal, using both a "Data-Signal" and a "Clock-Signal". In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data-Signal.
- However, as the Mapper IC output this STS-1 data-stream, it will typically supply clock pulses (via the Clock-Signal output) coincident to whenever a DS3 bit is being output via the Data-Signal. In this case, the Mapper IC will NOT supply a clock pulse coincident to when a TOH, POH, or any "non-DS3 data-bit" is being output via the "Data-Signal".

Now, since the Mapper IC will output the entire STS-1 data stream (via the Data-Signal), the output Clock-Signal will be of the form such that it has a period of 19.3ns (e.g., a 51.84MHz clock signal). However, the Mapper IC will still generate approximately 44,736,000 clock pulses during any given one second period. Hence, the clock signal that is output from the Mapper IC will be a horribly gapped 44.736MHz clock signal. One can view such a clock signal as being a very-jittery 44.736MHz clock signal. This jitter that exists within the "Clock-Signal" is referred to as "Clock-Gapping" Jitter. A more detailed discussion on how the user must handle this type of jitter is presented in “Section 8.8.2, Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU” on page 117.

8.5 *A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications*

The "Category I Intrinsic Jitter Requirements" per Telcordia GR-253-CORE (for DS3 applications) mandates that the user perform a large series of tests against certain specified "Scenarios". These "Scenarios" and their corresponding requirements is summarized in Table 46, below.

TABLE 46: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
DS3 De-Mapping Jitter		0.4UI-pp	Includes effects of De-Mapping and Clock Gapping Jitter
Single Pointer Adjustment	A1	0.3UI-pp + Ao	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.NOTE: Ao is the amount of intrinsic jitter that was measured during the "DS3 De-Mapping Jitter" phase of the Test.
Pointer Bursts	A2	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Phase Transients	A3	1.2UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

TABLE 46: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
Continuous Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

NOTE: *All of these intrinsic jitter measurements are to be performed using a band-pass filter of 10Hz to 400kHz.*

Each of the scenarios presented in Table 46, are briefly described below.

8.5.1 DS3 De-Mapping Jitter

DS3 De-Mapping Jitter is the amount of Intrinsic Jitter that will be measured within the "Line" or "Facility-side" DS3 signal, (after it has been de-mapped from a SONET signal) without the occurrence of "Pointer Adjustments" within the SONET signal.

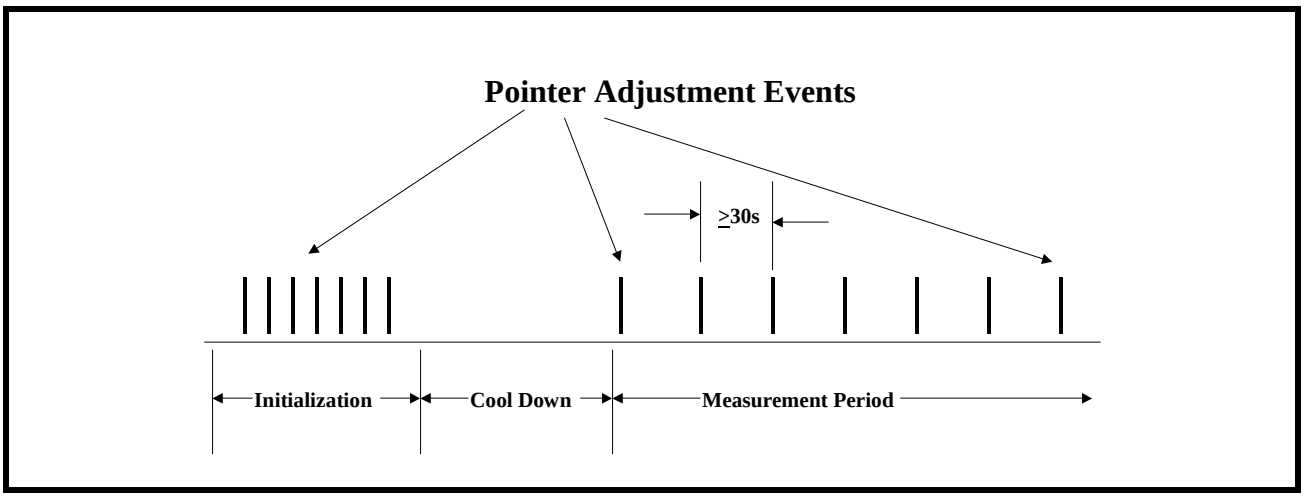
Telcordia GR-253-CORE requires that the "DS3 De-Mapping" Jitter be less than 0.4UI-pp, when measured over all possible combinations of DS3 and STS-1 frequency offsets.

8.5.2 Single Pointer Adjustment

Telcordia GR-253-CORE states that if each pointer adjustment (within a continuous stream of pointer adjustments) is separated from each other by a period of 30 seconds, or more; then they are sufficiently isolated to be considered "Single-Pointer Adjustments".

Figure 55 presents an illustration of the "Single Pointer Adjustment" Scenario.

FIGURE 55. ILLUSTRATION OF SINGLE POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE states that the Intrinsic Jitter that is measured (within the DS3 signal) that is ultimately de-mapped from a SONET signal that is experiencing "Single-Pointer Adjustment" events, must NOT exceed the value 0.3UI-pp + Ao.

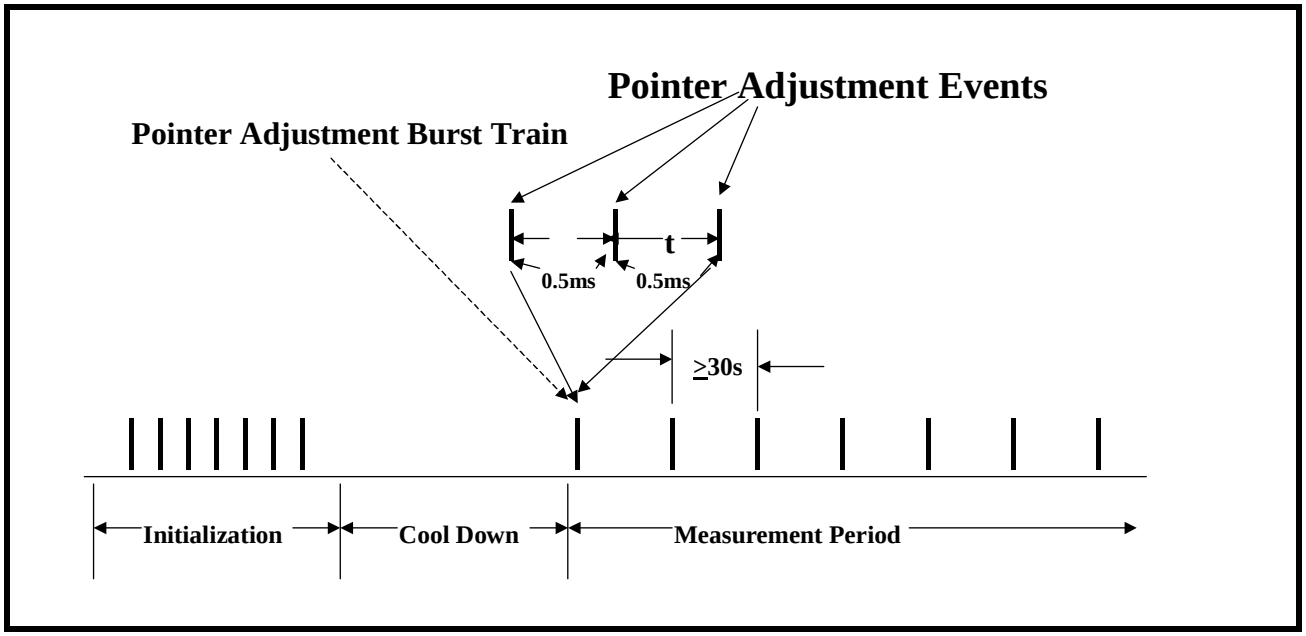
NOTES:

1. *Ao is the amount of Intrinsic Jitter that was measured during the "De-Mapping" Jitter portion of this test.*
2. *Testing must be performed for both Incrementing and Decrementing Pointer Adjustments.*

8.5.3 Pointer Burst

Figure 56 presents an illustration of the "Pointer Burst" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 56. ILLUSTRATION OF BURST OF POINTER ADJUSTMENT SCENARIO

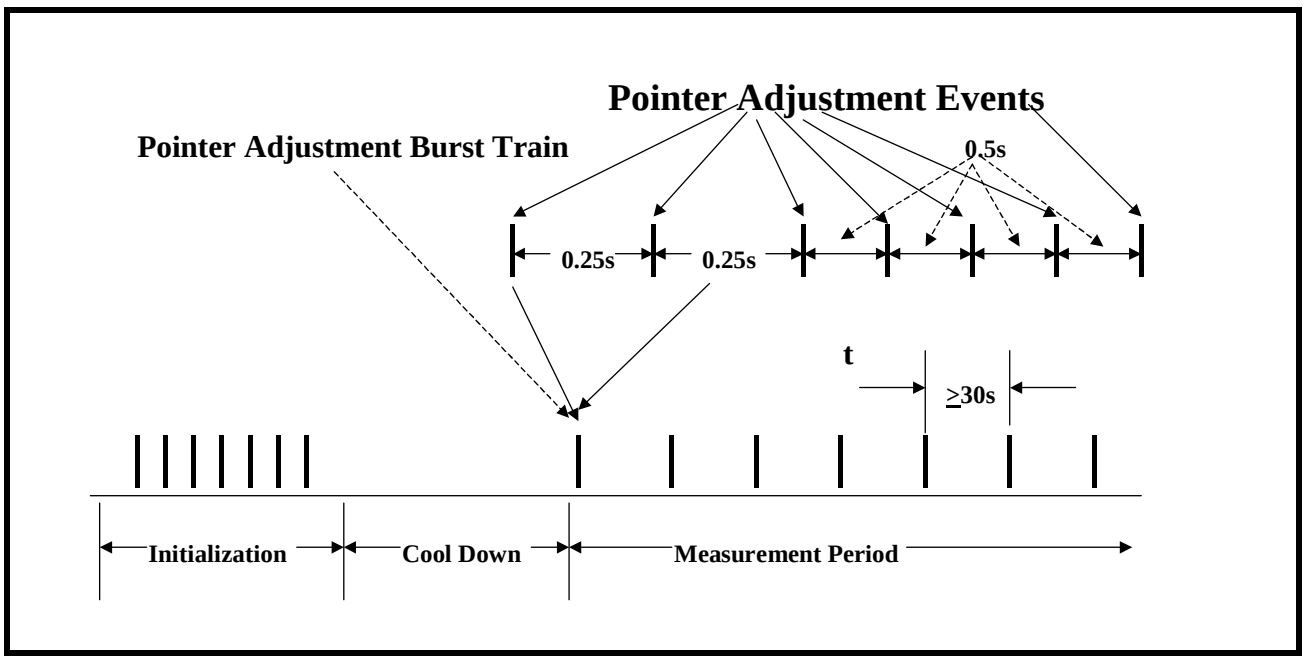


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Burst of Pointer Adjustment" scenario, must NOT exceed 1.3UI-pp.

8.5.4 Phase Transients

Figure 57 presents an illustration of the "Phase Transients" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 57. ILLUSTRATION OF "PHASE-TRANSIENT" POINTER ADJUSTMENT SCENARIO

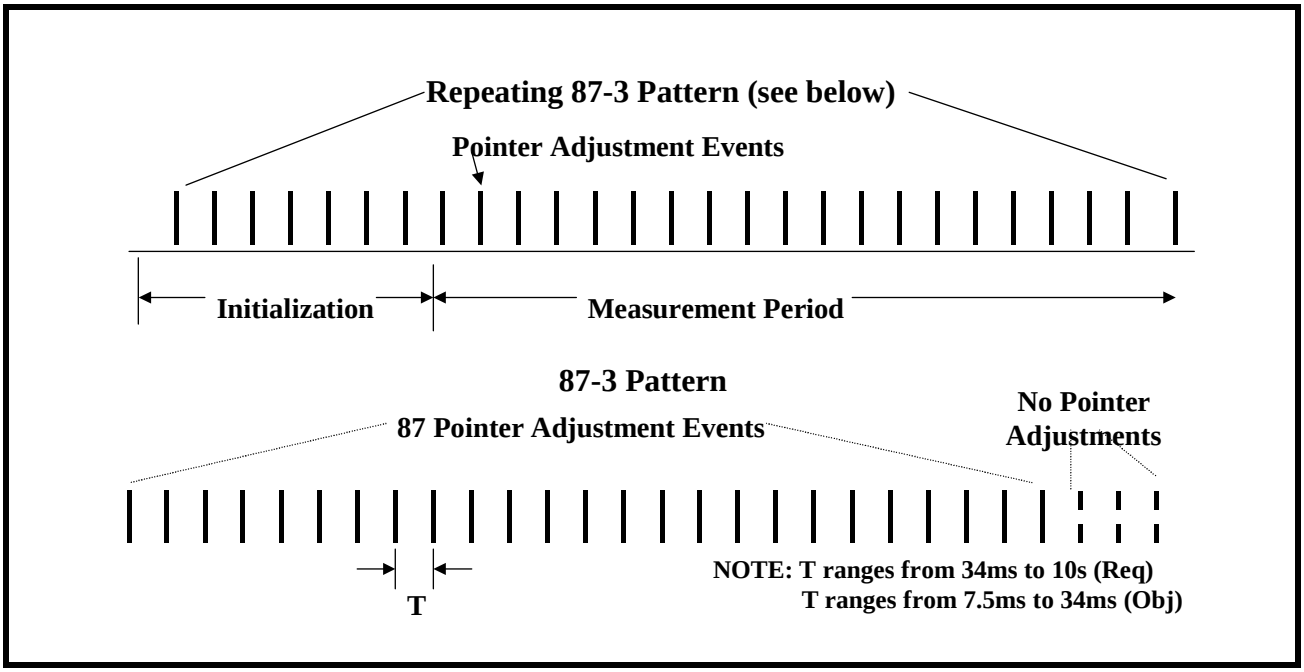


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Phase Transient - Pointer Adjustment" scenario must NOT exceed 1.2UI-pp.

8.5.5 87-3 Pattern

Figure 58 presents an illustration of the "87-3 Continuous Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 58. AN ILLUSTRATION OF THE 87-3 CONTINUOUS POINTER ADJUSTMENT PATTERN



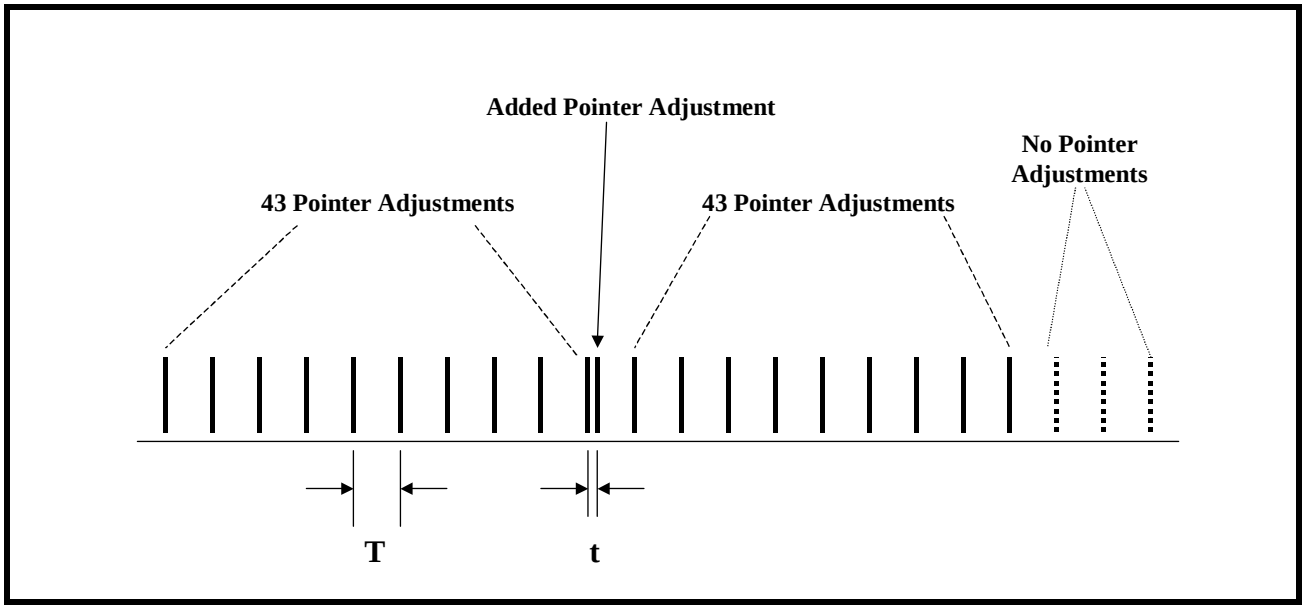
Telcordia GR-253-CORE defines an "87-3 Continuous" Pointer Adjustment pattern, as a repeating sequence of 90 pointer adjustment events. Within this 90 pointer adjustment event, 87 pointer adjustments are actually executed. The remaining 3 pointer adjustments are never executed. The spacing between individual pointer adjustment events (within this scenario) can range from 7.5ms to 10seconds.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp.

8.5.6 87-3 Add

Figure 59 presents an illustration of the "87-3 Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 59. ILLUSTRATION OF THE 87-3 ADD POINTER ADJUSTMENT PATTERN



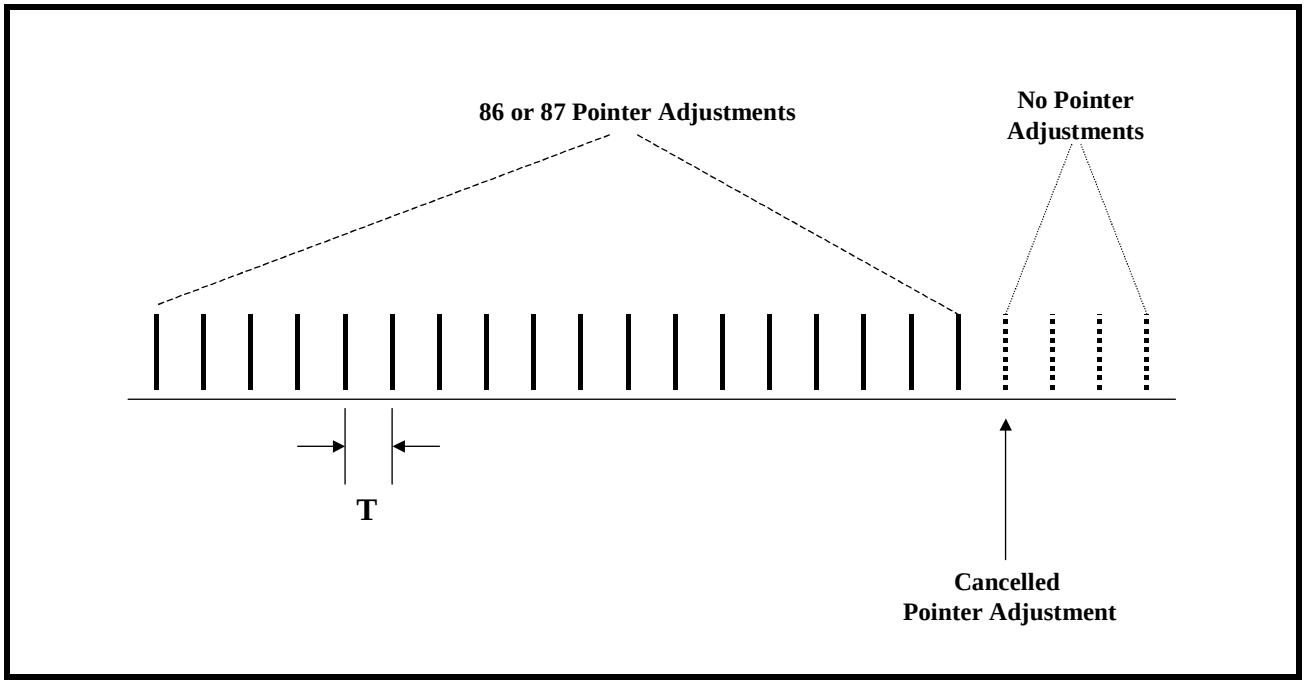
Telcordia GR-253-CORE defines an "87-3 Add" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 59.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.7 87-3 Cancel

Figure 60 presents an illustration of the 87-3 Cancel Pattern Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 60. ILLUSTRATION OF 87-3 CANCEL POINTER ADJUSTMENT SCENARIO



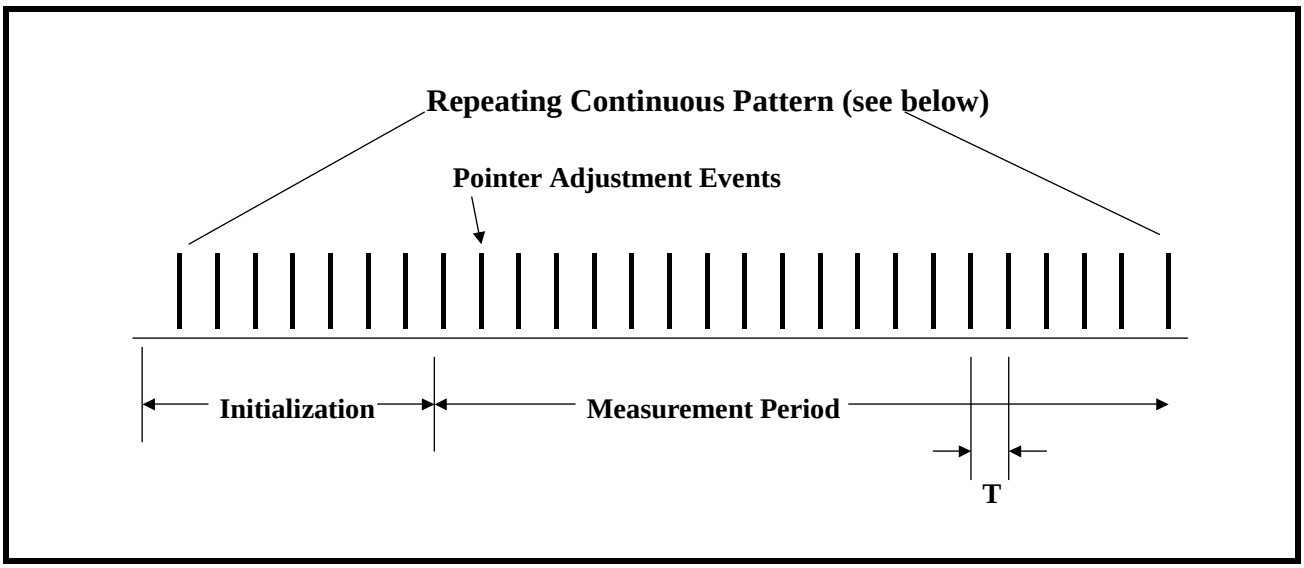
Telcordia GR-253-CORE defines an "87-3 Cancel" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 60.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.8 Continuous Pattern

Figure 61 presents an illustration of the "Continuous" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 61. ILLUSTRATION OF CONTINUOUS PERIODIC POINTER ADJUSTMENT SCENARIO

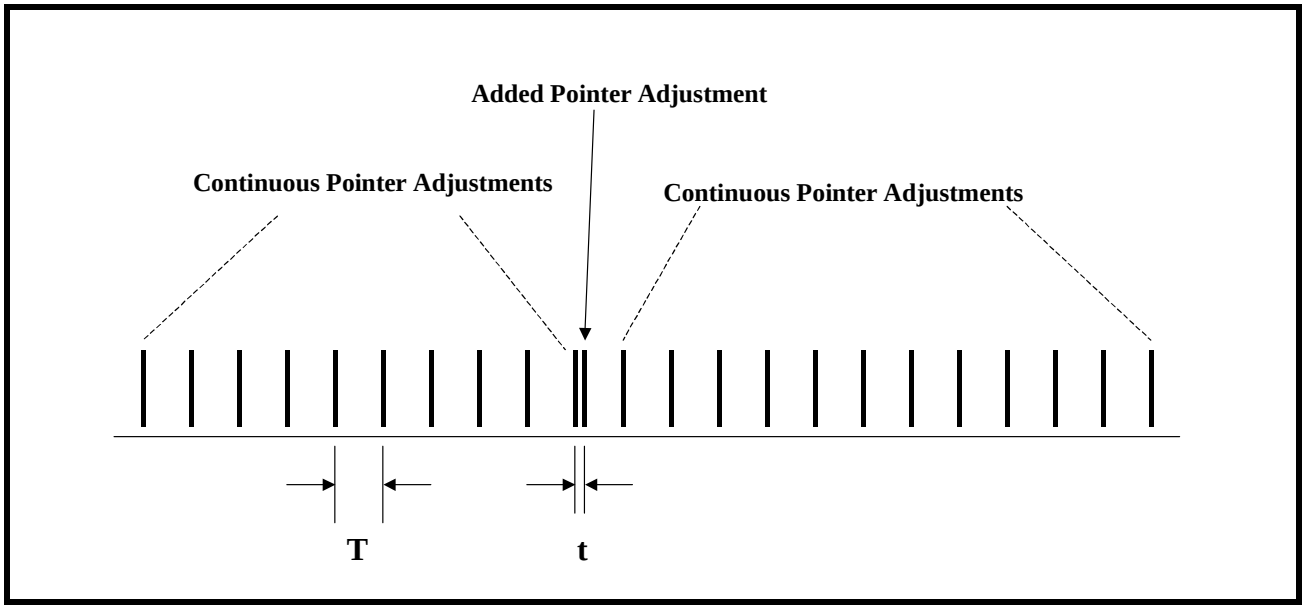


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp. The spacing between individual pointer adjustments (within this scenario) can range from 7.5ms to 10s.

8.5.9 Continuous Add

Figure 62 presents an illustration of the "Continuous Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 62. ILLUSTRATION OF CONTINUOUS-ADD POINTER ADJUSTMENT SCENARIO



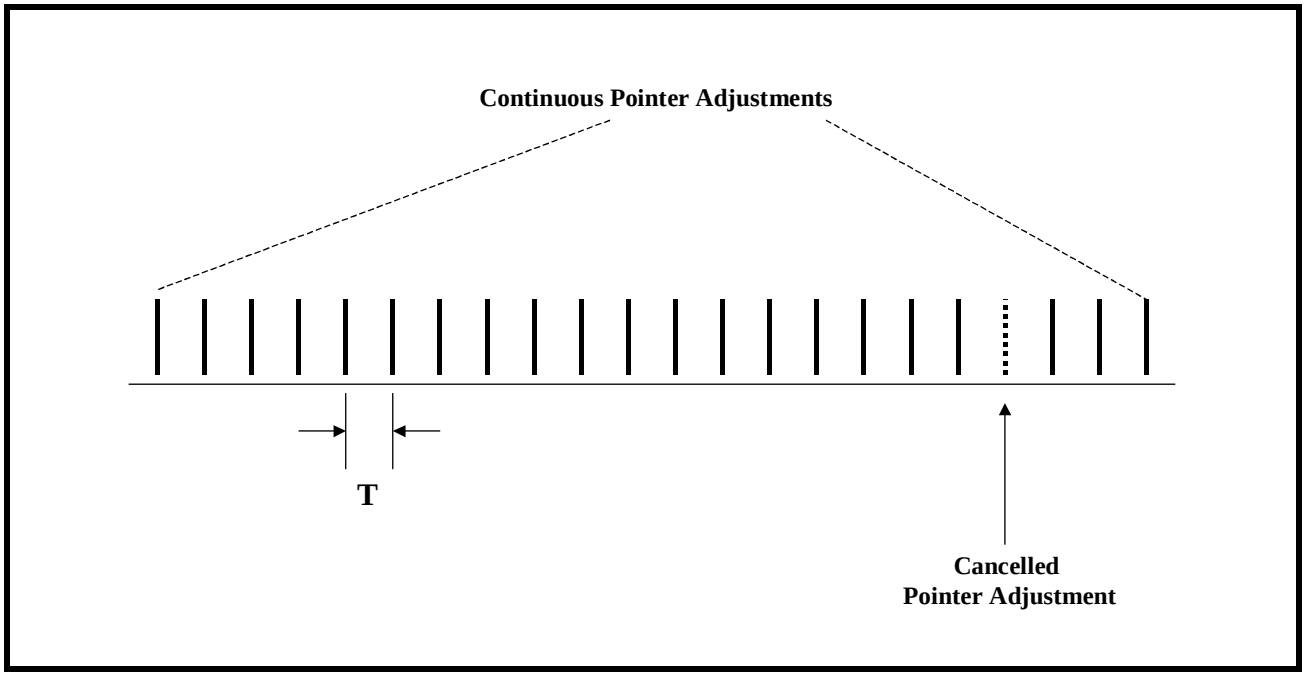
Telcordia GR-253-CORE defines an "Continuous Add" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 62.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.10 Continuous Cancel

Figure 63 presents an illustration of the "Continuous Cancel Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 63. ILLUSTRATION OF CONTINUOUS-CANCEL POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE defines a "Continuous Cancel" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 63.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.6 *A Review of the DS3 Wander Requirements per ANSI T1.105.03b-1997.*

To be provided in the next revision of this data sheet.

8.7 *A Review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application*

The Intrinsic Jitter and Wander Test results are summarized in this section.

8.7.1 Intrinsic Jitter Test results

The Intrinsic Jitter Test results for the LIU in DS3 being de-mapped from SONET is summarized below in Table 2.

TABLE 47: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	LIU INTRINSIC JITTER TEST RESULTS	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS
DS3 De-Mapping Jitter		0.13UI-pp	0.4UI-pp
Single Pointer Adjustment	A1	0.201UI-pp	0.43UI-pp (e.g. 0.13UI-pp + 0.3UI-pp)
Pointer Bursts	A2	0.582UI-pp	1.3UI-pp
Phase Transients	A3	0.526UI-pp	1.2UI-pp
87-3 Pattern	A4	0.790UI-pp	1.0UI-pp
87-3 Add	A5	0.926UI-pp	1.3UI-pp
87-3 Cancel	A5	0.885UI-pp	1.3UI-pp
Continuous Pattern	A4	0.497UI-pp	1.0UI-pp
Continuous Add	A5	0.598UI-pp	1.3UI-pp
Continuous Cancel	A5	0.589UI-pp	1.3UI-pp

NOTES:

1. *A detailed test report on our Test Procedures and Test Results is available and can be obtained by contacting your Exar Sales Representative.*
2. *These test results were obtained via the LIUs mounted on our XRT94L43 12-Channel DS3/E3/STS-1 Mapper Evaluation Board.*
3. *These same results apply to SDH/AU-3 Mapping applications.*

8.7.2 Wander Measurement Test Results

Wander Measurement test results will be provided in the next revision of the LIU Data Sheet.

8.8 *Designing with the LIU*

In this section, we will discuss the following topics.

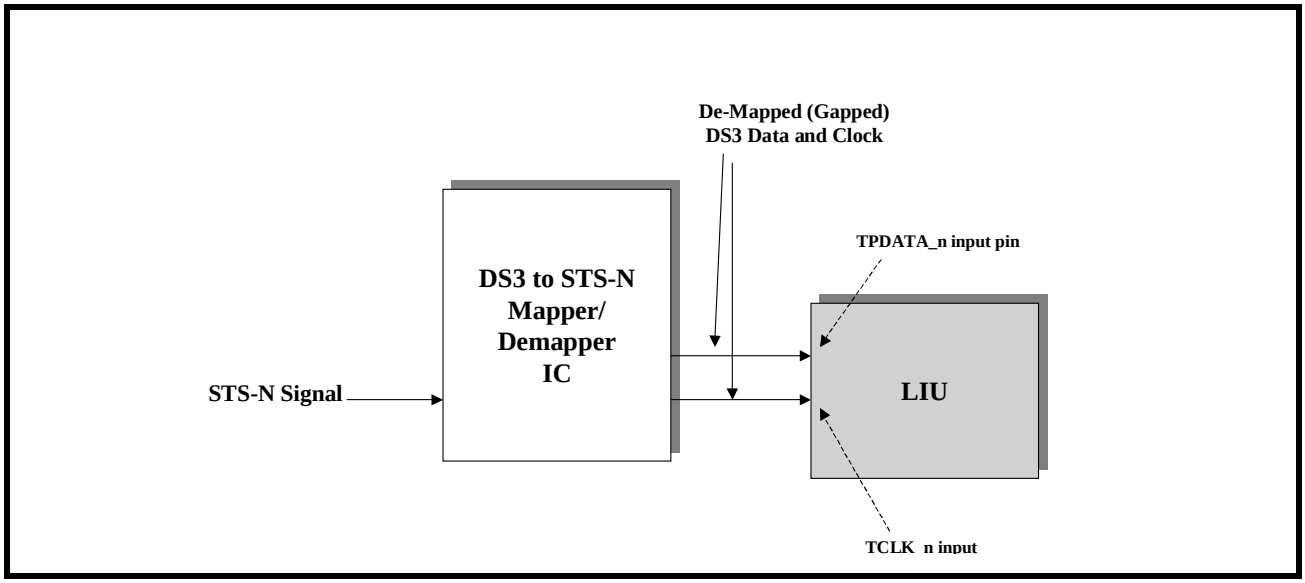
- How to design with and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements.
- How is the LIU able to meet the above-mentioned requirements?
- How does the LIU permits the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?
- How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

8.8.1 How to design and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements

As mentioned earlier, in most application (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper device in the manner as presented below in Figure 64.

In this application, the Mapper has the responsibility of receiving a SONET STS-N/OC-N signal and extracting as many as N DS3 signals from this signal. As a given channel within the Mapper IC extracts out a given DS3 signal (from SONET) it will typically be applying a Clock and Data signal to the "Transmit Input" of the LIU IC. Figure 64 presents a simple illustration as to how one channel, within the LIU should be connected to the Mapper IC.

FIGURE 64. ILLUSTRATION OF THE LIU BEING CONNECTED TO A MAPPER IC FOR SONET DE-SYNC APPLICATIONS



As mentioned above, the Mapper IC will typically output a Clock and Data signal to the LIU. In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data Signal to the LIU. However, the Mapper IC typically only supplies a clock pulse via the Clock Signal to the LIU coincident to whenever a DS3 bit is being output via the Data Signal. In this case, the Mapper IC would not supply a clock edge coincident to when a TOH, POH or any non-DS3 data-bit is being output via the Data-Signal.

Figure 64 indicates that the Data Signal from the Mapper device should be connected to the TPDATA_n input pin of the LIU IC and that the Clock Signal from the Mapper device should be connected to the TCLK_n input pin of the LIU IC.

In this application, the LIU has the following responsibilities.

- Using a particular clock edge within the "gapped" clock signal (from the Mapper IC) to sample and latch the value of each DS3 data-bit that is output from the Mapper IC.
- To (through the user of the Jitter Attenuator block) attenuate the jitter within this "DS3 data" and "clock signal" that is output from the Mapper IC.
- To convert this "smoothed" DS3 data and clock into industry-compliant DS3 pulses, and to output these pulses onto the line.

To configure the LIU to operate in the correct mode for this application, the user must execute the following configuration steps.

a. *Configure the LIU to operate in the DS3 Mode*

The user can configure a given channel (within the LIU) to operate in the DS3 Mode, by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting both Bits 2 (E3_n) and Bits 1 (STS-1/DS3*_n), within each of the "Channel Control Registers" to "0" as depicted below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06
CHANNEL 1 ADDRESS LOCATION = 0X0E
CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

- **If the LIU has been configured to operate in the Hardware Mode**

The user can accomplish this by pulling all of the following input pins "Low".

Pin 76 - E3_0

Pin 94 - E3_1

Pin 85 - E3_2

Pin 72 - STS-1/$\overline{DS3}$_0

Pin 98 - STS-1/$\overline{DS3}$_1

Pin 81 - STS-1/$\overline{DS3}$_2

b. *Configure the LIU to operate in the Single-Rail Mode*

Since the Mapper IC will typically output a single "Data Line" and a "Clock Line" for each DS3 signal that it demaps from the incoming STS-N signal, it is imperative to configure each channel within the LIU to operate in the Single Rail Mode.

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting Bit 0 (SR/DR*), within the each of the "Channel Control" Registers to 1, as illustrated below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06

CHANNEL 1 ADDRESS LOCATION = 0X0E

CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/ DS3_n	SR/DR_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie pin 65 (SR/DR*) to "High".

c. ***Configure each of the channels within the LIU to operate in the SONET De-Sync Mode***

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should set Bit D2 (JA0) to "0" and Bit D0 (JA1) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie pin 44 (JA0) to a logic "HIGH" and pin 42 (JA1) to a logic "LOW".

Once the user accomplishes either of these steps, then the Jitter Attenuator (within the LIU) will be configured to operate with a very narrow bandwidth.

d. ***Configure the Jitter Attenuator (within each of the channels) to operate in the Transmit Direction.***

The user can accomplish this by executing either the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should be Bit D1 (JATx/JARx*) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

- **If the LIU has been configured to operate in the Hardware Mode.**

Then the user should tie pin 43 (JATx/JARx*) to "1".

e. *Enable the "SONET APS Recovery Time" Mode*

Finally, if the user intends to use the LIU in an Application that is required to reacquire proper SONET and DS3 traffic, prior within 50ms of an APS (Automatic Protection Switching) event (per Telcordia GR-253-CORE), then the user should set Bit 4 (SONET APS Recovery Time Disable), within the "Jitter Attenuator Control" Register, to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

NOTES:

1. *The ability to disable the "SONET APS Recovery Time" mode is only available if the LIU is operating in the Host Mode. If the LIU is operating in the "Hardware" Mode, then this "SONET APS Recovery Time Mode" feature will always be enabled.*
2. *The "SONET APS Recovery Time" mode will be discussed in greater detail in “Section 8.8.3, How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?” on page 121.*

8.8.2 Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU

In order to minimize the effects of "Clock-Gapping" Jitter within the DS3 signal that is ultimately transmitted to the DS3 Line (or facility), we recommend that some "pre-processing" of the "Data-Signals" and "Clock-Signals" (which are output from the Mapper device) be implemented prior to routing these signals to the "Transmit Inputs" of the LIU.

8.8.2.1 *SOME NOTES PRIOR TO STARTING THIS DISCUSSION:*

Our simulation results indicate that Jitter Attenuator PLL (within the LIU LIU IC) will have no problem handling and processing the "Data-Signal" and "Clock-Signal" from a Mapper IC/ASIC if no pre-processing has been performed on these signals. In order words, our simulation results indicate that the Jitter Attenuator PLL (within the LIU IC) will have no problem handling the "worst-case" of 59 consecutive bits of no clock pulses in the "Clock-Signal (due to the Mapper IC processing the TOH bytes, an Incrementing Pointer-Adjustment-induced "stuffed-byte", the POH byte, and the two fixed-stuff bytes within the STS-1 SPE, etc), immediately followed be processing clusters of DS3 data-bits (as shown in Figure 44) and still comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE for DS3 applications.

NOTE: *If this sort of "pre-processing" is already supported by the Mapper device that you are using, then no further action is required by the user.*

8.8.2.2 *OUR PRE-PROCESSING RECOMMENDATIONS*

For the time-being, we recommend that the customer implement the "pre-processing" of the DS3 "Data-Signal" and "Clock-Signal" as described below. Currently we are aware that some of the Mapper products on the Market do implement this exact "pre-processing" algorithm. However, if the customer is implementing their Mapper Design in an ASIC or FPGA solution, then we strongly recommend that the user implement the necessary logic design to realize the following recommendations.

Some time ago, we spent some time, studying (and then later testing our solution with) the PM5342 OC-3 to DS3 Mapper IC from PMC-Sierra. In particular, we wanted to understand the type of "DS3 Clock" and "Data" signal that this DS3 to OC-3 Mapper IC outputs.

During this effort, we learned the following.

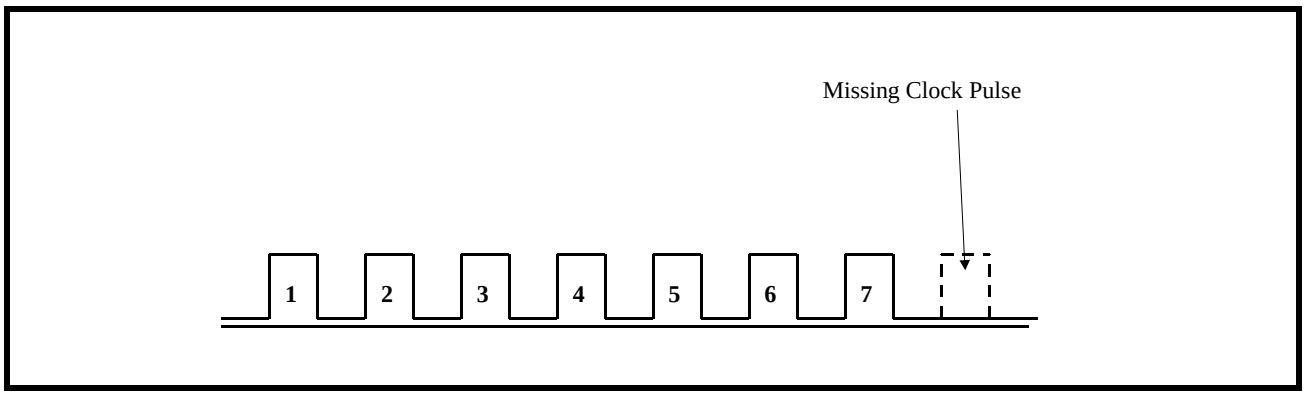
1. This "DS3 Clock" and "Data" signal, which is output from the Mapper IC consists of two major "repeating" patterns (which we will refer to as "MAJOR PATTERN A" and "MAJOR PATTERN B". The behavior of each of these patterns is presented below.

MAJOR PATTERN A

MAJOR PATTERN A consists of two "sub" or minor-patterns, (which we will refer to as "MINOR PATTERN P1 and P2).

MINOR PATTERN P1 consists of a string of seven (7) clock pulses, followed by a single gap (no clock pulse). An illustration of MINOR PATTERN P1 is presented below in Figure 65.

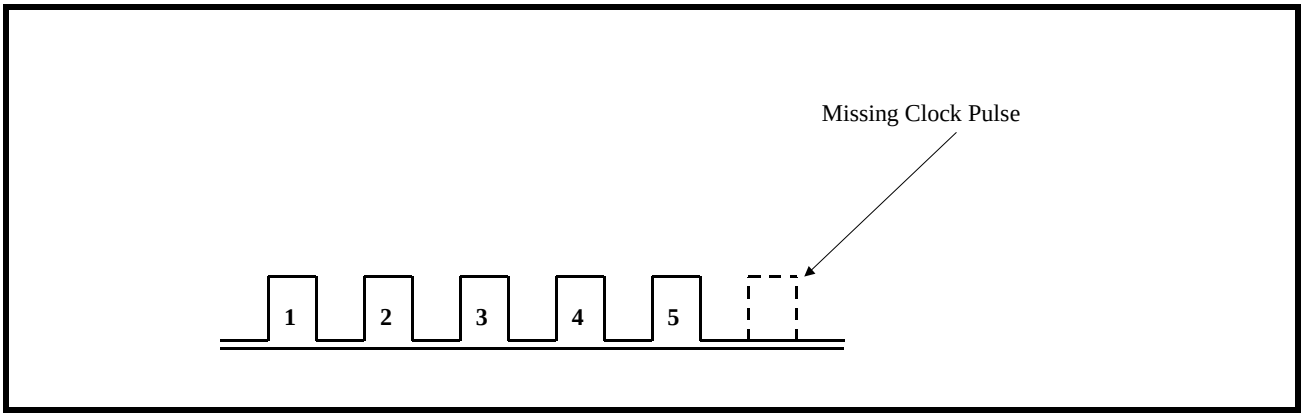
FIGURE 65. ILLUSTRATION OF MINOR PATTERN P1



It should be noted that each of these clock pulses has a period of approximately 19.3ns (or has an "instantaneously frequency of 51.84MHz).

MINOR Pattern P2 consists of string of five (5) clock pulses, which is also followed by a single gap (no clock pulse). An illustration of Pattern P2 is presented below in Figure 66.

FIGURE 66. ILLUSTRATION OF MINOR PATTERN P2



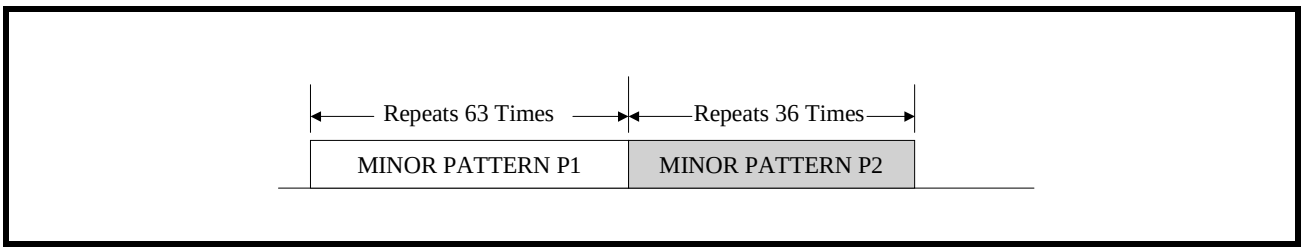
HOW MAJOR PATTERN A IS SYNTHESIZED

MAJOR PATTERN A is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.

Figure 67 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN A

FIGURE 67. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE MAJOR PATTERN A



Hence, MAJOR PATTERN A consists of "(63 x 7) + (36 x 5)" = 621 clock pulses. These 621 clock pulses were delivered over a period of "(63 x 8) + (36 x 6)" = 720 STS-1 (or 51.84MHz) clock periods.

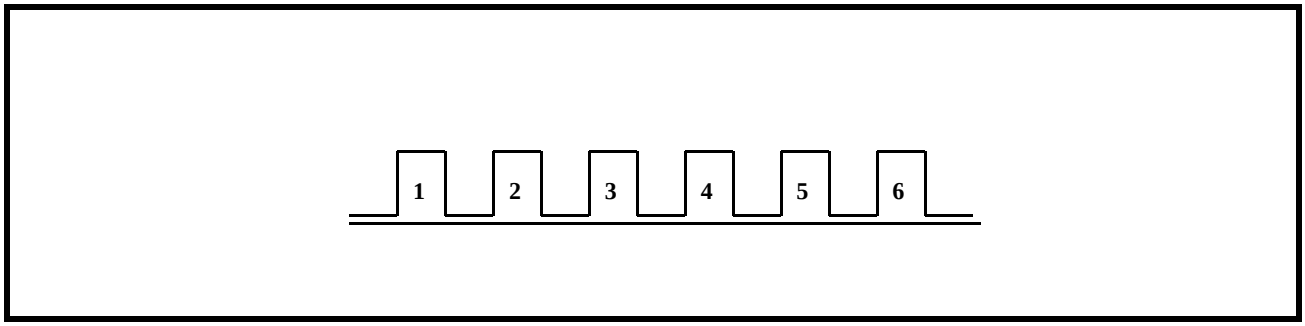
MAJOR PATTERN B

MAJOR PATTERN B consists of three sub or minor-patterns (which we will refer to as "MINOR PATTERNS P1, P2 and P3).

MINOR PATTERN P1, which is used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P1" as was presented above in Figure 37. Similarly, the MINOR PATTERN P2, which is also used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P2" as was presented in Figure 38.

MINOR PATTERN P3 (which has yet to be defined) consists of a string of six (6) clock pulses, which contains no gaps. An illustration of MINOR PATTERN P3 is presented below in Figure 68.

FIGURE 68. ILLUSTRATION OF MINOR PATTERN P3



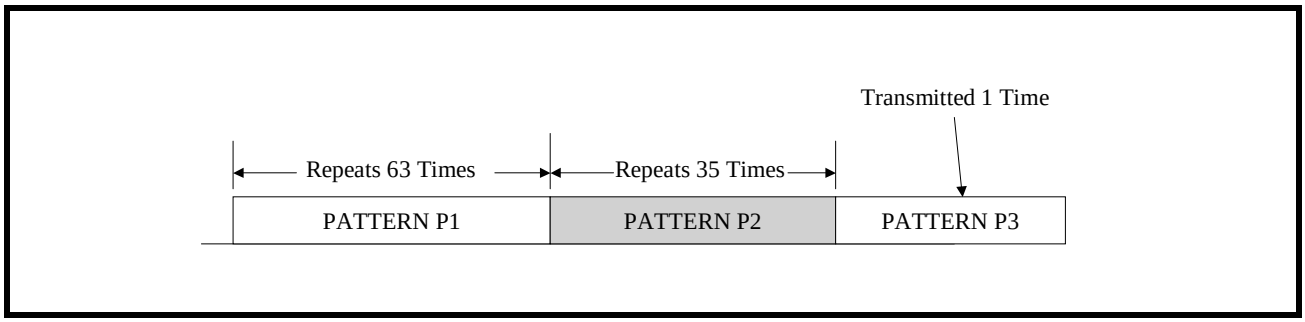
HOW MAJOR PATTERN B IS SYNTHESIZED

MAJOR PATTERN B is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.
- pon completion of the 35th transmission of MINOR PATTERN P2, MINOR PATTERN P3 is transmitted once.

Figure 69 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN B.

FIGURE 69. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE PATTERN B



Hence, MAJOR PATTERN B consists of "(63 x 7) + (35 x 5)" + 6 = 622 clock pulses.

These 622 clock pulses were delivered over a period of "(63 x 8) + (35 x 6) + 6 = 720 STS-1 (or 51.84MHz) clock periods.

PUTTING THE PATTERNS TOGETHER

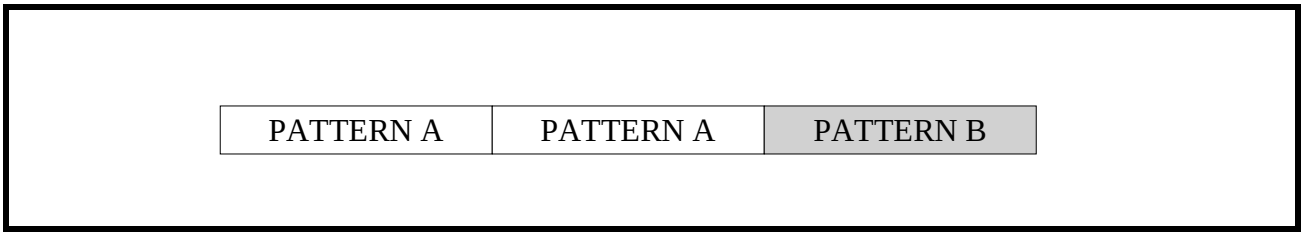
Finally, the DS3 to OC-N Mapper IC clock output is reproduced by doing the following.

- MAJOR PATTERN A is transmitted two times (repeatedly).
- After the second transmission of MAJOR PATTERN A, MAJOR PATTERN B is transmitted once.
- Then the whole process repeats.

Throughout the remainder of this document, we will refer to this particular pattern as the "SUPER PATTERN".

Figure 70 presents an illustration of this "SUPER PATTERN" which is output via the Mapper IC.

FIGURE 70. ILLUSTRATION OF THE SUPER PATTERN WHICH IS OUTPUT VIA THE "OC-N TO DS3" MAPPER IC



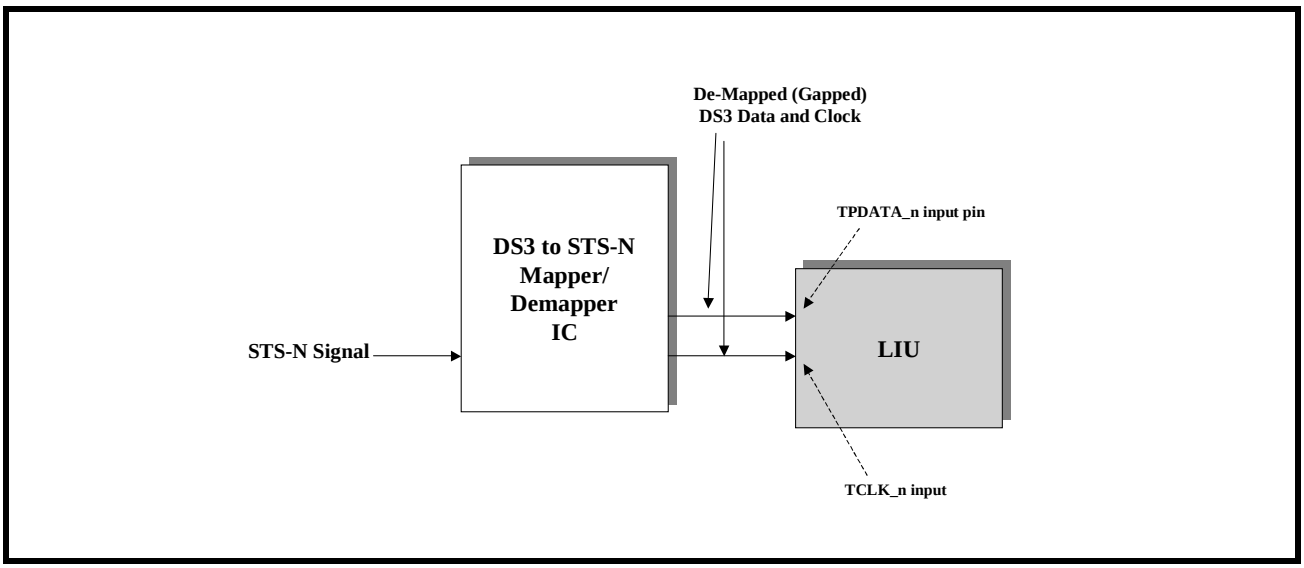
CROSS-CHECKING OUR DATA

- Each SUPER PATTERN consists of (621 + 621 + 622) = 1864 clock pulses.
- The total amount of time, which is required for the "DS3 to OC-N Mapper" IC to transmit this SUPER PATTERN is (720 + 720 + 720) = 2160 "STS-1" clock periods.
- This amount to a period of (2160/51.84MHz) = 41,667ns.
- In a period of 41, 667ns, the LIU (when configured to operate in the DS3 Mode), will output a total (41,667ns x 44,736,000) = 1864 uniformly spaced DS3 clock pulses.
- Hence, the number of clock pulses match.

APPLYING THE SUPER PATTERN TO THE LIU

Whenever the LIU is configured to operate in a "SONET De-Sync" application, the device will accept a continuous string of the above-defined SUPER PATTERN, via the TCLK input pin (along with the corresponding data). The channel within the LIU (which will be configured to operate in the "DS3" Mode) will output a DS3 line signal (to the DS3 facility) that complies with the "Category I Intrinsic Jitter Requirements - per Telcordia GR-253-CORE (for DS3 applications). This scheme is illustrated below in Figure 71.

FIGURE 71. SIMPLE ILLUSTRATION OF THE LIU BEING USED IN A SONET DE-SYNCHRONIZER" APPLICATION



8.8.3 How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?

Telcordia GR-253-CORE, Section 5.3.3.3 mandates that the "APS Completion" (or Recovery) time be 50ms or less. Many of our customers interpret this particular requirement as follows.

"From the instant that an APS is initiated on a high-speed SONET signal, all lower-speed SONET traffic (which is being transported via this "high-speed" SONET signal) must be fully restored within 50ms. Similarly, if the "high-speed" SONET signal is transporting some PDH signals (such as DS1 or DS3, etc.), then those entities

that are responsible for acquiring and maintaining DS1 or DS3 frame synchronization (with these DS1 or DS3 data-streams that have been de-mapped from SONET) must have re-acquired DS1 or DS3 frame synchronization within 50ms" after APS has been initiated."

The LIU was designed such that the DS3 signals that it receives from a SONET Mapper device and processes will comply with the Category I Intrinsic Jitter requirements per Telcordia GR-253-CORE.

Reference 1 documents some APS Recovery Time testing, which was performed to verify that the Jitter Attenuator blocks (within the LIU) device that permit it to comply with the Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE, do not cause it to fail to comply with the "APS Completion Time" requirements per Section 5.3.3.3 of Telcordia GR-253-CORE. However, Table 3 presents a summary of some APS Recovery Time requirements that were documented within this test report.

Table 3,

TABLE 48: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET

DS3 PPM OFFSET (PER W&G ANT-20SE)	MEASURED APS RECOVERY TIME (PER LOGIC ANALYZER)
-99 ppm	1.25ms
-40ppm	1.54ms
-30 ppm	1.34ms
-20 ppm	1.49ms
-10 ppm	1.30ms
0 ppm	1.89ms
+10 ppm	1.21ms
+20 ppm	1.64ms
+30 ppm	1.32ms
+40 ppm	1.25ms
+99 ppm	1.35ms

NOTE: *The APS Completion (or Recovery) time requirement is 50ms.*

Configuring the LIU to be able to comply with the SONET APS Recovery Time Requirements of 50ms

Quite simply, the user can configure a given Jitter Attenuator block (associated with a given channel) to (1) comply with the "APS Completion Time" requirements per Telcordia GR-253-CORE, and (2) also comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 applications) by making sure that Bit 4 (SONET APS Recovery Time Disable Ch_n), within the Jitter Attenuator Control Register is set to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: *The user can only disable the "SONET APS Recovery Time Mode" if the LIU is operating in the Host Mode. If the user is operating the LIU in the Hardware Mode, then the user will have NO ability to disable the "SONET APS Recovery Time Mode" feature.*

8.8.4 How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

Daisy-Chain testing is emerging as a new requirements that many of our customers are imposing on our SONET Mapper and LIU products. Many System Designer/Manufacturers are finding out that whenever their end-customers that are evaluating and testing out their systems (in order to determine if they wish to move forward and start purchasing this equipment in volume) are routinely demanding that they be able to test out these systems with a single piece of test equipment. This means that the end-customer would like to take a single piece of DS3 or STS-1 test equipment and (with this test equipment) snake the DS3 or STS-1 traffic (that this test equipment will generate) through many or (preferably all) channels within the system. For example, we have had request from our customers that (on a system that supports OC-192) our silicon be able to support this DS3 or STS-1 traffic snaking through the 192 DS3 or STS-1 ports within this system.

After extensive testing, we have determined that the best approach to complying with test "Daisy-Chain" Testing requirements, is to configure the Jitter Attenuator blocks (within each of the Channels within the LIU) into the "32-Bit" Mode. The user can configure the Jitter Attenuator block (within a given channel of the LIU) to operate in this mode by settings in the table below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	0

REFERENCES

1. TEST REPORT - AUTOMATIC PROTECTION SWITCHING (APS) RECOVERY TIME TESTING WITH THE XRT94L43 DS3/E3/STS-1 TO STS-12 MAPPER IC - Revision C Silicon

9.0 ELECTRICAL CHARACTERISTICS

TABLE 49: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
Theta JA	Thermal Resistance		23	$^0C/W$	linear air flow 0ft/min (See Note 3 below)
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating	2000		V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*
3. *With Linear Air flow of 200 ft/min, reduce Theta JA by 20%, Theta JC is unchanged.*

TABLE 50: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current requirements		TBD	TBD	mA
P_{DD}	Power Dissipation		TBD	TBD	W
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

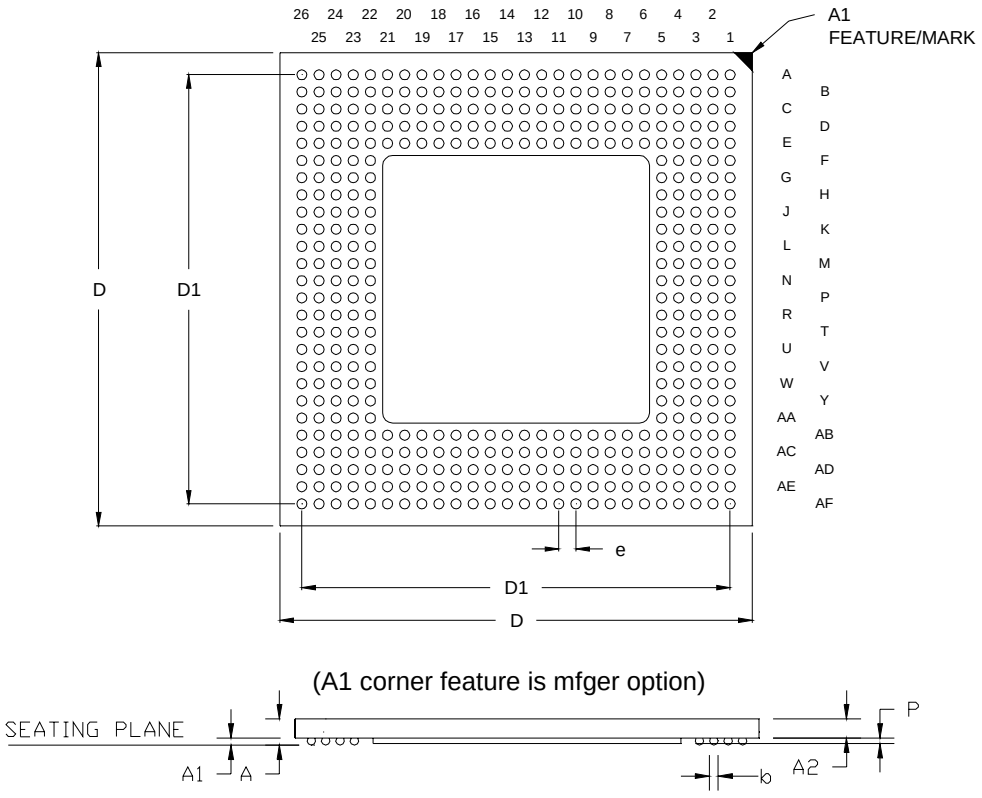
1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs are TTL 5V compliant.*

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R12DIB	420 TBGA	-40°C to +85°C

PACKAGE DIMENSIONS -

420 Tape Ball Grid Array
(35 mm x 35 mm, TBGA)
Rev. 1.00



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.051	0.067	1.30	1.70
A1	0.020	0.028	0.50	0.70
A2	0.031	0.039	0.80	1.00
D	1.370	1.386	34.80	35.20
D1	1.5000 BSC		38.10 BSC	
b	0.024	0.035	0.60	0.90
e	0.0500 BSC		1.27 BSC	
P	0.006	0.012	0.15	0.30

REVISIONS

REVISION	DATE	COMMENTS
P1.0.0	09/22/03	Original
P1.0.1	10/30/03	Added Pull-Up resistor information for $\overline{RDY}$ and $\overline{INT}$.

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