SONY

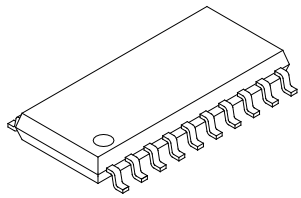
CXD1268M

CCD Vertical Clock Driver

Description

The CXD1268M is a clock driver for CCD vertical register drive.

20 pin SOP (Plastic)



Features

- On-chip 4-channel driver.
  (Binary driver × 2, and trinary driver × 2)
- Low output ON resistance provides optimal drive for large load capacity CCD.

Applications

CCD cameras

Structure

CMOS

Absolute Maximum Ratings (GND = 0V, Ta = 25°C)

• Supply voltage	V_H	V_L to V_L + 25	V
• Supply voltage	V_M	V_L to V_L + 17*1	V
• Supply voltage	V_{DD}	GND to GND + 7	V
• Supply voltage	V_L	GND – 10 to GND	V
• Input voltage	V_I	–0.5 to V_{DD} + 0.5	V
• Input/output clamp diode current	I_{IC}, I_{OC}	–10 to +10	mA
• Maximum DC load current	I_{ODC}	–3 to +3	mA
• Maximum load capacity	C_L	to 30,000	pF/pin
• Allowable power dissipation	P_D	to 200	mW
• Storage temperature	Tstg	–60 to +150	°C

*1 Use V_M at less than V_{DD}.

Recommended Operating Conditions

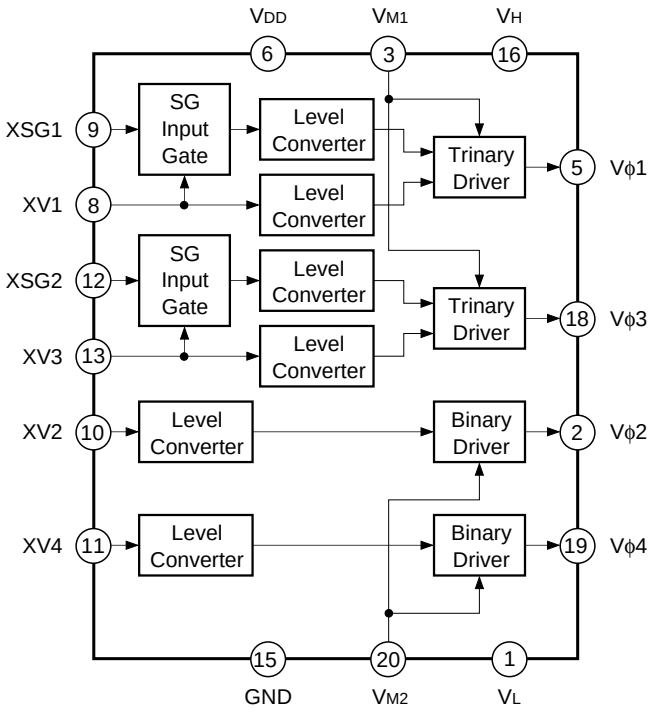
• Supply voltage	V_H	V_M + 6.5 to V_M + 15.5	V
• Supply voltage	V_L	V_M – 10.0 to V_M – 7.0	V
• Supply voltage	V_M	0.0 to 4.0	V
• Supply voltage	V_{DD}	4.75 to 5.25	V
• High level input voltage	V_{IH}*2	3.5 to V_{DD}	V
• Low level input voltage	V_{IL}*2	0.0 to 1.0	V
• Operating temperature	Topr	–10 to +60	°C

*2 V_{DD} = 5V

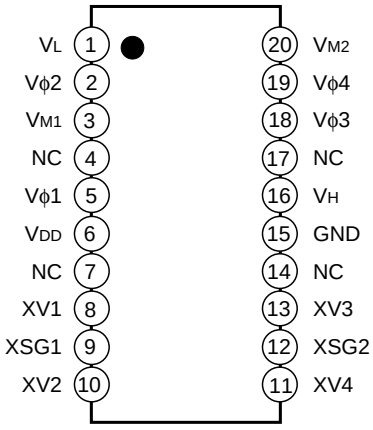
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E96635-PS

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	V_L	—	Low level power supply
2	Vϕ2	O	High-voltage output (2 levels: V_{M2}, V_L)
3	V_{M1}	—	Middle level power supply for trinary
4	NC		
5	Vϕ1	O	High-voltage output (3 levels: V_H, V_{M1}, V_L)
6	V_{DD}	—	Input section power supply
7	NC		
8	XV1	I	Output control (Vϕ1)
9	XSG1	I	Output control (Vϕ1)
10	XV2	I	Output control (Vϕ2)
11	XV4	I	Output control (Vϕ4)
12	XSG2	I	Output control (Vϕ3)
13	XV3	I	Output control (Vϕ3)
14	NC		
15	GND	—	GND
16	V_H	—	High level power supply for trinary
17	NC		
18	Vϕ3	O	High-voltage output (3 levels: V_H, V_{M1}, V_L)
19	Vϕ4	O	High-voltage output (2 levels: V_{M2}, V_L)
20	V_{M2}	—	Middle level power supply for binary

Truth Table

X: Don't care

Input			Output	
XV1, XV3	XSG1, XSG2	XV2, XV4	Vϕ1, Vϕ3	Vϕ2, Vϕ4
H	L	X	V_L	X
H	H	X	V_L	X
L	L	X	V_H	X
L	H	X	V_{M1}	X
X	X	L	X	V_{M2}
X	X	H	X	V_L

Electrical Characteristics

1. DC Characteristics

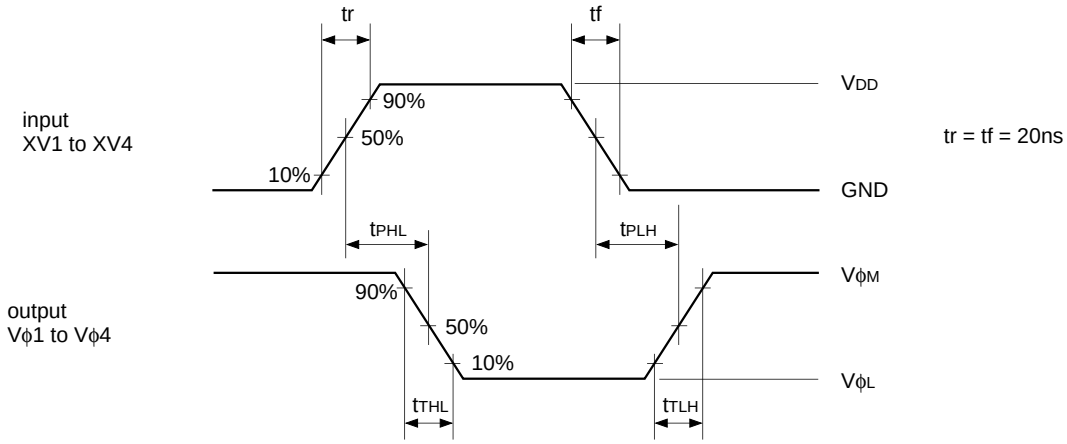
(Unless otherwise specified, V_H = 14.5V, V_M = 1V, V_{DD} = 5V, GND = 0V, V_L = –6V, V_{IL} = GND, V_{IH} = V_{DD}, Ta = –10 to +60°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level output voltage	$V\phi_H$	$I\phi_H$ = –1mA	V_H – 0.1		V_H	V
"M" level output voltage	$V\phi_M$	$I\phi_M$ = –1mA	V_M – 0.1		V_M	V
"L" level output voltage	$V\phi_L$	$I\phi_L$ = 1mA	V_L		V_L + 0.1	V
Input current	I_I				1.0	µA
"H" level output ON resistance	Ron (H)	$I\phi_H$ = –50mA		18	30	Ω
"M" level output ON resistance	Ron (M)	$I\phi_M$ = –50mA		18	30	Ω
"L" level output ON resistance	Ron (L)	$I\phi_L$ = 50mA		18	30	Ω
Static current consumption	$I_{DD} + I_H + I_M$			10^{-4}	100	µA

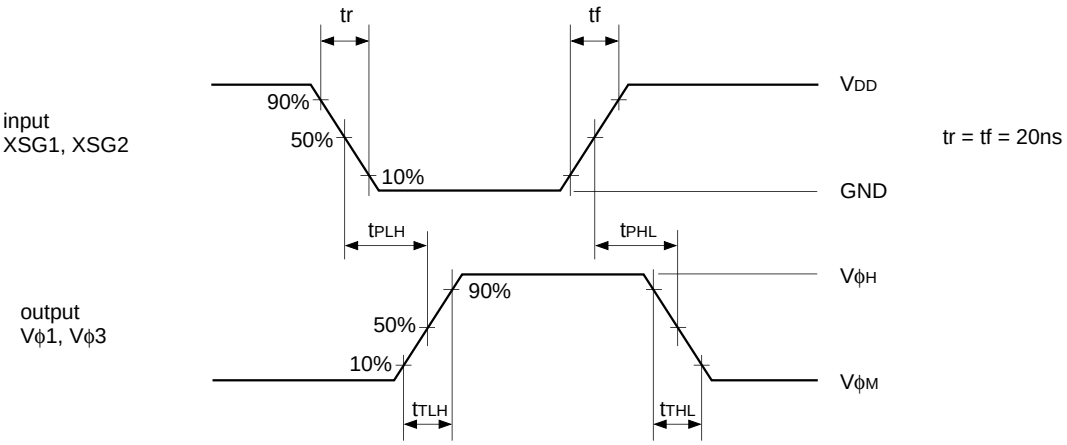
2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time L → M, M → L	t_{PLH}, t_{PHL}	Waveform diagram (1), no load		100	200	ns
Propagation delay time M → H, H → M	t_{PLH}, t_{PHL}	Waveform diagram (2), no load		200	400	ns
Rise time L → M Fall time M → L	t_{TLH}, t_{THL}	Refer to waveform diagram (1), output load circuit diagram		200	300	ns
Rise time M → H Fall time H → M	t_{TLH}, t_{THL}	Refer to waveform diagram (2), output load circuit diagram		200	300	ns
Operating current consumption	Idyn ($I_{DD} + I_H + I_M + I_L$)	Refer to input pulse timing diagram, output load circuit diagram		6.0	10.0	mA
	I_{DD}			0.02	0.2	mA
	$I_H + I_M$			3.8	5.0	mA
	I_L		–5.0	–3.8		mA

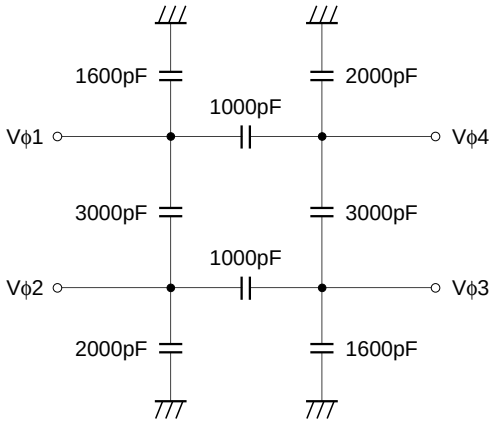
Waveform Diagram (1)



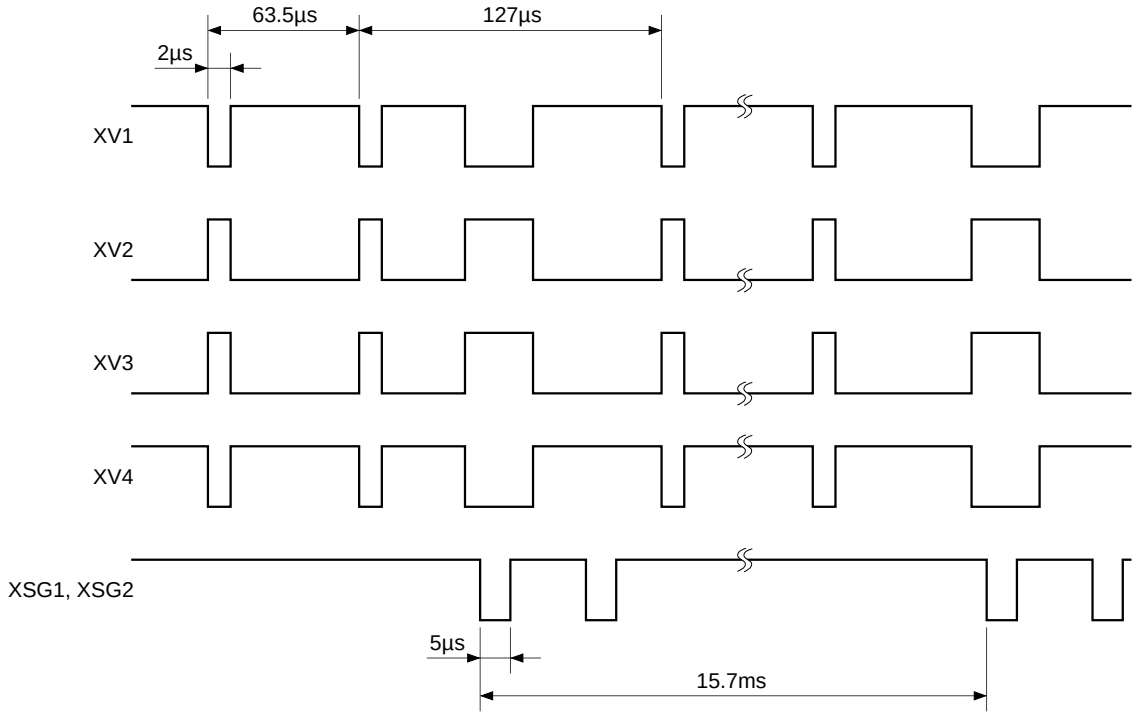
Waveform Diagram (2)



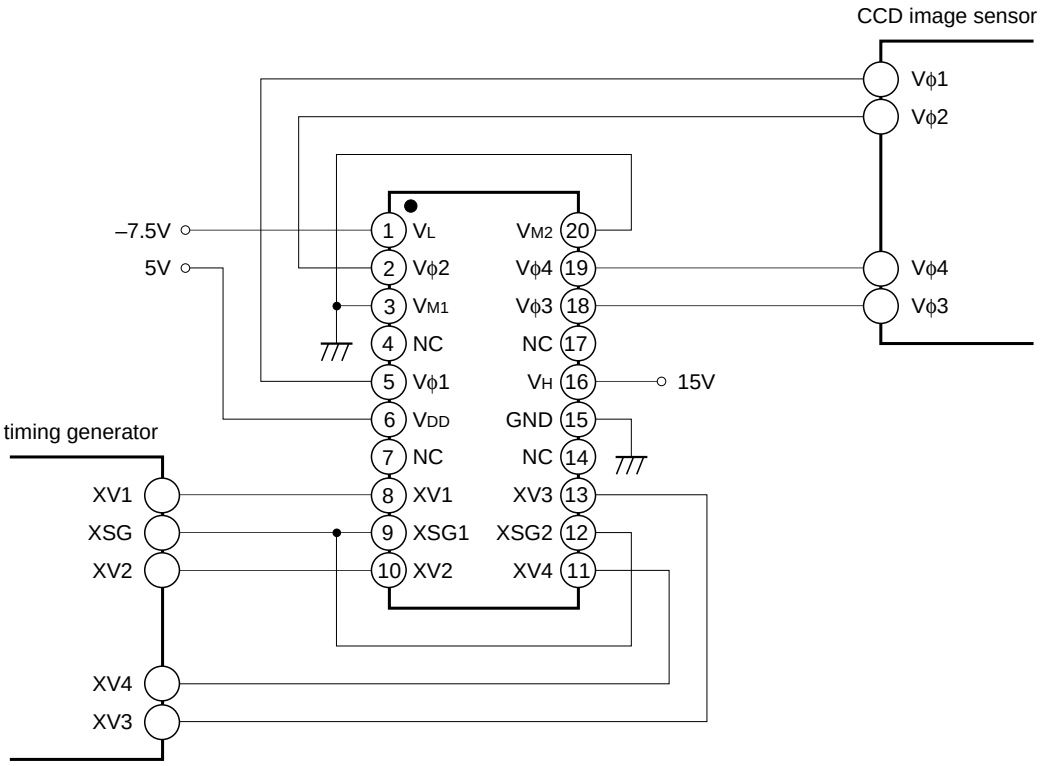
Output Load Circuit Diagram



Input Pulse Timing Diagram



Application Circuit



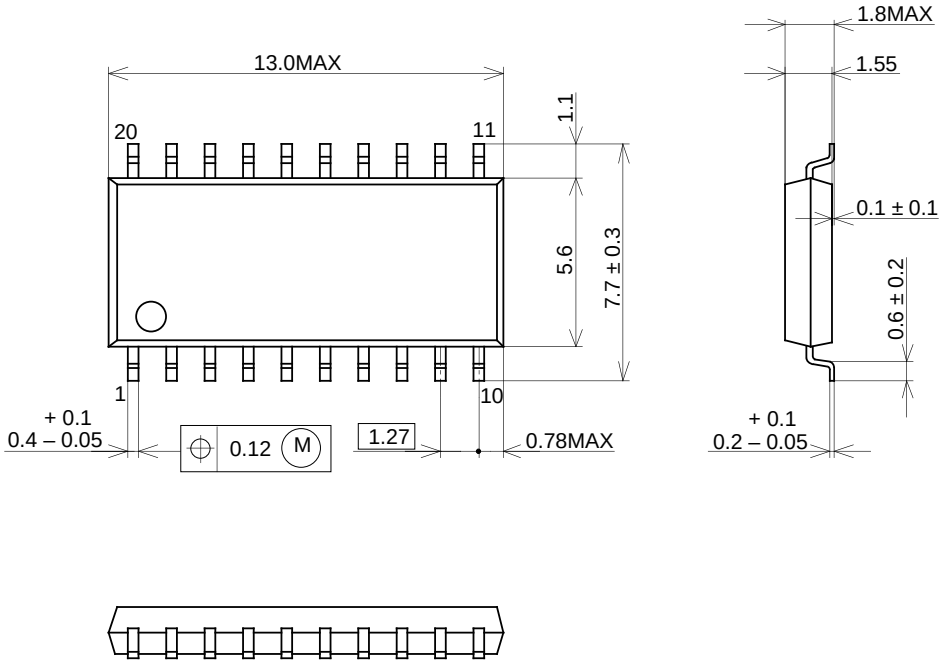
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. When applying power, be sure to apply V_H before V_{DD} and V_M.
2. XSG1 (Pin 9) and XSG2 (Pin 12) can be input separately, although they are also common input.

Package Outline Unit: mm

20PIN SOP (PLASTIC)



SONY CODE	SOP-20P-L071
EIAJ CODE	SOP020-P-0300
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g