FET BIAS CONTROLLER

ZNBG4000 ZNBG4001
ZNBG6000 ZNBG6001

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DEVICE DESCRIPTION

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs, PMR, cellular telephones etc. with a minimum of external components.

With the addition of two capacitors and resistors the devices provide drain voltage and current control for a number of external grounded source FETs, generating the regulated negative rail required for FET gate biasing whilst operating from a single supply. This negative bias, at -3 volts, can also be used to supply other external circuits.

The ZNBG4000/1 and ZNBG6000/1 contain four and six bias stages respectively. In setting drain current the ZNBG4000/1 two resistors allows individual FET pair control to different levels, the ZNBG6000/1 two resistors split control between two and four FETs. This allows the operating current of input FETs to be adjusted to minimise noise, whilst the following FET stages can separately be adjusted for maximum gain. The series also offers the choice of drain voltage to be set for the FETs, the ZNBG4000/6000 gives 2.2 volts drain whilst the ZNBG4001/6001 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 0.7V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The ZNBG4000/1 and ZNBG6000/1 are available in QSOP16 and 20 pin packages respectively for the minimum in devices size. Device operating temperature is -40 to 70°C to suit a wide range of environmental conditions.

FEATURES

- Provides bias for GaAs and HEMT FETs
- Drives up to four or six FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- QSOP surface mount package

APPLICATIONS

- Satellite receiver LNBs
- Private mobile radio (PMR)
- Cellular telephones

ZNBG4000 ZNBG4001
ZNBG6000 ZNBG6001

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.6V to 15V
Supply Current	100mA
Drain Current (per FET) (set by R_{CAL1} and R_{CAL2})	0 to 15mA
Output Current	100mA
Operating Temperature	-40 to 70°C
Storage Temperature	-50 to 85°C

Power Dissipation (T_{amb}= 25°C)

QSOP16	500mW
QSOP20	650mW

ELECTRICAL CHARACTERISTICS TEST CONDITIONS (Unless otherwise stated): T_{amb}= 25°C, V_{CC}=5V, I_D=10mA (R_{CAL1}=33kΩ; R_{CAL2}=33kΩ)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CC}	Supply Voltage		5		12	V
I_{CC}	Supply Current ZNBG4000/1	I_{D1} to I_{D4}=0 I_{D1} to I_{D4}=10mA			10 50	mA mA
I_{CC}	Supply Current ZNBG6000/1	ID1 to I_{D6}=0 I_{D1} to I_{D6}=10mA			15 75	mA mA
V_{SUB}	Substrate Voltage (Internally generated)	I_{SUB}= 0 I_{SUB}= -200µA	-3.5	-3	-2 -2	V V
E_{ND} E_{NG}	Output Noise Drain Voltage Gate Voltage	C_G=4.7nF, C_D=10nF C_G=4.7nF, C_D=10nF			0.02 0.005	Vpkpk Vpkpk
f_O	Oscillator Freq.		200	350	800	kHz

DRAIN CHARACTERISTICS

I_D	Current		8	10	12	mA
	Current Change					
ΔI_{DV}	with V_{CC}	V_{CC}=5 to 12V		0.02		%/V
ΔI_{DT}	with T_j	T_j=-40 to +70°C		0.05		%/°C
V_D	Voltage ZNBG4000, ZNGB6000 ZNBG4001, ZNBG6001		 2 1.8	 2.2 2	 2.4 2.2	 V V
	Voltage Change					
ΔV_{DV}	with V_{CC}	V_{CC}= 5 to 12V		0.5		%/V
ΔV_{DT}	with T_j	T_j = -40 to +70°C		50		ppm

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
GATE CHARACTERISTICS						
I_{GO}	Output Current Range		-30		2000	μA
	Output Voltage ZNBG4000/1					
V_{OL}	Output Low	I_{D1} to I_{D4}=12mA I_{G1} to I_{G4}=0	-3.5		-2	V
		I_{D1} to I_{D4}=12mA I_{G1} to I_{G4}= -10μA	-3.5		-2	V
V_{OH}	Output High	I_{D1} to I_{D4}= 8mA I_{G1} to I_{G4}= 0	0		1	V
	Output Voltage ZNBG6000/1					
V_{OL}	Output Low	I_{D1} to I_{D6}=12mA I_{G1} to I_{G6}= 0	-3.5		-2	V
		I_{D1} to I_{D6}=12mA I_{G1} to I_{G6}= -10μA	-3.5		-2	V
V_{OH}	Output High	I_{D1} to I_{D6}= 8mA I_{G1} to I_{G6}= 0	0		1	V

Notes:

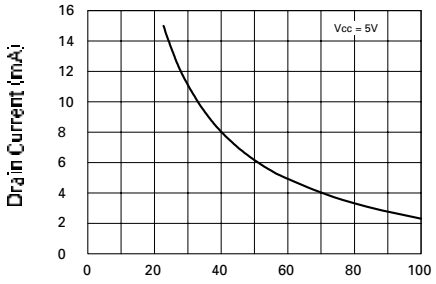
1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB}, of 47nF are required for this purpose.

2. The characteristics are measured using two external reference resistors R_{CAL1} and R_{CAL2} of value 33kΩ wired from pins $R_{CAL1/2}$ to ground. For the ZNBG4000, resistor R_{CAL1} sets the drain current of FETs 1 and 2, resistor R_{CAL2} sets the drain current of FETs 3 and 4. For the ZNBG6000, resistor R_{CAL1} sets the drain current of FETs 1 and 4, resistor R_{CAL2} sets the drain current of FETs 2, 3, 5 and 6.

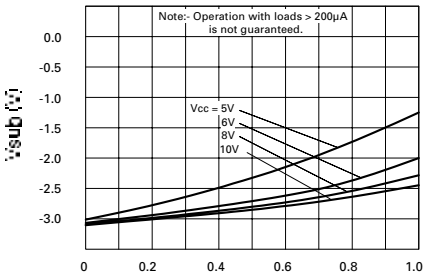
3. Noise voltage is not measured in production.

4. Noise voltage measurement is made with FETs and gate and drain capacitors in place on all outputs. C_G, 4.7nF, are connected between gate outputs and ground, C_D, 10nF, are connected between drain outputs and ground.

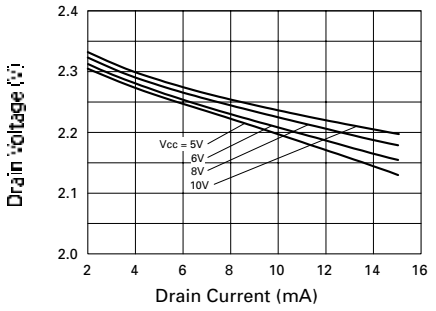
TYPICAL CHARACTERISTICS



JFET Drain Current v R_{cal}

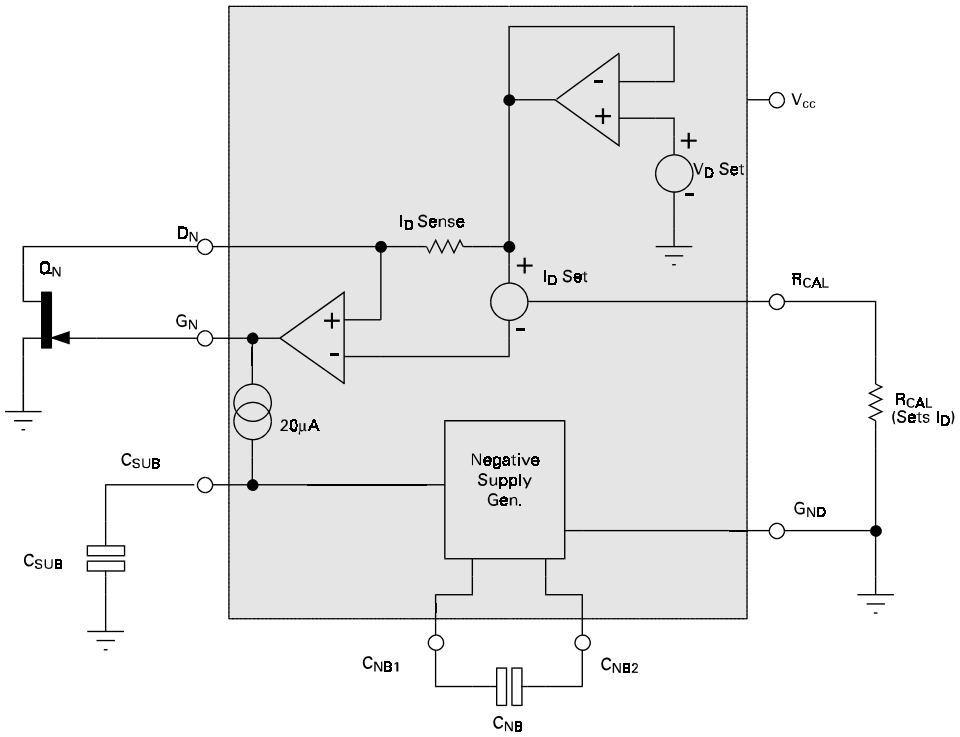


V_{sub} v External Load



JFET Drain Voltage v Drain Current

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The ZNBG devices provide all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage.

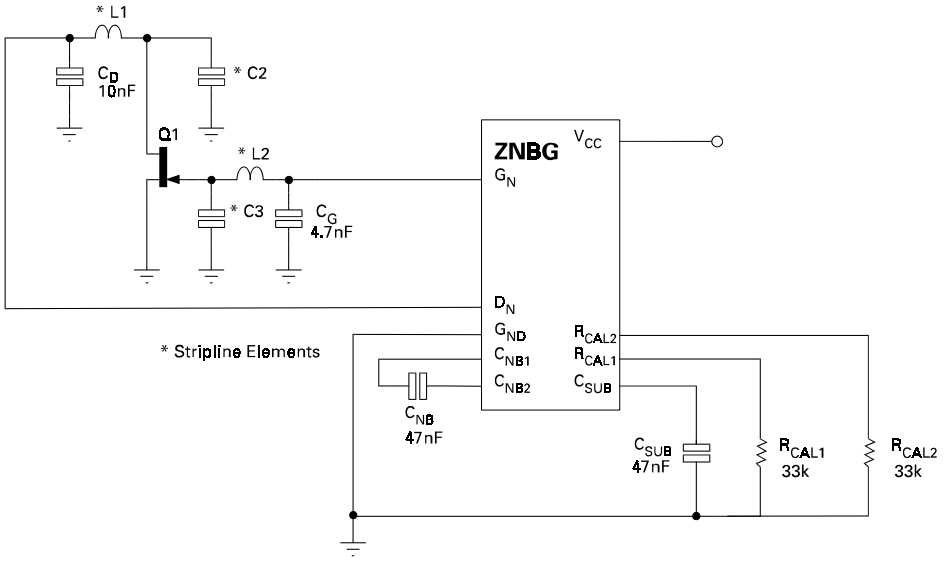
The diagram above shows a single stage from the ZNBG series. The ZNBG4000/1 contains 4 such stages, the ZNBG6000/1 contains 6. The negative rail generator is common to all devices.

The drain voltage of the external FET Q_N is set by the ZNBG device to its normal operating voltage. This is determined by the on board V_D Set reference, for the ZNBG4000/6000 this is nominally 2.2 volts whilst the ZNBG4001/6001 provides nominally 2 volts.

The drain current taken by the FET is monitored by the low value resistor I_D Sense. The amplifier driving the gate of the FET adjusts the gate voltage of Q_N so that the drain current taken matches the current called for by an external resistor R_{CAL}. Both ZNBG devices have the facility to program different drain currents into selected FETs. Two R_{CAL} inputs are provided. For the ZNBG4000, resistor R_{CAL1} sets the drain current of FETs 1 and 2, resistor R_{CAL2} sets the drain current of FETs 3 and 4. For the ZNBG6000, resistor R_{CAL1} sets the drain current of FETs 1 and 4, resistor R_{CAL2} sets the drain current of FETs 2, 3, 5 and 6.

Since the FET is a depletion mode transistor, it is usually necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, C_{NB} and C_{SUB}.

TYPICAL APPLICATION CIRCUIT



APPLICATIONS INFORMATION

The above is a partial application circuit for the ZNBG series showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit.

Capacitors C_D and C_G ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the ZNBG device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used.

The capacitors C_{NB} and C_{SUB} are an integral part of the ZNBGs negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors C_{NB} and C_{SUB} is 47nF. This generator produces a low current supply of approximately -3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the C_{SUB} pin.

Resistors $R_{CAL1/2}$ sets the drain current at which all external FETs are operated. Both ZNBG devices have the facility to program different drain currents into selected FETs. Two R_{CAL} inputs are provided. For the ZNBG4000, resistor R_{CAL1} sets the drain current of FETs 1 and 2, resistor R_{CAL2} sets the drain current of FETs 3 and 4. For the ZNBG6000, resistor R_{CAL1} sets the drain current of FETs 1 and 4, resistor R_{CAL2} sets the drain current of FETs 2, 3, 5 and 6. If the same drain current is required for all FETs on either device then pins R_{CAL1} and R_{CAL2} can be wired together and shunted to ground by a single calibration resistor of half normal value.

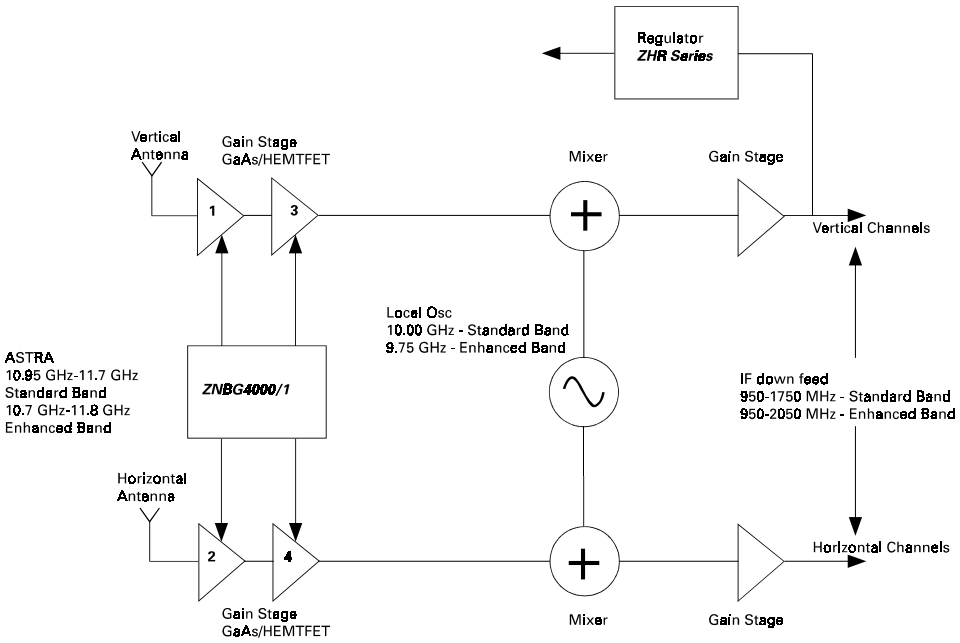
If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits. If all FETs associated with a current setting resistor are omitted, the particular R_{CAL} should still be included. The supply current can be reduced, if required, by using a high value R_{CAL} resistor (e.g. 470k).

APPLICATIONS INFORMATION (Continued)

The ZNBG devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.5V to 0.7V, under any conditions including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

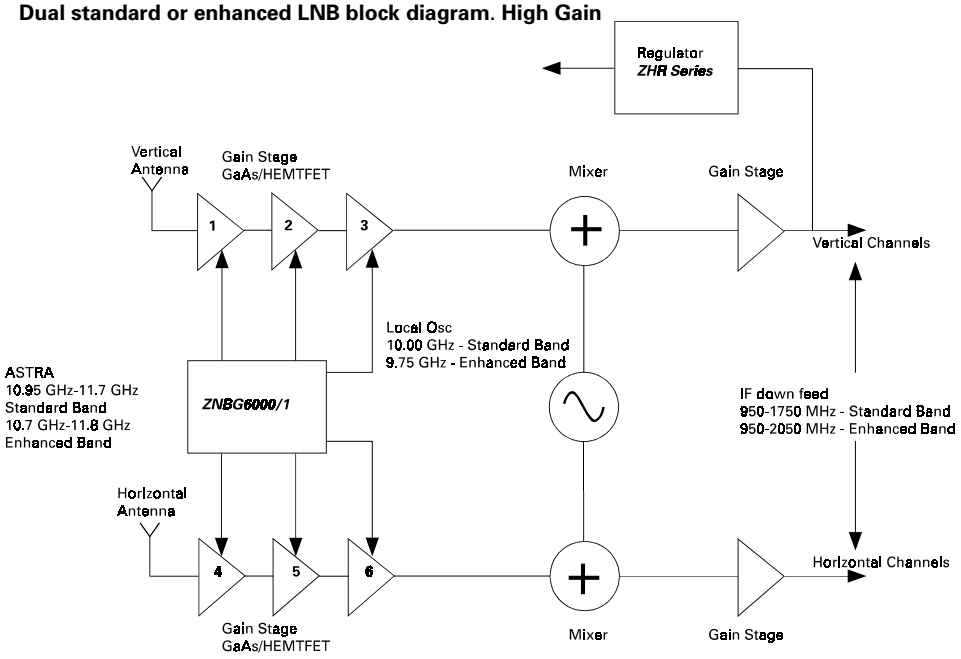
The following diagrams show the ZNBG4000/1 and ZNBG6000/1 in typical LNB applications. Within each FET gain stage the numbering system indicates how the bias stages relate to the application circuits. This is important when RCAL values are used to set differing drain currents.

Dual standard or enhanced LNB block diagram

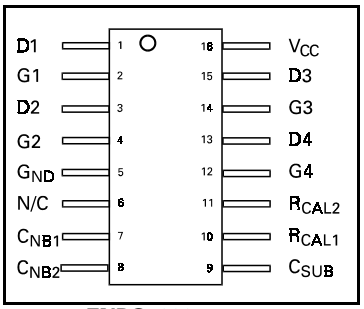


ZNBG4000 ZNBG4001
ZNBG6000 ZNBG6001

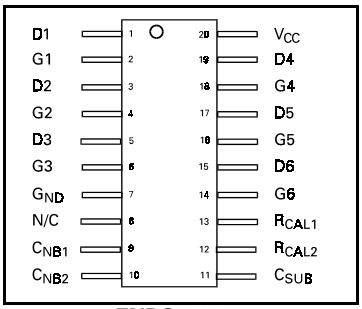
Dual standard or enhanced LNB block diagram. High Gain



CONNECTION DIAGRAMS



ZNBG4000
ZNBG4001



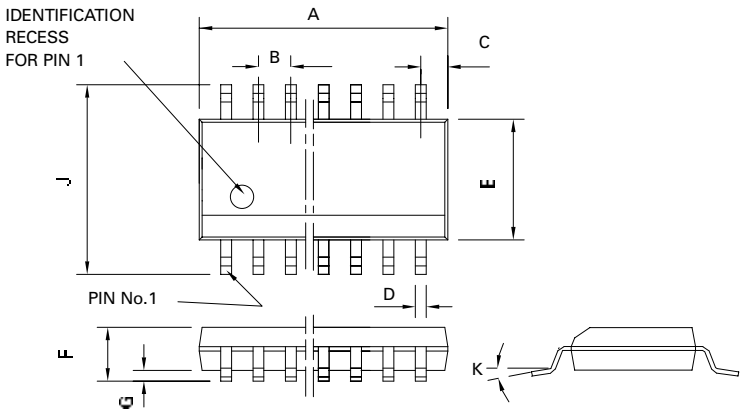
ZNBG6000
ZNBG6001

ORDERING INFORMATION

Part Number	Package	Part Mark
ZNBG4000Q16	QSOP16	ZNBG4000
ZNBG4001Q16	QSOP16	ZNBG4001
ZNBG6000Q20	QSOP20	ZNBG6000
ZNBG6001Q20	QSOP20	ZNBG6001

ZNBG4000 ZNBG4001
ZNBG6000 ZNBG6001

PACKAGE DIMENSIONS



QSOP16

PIN	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	4.80	4.90	0.033	0.039
B	0.635		0.025 NOM	
C	0.177	0.267	0.007	0.011
D	0.20	0.30	0.008	0.012
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.053	0.069
G	0.10	0.25	0.004	0.01
J	5.79	6.20	0.228	0.244
K	0°	8°	0°	8°

QSOP20

PIN	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	8.55	8.74	0.337	0.344
B	0.635		0.025 NOM	
C	1.42	1.52	0.056	0.06
D	0.20	0.30	0.008	0.012
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.053	0.069
G	0.10	0.25	0.004	0.01
J	5.79	6.20	0.228	0.244
K	0°	8°	0°	8°

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