HIGH-SPEED, LOW-NOISE, FULLY-DIFFERENTIAL I/O AMPLIFIERS

Check for Samples: THS4130, THS4131

FEATURES

- **High Performance**
  - **150 MHz, –3 dB Bandwidth (V_{CC} = ±15 V)**
  - **51 V/µs Slew Rate**
  - **–100 dB Third Harmonic Distortion at 250 kHz**
- **Low Noise**
  - **1.3 nV/√Hz Input-Referred Noise**
- **Differential-Input/Differential-Output**
  - **Balanced Outputs Reject Common-Mode Noise**
  - **Reduced Second-Harmonic Distortion Due to Differential Output**
- **Wide Power-Supply Range**
  - **V_{CC} = 5 V Single Supply to ±15 V Dual Supply**
- **$I_{CC(SD)}$ = 860 µA in Shutdown Mode (THS4130)**

APPLICATIONS

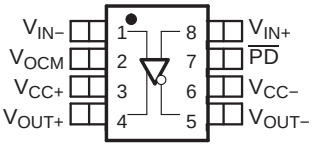
- **Single-Ended To Differential Conversion**
- **Differential ADC Driver**
- **Differential Antialiasing**
- **Differential Transmitter And Receiver**
- **Output Level Shifter**

DESCRIPTION

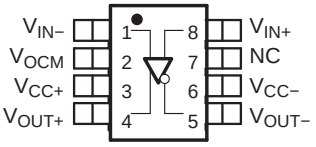
The THS413x is one in a family of fully-differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiComI complementary bipolar process.

The THS413x is made of a true fully-differential signal path from input to output. This design leads to an excellent common-mode noise rejection and improved total harmonic distortion.

THS4130
D, DGN, OR DGK PACKAGE
(TOP VIEW)



THS4131
D, DGN, OR DGK PACKAGE
(TOP VIEW)



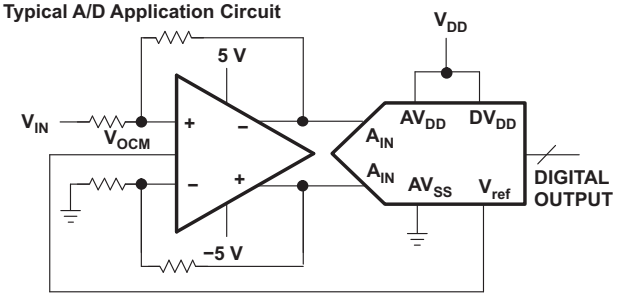
HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	SHUTDOWN
THS4130	1	X
THS4131	1	–

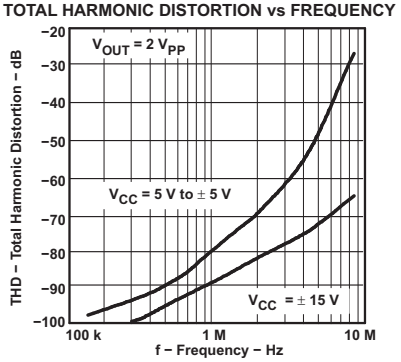
RELATED DEVICES

DEVICE	DESCRIPTION
THS412x	100 MHz, 43 V/µs, 3.7 nV/√Hz
THS414x	160 MHz, 450 V/µs, 6.5 nV/√Hz
THS415x	180 MHz, 850 V/µs, 9 nV/√Hz

Typical A/D Application Circuit



TOTAL HARMONIC DISTORTION vs FREQUENCY



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All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES					EVALUATION MODULES
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)	SYMBOL	MSOP (DGK)	SYMBOL	
0°C to +70°C	THS4130CD	THS4130CDGN	AOB	THS4130CDGK	ATP	THS4130EVM
	THS4131CD	THS4131CDGN	AOD	THS4131CDGK	ATQ	THS4131EVM
–40°C to +85°C	THS4130ID	THS4130IDGN	AOC	THS4130IDGK	ASO	—
	THS4131ID	THS4131IDGN	AOE	THS4131IDGK	ASP	—

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range,unless otherwise noted.

			UNIT
$V_{CC–}$ to V_{CC+}	Supply voltage		±33 V
V_I	Input voltage		$\pm V_{CC}$
I_O(2)	Output current		150 mA
V_{ID}	Differential input voltage		±6 V
	Continuous total power dissipation		See Dissipation Rating table
T_J(3)	Maximum junction temperature		+150°C
T_J(4)	Maximum junction temperature, continuous operation, long-term reliability		+125°C
T_A	Operating free-air temperature	C-suffix	0°C to +70°C
		I-suffix	–40°C to +85°C
T_{STG}	Storage temperature		–65°C to +150°C
	ESD ratings:	HBM	2500 V
		CDM	1500 V
		MM	200 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS413x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally-enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}(1) (°C/W)	θ_{JC} (°C/W)	POWER RATING(2)	
			T_A= +25°C	T_A = +85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	134	72	750 mW	300 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long-term reliability.

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RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±2.5		±15	V
	Single supply	5		30	
Operating free-air temperature, T_A	C-suffix	0		+70	°C
	I-suffix	–40		+85	

ELECTRICAL CHARACTERISTICS(1)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 1, R_f = 390 Ω		125		MHz
		V_{CC} = ±5	Gain = 1, R_f = 390 Ω		135		
		V_{CC} = ±15	Gain = 1, R_f = 390 Ω		150		
	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		
		V_{CC} = ±5	Gain = 2, R_f = 750 Ω		85		
		V_{CC} = ±15	Gain = 2, R_f = 750 Ω		90		
SR	Slew rate(2)	Gain = 1			52		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V, gain = 1			78		ns
	Settling time to 0.01%				213		ns
DISTORTION PERFORMANCE							
THD	Total harmonic distortion, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O= 2 V_{PP}	V_{CC} = 5	f = 250 kHz		–95		dBc
			f = 1 MHz		–81		
		V_{CC} = ±5	f = 250 kHz		–96		
			f = 1 MHz		–80		
		V_{CC} = ±15	f = 250 kHz		–97		
			f = 1 MHz		–80		
	V_O = 4 V_{PP}	V_{CC} = ±5	f = 250 kHz		–91		
			f = 1 MHz		–75		
		V_{CC} = ±15	f = 250 kHz		–91		
			f = 1 MHz		–75		
SFDR	Spurious-free dynamic range, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, f = 250 kHz	V_O= 2 V_{PP}	V_{CC} = ±2.5		97		dB
			V_{CC} = ±5		98		
			V_{CC} = ±15		99		
		V_O = 4 V_{PP}	V_{CC} = ±5		93		
			V_{CC} = ±15		95		
Third intermodulation distortion		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			–53		dBc
Third-order intercept		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz			1		pA/√Hz
DC PERFORMANCE							
Open-loop gain		T_A = +25°C		71	78		dB
		T_A = full range		69			
$V_{(OS)}$	Input offset voltage	T_A = +25°C			0.2	2	mV
		T_A = full range				3	
	Common-mode input offset voltage, referred to V_{OCM}	T_A = +25°C			0.2	3.5	
	Input offset voltage drift	T_A = full range			4.5		µV/°C
I_{IB}	Input bias current	T_A = full range			2	6	µA
I_{OS}	Input offset current	T_A = full range			100	500	nA
	Offset drift				2		nA/°C

(1) The full range temperature is 0°C to +70°C for the C-suffix, and –40°C to +85°C for the I-suffix.
(2) Slew rate is measured from an output level range of 25% to 75%.

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ELECTRICAL CHARACTERISTICS[1] (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		80	95		dB
V_{ICR}	Common-mode input voltage range			–3.77 to 4.3	–4 to 4.5		V
R_I	Input resistance	Measured into each input terminal			34		MΩ
C_I	Input capacitance, closed loop				4		pF
r_o	Output resistance	Open loop			41		Ω
OUTPUT CHARACTERISTICS							
Output voltage swing		V_{CC} = 5 V	T_A = +25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.3 to 3.7	±4		
		V_{CC} = ±5 V	T_A = +25°C	±3.7			
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = +25°C	±10.5	±12.4		
			T_A = full range	±10.2			
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = +25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = +25°C	30	55		
			T_A = full range	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = +25°C	60	85		
			T_A = full range	65			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		4		33	V
		Split supply		±2		±16.5	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = +25°C		12.3	15	mA
			T_A = full range			16	
		V_{CC} = ±15 V	T_A = +25°C		14		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)[3]	V = –5 V	T_A = +25°C		0.86	1.4	mA
			T_A = full range			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range	70			

(3) For detailed information on the behavior of the power-down circuit, see the *Power-Down Mode* section in the *Principles of Operation*.

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TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
	Small-signal frequency response		Figure 1, Figure 2
	Small-signal frequency response (various supplies)		Figure 3
	Small-signal frequency response (various C_F)		Figure 4
	Small-signal frequency response (various C_L)		Figure 5
	Large-signal transient response (differential in/single out)		Figure 6
	Large-signal frequency response		Figure 7
CMMR	Common-mode rejection ratio	vs Frequency	Figure 8
I_{CC}	Supply current	vs Free-air temperature	Figure 9
		vs Free-air temperature (shutdown state)	Figure 10
I_{IB}	Input bias current	vs Free-air temperature	Figure 11
	Settling time		Figure 12
PSRR	Power-supply rejection ratio	vs Frequency (differential out)	Figure 13
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THD	Total harmonic distortion	vs Frequency	Figure 15
	Second-harmonic distortion	vs Frequency	Figure 16, Figure 17
		vs Output voltage	Figure 18, Figure 19
	Third-harmonic distortion	vs Frequency	Figure 20, Figure 21
		vs Output voltage	Figure 22, Figure 23
V_n	Voltage noise	vs Frequency	Figure 24
I_n	Current noise	vs Frequency	Figure 25
$V_{(OS)}$	Input offset voltage	vs Common-mode output voltage	Figure 26
V_O	Output voltage	vs Differential load resistance	Figure 27
z_o	Output impedance	vs Frequency	Figure 28

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TYPICAL CHARACTERISTICS

SMALL-SIGNAL FREQUENCY RESPONSE

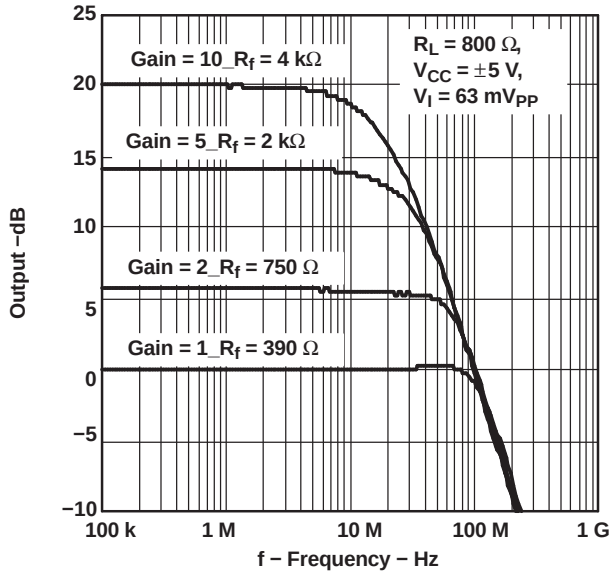


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

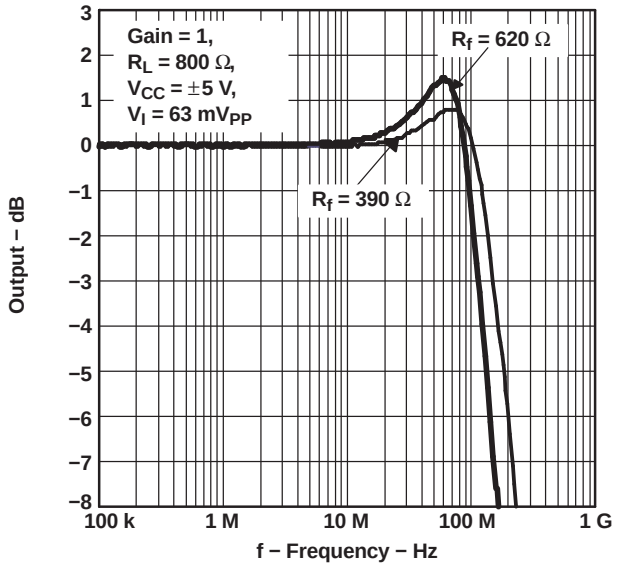


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE (VARIOUS SUPPLIES)

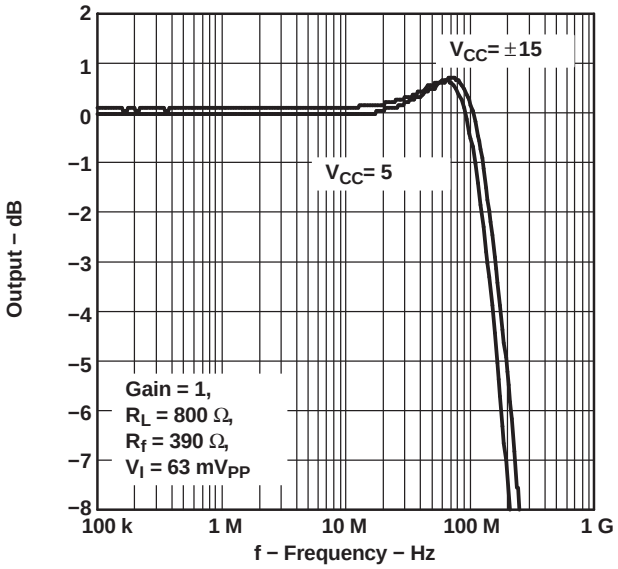


Figure 3.

SMALL-SIGNAL FREQUENCY RESPONSE (VARIOUS C_F)

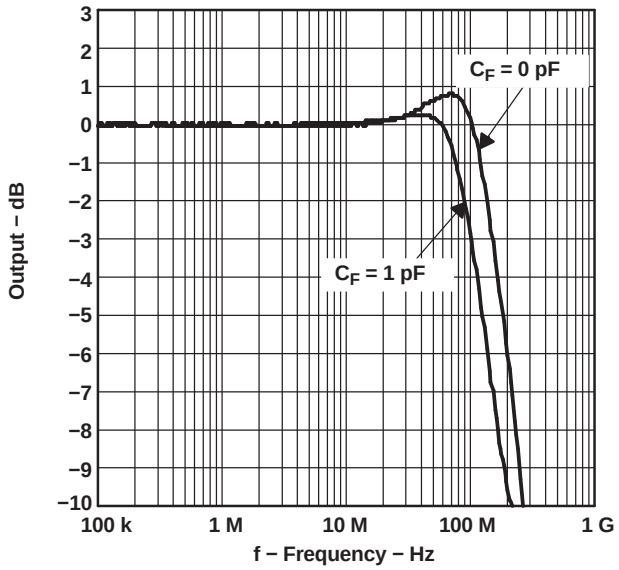


Figure 4.

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TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL FREQUENCY RESPONSE (VARIOUS C_L)

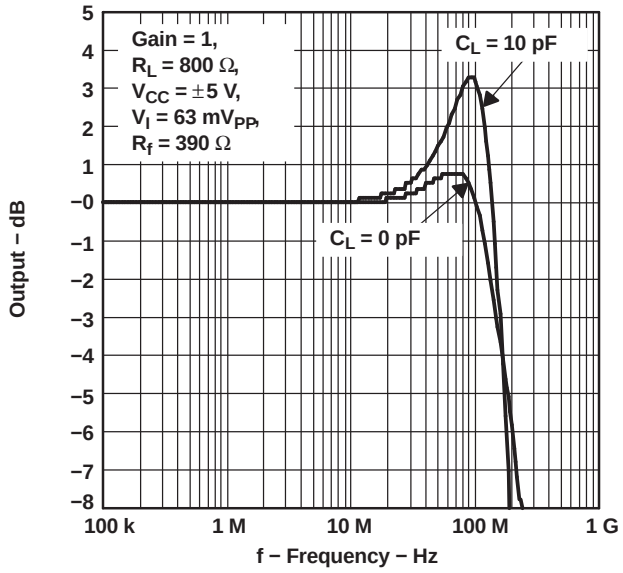


Figure 5.

LARGE-SIGNAL TRANSIENT RESPONSE (DIFFERENTIAL IN/SINGLE OUT)

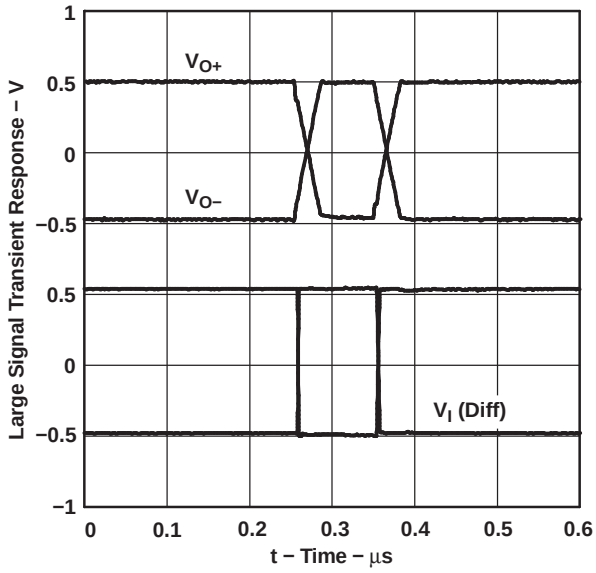


Figure 6.

LARGE-SIGNAL FREQUENCY RESPONSE

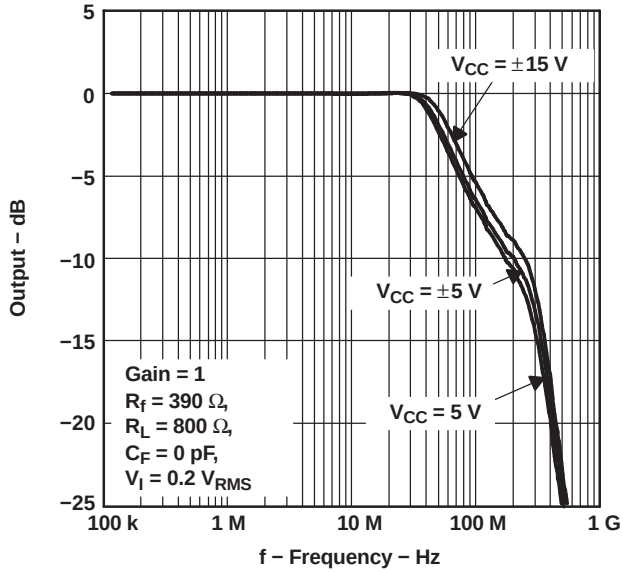


Figure 7.

COMMON-MODE REJECTION RATIO vs FREQUENCY

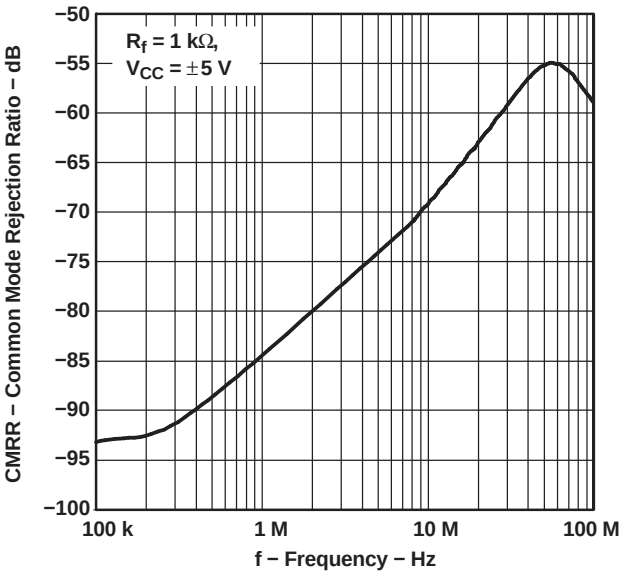


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

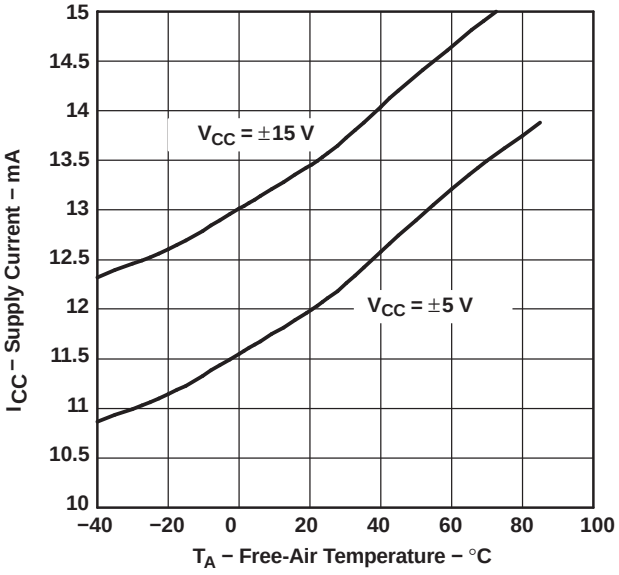


Figure 9.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE (SHUTDOWN STATE)

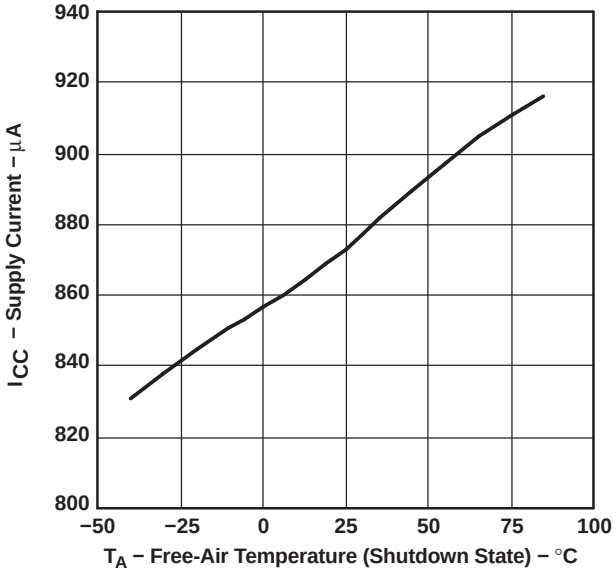


Figure 10.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

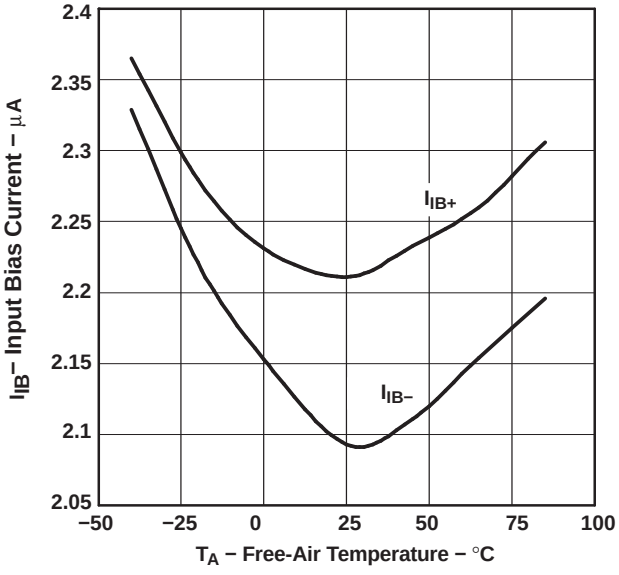


Figure 11.

SETTLING TIME

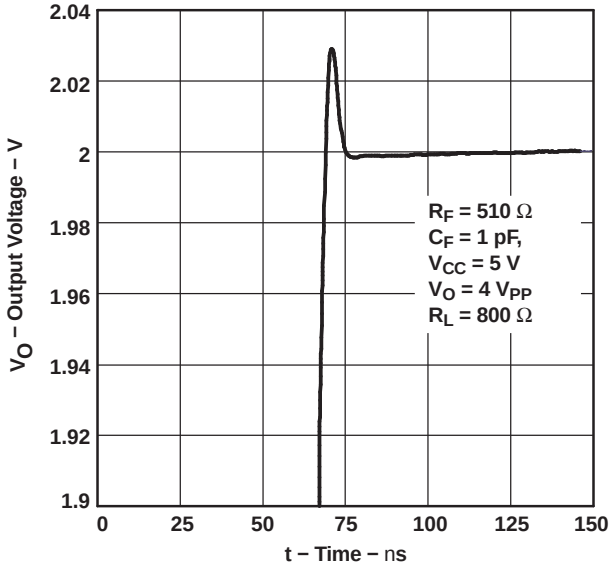


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (DIFFERENTIAL OUT)

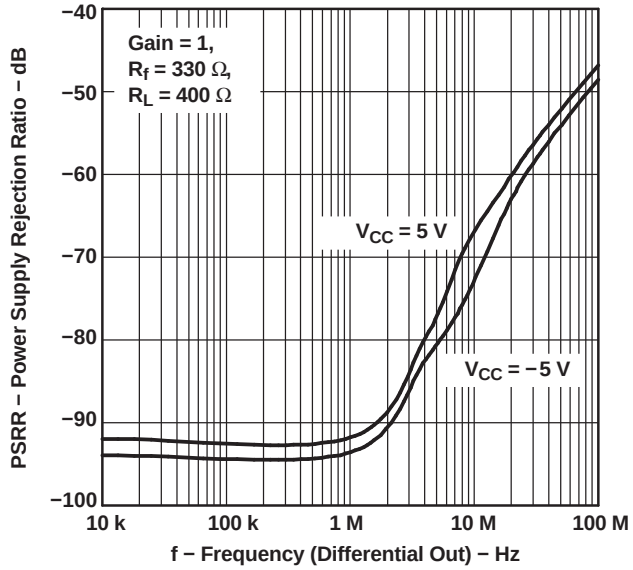


Figure 13.

LARGE-SIGNAL TRANSIENT RESPONSE

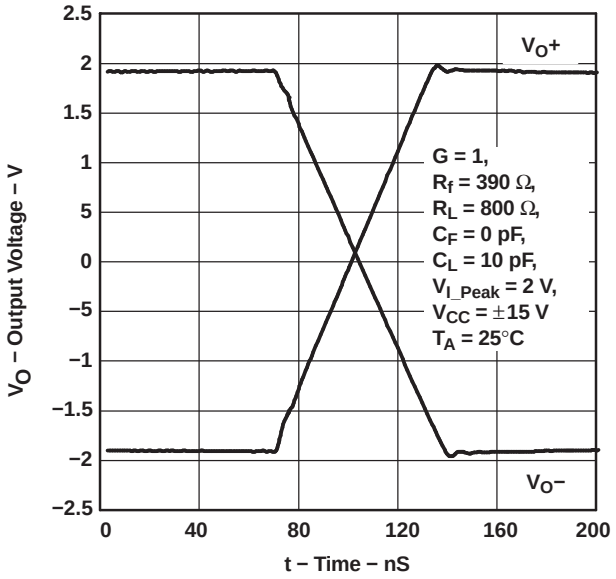


Figure 14.

TOTAL HARMONIC DISTORTION vs FREQUENCY

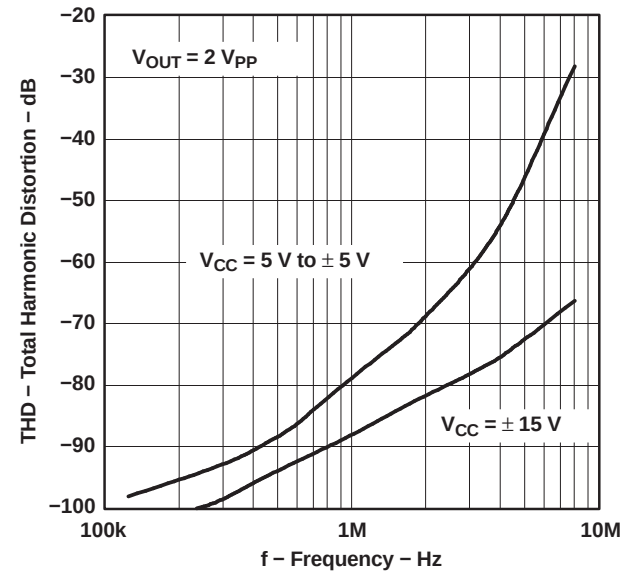


Figure 15.

SECOND-HARMONIC DISTORTION vs FREQUENCY

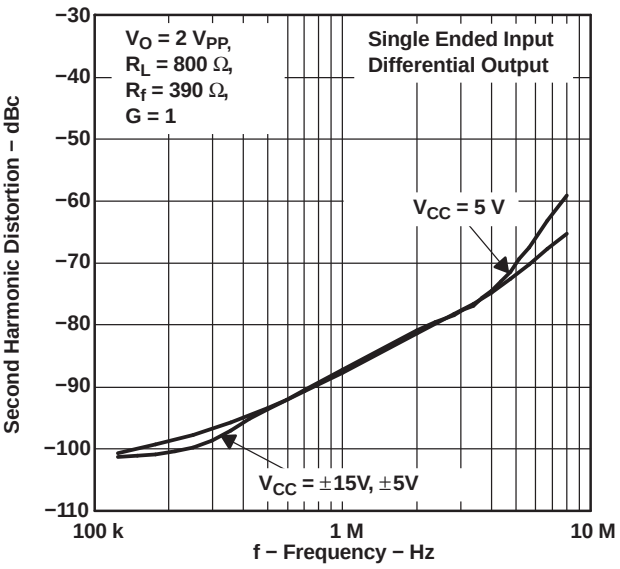


Figure 16.

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TYPICAL CHARACTERISTICS (continued)

SECOND-HARMONIC DISTORTION vs FREQUENCY

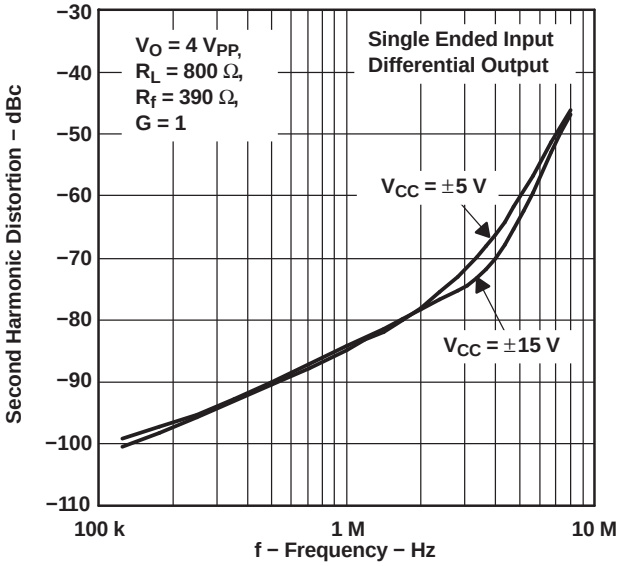


Figure 17.

SECOND-HARMONIC DISTORTION vs OUTPUT VOLTAGE

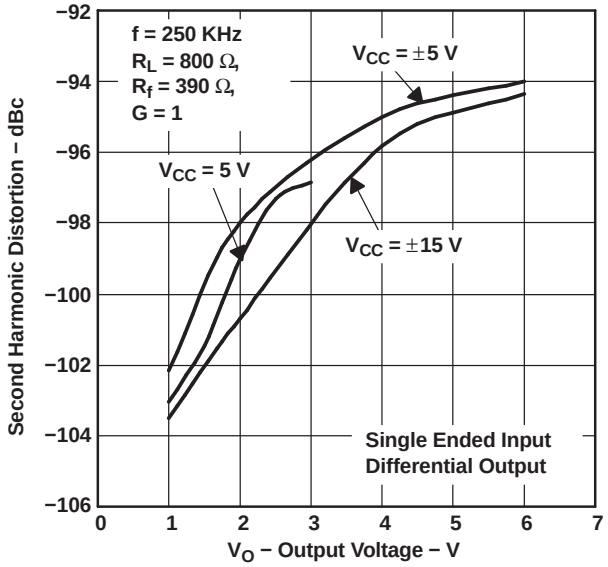


Figure 18.

SECOND-HARMONIC DISTORTION vs OUTPUT VOLTAGE

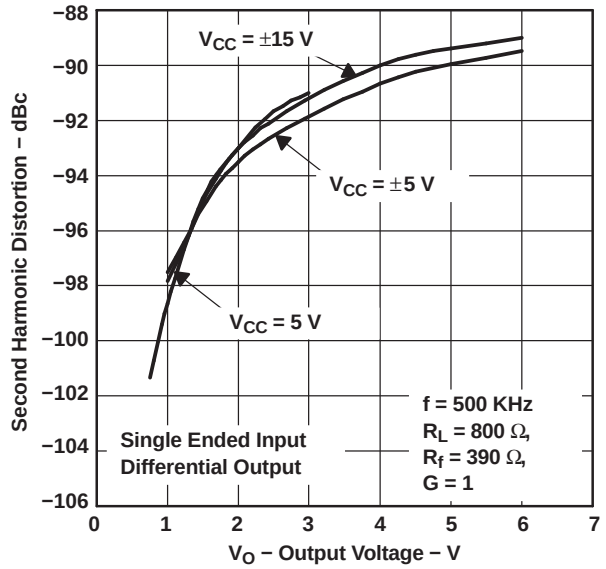


Figure 19.

THIRD-HARMONIC DISTORTION vs FREQUENCY

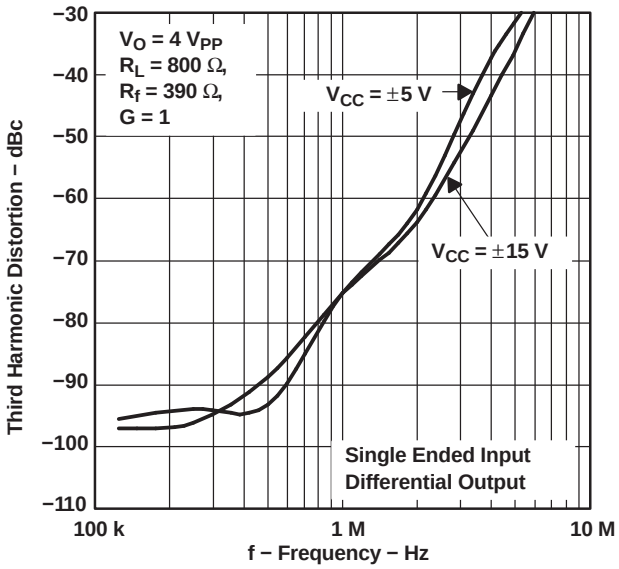


Figure 20.

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TYPICAL CHARACTERISTICS (continued)

THIRD-HARMONIC DISTORTION vs FREQUENCY

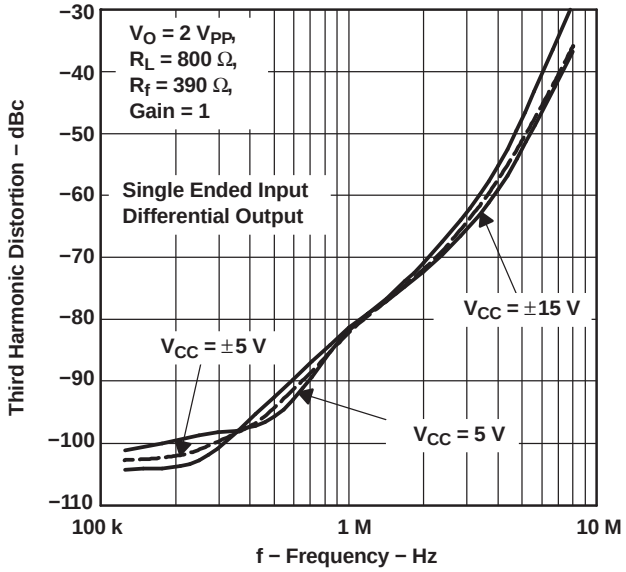


Figure 21.

THIRD-HARMONIC DISTORTION vs OUTPUT VOLTAGE

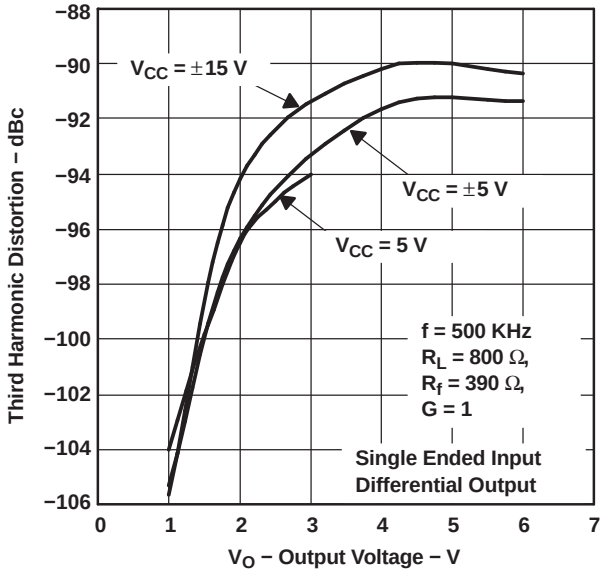


Figure 22.

THIRD-HARMONIC DISTORTION vs OUTPUT VOLTAGE

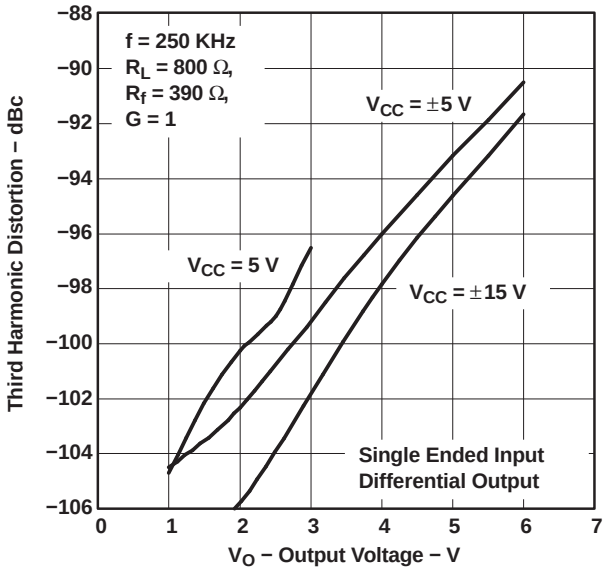


Figure 23.

VOLTAGE NOISE vs FREQUENCY

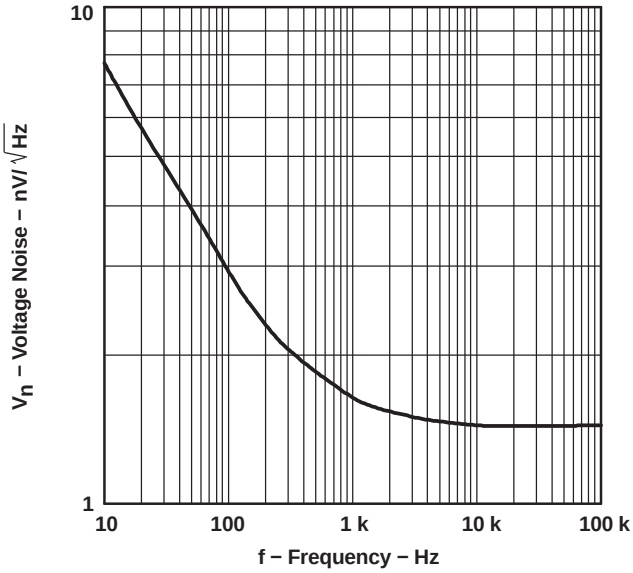


Figure 24.

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TYPICAL CHARACTERISTICS (continued)

CURRENT NOISE vs FREQUENCY

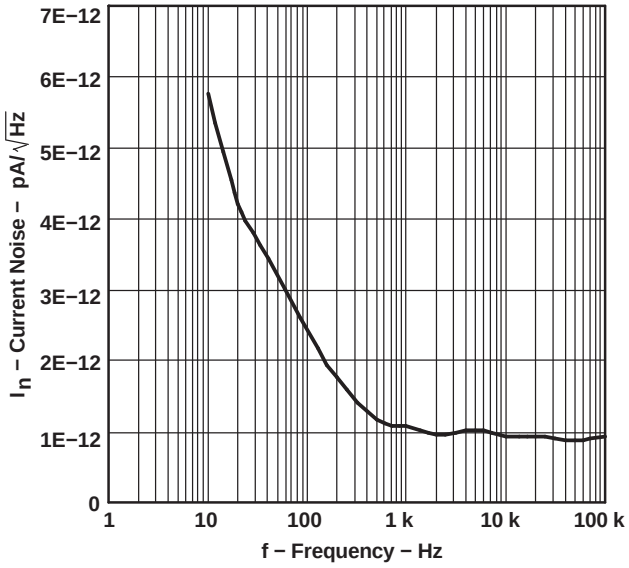


Figure 25.

INPUT OFFSET VOLTAGE vs COMMON-MODE OUTPUT VOLTAGE

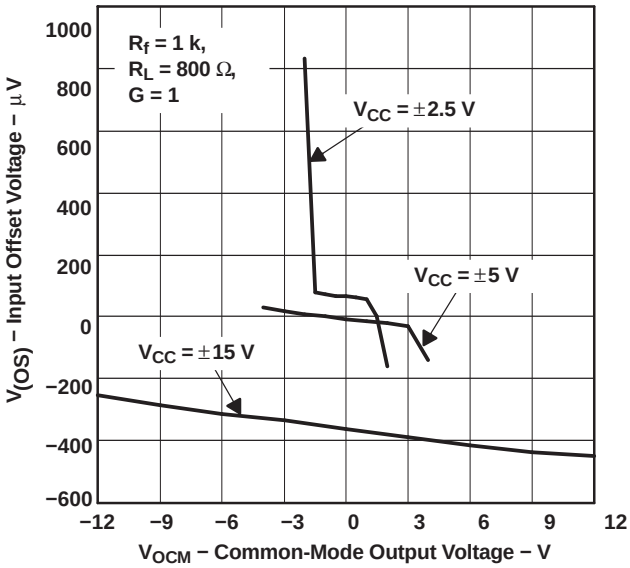


Figure 26.

OUTPUT VOLTAGE vs DIFFERENTIAL LOAD RESISTANCE

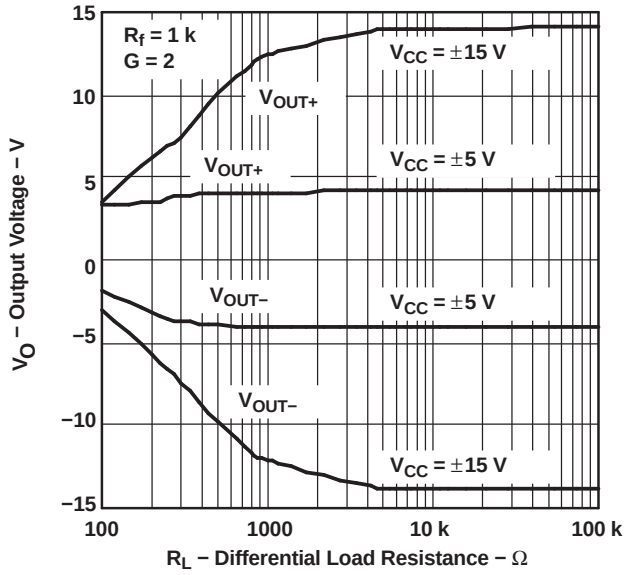


Figure 27.

OUTPUT IMPEDANCE vs FREQUENCY

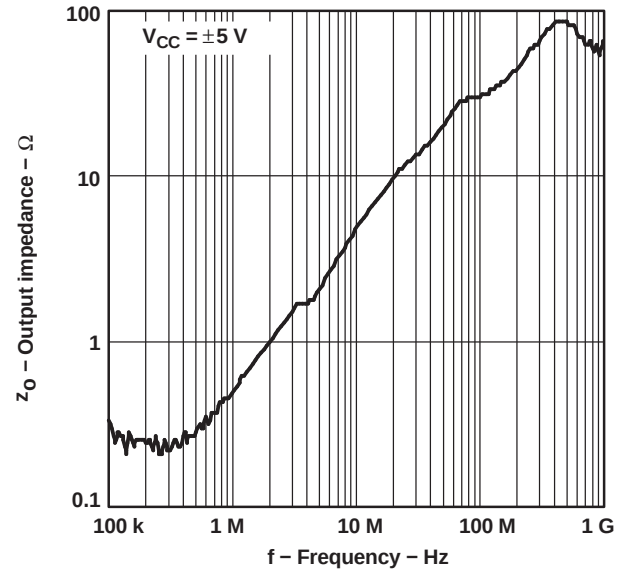


Figure 28.

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APPLICATION INFORMATION

RESISTOR MATCHING

Resistor matching is important in fully-differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistor. CMRR, PSRR, and cancellation of the second-harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM}pin, it is set to the midrail voltage internally defined as:

$$\frac{\left(V_{CC+}\right) + \left(V_{CC-}\right)}{2} \quad (1)$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. Figure 29 shows the simplified diagram of the THS413x.

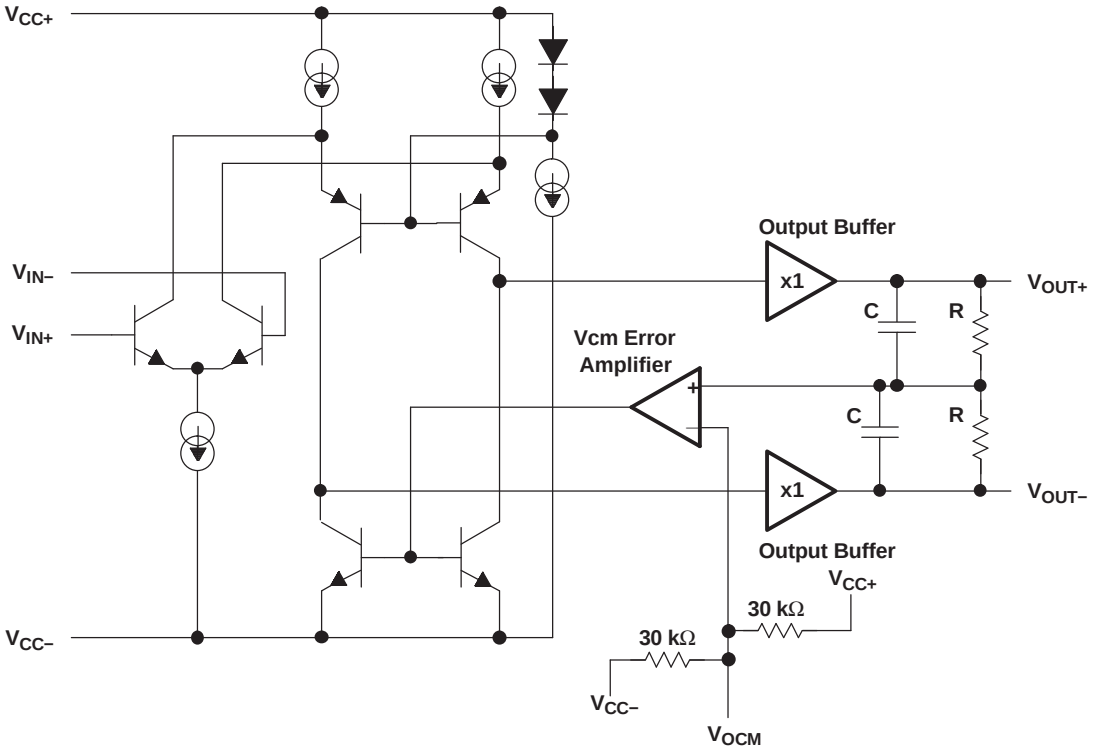


Figure 29. THS413x Simplified Diagram

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DATA CONVERTERS

Data converters are one of the most popular applications for the fully-differential amplifiers. Figure 30 shows a typical configuration of a fully-differential amplifier attached to a differential analog-to-digital converter (ADC).

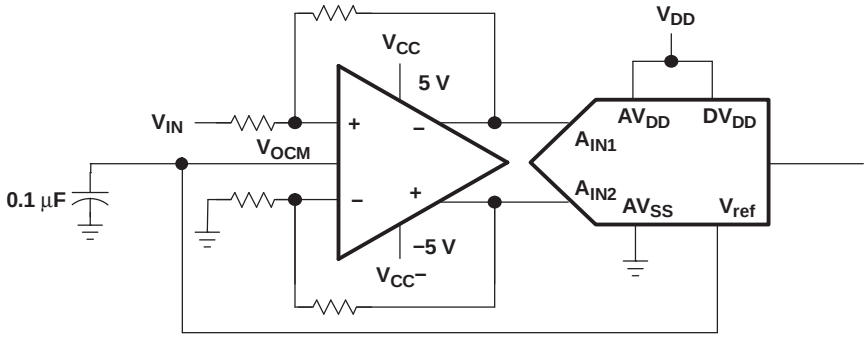


Figure 30. Fully-Differential Amplifier Attached to a Differential ADC

Fully-differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

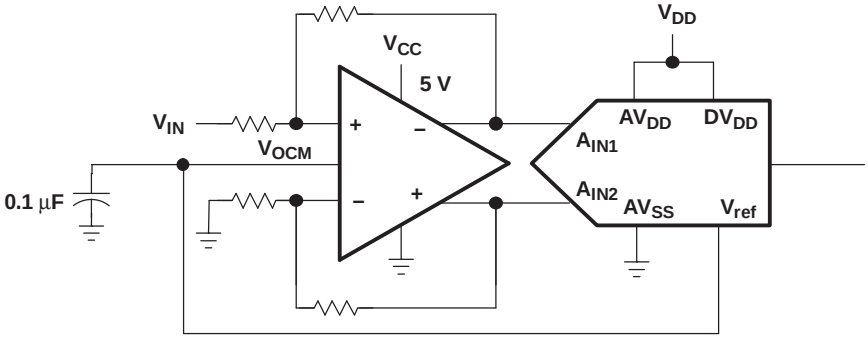


Figure 31. Fully-Differential Amplifier Using a Single Supply

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Some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the circuit configuration of Figure 32 is suggested to bring the common-mode input voltage within the specifications of the amplifier.

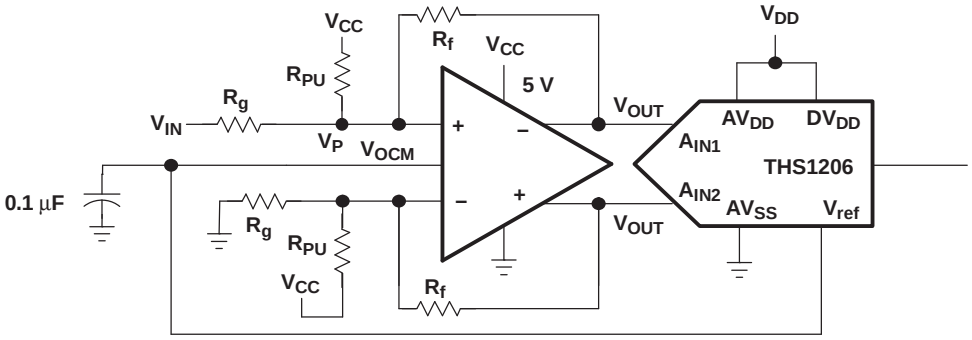


Figure 32. Circuit With Improved Common-Mode Input Voltage

Equation 2 is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{\left(V_{IN} - V_P\right)\frac{1}{RG} + \left(V_{OUT} - V_P\right)\frac{1}{RF}} \quad (2)$$

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS413x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 33. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

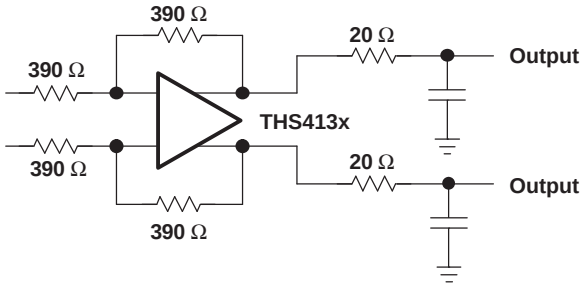


Figure 33. Driving a Capacitive Load

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ACTIVE ANTIALIAS FILTERING

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. Figure 34 presents a method by which the noise may be filtered in the THS413x.

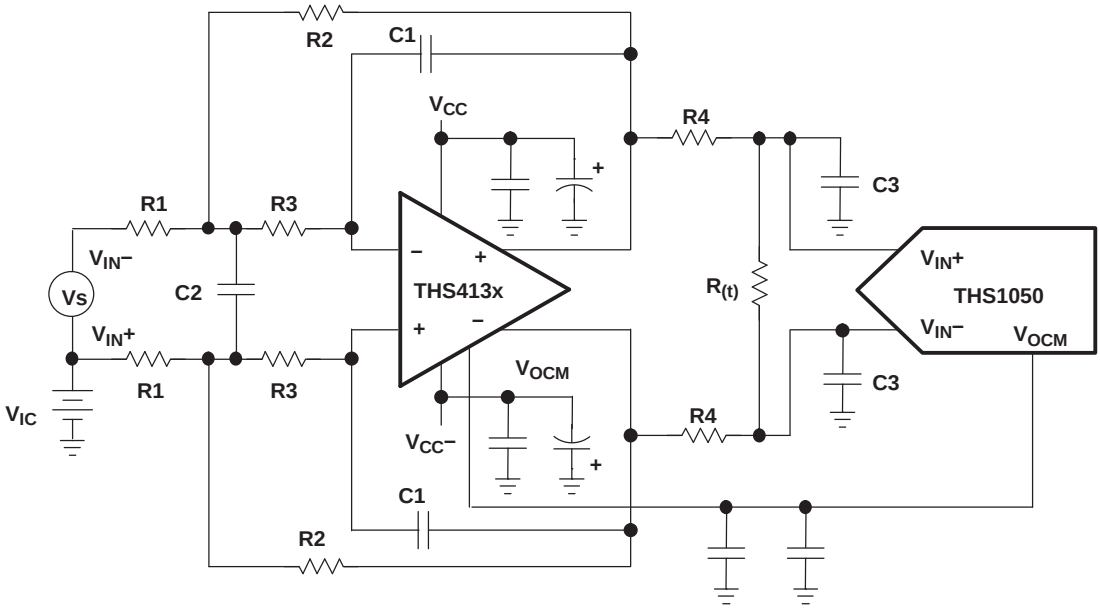


Figure 34. Antialias Filtering

The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \quad \text{Where } K = \frac{R2}{R1} \tag{3}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \text{ and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \tag{4}$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \tag{5}$$

where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \tag{6}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

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PRINCIPLES OF OPERATION

THEORY OF OPERATION

The THS413x is a fully-differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully-differential amplifiers are *differential in/differential out*.

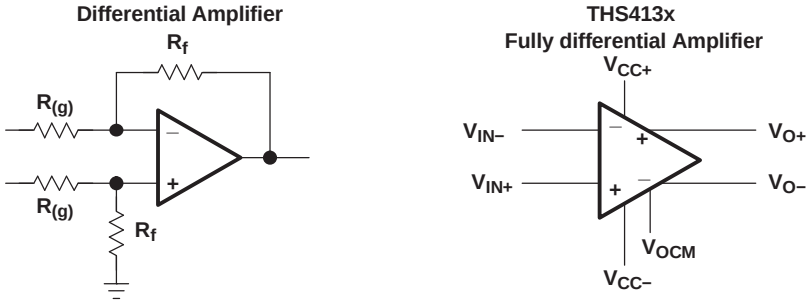


Figure 35. Differential Amplifier Versus a Fully-Differential Amplifier

To understand the THS413x fully-differential amplifiers, the definition for the pin outs of the amplifier are provided.

Input voltage definition $$V_{ID} = (V_{I+}) - (V_{I-}) \qquad V_{IC} = \frac{(V_{I+}) + (V_{I-})}{2} \tag{7}$$

Output voltage definition $$V_{OD} = (V_{O+}) - (V_{O-}) \qquad V_{OC} = \frac{(V_{O+}) + (V_{O-})}{2} \tag{8}$$

Transfer function $$V_{OD} = V_{ID} \times A_{(f)} \tag{9}$$

Output common mode voltage $$V_{OC} = V_{OCM} \tag{10}$$

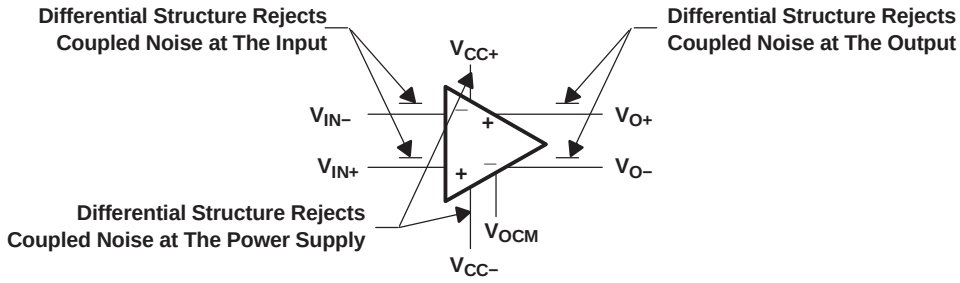
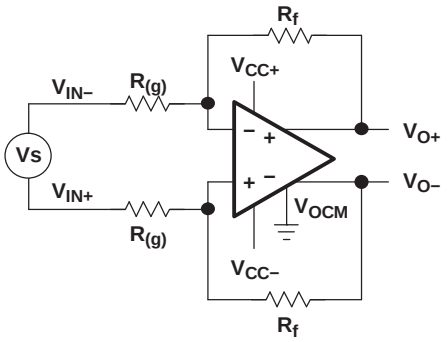


Figure 36. Definition of the Fully-Differential Amplifier

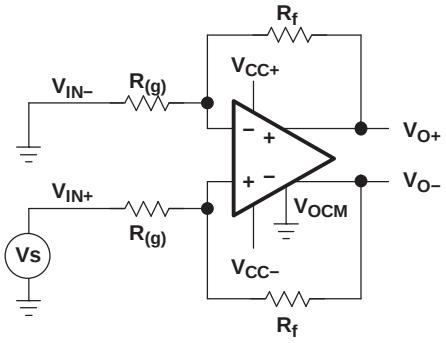
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Figure 37 and Figure 38 depict the differences between the operation of the THS413x fully-differential amplifier in two different modes. Fully-differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting $R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)} \Rightarrow A = R_f/R_{(g)}$

Figure 37. Amplifying Differential Signals



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 38. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \tag{11}$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \tag{12}$$

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Fully-differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully-differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it is not as practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully-differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully-differential amplifier. The final result indicates twice as much dynamic range. Figure 39 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS413x fully-differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second-harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

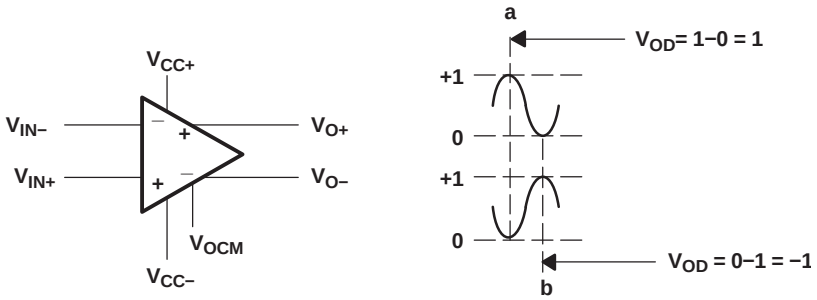


Figure 39. Fully-Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully-differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully-differential amplifier. Figure 40 depicts the general format of instrumentation amplifiers.

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1} - V_{IN2}} = \frac{R_f}{R_{(g)}}\left(1 + \frac{2R2}{R1}\right) \quad (13)$$

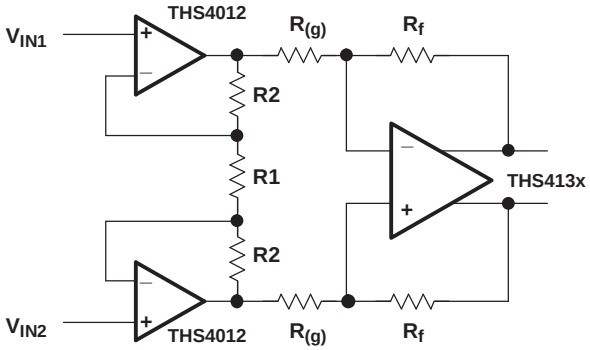


Figure 40. Instrumentation Amplifier

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CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high-frequency performance of the THS413x, follow proper printed-circuit board (PCB) high-frequency design techniques. A general set of guidelines is given below. In addition, a THS413x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board are the best implementation.
- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

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POWER-DOWN MODE

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS413x is an active low terminal. If it is left as a no-connect terminal, the device always stays on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above V_{CC-}. This means that if the $\overline{PD}$ terminal is 1.4 V above V_{CC-}, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above V_{CC-}, the device is off. For example, if V_{CC-} = –5 V, then the device is on when PD reaches –3.6 V, (–5 V + 1.4 V = –3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to V_{CC-} in order to turn the device off. Figure 41 shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

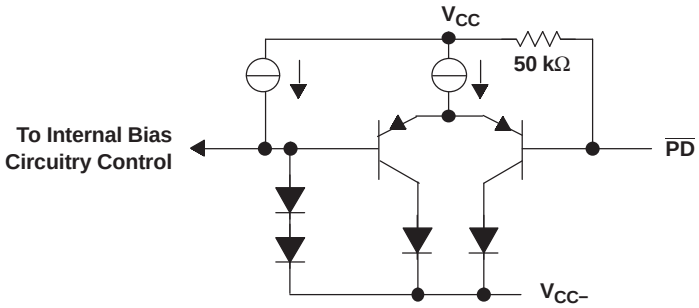


Figure 41. Simplified Power-Down Circuit

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed loop output impedance is shown in Figure 42.

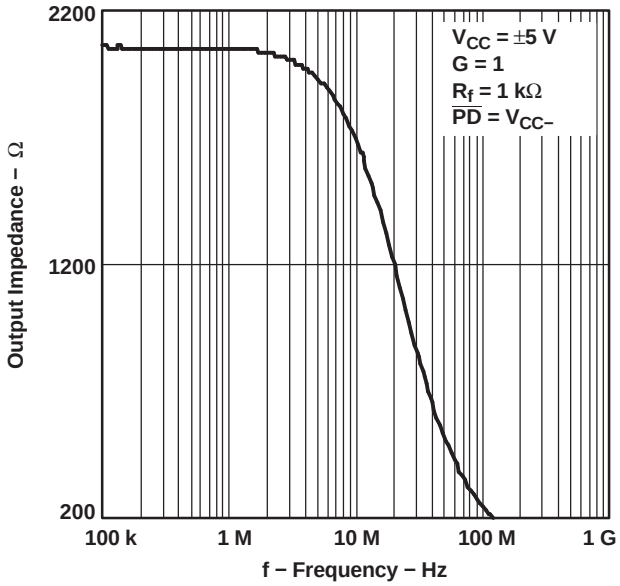


Figure 42. Output Impedance (In Power-Down) vs Frequency

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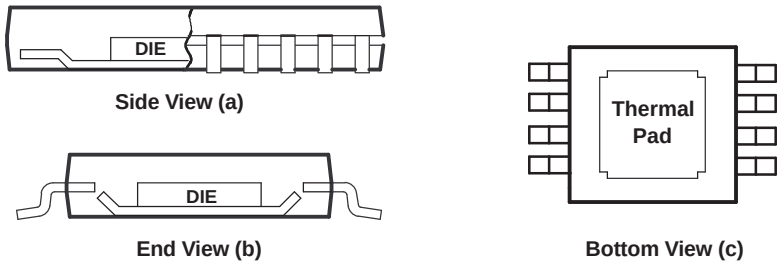
GENERAL PowerPAD DESIGN CONSIDERATIONS

The THS413x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted (see Figure 43a and Figure 43b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 43c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, (*PowerPAD Thermally-Enhanced Package* SLMA002). This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.



A. The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane becase this plane tends to physically be the largest and is able to dissipate the most amount of heat.

Figure 43. Views of Thermally-Enhanced DGN Package

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2010) to Revision H	Page
• Changed footnote A in Figure 43	22

Changes from Revision F (January 2006) to Revision G	Page
• Changed DGK package specifications in the *Dissipation Rating* table	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATP	Samples
THS4130CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ATP	Samples
THS4130CDGKR	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	0 to 70	ATP	
THS4130CDGKRG4	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	0 to 70		
THS4130CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4131CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4131IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

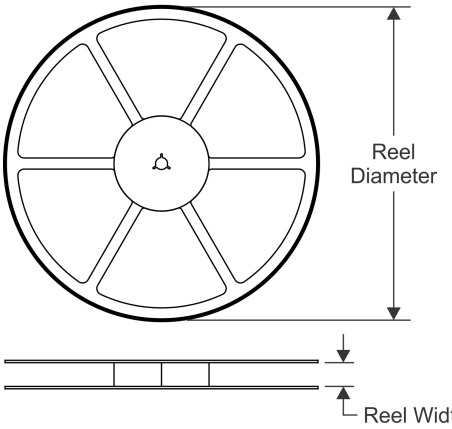
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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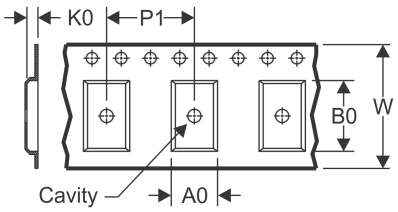
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

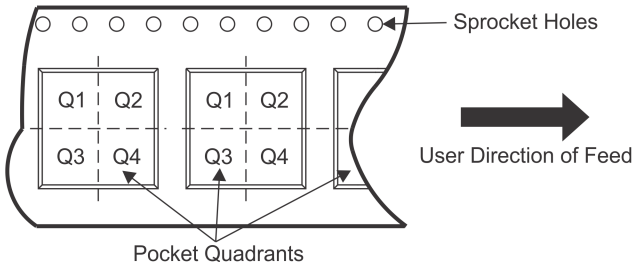


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

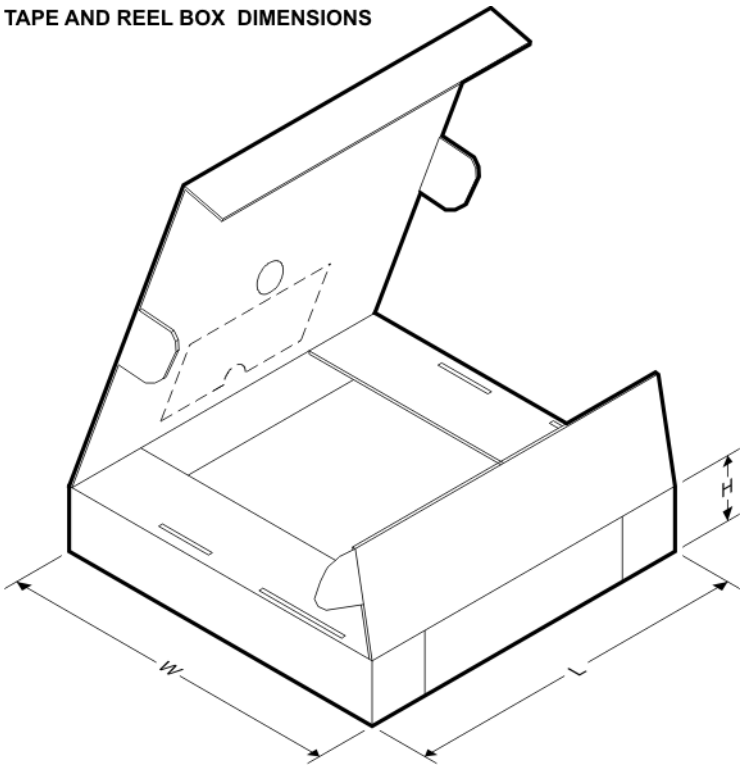
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

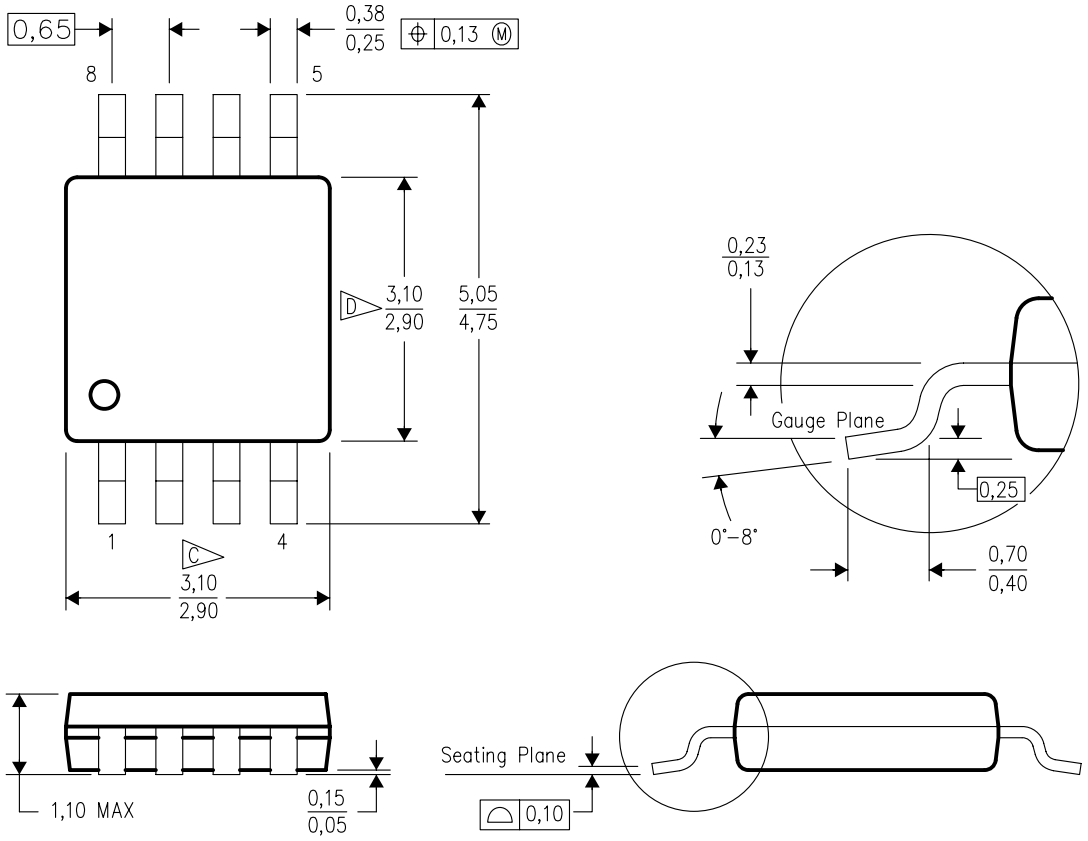
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130CDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4130IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4130IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4130IDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4131CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131CDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4131CDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4131IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4131IDR	SOIC	D	8	2500	367.0	367.0	35.0

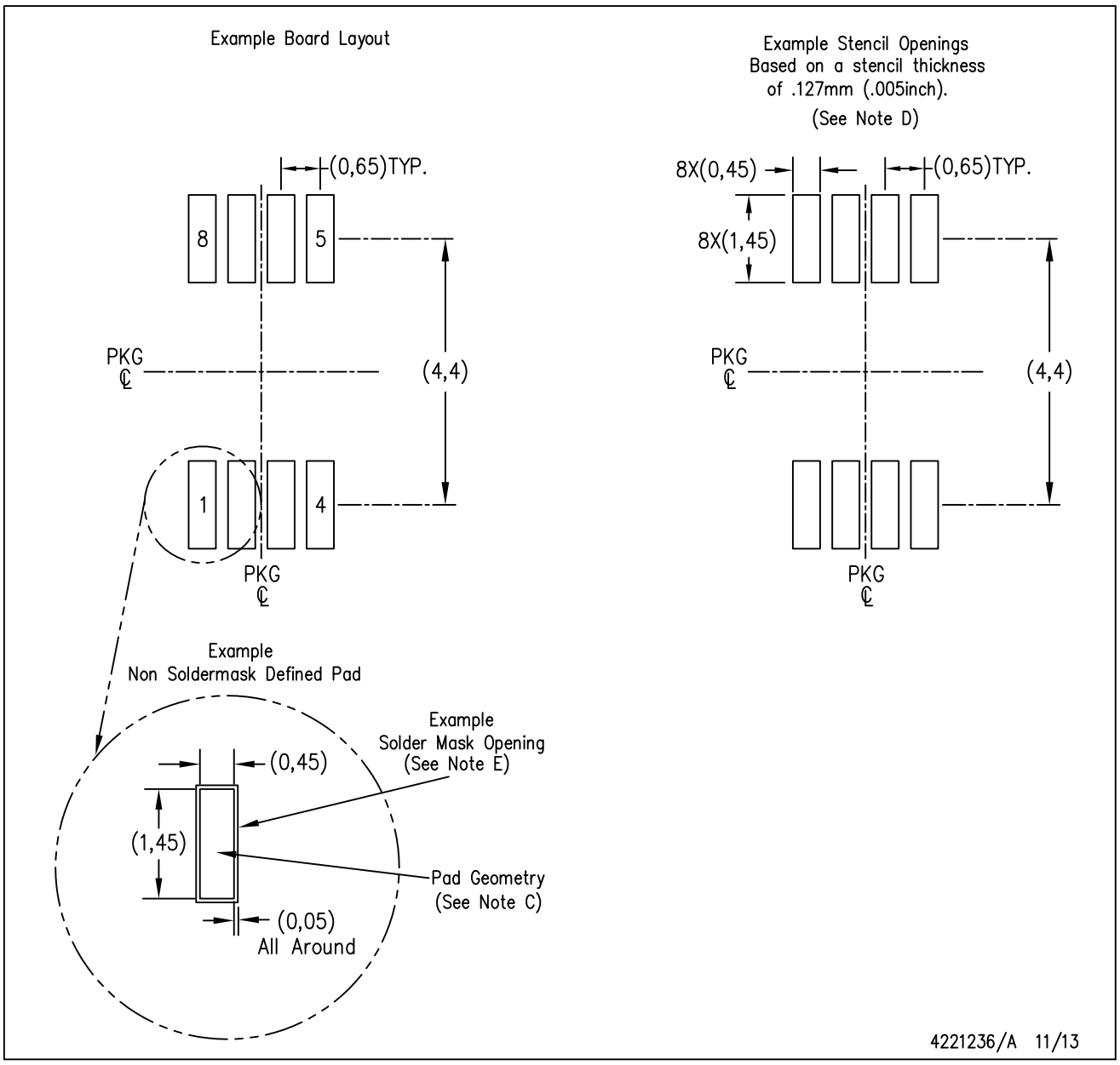
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

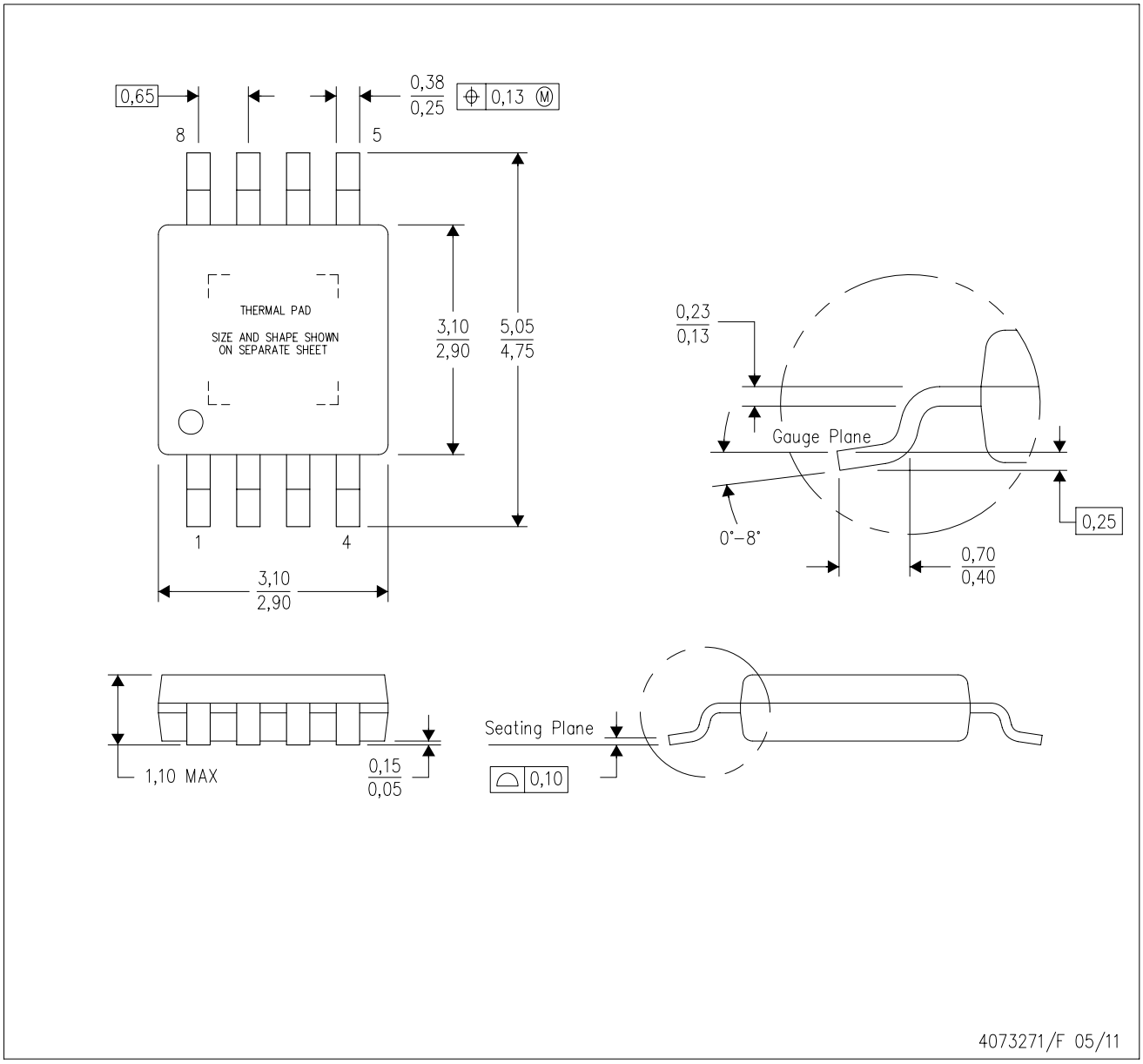
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

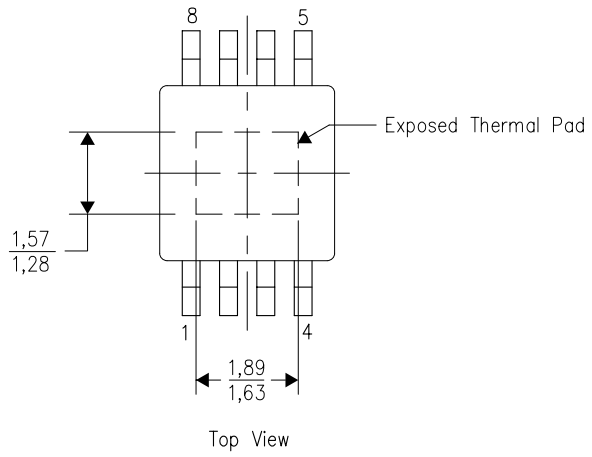
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

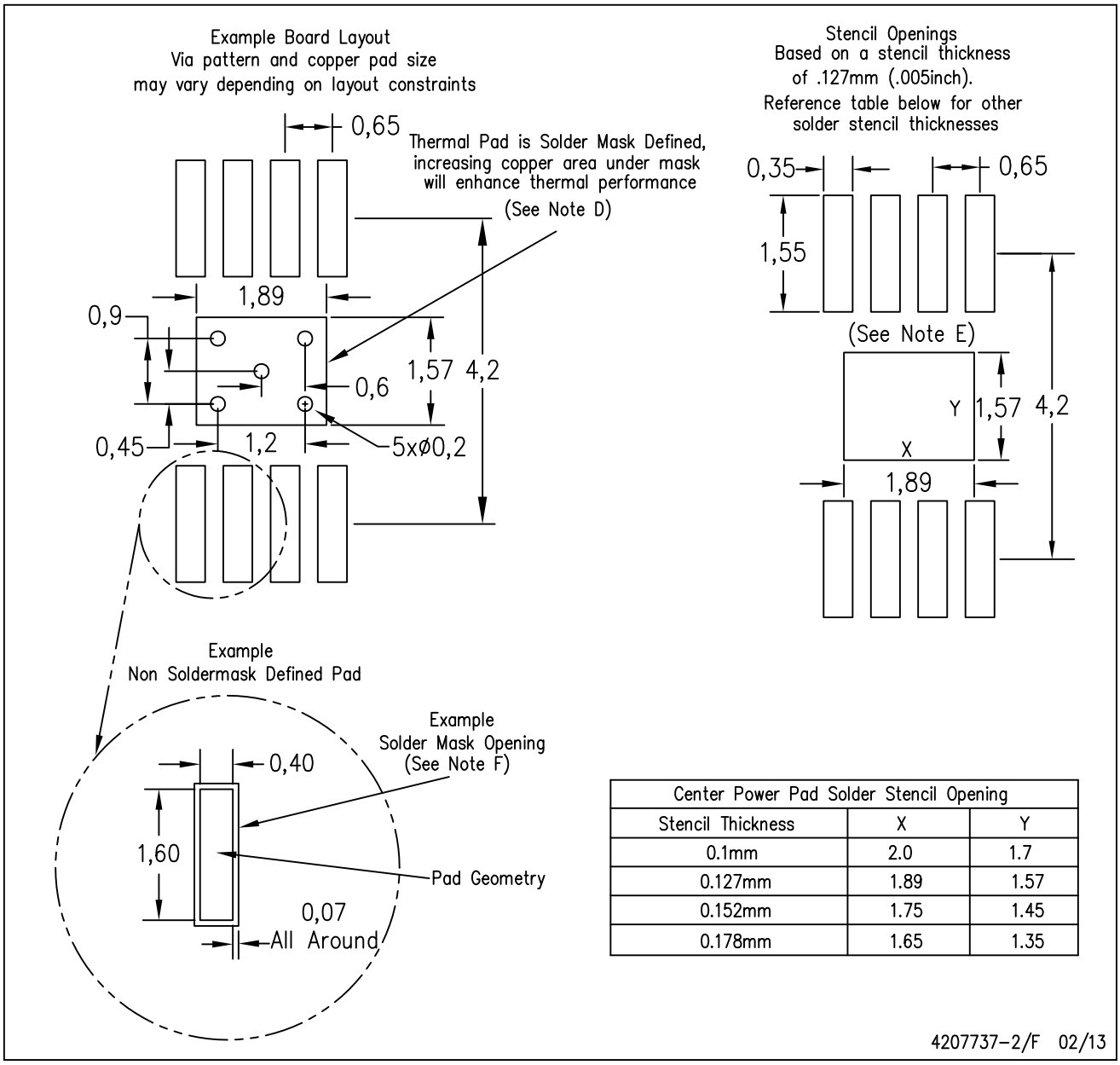
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



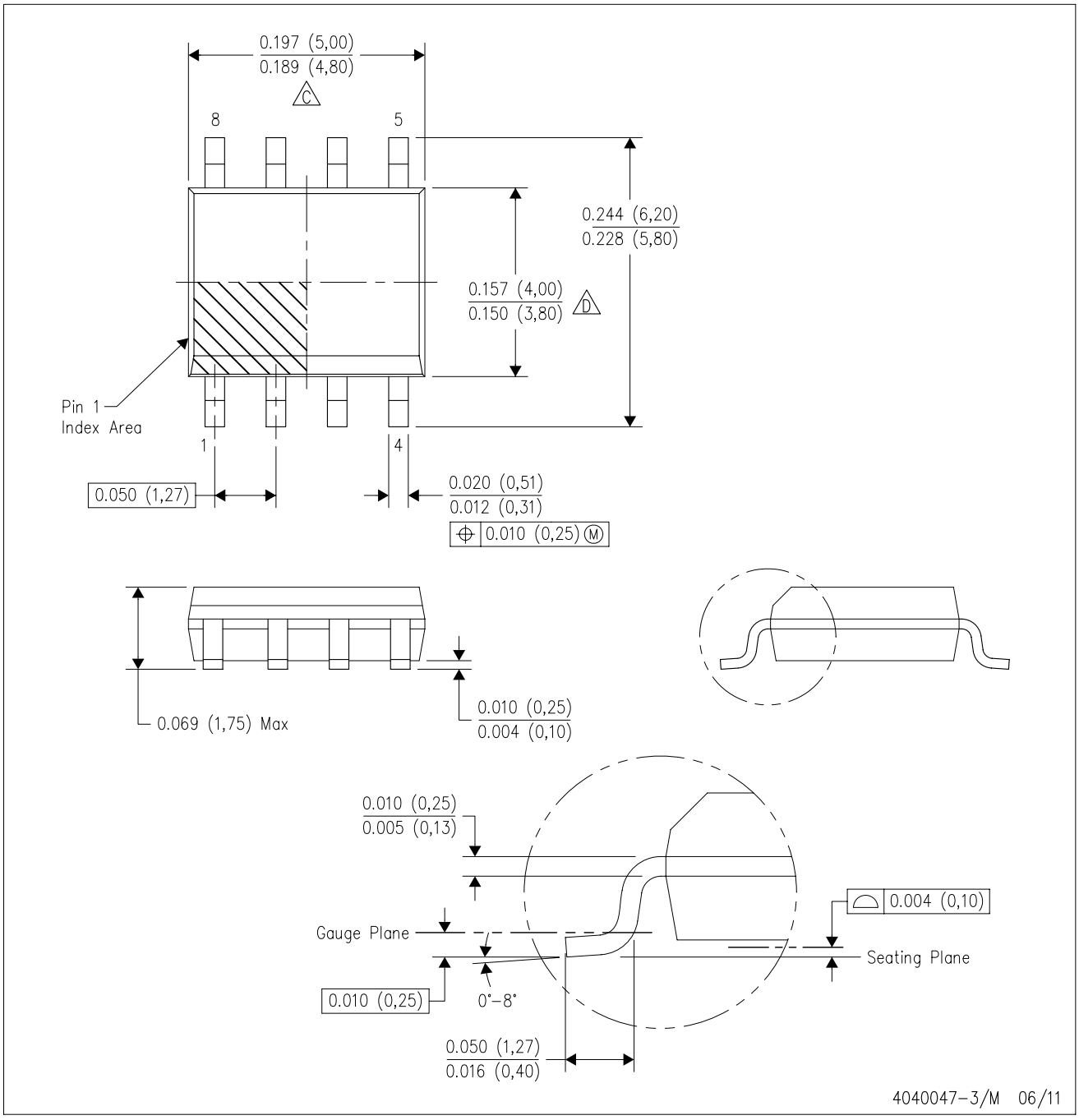
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

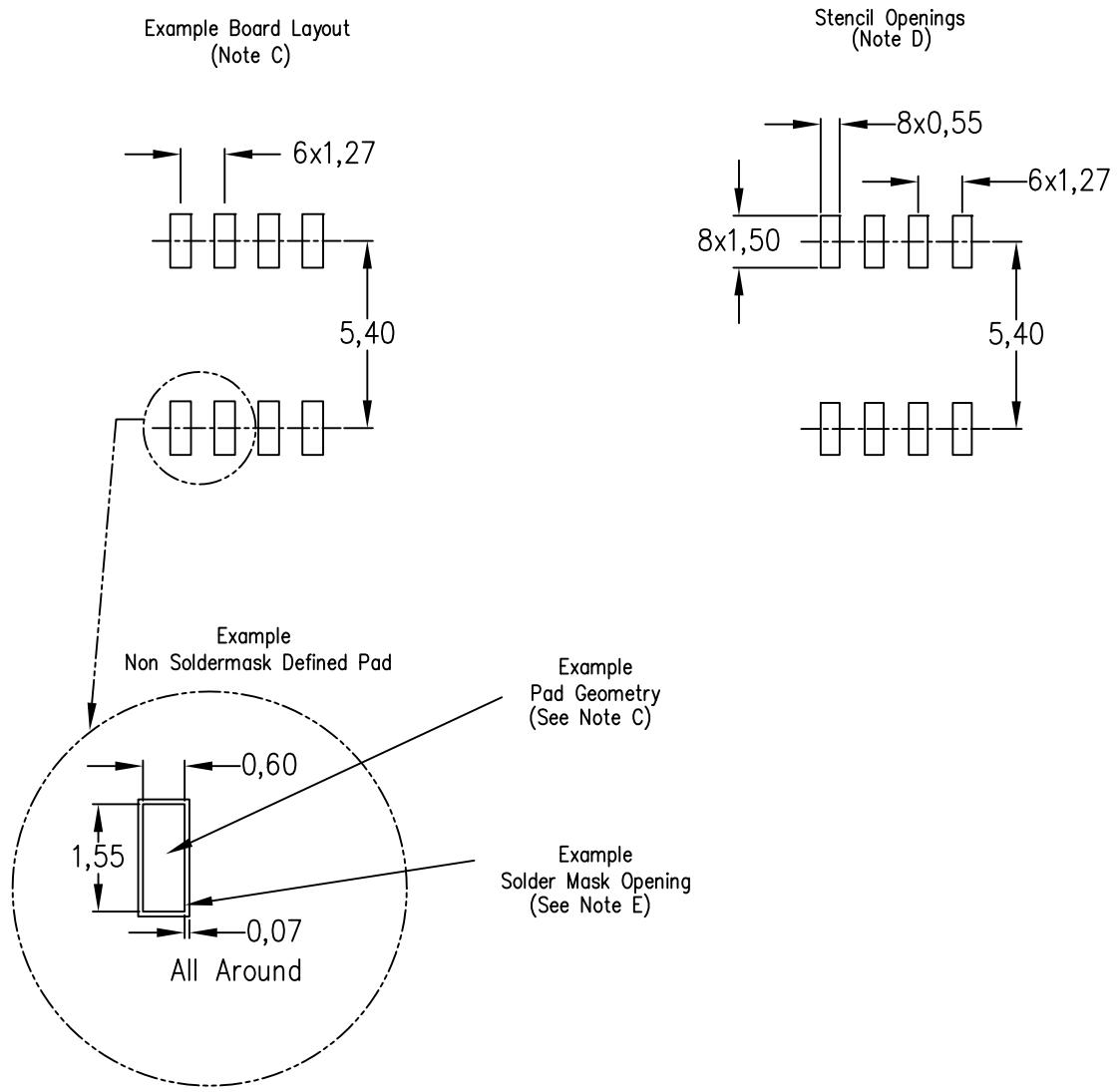
PowerPAD is a trademark of Texas Instruments

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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