FEATURES

- **620ps typical propagation delay**
- **Fully differential design**
- **Supports standard operation**
- **Available in 20-pin SOIC package**

DESCRIPTION

The SY100EL91 is a triple PECL-to-ECL translator. It receives standard voltage PECL signals and translates them to different ECL output signals.

A V_{BB} output is provided for interfacing with single ended PECL signals at the input. If a single ended input is to be used, the V_{BB} output should be connected to the $\overline{D}$ input. The active signal would then drive the D input. When used, the V_{BB} output should be bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the EL91 under single ended input switching conditions. As a result this pin can only source/sink up to 0.5mA of current.

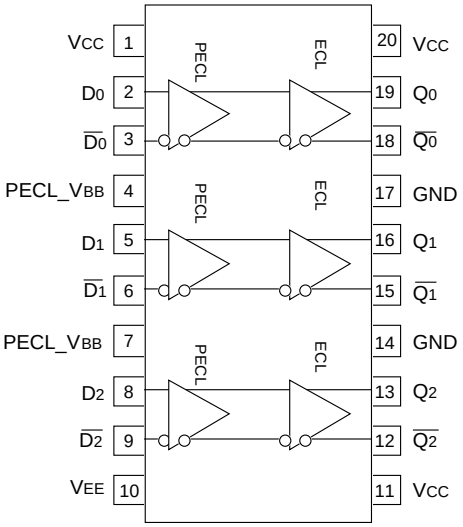
To accomplish the level translation the EL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins as expected are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01µF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a LOW, ensuring stability.

PIN NAMES

Pin	Function
Dn	PECL Inputs
Q_n	ECL Outputs
PECL_V_{BB}	PECL Reference Voltage Output

PACKAGE/ORDERING INFORMATION



20-Pin Wide SOIC (Z20-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL91ZC	Z20-1	Commercial	SY100EL91ZC	Sn-Pb
SY100EL91ZCTR[2]	Z20-1	Commercial	SY100EL91ZC	Sn-Pb
SY100EL91ZI	Z20-1	Industrial	SY100EL91ZI	Sn-Pb
SY100EL91ZITR[2]	Z20-1	Industrial	SY100EL91ZI	Sn-Pb
SY100EL91ZG[3]	Z20-1	Industiral	SY100EL91ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EL91ZGTR[2, 3]	Z20-1	Industrial	SY100EL91ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PECL INPUT DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Power Supply Voltage	4.75	—	5.25	4.75	—	5.25	4.75	—	5.25	4.75	—	5.25	V
V_{IH}	Input HIGH Voltage(1)	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
V_{IL}	Input LOW Voltage(1)	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	µA
V_{BB}	Output Reference(1)	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	V
I_{CC}	Power Supply Current	—	—	11	—	—	11	—	6.0	11	—	—	11	mA

Note:

1. These values are for V_{CC} = 5V. Level specifications will vary 1:1 with V_{CC}.

ECL OUTPUT DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{EE}	Power Supply Voltage	–4.2	—	–5.5	–4.2	—	–5.5	–4.2	—	–5.5	–4.2	—	–5.5	V
V_{OH}	Output HIGH Voltage	–1085	—	–880	–1025	—	–880	–1025	–955	–880	–1025	—	–880	mV
V_{OL}	Output LOW Voltage	–1830	—	–1555	–1810	—	–1620	–1810	–1705	–1620	–1810	—	–1620	mV
I_{EE}	Power Supply Current	—	—	28	—	—	28	—	22	28	—	—	30	mA

AC ELECTRICAL CHARACTERISTICS

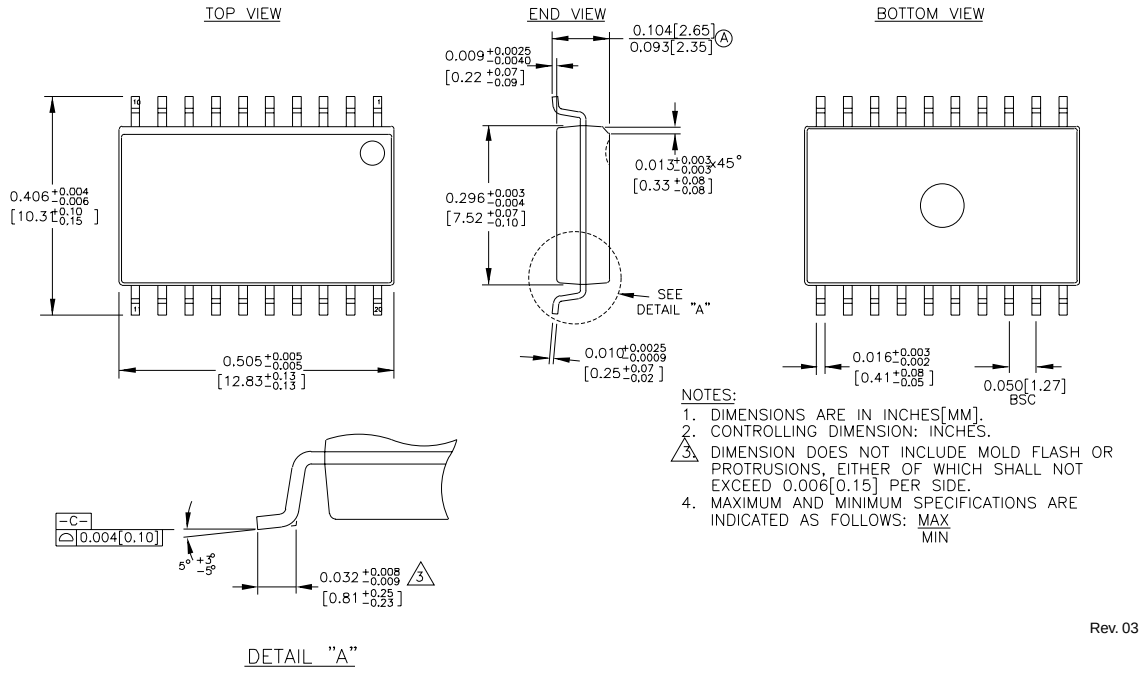
PECL: V_{CC} = +4.75V to +5.25V, ECL: V_{EE} = -4.2V to -5.5V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	Propagation Delay Diff. D to Q S.E.	520 470	620 620	720 770	520 470	620 620	720 770	520 470	620 620	720 770	550 500	650 650	750 800	ps
t_{skew}	Within-Device Skew(1) Output-to-Output Part-to-Part (Diff.) Duty Cycle (Diff.)	 — — —	 — — 25	 100 200 —	 — — —	 — — 25	 100 200 —	 — — —	 20 — 25	 100 200 —	 — — —	 — — 25	 100 200 —	ps
V_{PP}	Minimum Input Swing(2)	200	—	—	200	—	—	200	—	—	200	—	—	mV
V_{CMR}	Common Mode Range(3) V_{PP} < 500mV V_{PP} > 500mV	 1.3 1.5	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	320	400	580	320	400	580	320	400	580	320	400	580	ps

Notes:

1. Skew is measured between outputs under identical transitions.
2. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ~40.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.

20-PIN SOIC .300" WIDE (Z20-1)



Rev. 03

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