MC145740

Product Preview

Dual Tone Multiple Frequency Line Interface

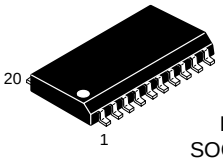
The MC145740 is a silicon gate HCMOS LSI designed for general purpose Dual Tone Multiple Frequency (DTMF) communications, and contains a DTMF signal generator and a receiver for all 16 standard digits.

The generator block has a differential line driver which drives a 600 Ω load with 0 dBm level. The transmit signal level is adjusted in 1 dB steps by the programmable attenuator.

The receiver block has an Auto Gain Control (AGC) amplifier to demodulate 50 dB (typ) dynamic range of DTMF signals to the hexadecimal codes.

The device also includes a serial control interface that permits a CPU to exercise the following built–in features.

- Single Power Supply: 3.6 to 5.5 V
- DTMF Generator and Receiver for All 16 Standard Digits
- 0 dBm Line Driver Into 600 Ω Load
- AGC Amplifier
- Programmable Transmit Attenuator
- Serial Control Interface
- Power Down Mode, Less Than 1 μA

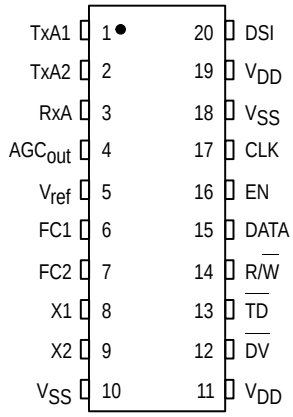


F SUFFIX
SOG PACKAGE
CASE 751J

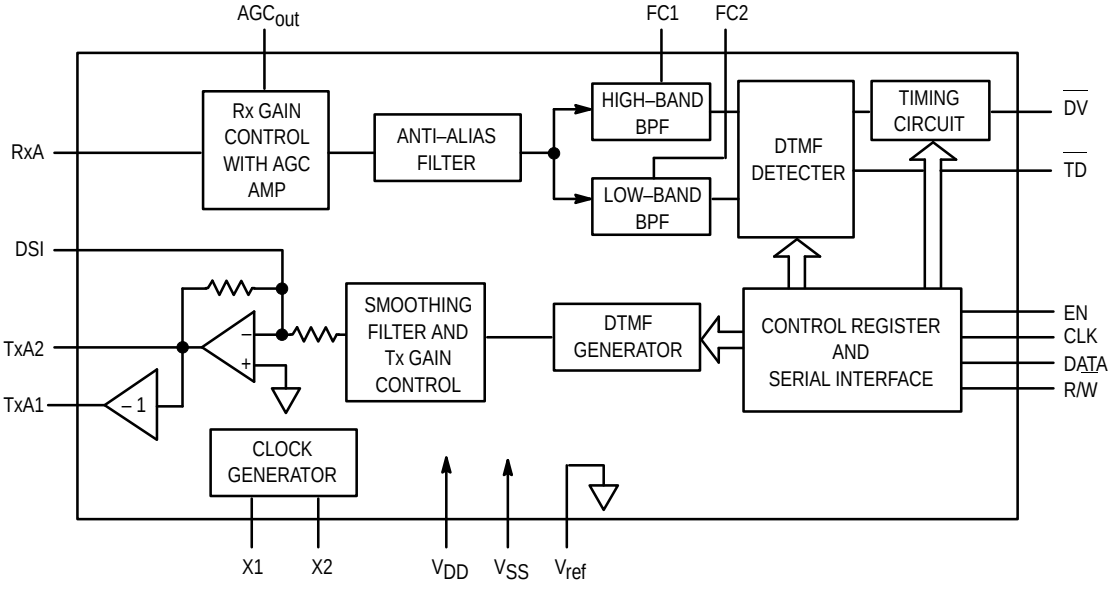
ORDERING INFORMATION

MC145740F	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



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MAXIMUM RATINGS (Voltages Referenced to V_{SS} Unless Otherwise Noted)

Ratings	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Input Voltage, All Pins	V_{in}	– 0.5 to V_{CC} + 0.5	V
DC Current Per Pin	I	± 20	mA
Power Dissipation	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Reliability of operation is enhanced if unused logic inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	3.6	5	5.5	V
Input Voltage, All Pins	V_{in}	0	—	V_{CC}	V
Input Rise or Fall Time	t_r, t_f	0	—	500	ns
Crystal Frequency	f_{osc}	—	3.5795	—	MHz
Operating Temperature Range	T_A	– 20	25	70	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = – 20 to 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	H Level	V_{IH}		3.15	—	—	V
EN, CLK, DATA, R/$\overline{W}$	L Level	V_{IL}		—	—	1.1	
Output Voltage	H Level	V_{OH}	I_{OH} = 20 µA	V_{CC} – 0.1	V_{CC} – 0.01	—	V
$\overline{DV}$, $\overline{TD}$, DATA	L Level	V_{OL}	I_{OL} = – 20 µA I_{OL} = – 2 mA	— —	0.01 —	0.1 0.4	
Input Current	R/W, DATA, EN, CLK	I_{in}	$V_{in} = V_{DD}$ or V_{SS}	—	± 1.0	± 10.0	µA
Supply Current		I_{DD}	DTMF Tx Mode	—	5	—	mA
			DTMF Rx Mode	—	8	—	
Standby Current		I_{DD}	Power Down 1	—	—	500	µA
			Power Down 2	—	—	1	

AC ELECTRICAL CHARACTERISTICS

DTMF TRANSMIT CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = – 20 to 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit Level	Low Group	V_{fl}	Attenuator = 0 dB f_{osc} = 3.579545 MHz $V_{TxA1} - V_{TxA2}$ R_L = 1.2 kΩ	—	2.5	—	dBm
	High Group	V_{fh}		—	3.5	—	
High Group Pre–Emphasis		PE		0	—	3	dB
DTMF Distortion		DIST		—	5	—	%
DTMF Frequency Variation		ΔfV		– 1	—	1	%
Out–of–Band Energy (See Figure 1)		V_{OE}		—	—	—	
Setup Time		t_{osc}		—	4	—	ms

TRANSMIT ATTENUATOR CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = – 20 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Attenuator Range	ARNG		0	—	15	dB
Attenuator Accuracy	AACC	1 dB – 5 dB	– 0.5	—	0.5	dB
		6 dB – 9 dB	– 1	—	1	
		10 dB – 15 dB	– 1.7	—	1	

DTMF RECEIVER CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = – 20 to 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input Impedance		RIDTMF		50	—	—	kΩ
Detect Signal Level (Each Tone)				– 48	—	0	dBm
Twist (High Group/Low Group)				– 10	—	10	dB
Frequency Detect Band Width			See Figure 3	± 1.5% ± 2 Hz	—	—	% fc
Frequency Reject Band Width				—	—	± 3.5	
DTMF Detect Timing (See Figure 2)	OFF to ON	TVD_{ON}	CD1 = 0, CD0 = 1	—	20	—	ms
			CD1 = 1, CD0 = 0	—	30	—	
			CD1 = 1, CD0 = 1	—	40	—	
	ON to OFF	TVD_{OFF}	CD1 = 0, CD0 = 1	—	20	—	
			CD1 = 1, CD0 = 0	—	30	—	
			CD1 = 1, CD0 = 1	—	20	—	

SWITCHING CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = – 20 to 70°C, See Figure 4)

Parameter		Symbol	Number	Min	Typ	Max	Unit
Pulse Width (H)	EN, SCK	t_{wh}	1	50	—	—	ns
Pulse Width (L)	EN, SCK	t_{wl}	2	50	—	—	ns
Clock Cycle		t_c	3	100	—	—	ns
Input Rise Time		t_r	4	—	—	2	µs
Input Fall Time		t_f	5	—	—	2	µs
Recovery Time	EN to SCK	t_{rec}	6, 18	50	—	—	ns
Setup Time	DATA to SCK	t_{su}	7	50	—	—	ns
	$\overline{R/W}$ Low to DATA		9	100	—	—	
	$\overline{R/W}$ High to DATA		12	50	—	—	
Hold Time	SCK to DATA	t_h	8	50	—	—	ns
	EN to $\overline{R/W}$		10	50	—	—	
	DATA to $\overline{R/W}$		14	50	—	—	
	$\overline{R/W}$ to DATA		15	50	—	—	
Read Data Delay Time	EN to DATA	t_d	13	—	—	50	ns
	SCK to DATA		17	—	—	50	

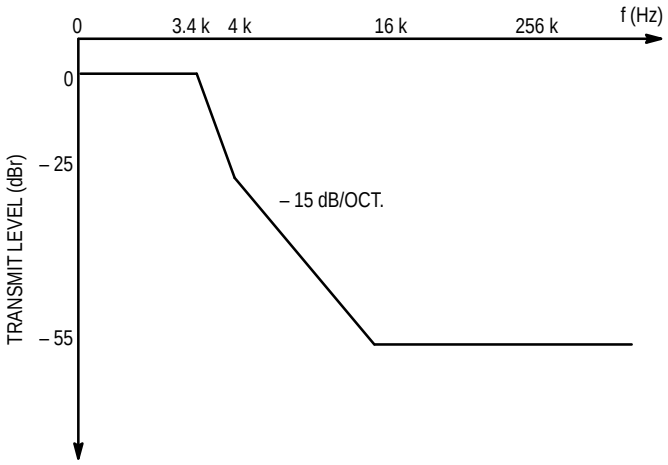
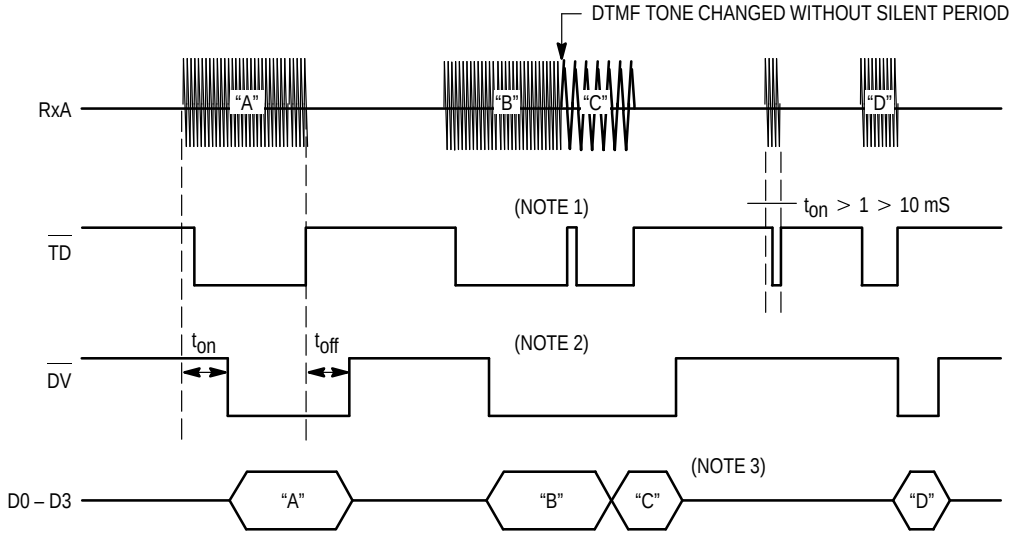


Figure 1. Out–of–Band Energy



NOTES:

1. The high–to–low and low–to–high transition on the $\overline{TD}$ pin will appear immediately after the valid DTMF tones are detected. The TD will also output a short H pulse when the device detects the DTMF tones being changed without a silent period.
2. The high–to–low and low–to–high transition on the $\overline{DV}$ pin will appear after the programmed guard time determined by two bits of serial data (CD1, CD0).
3. The device recognizes the DTMF tones changed without a silent period, and the four bits of data can be read from the status register.

Figure 2. DTMF Detect Timing

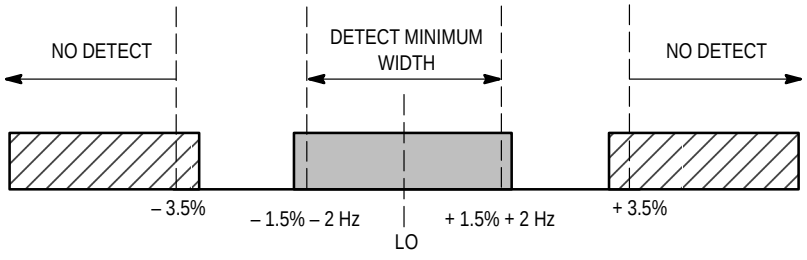
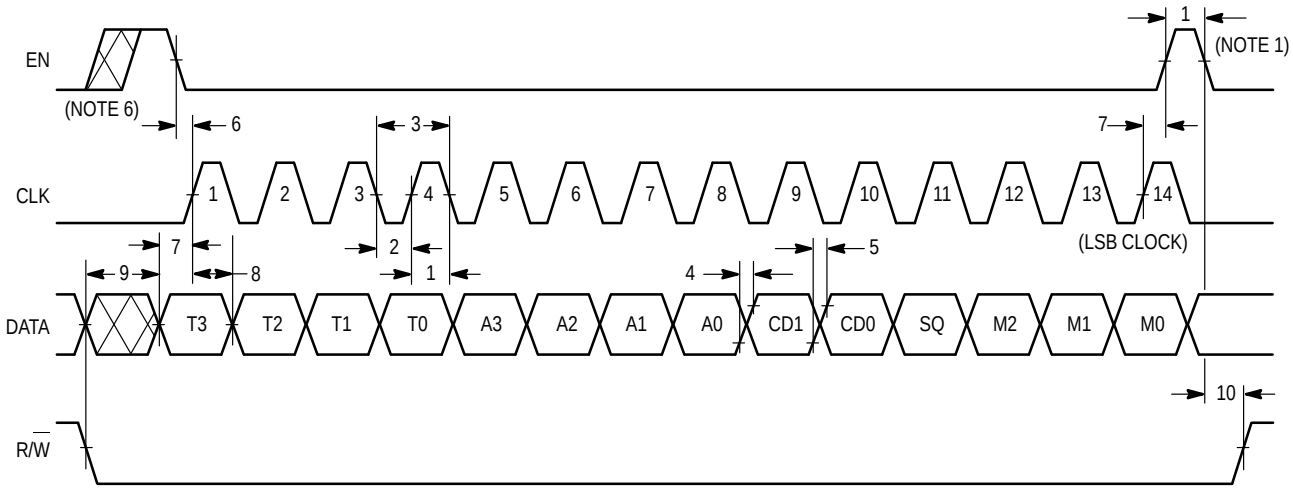
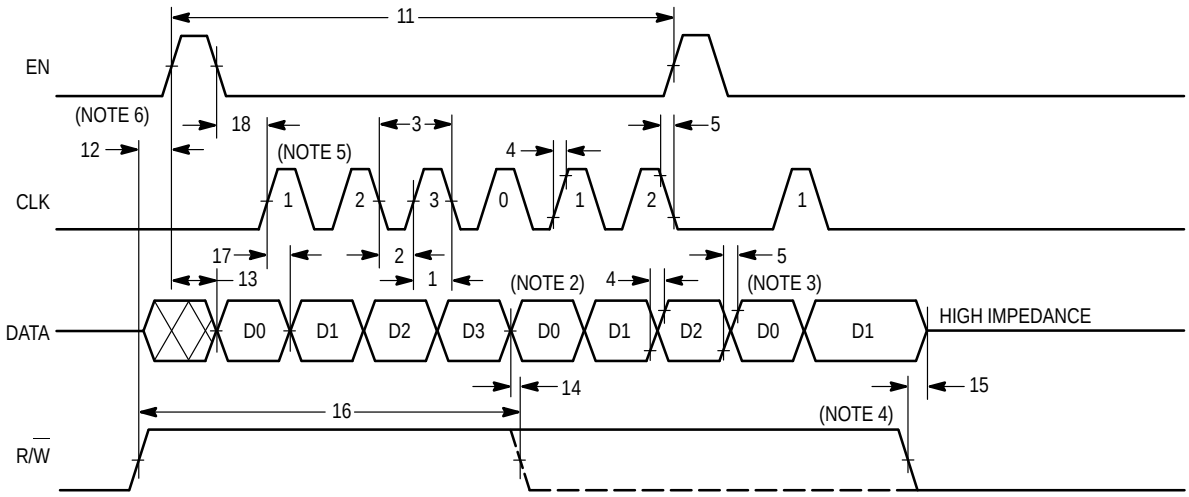


Figure 3. DTMF Frequency Detect Band Width

CONTROL REGISTER



STATUS REGISTER



NOTES:

1. The data in front of the EN signal will be latched.
2. The latched data will be repeated until there is an EN pulse.
3. The detected data will be updated with the next EN pulse.
4. After the R/W pin becomes inactive, the data will be lost.
5. D1 corresponds to CLK1.
6. The EN and CLK signals need to be set at the logic low level when the R/W signal changes.
7. The CLK signal must be held low when the EN signal is high.

Figure 4. Serial Interface Timing

PIN DESCRIPTIONS

TxA1
Non–Inverting Analog Output (Pin 1)

This pin is the line driver non–inverting output. A + 7 dBm (typ) differential output voltage can be obtained by connecting a 1.2 kΩ load resistor between TxA1 and TxA2. Note that the DSI input, if used, must be controlled for the output level not to exceed the above signal level.

TxA2
Inverting Analog Output (Pin 2)

This pin is the driver inverting output. Refer to TxA1.

RxA
DTMF Receive Input (Pin 3)

This pin is the DTMF signal input (AGC input).

AGC_{out}
AGC Output (Pin 4)

This pin is the AGC amplifier output. The signal received from the RxA pin appears at this pin through the AGC amplifier so that any signal receivers can be connected on this pin to decode the non–DTMF signals. The AGC amplifier gain is software programmable as shown in Table 3.

V_{ref}
Reference Analog Ground (Pin 5)

This pin provides the analog ground voltage, $V_{CC}/2$, which is internally regulated from V_{CC}. This pin should be decoupled to GND with 0.1 μF and 100 μF capacitors.

FTLC1, FTLC2
Band–Pass Filter Test (Pins 6, 7)

These pins are high impedance filter outputs. They may be used for testing the DTMF receive high and low band–pass filter characteristics, and are reserved for manufacturer's use only. In normal operation, each pin is decoupled to V_{ref} with 0.1 μF capacitors.

X1
Crystal Oscillator Output (Pin 8)

A 3.579545 MHz ± 0.1% crystal oscillator is tied to this pin with the other end connected to X2.

X2
Crystal Oscillator Input (Pin 9)

A 3.579545 MHz ± 0.1% crystal oscillator is tied to this pin with the other end connected to X1. X2 may be driven directly from an appropriate external clock source. In this case, X1 should be held open.

GND
Ground (Pins 10, 18)

Ground pins are connected to the system ground.

V_{CC}
Power Supply (Pins 11, 19)

The digital supply pins are connected to the positive power supply (5 V).

$\overline{DV}$
DTMF Data Valid (Pin 12)

This pin goes low when valid DTMF tones are detected. The guard time of DTMF tone detection (t_{on}) and release (t_{off}) is programmed by two bits of serial data (CD1, CD0) as shown in Table 2. This feature improves the immunity to the short noise and momentary dropouts. See Figure 2 for the detailed timing diagram.

$\overline{TD}$
Tone Detect (Pin 13)

This pin goes low immediately after valid DTMF tones are detected, regardless of the guard time set by two bits of serial data. This pin also outputs the short high pulse when the device detects the change of DTMF tones without a silent period. For a detailed description, see Figure 2.

R/$\overline{W}$
Read/Write Data Switch (Pin 14)

This pin is used for controlling the input/output direction of the DATA I/O pin.

DATA
Serial Data Input/Output (Pin 15)

When the R/$\overline{W}$ pin is at logic low, the DATA pin works as the 14–bit control register input which determines the function mode, DTMF tones, transmit level (or receiver gain level), detect time, and transmit squelch. When the R/W pin is at logic high, the DATA pin works as the 4–bit status register output which provides the hexadecimal codes corresponding to the detected digit.

EN
Enable Input (Pin 16)

When the R/$\overline{W}$ pin is held low, high level input to this pin transfers the 14 bits of control register data to the mode control logic, then the function mode is immediately changed. When this pin is at logic low, the control register and the mode control logic are isolated. Therefore, the 14 bits of data in the control register must not be changed while EN is at logic high level.

When the R/W pin is held high, the rising edge of the EN pin loads the DTMF data from the DTMF decoder into the status register, and shifts out the first bit (LSB = D0) to the DATA pin.

CLK
SPI Clock Input (Pin 17)

This pin is the SPI clock input for the 14–bit control register and the 4–bit status register. At the rising edge of CLK, the 14 bits of data are captured into the control register when R/W is at logic low, and the 4 bits of data are shifted out from the status register when R/W is at logic high.

DSI
Driver Summing Input (Pin 20)

This pin is the inverting input of the line driver. An external signal source may be connected to this pin through a series resistor R_{DSI}, transmitting the signal from the TxA1 and TxA2. The differential gain $G_{DSI} = (V_{TxA1} - V_{TxA2})/V_{DSI}$ is determined by the following equation:

$$G_{DSI} = -2\ R_F/R_{DSI},\ R_F - 20\ k\Omega$$

Note that the programmable transmit attenuator does not affect this case.

The DSI pin should be held open when not in use.

SERIAL DATA INTERFACE

REGISTER MAP DESCRIPTION

The timing diagram of the 14–bit control register input and the 4–bit status register output is shown in Figure 4. When the R/W pin is at logic low (write is selected), the control register is enabled. The 14 bits of data are captured into the control register at the rising edge of SCK. The 14 bits of data in the control register are transferred to the mode control logic at logic high to the EN pin, and then the function mode is immediately changed.

When the R/W pin is at logic high (read is selected), the status register is enabled to read out the decoded DTMF data. At the rising edge of EN, the four bits of data in the DTMF decoder are loaded into the status register, and the first bit (D0) is presented on the DATA pin. The next three bits are shifted out by following rising edges of CLK (see Figure 4).

FUNCTION MODE (M2 – M0)

These three bits (M2 – M0) determine the function mode shown in Table 1.

Table 1. Function Mode Truth Table

M2	M1	M0	Function Mode
0	0	0	DTMF Receive
0	0	1	DTMF Transmit
0	1	0	Single Tone Transmit
0	1	1	Power Down 1
1	0	0	Power Down 2
1	0	1	Analog Loopback

DTMF Receive Mode (M2 – M0 = 0, 0, 0)

The DTMF receiver is enabled. The transmitter is disabled.

DTMF Transmit Mode (M2 – M0 = 0, 0, 1)

The DTMF tone generator is enabled. The receiver is disabled.

Single Tone Mode (M2 – M0 = 0, 1, 0)

The transmitter generates one of the eight frequencies of DTMF tones. The receiver is disabled.

Power Down Mode (Mode 1: M2 – M0 = 0, 1, 1; Mode 2: M2 – M0 = 1, 0, 0)

In Power Down Mode 1, all internal circuits except for the oscillator are disabled, so that all output pins except for the X1 are in high–impedance state. The device current is decreased to 500 μA (max). In Power Down Mode 2, all internal circuits are disabled, so all output pins are in high impedance state. The device current is decreased to 1 μA (max).

Analog Loopback Mode (M2 – M0 = 1, 0, 1)

The transmitter output is internally connected to the receiver input.

TRANSMIT SQUELCH (SQ)

When the SQ bit is 1, the DTMF and single tone transmission are disabled (squelch is selected). However, the transmit squelch does not affect the external signal input from DSI.

DTMF TONE DETECT/REJECT TIME (CD1, CD0)

The CD1 and CD0 bits determine DTMF tones detect time (t_{on}) and release time (t_{off}) of the DV pin, as shown in Table 2. The timing diagram is shown in Figure 2.

Table 2. DTMF Detect Time Truth Table

CD1	CD0	t_{on} (ms)	t_{off} (ms)
0	0	Reserved	
0	1	20	20
1	0	30	30
1	1	40	20

CONTROL REGISTER (R/$\overline{W}$ = "L")

FUNCTION MODE	: 3 BITS	M2	M1	M0	
TRANSMIT SQUELCH	: 1 BIT	SQ			
DTMF DETECT TIME	: 2 BITS	CD1	CD0		
TRANSMIT ATTENUATOR/AGC GAIN	: 4 BITS	A3	A2	A1	A0
TRANSMIT FREQUENCY	: 4 BITS	T3	T2	T1	T0

STATUS REGISTER (R/$\overline{W}$ = "H")

RECEIVED TONE FREQUENCY	: 4 BITS	D3	D2	D1	D0

TRANSMIT ATTENUATOR/AGC GAIN (A3 – A0)

The A3 – A0 bits determine the analog transmit level of DTMF tones. The transmit attenuator range is controlled from 0 to 15 dB in 1 dB steps as shown in Table 3. However, this attenuator does not affect the external signal source from DSI. These four bits also determine the AGC amplifier gain in DTMF receive mode. In normal operation, “automatic” may be selected so that the receiver’s gain is automatically adjusted, corresponding to the input signal level.

TRANSMIT TONE FREQUENCY (T3 – T0)

The T3 – T0 bits determine DTMF tone frequencies transmitted from TxA1 and TxA2 in DTMF transmit and analog loopback mode, and determine the single tone frequency in single tone mode. Tone frequency assignments for the T3 – T0 bits are shown in Table 4.

RECEIVED TONE FREQUENCY (D3 – D0)

The D3 – D0 bits provide hexadecimal codes corresponding to detected DTMF tones. Tone frequency assignments for the D3 – D0 bits are shown in Table 4.

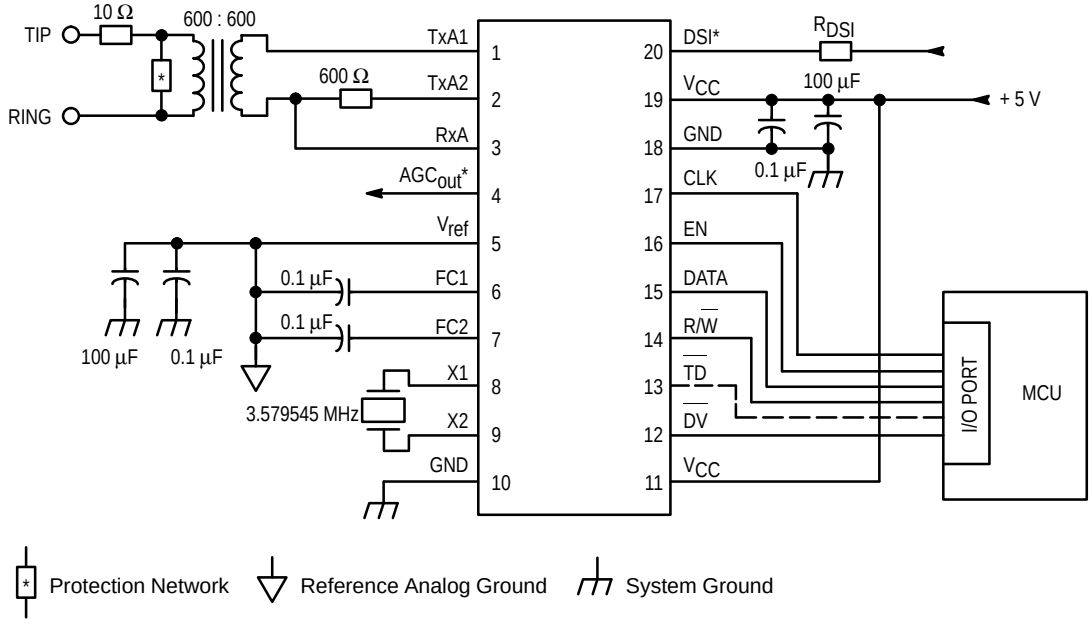
Table 3. Transmit Attenuator/AGC Gain Set Truth Table

A3	A2	A1	A0	Tx Attenuation (dB)	Rx AGC Gain (dB)
0	0	0	0	0	– 5.0
0	0	0	1	1	– 2.5
0	0	1	0	2	0.0
0	0	1	1	3	2.5
0	1	0	0	4	5.0
0	1	0	1	5	7.5
0	1	1	0	6	10.0
0	1	1	1	7	12.5
1	0	0	0	8	15.0
1	0	0	1	9	17.5
1	0	1	0	10	20.0
1	0	1	1	11	Clamp
1	1	0	0	12	Automatic
1	1	0	1	13	—
1	1	1	0	14	—
1	1	1	1	15	—

Table 4. Tone Frequency Truth Table

T3/D3	T2/D2	T1/D1	T0/D0	Tone Frequency (Hz)			
				DTMF Tx/Rx Mode Frequency			Single Tone Mode
				High Group	Low Group	Keyboard Equivalent	
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633
1	1	1	1	852	1633	C	1633
0	0	0	0	941	1633	D	941

APPLICATION CIRCUIT

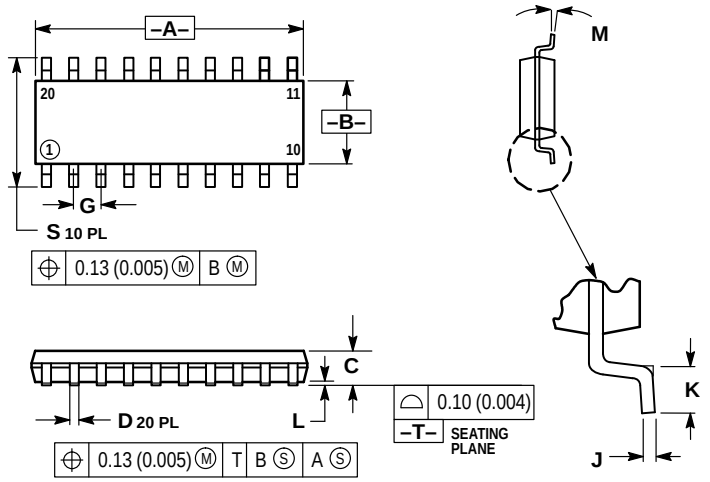


Protection Network Reference Analog Ground System Ground

* The external devices (i.e., modem) may be connected on these pins, using the built–in line interface circuit.

PACKAGE DIMENSIONS

F SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751J–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.12 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	—	2.00	—	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0 °	7 °	0 °	7 °
S	7.40	8.20	0.291	0.323

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