- **Organization . . . 524288 By 8 Bits**
  262144 By 16 Bits
- **Array-Blocking Architecture**
  - **One 16K-Byte Protected Boot Block**
  - **Two 8K-Byte Parameter Blocks**
  - **One 96K-Byte Main Block**
  - **Three 128K-Byte Main Blocks**
  - **Top or Bottom Boot Locations**
- **'28F400Axy Offers a User-Defined 8-Bit (Byte) or 16-Bit (Word) Organization**
- **'28F004Axy Offers Only the 8-Bit Organization**
- **Maximum Access/Minimum Cycle Time**
  - **Commercial and Extended**

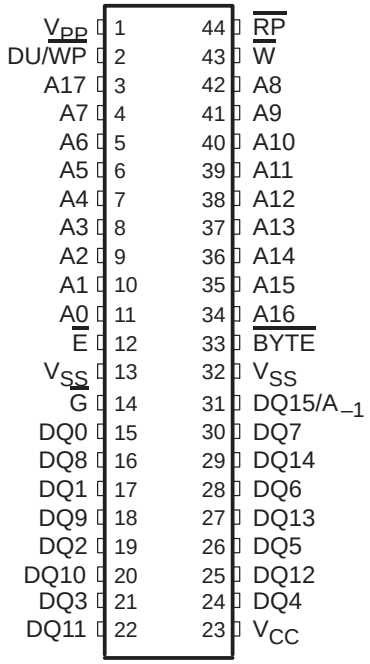
5-V $V_{CC} \pm 10\%$		3.3-V $V_{CC} \pm 0.3$ V
'28F400Axy60	60 ns	110 ns
'28F400Axy70	70 ns	130ns
'28F400Axy80	80 ns	150 ns

  - **Automotive (offered for only 5-V V_{CC} voltage configurations)**

5-V $V_{CC} \pm 10\%$	
'28F400Axy70	70 ns
'28F400Axy80	80 ns
'28F400Axy90	90 ns

  (x = S, E, F, M, or Z Depending on V_{CC}/V_{PP} Configuration)
  (y = T or B for Top or Bottom Boot-Block Configuration)
- **100000 and 10000 Program/Erase Cycle Versions**
- **Three Temperature Ranges**
  - **Commercial . . . 0°C to 70°C**
  - **Extended . . . – 40°C to 85°C**
  - **Automotive . . . – 40°C to 125°C**
- **Industry Standard Packages Offered in**
  - **40-Pin TSOP (DCD Suffix)**
  - **44-Pin PSOP (DBJ Suffix)**
  - **48-Pin TSOP (DCD Suffix)**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active Write . . . 248 mW (Byte Write)**
  - **Active Read . . . 330 mW (Byte Read)**
  - **Active Write . . . 248 mW (Word Write)**
  - **Active Read . . . 330 mW (Word Read)**
  - **Block Erase . . . 165 mW**
  - **Standby . . . 0.72 mW (CMOS-Input Levels)**

DBJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
BYTE	Byte Enable
DQ0–DQ14	Data In/Out
DQ15/A$_{-1}$	Data In/Out (word-wide mode), Low-Order Address (byte-wide mode)
E	Chip Enable
G	Output Enable
NC	No Internal Connection
RP	Reset/Deep Power-Down
V_{CC}	Power Supply
V_{PP}	Power Supply for Program/Erase
V_{SS}	Ground
W	Write Enable
DU/WP	Do Not Use for 'AMy or 'AZy /Write Protect

- **Fully Automated On-Chip Erase and Word/Byte Program Operations**
- **Write Protection for Boot Block**
- **Industry Standard Command-State Machine (CSM)**
  - **Erase Suspend/Resume**
  - **Algorithm-Selection Identifier**
- **Three Different Combinations of Supply Voltages Offered**
- **All Inputs/Outputs TTL Compatible**

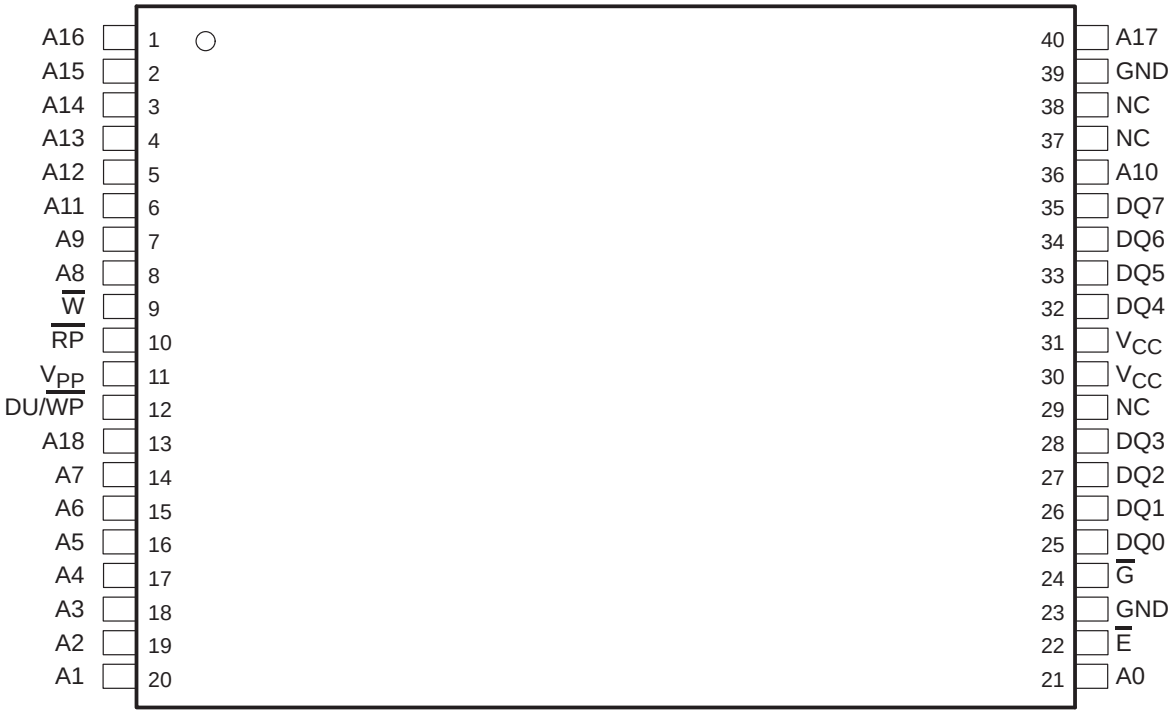


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DCD PACKAGE-40 PIN
(TOP VIEW)



DCD PACKAGE-48 PIN
(TOP VIEW)

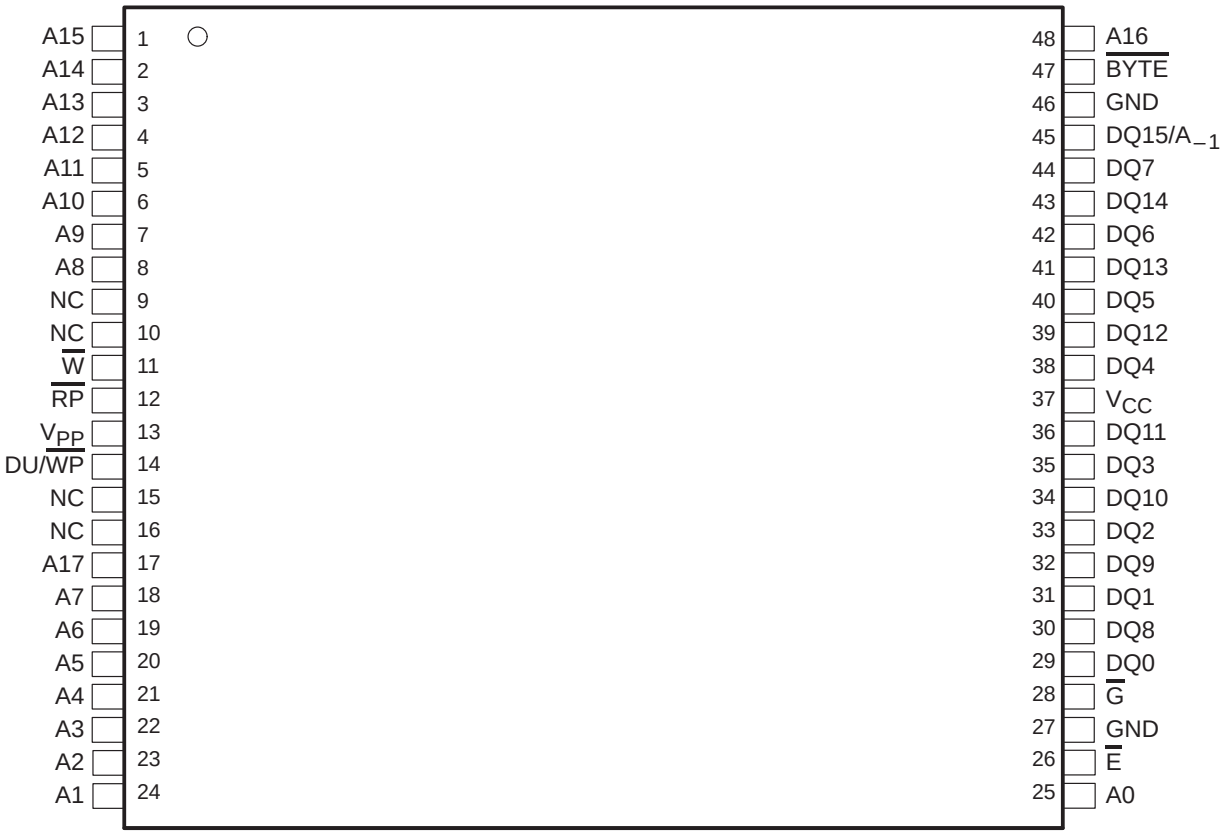


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description

The TMS28F400Axy is a 524288 by 8 bits/262144 by 16 bits (4194304-bit), boot-block flash memory that can be electrically block-erased and reprogrammed. The TMS28F400Axy is organized in a blocked architecture consisting of:

- One 16K-byte protected boot block
- Two 8K-byte parameter blocks
- One 96K-byte main block
- Three 128K-byte main blocks

Table 1 lists the five different voltage configurations available for ordering. Operation as a 512K-byte (8-bit) or a 256K-word (16-bit) organization is user-definable.

Table 1. V_{CC}/V_{PP} Voltage Configurations, Temperature, and Speeds Matrix

DEVICE	DEVICE CONFIGURATION		TEMPERATURE (T_A)	ACCESS SPEEDS – 5-V(3.3-V) V_{CC}
	READ (V_{CC})	PROGRAM/ERASE (V_{PP})		
TMS28F400ASy	3.3 V± 0.3 V or 5 V±10%	5 V±10% or 12 V±5%	0°C to 70°C	60(110), 70(130), 80(150) ns
			–40°C to 85°C	60(110), 70(130), 80(150) ns
TMS28F400AEy	2.7 to 3.6 V or 5 V±10%	5 V±10% or 12 V±5%	0°C to 70°C	60(110), 70(130), 80(150) ns
			–40°C to 85°C	60(110), 70(130), 80(150) ns
TMS28F400AMy	3.3 V± 0.3 V or 5 V±10%	12 V±10%	0°C to 70°C	60(110), 70(130), 80(150) ns
			–40°C to 85°C	60(110), 70(130), 80(150) ns
TMS28F400AFy	5 V±10%	5 V±10% or 12 V±5%	0°C to 70°C	60, 70, 80 ns
			–40°C to 85°C	60, 70, 80 ns
			–40°C to 125°C†	70, 80, 90 ns
TMS28F400AZy	5 V±10%	12 V±10%	0°C to 70°C	60, 70, 80 ns
			–40°C to 85°C	60, 70, 80 ns
			–40°C to 125°C†	70, 80, 90 ns

† Only the 44-pin PSOP is offered in the –40°C to 125°C temperature range.
NOTE 1: All configurations are available in the TMS28F004Axy (8 bit configuration only) and top or bottom boot.

description (continued)

The TMS28F004Axy is offered in a 512K-byte organization only. The operation for this device is the same as the TMS28F400Axy and is offered in the same voltage configurations. TMS28F004Axy can be substituted for the byte-wide TMS28F400Axy with the latter being the generic name for this device family.

Embedded program and block-erase functions are fully automated by the on-chip write state machine (WSM), simplifying these operations and relieving the system microcontroller of secondary tasks. WSM status can be monitored by an on-chip status register to determine progress of program/erase tasks. The device features user-selectable block erasure.

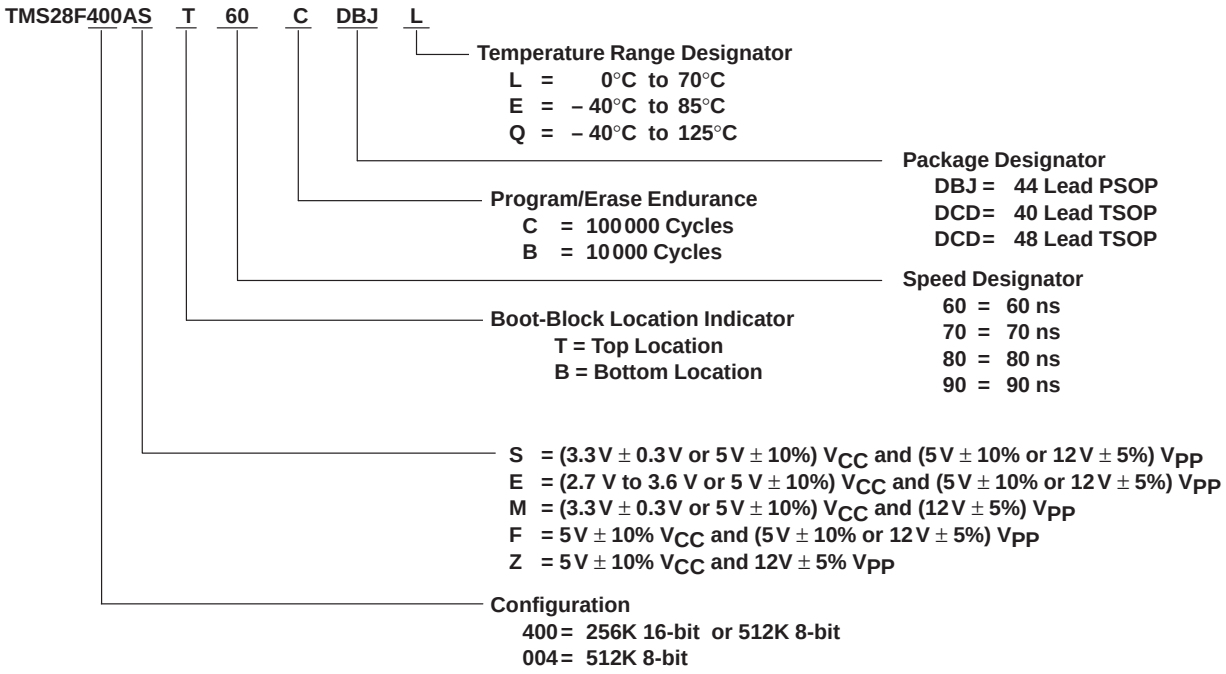
The configurations are as follows:

- The TMS28F400ASy configuration has the auto-select feature that allows the user alternative read and program/erase voltages. Memory reads can be performed using 3.3-V V_{CC} for optimum power consumption or 5-V V_{CC} for device performance. Erasing or programming the device can be accomplished with 5-V V_{PP}, which eliminates having to use a 12-V source and/or in-system voltage converters. Alternatively,12-V V_{PP} operation exists for systems that already have a 12-V power supply, which provides faster programming and erasing times. This configuration is offered in two temperature ranges: 0°C to 70°C and –40°C to 85°C.
- The TMS28F400AEy configuration offers the auto-select feature of the TMS28F400ASy with an extended V_{CC} range of 2.7-V to 3.6-V (3-V nominal). Memory reads can be performed using 3-V V_{CC}, for more efficient power consumption than the 'ASy device.
- The TMS28F400AMy configuration offers a 3-V or 5-V memory read with a 12-V program and erase. This configuration is intended for low 3.3-V reads and the fast programming offered with the 12-V V_{PP} and 5-V V_{CC}. This configuration is offered in two temperature ranges: 0°C to 70°C and – 40°C to 85°C.
- The TMS28F400AFy configuration offers a 5-V memory read with a 5-V or 12-V program and erase. This configuration is intended for systems using a single 5-V power supply. This configuration is offered in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.
- The TMS28F400AZy configuration offers a 5-V memory read with a 12-V program and erase for fast programming and erasing times. This configuration is offered in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

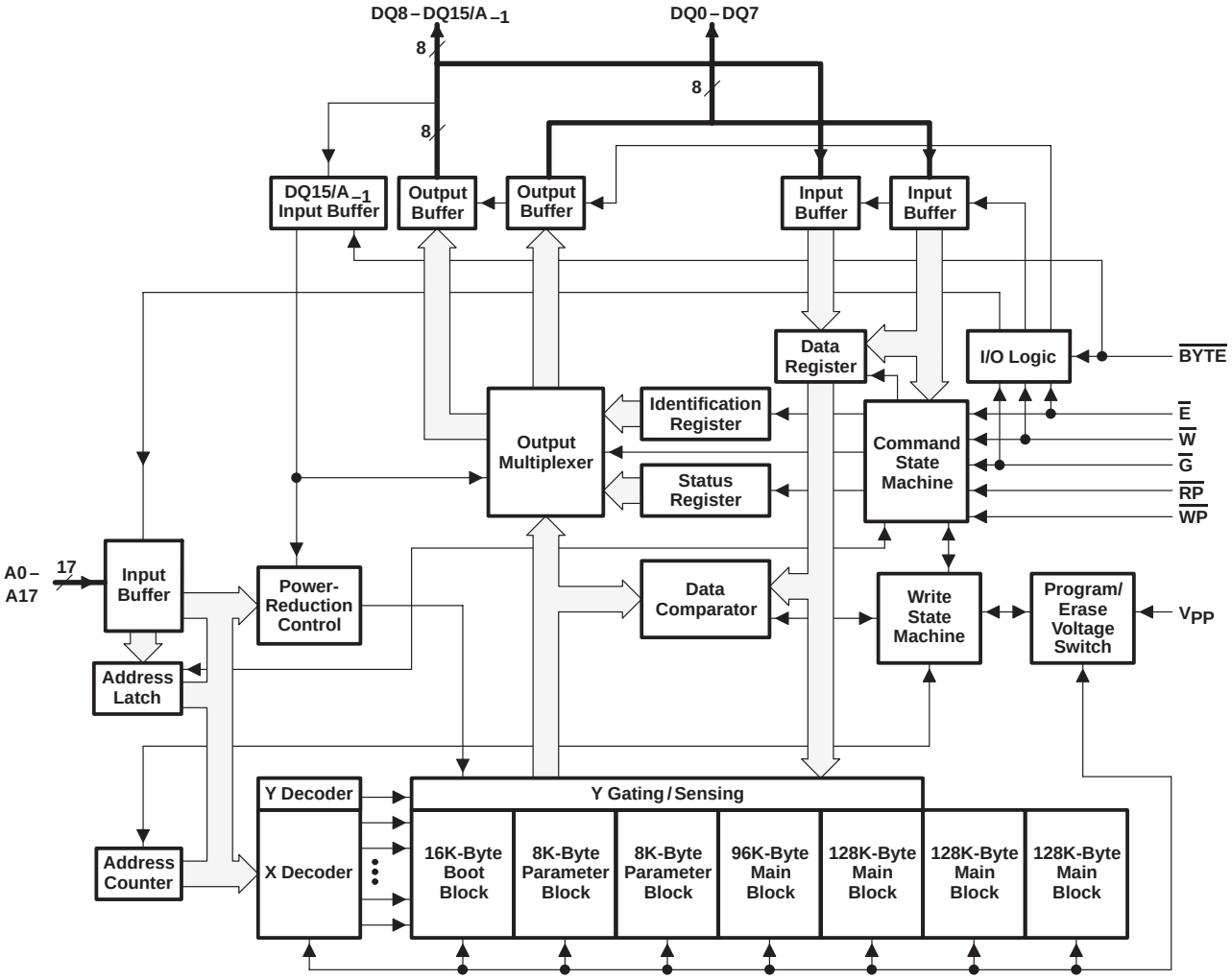
The y in the device name represents a T for top or B for bottom boot-block configuration.

All configurations of the TMS28F400Axy are offered in a 44-pin plastic small-outline package (PSOP) and a 48-pin thin small-outline package (TSOP). The TMS28F004Axy is offered in a 40-pin TSOP only. Both the 40-pin and 48-pin TSOP are offered for the 0°C to 70°C and – 40°C to 85°C temperature ranges only.

device symbol nomenclature



functional block diagram



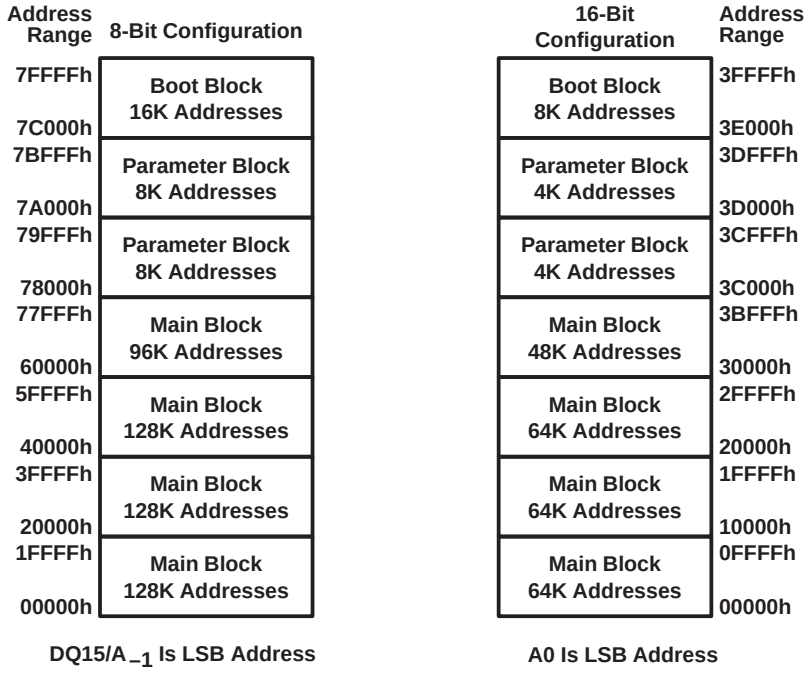
architecture

The TMS28F400Axy uses a blocked architecture to allow independent erasure of selected memory blocks. The block to be erased is selected by using any valid address within that block.

block memory maps

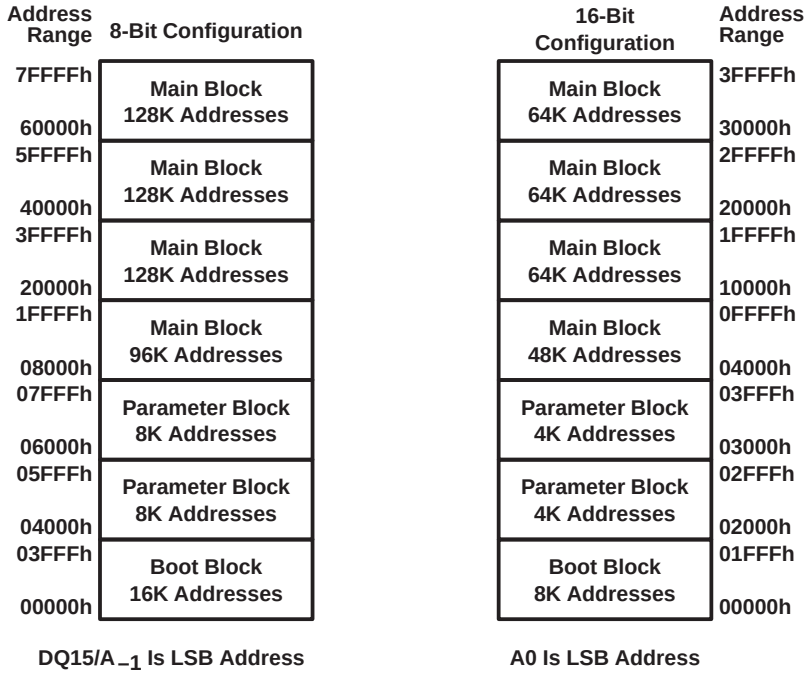
The TMS28F400Axy is available with the block architecture mapped in either of two configurations: the boot block located at the top or at the bottom of the memory array, as required by different microprocessors. The TMS28F400AxB (bottom boot block) is mapped with the 16K-byte boot block located at the low-order address range (00000h to 01FFFh). The TMS28F400AxT (top boot block) is inverted with respect to the TMS28F400AxB with the boot block located at the high-order address range (3E000h to 3FFFFh). Both of these address ranges are for word-wide mode. Figure 1 and Figure 2 show the memory maps for these configurations. The TMS28F004Axy is mapped as the 8-bit configuration of the TMS28F400Axy, except that the least significant bit (LSB) is A0 instead of A_{-1}.

block memory maps (continued)



NOTE A: The TMS28F004AxT is mapped the same as the 8-bit configuration of the TMS28F400AxT except that the LSB is A0.

Figure 1. TMS28F400AxT (Top Boot Block) Memory Map (See Note A)



NOTE A: The TMS28F004AxB is mapped the same as the 8-bit configuration of the TMS28F400AxB except that the LSB is A0.

Figure 2. TMS28F400AxB (Bottom Boot Block) Memory Map (See Note A)

boot-block data protection

The 16K-byte boot block can be used to store key system data that is seldom changed in normal operation. Data in this block can be secured by using different combinations of the reset/power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$) and V_{PP} supply levels. Table 2 provides a list of these combinations.

parameter block

Two parameter blocks of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternatively, the parameter blocks can be used for additional boot- or main-block data. If a parameter block is used to store additional boot-block data, caution must be exercised because the parameter block does not have the boot-block data-protection safety feature.

main block

Primary memory on the TMS28F400Axy is located in four main blocks. Three of the blocks have storage capacity for 128K bytes and the fourth block has storage capacity for 96K bytes.

data protection

Data is secured or unsecured by using different combinations of the reset/power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$), and V_{PP} supply levels. Table 2 provides a list of these combinations.

There are two configurations to secure the entire memory against inadvertant alteration of data. The V_{PP} supply pin can be held below the V_{PP} lock-out voltage level (V_{PPLK}) or the reset/deep power-down pin ($\overline{RP}$) can be pulled to a logic-low level. Note if $\overline{RP}$ is held low, the device resets which means it powers down and, therefore, cannot be read. Typically this pin tied to the system reset for additional protection during system power up.

The boot block sector has an additional security feature through the $\overline{WP}$ pin ('ASy, 'AEy, and 'AFy device configurations only). When the $\overline{RP}$ pin is at a logic-high level, the $\overline{WP}$ pin controls whether the boot block sector is protected. When $\overline{WP}$ is held at the logic-low level, the boot block is protected. When $\overline{WP}$ is held at the logic-high level, the boot block is unprotected along with the rest of the other sectors. Alternatively, the entire memory for all voltage configurations can be unprotected by pulling the $\overline{RP}$ pin to V_{HH} (12 V).

Table 2. Data-Protection Combinations

DATA PROTECTION PROVIDED	'ASy, 'AEy, OR 'AFy			'AMy OR 'AZy		
	V_{PP}	$\overline{RP}$	$\overline{WP}$†	V_{PP}	$\overline{RP}$	$\overline{WP}$†
All blocks locked	V_{IL}	X	X	V_{IL}	X	X
All blocks locked (reset)	X	V_{IL}	X	X	V_{IL}	X
All blocks unlocked	$>V_{PPLK}$ $>V_{PPLK}$	V_{HH} V_{IH}	X V_{IH}	V_{HH}	V_{HH}	X
Only boot block locked	$>V_{PPLK}$	V_{IH}	V_{IL}	V_{HH}	V_{IH}	X

† For the TMS28F400AZy and TMS28F400AMy 12-V V_{PP}-only products, the $\overline{WP}$ pin is disabled and can be left floating. To unlock blocks, $\overline{RP}$ must be at V_{HH}.

command-state machine (CSM)

Commands are issued to the CSM using standard microprocessor write timings. The CSM acts as an interface between the external microprocessor and the internal WSM. The available commands are listed in Table 3 and the descriptions of these commands are shown in Table 4. When a program or erase command is issued to the CSM, the WSM controls the internal sequences and the CSM responds only to status reads. After the WSM completes its task, the WSM status bit (SB7) is set to a logic-high level (1), allowing the CSM to respond to the full command set again.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip CSM through I/O pins DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires a command code to be entered into the CSM. Table 3 lists the CSM codes for all modes of operation.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status-register command into the CSM (cycle 1) and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status-register bits SB0 through SB7 correspond to DQ0 through DQ7.

Table 3. CSM Codes for Device Mode Selection

COMMAND CODE ON DQ0–DQ7†	DEVICE MODE
00h	Invalid/Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear Status Register
70h	Read Status Register
90h	Algorithm Selection
B0h	Erase-Suspend
D0h	Erase-Resume/Block-Erase Confirm
FFh	Read Array

† DQ0 is the least significant bit. DQ8–DQ15 can be any valid 2-state level.

command definitions

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 4 for the CSM command definitions and data for each of the bus cycles. Table 5 lists the status register bits and definitions.

Following the read-algorithm-selection-code command, two read cycles are required to access the manufacturer-equivalent code and the device-equivalent code. Table 6, Table 7, and Table 8 list the code.

command definitions (continued)

Table 4. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	CSM INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	X	FFh	Read	X	Data Out
Read Algorithm-Selection Code	2	Write	X	90h	Read	A0	M/D
Read-Status Register	2	Write	X	70h	Read	X	SRB
Clear-Status Register	1	Write	X	50h			
Program Mode							
Program Setup/Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase Suspend/ Erase Resume	2	Write	X	B0h	Write	X	D0h

Legend:

BEA Block-erase address. Any address selected within a block selects that block for erase.
M/D Manufacturer-equivalent/device-equivalent code
PA Address to be programmed
PD Data to be programmed at PA
SRB Status-register data byte that can be found on DQ0–DQ7
X Don't care

status register

The status register allows the user to determine whether the state of a program/erase operation is pending or complete. The status register is monitored by writing a read-status command to the CSM and reading the resulting status code on I/O pins DQ0–DQ7. This is valid for operation in either the byte- or word-wide mode. When writing to the CSM in word-wide mode, the high order I/O pins (DQ8–DQ15) can be set to any valid 2-state level. When reading the status bits during a word-wide read operation, the high order I/Os (DQ8–DQ15) are set to 00h internally, so the user needs to interpret only the low order I/O pins (D0–DQ7).

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{G}$ or $\overline{E}$. The latest falling edge of either of these two signals updates the latch within a given read cycle. Latching the data prevents errors from occurring if the register input change during a status-register read. To ensure that the status-register output contains updated status data, $\overline{E}$ or $\overline{G}$ must be toggled for each subsequent status read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 5 defines the status register bits and their functions.

status register (continued)

Table 5. Status-Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-state-machine status	1 = Ready 0 = Busy	If SB7 = 0 (busy), the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. Until this occurs, the other status bits are not valid. If the WSM status bit shows busy (0), the user must toggle $\overline{E}$ or $\overline{G}$ periodically to determine when the WSM has completed an operation (SB7 = 1) since SB7 is not updated automatically at the completion of a WSM task.
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1) indicating that the erase operation has been suspended. The WSM status bit also is set high (SB7 = 1) indicating that the erase-suspend operation has been completed successfully. The ESS bit remains at a logic-high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Block erase error 0 = Block erase good	SB5 = 0 indicates that a successful block erasure has occurred. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to erase the device completely.
SB4	Program status (PS)	1 = Byte/word program error 0 = Byte/word program good	SB4 = 0 indicates successful programming has occurred at the addressed block location. SB4 = 1 indicates that the WSM was unable to program the addressed block location correctly.
SB3	V_{PP} status (V_{PPS})	1 = Program abort: V_{PP} range error 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming. If V_{PP} is lower than V_{PPL} after a program or erase command has been issued, SB3 is set to a 1 indicating that the programming operation is aborted. If V_{PP} is between V_{PPH} and V_{PPL}, SB3 is not set.
SB2–SB0	Reserved		These bits must be masked out when reading the status register.

byte-wide or word-wide mode selection

The memory array is divided into two parts: an upper-half that outputs data through I/O pins DQ8–DQ15, and a lower-half that outputs data through DQ0–DQ7. Device operation in either byte-wide or word-wide mode is user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at a logic-high level, the device is in the word-wide mode and data is written to, or read from, I/O pins DQ0–DQ15. When $\overline{BYTE}$ is at a logic-low level, the device is in the byte-wide mode and data is written to or read from I/O pins DQ0–DQ7. In the byte-wide mode, I/O pins DQ8–DQ14 are placed in the high-impedance state and DQ15/A_{-1} becomes the low-order address pin and selects either the upper or lower half of the array. Array data from the upper half (DQ8–DQ15) and the lower half (DQ0–DQ7) are multiplexed to appear on DQ0–DQ7. Table 6, Table 7, and Table 8 summarize operational modes.

byte-wide or word-wide mode selection (continued)

Table 6. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH}) (see Note 2)

MODE	$\overline{WP}$	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ0–DQ15
Read	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 4470h (top boot block)
									Device-equivalent code 4471h (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

NOTES: 2. X = don't care
3. When writing commands to the '28F400Axy, V_{PP} must be in the appropriate V_{PP} voltage range (as shown in the recommended operating conditions table) for block-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for the combinations).

Table 7. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL}) (see Note 2)

MODE	$\overline{WP}$	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ15/A_{-1}	DQ8–DQ14	DQ0–DQ7
Read lower byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z	Data out
Read upper byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code 70h (top boot block)
											Device-equivalent code 71h (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	X	Hi-Z	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTES: 2. X = don't care
3. When writing commands to the '28F400Axy, V_{PP} must be in the appropriate V_{PP} voltage range (as shown in the recommended operating conditions table) for block-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for the combinations).

byte-wide or word-wide mode selection (continued)

Table 8. Operation Modes for TMS28F004Axy

MODE	$\overline{WP}$	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ0 – DQ7
Read	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 89h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 78h (top boot block)
									Device-equivalent code 79h (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

NOTES: 2. X = don't care

3. When writing commands to the '28F004Axy, V_{PP} must be in the appropriate V_{PP} voltage range (as shown in the recommended operating conditions table) for block-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for a list of the combinations).

command-state machine (CSM) operations

The CSM decodes instructions for read, read algorithm-selection code, read status register, clear status register, program, erase, erase-suspend, and erase-resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 3 for CSM codes). During a program or erase cycle, the CSM informs the WSM that a program or erase cycle has been requested. During a program cycle, the WSM controls the program sequences and the CSM responds only to status reads.

During an erase cycle, the CSM responds to status read and erase-suspend commands. When the WSM has completed its task, the WSM status bit (SB7) is set to a logic-high level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range. For data protection, it is recommended that $\overline{RP}$ be held at a logic-low level during a CPU reset.

clear status register

The internal circuitry can set only the V_{PP} status (SB3), the program status bit (SB4), and the erase status bit (SB5) of the status register. The clear-status-register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the device returns to the read array mode.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

- read array

  The array level is read by entering the command code FFh on DQ0–DQ7. Control pins $\overline{E}$ and $\overline{G}$ must be at a logic-low level (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the blocks selects that block and allows data to be read from the block.

- read algorithm-selection code

  Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and a second to read the device-equivalent code. Control pins $\overline{E}$ and $\overline{G}$ must be at a logic-low level (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at a logic-low level (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic-high level (V_{IH}). Alternatively, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are “don’t cares” (see Table 4, Table 6, Table 7, Table 8).

- read status register

  The status register is read by entering the command code 70h on DQ0–DQ7. Control pins $\overline{E}$ and $\overline{G}$ must be at a logic-low level (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status register contents are updated on the falling edge of $\overline{E}$ or $\overline{G}$, whichever occurs last within the cycle.

programming operations

There are two CSM commands for programming: program setup and alternate program setup (see Table 3). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM normally cannot be interrupted until the program algorithm is completed (see Figure 3 and Figure 4).

Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain in the appropriate V_{PP} voltage range, as shown in the recommended operating conditions table. Different combinations of $\overline{RP}$, $\overline{WP}$, and V_{PP} pin voltage levels ensure that data in certain blocks are secure, and, therefore, cannot be programmed (see Table 2 for a list of combinations). Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic-high level, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed by the TMS28F004Axy and TMS28F400Axy devices: block erase and erase suspend/erase resume. An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads or erase-suspend commands until the WSM completes its task.

- block erasure

  Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Note that different combinations of $\overline{RP}$, $\overline{WP}$ and V_{PP} pin voltage levels ensure that data in certain blocks are secure and, therefore, cannot be erased (see Table 2 for a list of combinations). Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h) followed by block-erase confirm (D0h) (see Figure 5). A two-command erase sequence protects against accidental erasure of memory contents.

  Erase setup and confirm commands are latched on the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first. Block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{E}$ or $\overline{W}$ (see Figure 14 and Figure 15). When the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally, verification is performed to ensure that all bits are correctly erased. Monitoring of the erase operation is possible through the status register (see the subsection, “read status register”).

- erase suspend/erase resume

  During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status-register, and erase-resume commands. During the erase-suspend operation, array data must be read from a block other than the one being erased. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 5 and Figure 6).

automatic power-saving mode

Substantial power savings are realized during periods when the array is not being read and the device is in the active mode. During this time, the device switches to the automatic power-saving (APS) mode. When the device switches to this mode, I_{CC} is typically reduced from 40 mA to 1 mA (I_{OUT} = 0 mA). The low level of power is maintained until another read operation is initiated. In this mode, the I/O pins retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control pins toggle within approximately a 200-ns time-out period. At least one transition on $\overline{E}$ must occur after power up to activate this mode.

reset/deep power-down mode

Very low levels of power consumption can be attained by using a special pin, $\overline{RP}$, to disable internal device circuitry. When $\overline{RP}$ is at a CMOS logic-low level of 0.0 V ± 0.2 V, a much lower I_{CC} value or power is achievable. This is important in portable applications where extended battery life is of major concern.

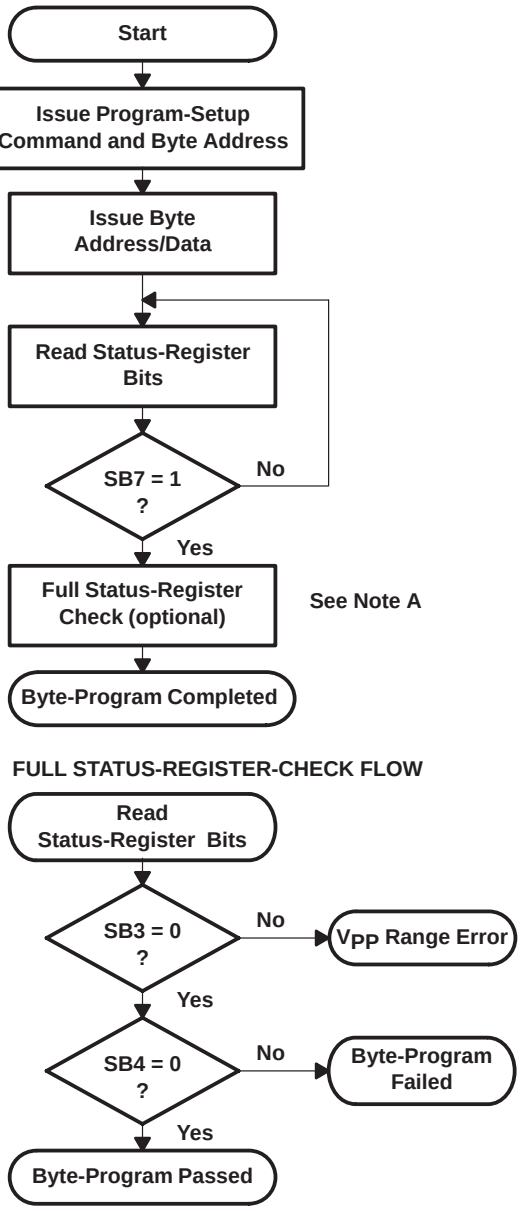
A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of $t_{d(RP)}$ is required before data is valid, and a minimum of $t_{rec(RPHE)}$ and $t_{rec(RPHW)}$ in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

reset/deep power-down mode (continued)

If $\overline{RP}$ goes low during a program or erase operation, the device powers down and, therefore, becomes nonfunctional. Data being written or erased at that time becomes invalid or indeterminate, requiring that the operation be performed again after power restoration.

power-supply detection

$\overline{RP}$ must be connected to the system reset/power good signal to ensure that proper synchronization is maintained between the CPU and the flash memory operating modes. The default state after power up and exit from deep power-down mode is read array. $\overline{RP}$ also is used to indicate that the power supply is stable so that the operating supply voltage can be established (3 V, 3.3 V or 5 V). Figure 10 shows the proper power-up sequence. To reset the operating supply voltage, the device must be completely powered off (V_{CC} = 0 V) before the new supply voltage is detected.



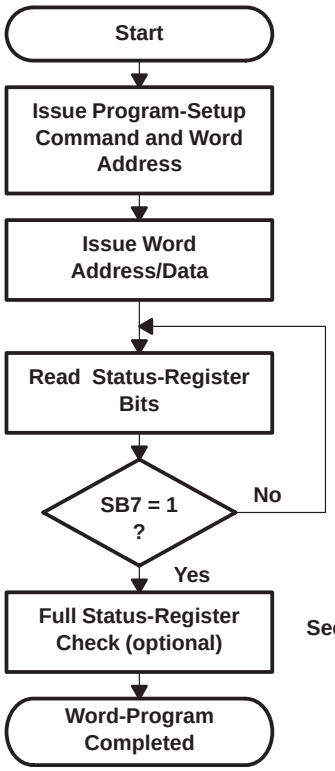
BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status-register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent bytes Write FFh after the last byte-programming operation to reset the device to read-array mode.		

FULL STATUS-REGISTER-CHECK FLOW

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Byte-program error (see Note C)

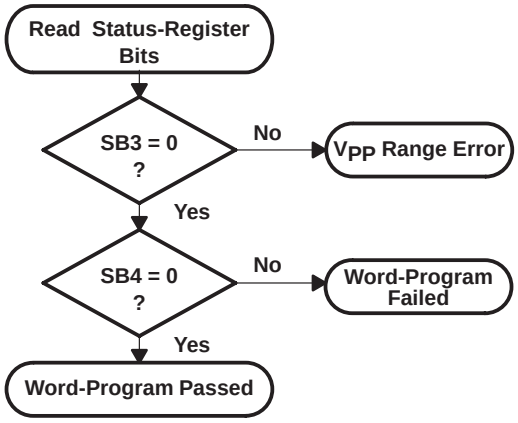
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status-register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read-array mode.		

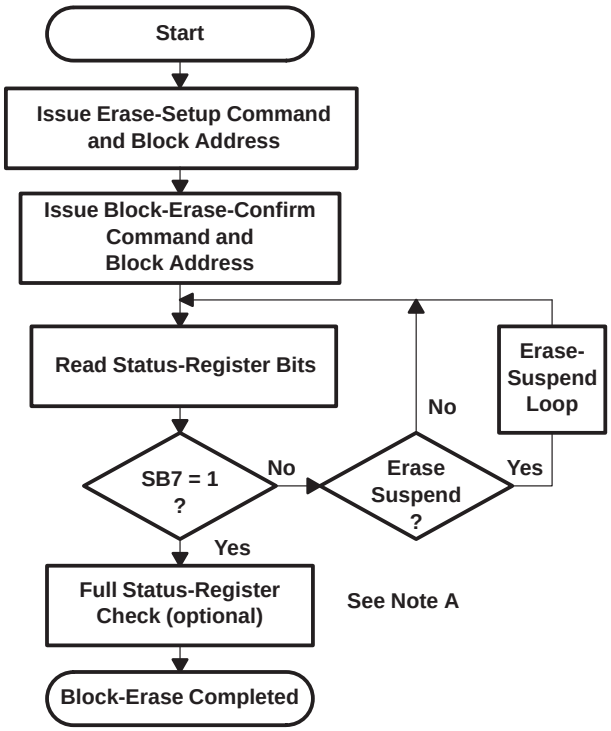
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Word-program error (see Note C)

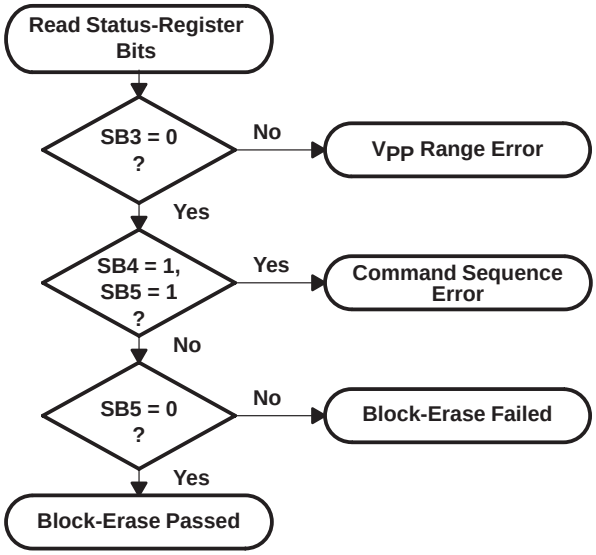
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Block Addr = Address within block to be erased
Write	Erase	Data = D0h Block Addr = Address within block to be erased
Read		Status-register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks Write FFh after the last block-erase operation to reset the device to read-array mode.		

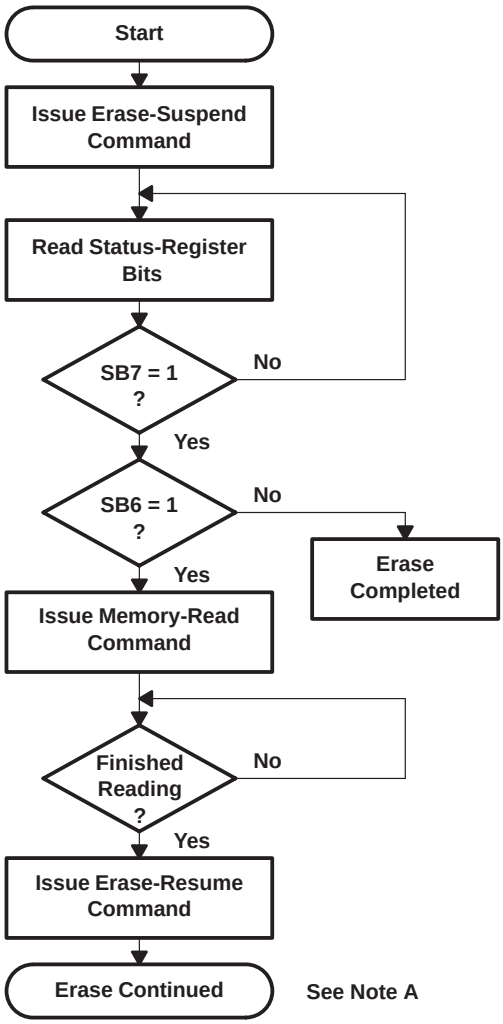
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Block-erase error
Standby		Check SB5 1 = Block-erase error (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 5. Automated Block-Erase Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h
Read		Status-register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Read memory	Data = FFh
Read		Read data from block other than that being erased.
Write	Erase resume	Data = D0h

NOTE A: See block-erase flowchart for complete erasure procedure.

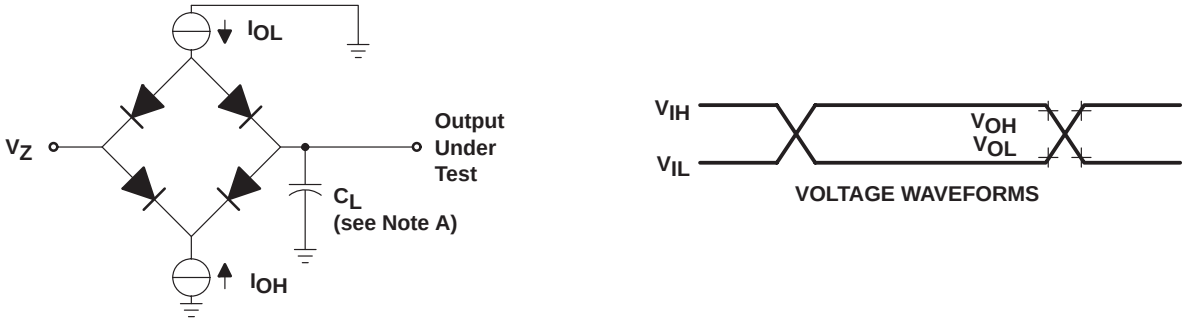
Figure 6. Erase-Suspend/Resume Flow Chart

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 4) . . . . . – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ . . . . . – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note 5) . . . . . – 0.6 V to 13.5 V
Output voltage range (see Note 6) . . . . . – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A, during read/erase/program: L suffix . . . . . 0°C to 70°C
E suffix . . . . . – 40°C to 85°C
Q suffix . . . . . – 40°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to V_{SS}.
5. The voltage on any input or output can undershoot to – 2 V for periods less than 20 ns. See Figure 8.
6. The voltage on any input or output can overshoot to 7 V for periods less than 20 ns. See Figure 9.



NOTES: A. C_L includes probe and fixture capacitance.
B. AC test conditions are driven at V_{IH} and V_{IL}, Timing measurements are made at V_{OH} and V_{OL} levels on both inputs and outputs. See Table 9 for values based on V_{CC} operating range..
C. Each device must have a 0.1 μF ceramic capacitor connected to V_{CC} and V_{SS} as close as possible to the device pins.

Figure 7. Load Circuit and Voltage Waveforms

Table 9. AC Test Conditions

V_{CC} RANGE	I_{OL}	I_{OH}	V_Z†	V_{OL}	V_{OH}	V_{IL}	V_{IH}	C_L	tf	tr
5 V ± 10%	2.1	–0.4	1.5	0.8	2.0	0.45	2.4	100	< 10	< 10
3.3 ± 0.3 V	0.5	–0.5	1.5	1.5	1.5	0.0	3.0	50	< 10	< 10
2.7 to 3.6 V	0.1	–0.1	1.35	1.35	1.35	0.0	2.7	50	< 10	< 10

† V_Z is the measured value used to detect high impedance.

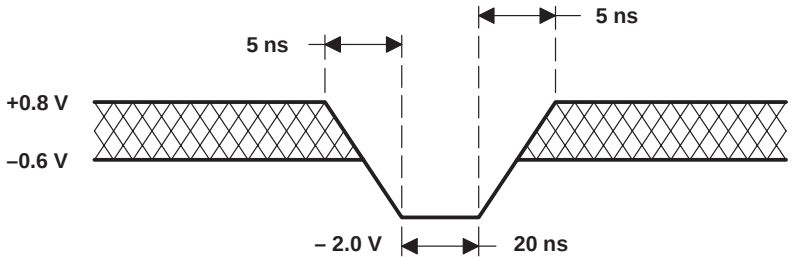


Figure 8. Maximum Negative Overshoot Waveform

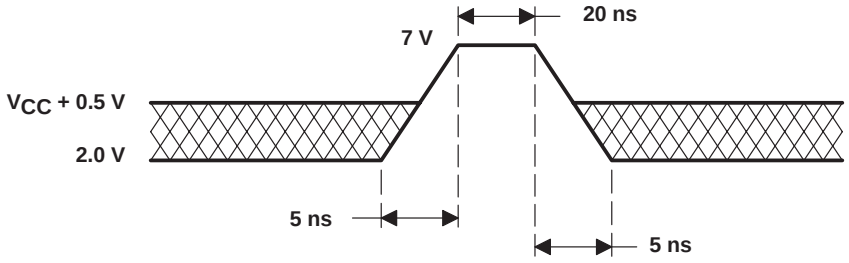


Figure 9. Maximum Positive Overshoot Waveform

capacitance over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Ci	Input capacitance			8	pF
C_O	Output capacitance	V_O = 0 V		12	pF

TMS28F004ASy and TMS28F400ASy

The TMS28F004ASy and the TMS28F400ASy configurations have the auto-select feature that allows alternative read and program/erase voltages. Memory reads can be performed using V_{CC} = 3.3 V for optimal power consumption or at V_{CC} = 5 V for device performance. Erasing or programming the device can be accomplished with V_{PP} = 5 V, which eliminates having to use a 12-V source and/or in-system voltage converters. Alternatively, the 12-V V_{PP} operation exists for systems that already have a 12-V power supply that provides faster programming and erasing times. This configuration is offered in two temperature ranges (0°C to 70°C and –40°C to 85°C).

recommended operating conditions for TMS28F004ASy and TMS28F400ASy

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	3.3-V V_{CC} range	3	3.3	3.6	V
			5-V V_{CC} range	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})	V_{PPL}	0		6.5	V
		During write/erase/erase suspend	5-V V_{PP} range	4.5	5	5.5	
			12-V V_{PP} range	11.4	12	12.6	
V_{IH}	High-level dc input voltage	3.3-V V_{CC} range	TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
		5-V V_{CC} range	TTL	2		V_{CC} + 0.3	
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage	3.3-V V_{CC} range	TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
		5-V V_{CC} range	TTL	– 0.3		0.8	
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase			0		1.5	V
T_A	Operating free-air temperature		L Suffix	0		70	°C
			E Suffix	– 40		85	

NOTE 7: Mimimum value at T_A = 25°C.

word/byte typical write and block-erase performance for TMS28F004ASy and TMS28F400ASy (see Notes 8 and 9)

PARAMETER	5-V V_{PP} RANGE						12-V V_{PP} RANGE					
	3.3-V V_{CC} RANGE			5-V V_{CC} RANGE			3.3-V V_{CC} RANGE			5-V V_{CC} RANGE		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Main block-erase time		2.4			1.9			1.3			1.1	14
Main block-byte program time		1.7			1.4			1.6			1.2	4.2
Main block-word program time		1.1			0.9			0.8			0.6	2.1
Parameter/boot-block erase time		0.84			0.8			0.44			0.34	7

NOTES: 8. Typical values shown are at T_A = 25°C and nominal conditions.
9. Excludes system-level overhead (all times in seconds)

electrical characteristics for TMS28F004ASy and TMS28F400ASy over recommended ranges of supply voltage and operating free-air temperature, using test conditions listed in Table 9 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	TTL	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -2.5$ mA		2.4		V
		CMOS	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -100$ µA		$V_{CC} - 0.4$		
V_{OL}	Low-level dc output voltage		$V_{CC} = V_{CC}$ MIN, $I_{OL} = 5.8$ mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 10)		$V_{CC} = V_{CC}$ MAX, $V_I = 0$ V to V_{CC} MAX, $\overline{RP} = V_{HH}$			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP} = V_{HH}$			500	µA
I_O	Output current (leakage)		$V_{CC} = V_{CC}$ MAX, $V_O = 0$ V to V_{CC} MAX			±10	µA
I_{PPS}	V_{PP} standby current (standby)		$V_{PP} \le V_{CC}$	3.3-V V_{CC} range		15	µA
				5-V V_{CC} range		10	
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V, $V_{PP} \le V_{CC}$	3.3-V V_{CC} range		5	µA
				5-V V_{CC} range		5	
I_{PP1}	V_{PP} supply current (active read)		$V_{PP} \ge V_{CC}$	3.3-V V_{CC} range		200	µA
				5-V V_{CC} range		200	
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		25	
				12-V V_{PP} range, 3.3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		25	
				12-V V_{PP} range, 3.3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP4}	V_{PP} supply current (block-erase (see Notes 11 and 12)		Block-erase in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		20	
				12-V V_{PP} range, 3.3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		15	

NOTES: 10. $DQ15/A_{-1}$ is tested for output leakage only.
11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004ASy and TMS28F400ASy over recommended ranges of supply voltage and operating free-air temperature, (as on the previous page) using test conditions listed in Table 9 (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{PP5}	V_{PP} supply current (erase-suspend) (see Notes 11 and 12)		Block-erase suspended	5-V V_{PP} range, 3.3-V V_{CC} range		200	μA
				5-V V_{PP} range, 5-V V_{CC} range		200	
				12-V V_{PP} range, 3.3-V V_{CC} range		200	
				12-V V_{PP} range, 5-V V_{CC} range		200	
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{CC} MAX, $\overline{E}$ = $\overline{RP}$ = V_{IH}	3.3-V V_{CC} range		1.5	mA
				5-V V_{CC} range		2	mA
		CMOS-input level	$\overline{E}$ = V_{CC} MAX, $\overline{E}$ = $\overline{RP}$ = V_{CC} ± 0.2 V	3.3-V V_{CC} range		110	μA
				5-V V_{CC} range		130	μA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP}$ = V_{SS} ± 0.2 V; V_{CC} = V_{CC} MAX	0°C to 70°C		8	μA
				– 40°C to 85°C		8	
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G}$ = V_{IH}	3.3-V V_{CC} range		30	mA
			$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G}$ = V_{IH}	5-V V_{CC} range		65	
		CMOS-input level	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G}$ = V_{CC}	3.3-V V_{CC} range		30	mA
			$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G}$ = V_{CC}	5-V V_{CC} range		60	
I_{CC2}	V_{CC} supply current (active byte write) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, Programming in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		50	
				12-V V_{PP} range, 3.3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, Programming in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		50	
				12-V V_{PP} range, 3.3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		45	

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004ASy and TMS28F400ASy over recommended ranges of supply voltage and operating free-air temperature, (as on the previous page) using test conditions listed in Table 9 (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC4}	V_{CC} supply current (block-erase) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, Block-erase in progress	5-V V_{PP} range, 3.3-V V_{CC} range		30	mA
			5-V V_{PP} range, 5-V V_{CC} range		35	
			12-V V_{PP} range, 3.3-V V_{CC} range		25	
			12-V V_{PP} range, 5-V V_{CC} range		30	
I_{CC5}	V_{CC} supply current (erase suspend) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, $\overline{E} = V_{IH}$, Block erase suspended	3.3-V V_{CC} range		8	mA
			5-V V_{CC} range		10	

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F004ASy and TMS28F400ASy over recommended ranges of supply voltage (commercial and extended temperature ranges)(see Notes 11, 12, and 13)

PARAMETER		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60		’28F004ASy70 ’28F400ASy70		’28F004ASy80 ’28F400ASy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (to V_{CC} at 3 V MIN or 3.6 V MAX) (see Note 14)	t_{PL5V} t_{PL3V}	0	0	0	0	0	0	ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}	110	60	130	70	150	80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}	800	450	800	450	800	450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2	2	2	2	2	2	µs
$t_{h(RP3)}$	Hold time, V_{CC} at 3 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2	2	2	2	2	2	µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

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switching characteristics for TMS28F004ASy and TMS28F400ASy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60				’28F004ASy70 ’28F400ASy70				’28F004ASy80 ’28F400ASy80				UNIT
			3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		110		60		130		70		150		80	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		110		60		130		70		150		80	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		65		35		80		40		90		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	110		60		130		70		150		80		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		55		25		70		30		80		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		45		25		55		30		60		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		800		450		800		450		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		45		25		55		30		60		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		110		60		130		70		150		80	ns

NOTE 15: A_{-1}–A17 for byte-wide

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timing requirements for TMS28F004ASy and TMS28F400ASy

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60		’28F004ASy70 ’28F400ASy70		’28F004ASy80 ’28F400ASy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	110	60	130	70	150	80	ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6	6	6	6	6	6	µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3	0.3	0.3	0.3	0.3	0.3	s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3	0.3	0.3	0.3	0.3	0.3	s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6	0.6	0.6	0.6	0.6	0.6	s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}	200	100	200	100	200	100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0	0	0	0	0	0	ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0	0	0	0	0	0	ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0	0	0	0	0	0	ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0	0	0	0	0	0	ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0	0	0	0	0	0	ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0	0	0	0	0	0	ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90	50	105	50	120	50	ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	90	50	105	50	120	50	ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90	50	105	50	120	50	ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0	0	0	0	0	0	ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004ASy and TMS28F400ASy (continued)

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60		’28F004ASy70 ’28F400ASy70		’28F004ASy80 ’28F400ASy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	200	100	200	100	200	100	ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	200	100	200	100	200	100	ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	90	50	105	50	120	50	ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20	10	25	20	30	30	ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	800	450	800	450	800	450	ns

timing requirements for TMS28F004ASy and TMS28F400ASy

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60		’28F004ASy70 ’28F400ASy70		’28F004ASy80 ’28F400ASy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	110	60	130	70	150	80	ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6	6	6	6	6	6	µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3	0.3	0.3	0.3	0.3	0.3	s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3	0.3	0.3	0.3	0.3	0.3	s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6	0.6	0.6	0.6	0.6	0.6	s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}	200	100	200	100	200	100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0	0	0	0	0	0	ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0	0	0	0	0	0	ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0	0	0	0	0	0	ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0	0	0	0	0	0	ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0	0	0	0	0	0	ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0	0	0	0	0	0	ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90	50	105	50	120	50	ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	90	50	105	50	120	50	ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90	50	105	50	120	50	ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0	0	0	0	0	0	ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004ASy and TMS28F400ASy (continued)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	’28F004ASy60 ’28F400ASy60				’28F004ASy70 ’28F400ASy70				’28F004ASy80 ’28F400ASy80				UNIT
			3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	200		100		200		100		200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	200		100		200		100		200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	90		50		105		50		120		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	20		10		25		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	800		450		800		450		800		450		ns

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TMS28F004AEy and TMS28F400AEy

The TMS28F004AEy and the TMS28F400AEy configurations offer the auto-select feature of the TMS28F400ASy with an extended V_{CC} from a low 2.7-V to 3.6-V range (3-V nominal). Memory reads can be performed using a V_{CC} = 3 V, allowing for more efficient power consumption than the 'ASy device.

recommended operating conditions for TMS28F004AEy and TMS28F400AEy

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	3-V V_{CC} range	2.7	3	3.6	V
			5-V V_{CC} range	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})	V_{PPL}	0		6.5	V
		During write/erase/erase suspend	5-V V_{PP} range	4.5	5	5.5	
			12-V V_{PP} range	11.4	12	12.6	
V_{IH}	High-level dc input voltage	3-V V_{CC} range	TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
		5-V V_{CC} range	TTL	2		V_{CC} + 0.3	
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage	3-V V_{CC} range	TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
		5-V V_{CC} range	TTL	– 0.3		0.8	
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase			0		1.5	V
T_A	Operating free-air temperature		L Suffix	0		70	°C
			E Suffix	– 40		85	

NOTE 7: Mimimum value at T_A = 25°C.

word/byte typical write and block-erase performance for TMS28F004AEy and TMS28F400AEy (see Notes 8 and 9)

PARAMETER	5-V V_{PP} RANGE						12-V V_{PP} RANGE					
	3-V V_{CC} RANGE			5-V V_{CC} RANGE			3-V V_{CC} RANGE			5-V V_{CC} RANGE		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Main block-erase time		2.4			1.9			1.3			1.1	14
Main block-byte program time		1.7			1.4			1.6			1.2	4.2
Main block-word program time		1.1			0.9			0.8			0.6	2.1
Parameter/boot-block erase time		0.84			0.8			0.44			0.34	7

NOTES: 8. Typical values shown are at T_A = 25°C and nominal conditions.
9. Excludes system-level overhead (all times in seconds)

electrical characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage and operating free-air temperature using test conditions listed in Table 9 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	TTL	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -2.5$ mA		2.4		V
		CMOS	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -100$ µA		$V_{CC} - 0.4$		
V_{OL}	Low-level dc output voltage		$V_{CC} = V_{CC}$ MIN, $I_{OL} = 5.8$ mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 10)		$V_{CC} = V_{CC}$ MAX, $V_I = 0$ V to V_{CC} MAX, $\overline{RP} = V_{HH}$			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP} = V_{HH}$			500	µA
I_O	Output current (leakage)		$V_{CC} = V_{CC}$ MAX, $V_O = 0$ V to V_{CC} MAX			±10	µA
I_{PPS}	V_{PP} standby current (standby)		$V_{PP} \le V_{CC}$	3-V V_{CC} range		15	µA
				5-V V_{CC} range		10	
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V, $V_{PP} \le V_{CC}$	3-V V_{CC} range		5	µA
				5-V V_{CC} range		5	
I_{PP1}	V_{PP} supply current (active read)		$V_{PP} \ge V_{CC}$	3-V V_{CC} range		200	µA
				5-V V_{CC} range		200	
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		25	
				12-V V_{PP} range, 3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		25	
				12-V V_{PP} range, 3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		20	

NOTES: 10. $DQ15/A_{-1}$ is tested for output leakage only.
11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{PP4}	V_{PP} supply current (block-erase) (see Notes 11 and 12)		Block-erase in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		20	
				12-V V_{PP} range, 3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		15	
I_{PP5}	V_{PP} supply current (erase-suspend) (see Notes 11 and 12)		Block-erase suspended	5-V V_{PP} range, 3-V V_{CC} range		200	µA
				5-V V_{PP} range, 5-V V_{CC} range		200	
				12-V V_{PP} range, 3-V V_{CC} range		200	µA
				12-V V_{PP} range, 5-V V_{CC} range		200	
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = V_{CC}$ MAX, $\overline{E} = \overline{RP} = V_{IH}$	3-V V_{CC} range		1.5	mA
				5-V V_{CC} range		2	
		CMOS-input level	$V_{CC} = V_{CC}$ MAX, $\overline{E} = \overline{RP} = \overline{WP} = V_{CC} \pm 0.2$ V	3-V V_{CC} range		110	µA
				5-V V_{CC} range		130	
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V; $V_{CC} = V_{CC}$ MAX	0°C to 70°C		8	µA
				– 40°C to 85°C		8	
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G} = V_{IH}$	3.3-V V_{CC} range		30	mA
			$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G} = V_{IH}$	5-V V_{CC} range		65	
		CMOS-input level	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G} = V_{CC}$	3.3-V V_{CC} range		30	mA
			$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G} = V_{CC}$	5-V V_{CC} range		60	
I_{CC2}	V_{CC} supply current (active byte-write) (see Notes 11 and 12)		$V_{CC} = V_{CC}$ MAX, Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		50	
				12-V V_{PP} range, 3-V V_{CC} range		25	
				12-V V_{PP} range, 5-V V_{CC} range		45	

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
			5-V V_{PP} range, 3-V V_{CC} range		50	
			12-V V_{PP} range, 3-V V_{CC} range		25	
			12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC4}	V_{CC} supply current (block-erase) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, Block-erase in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
			5-V V_{PP} range, 5-V V_{CC} range		35	
			12-V V_{PP} range, 3-V V_{CC} range		25	
			12-V V_{PP} range, 5-V V_{CC} range		30	
I_{CC5}	V_{CC} supply current (erase-suspend) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, $\overline{E} = V_{IH}$, Block-erase suspended	3-V V_{CC} range			mA
			3.3-V V_{CC} range		8	
			5-V V_{CC} range		10	

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 11, 12, and 13)

PARAMETER		ALT. SYMBOL	'28F004AEy60 '28F400AEy60				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (to V_{CC} at 2.7 V MIN or 3.6 V MAX) (see Note 14)	t_{PL5V} t_{PL3V}	0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		110		60	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		800		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		µs
$t_{h(RP3)}$	Hold time, V_{CC} at 2.7 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2		2		µs

PARAMETER		ALT. SYMBOL	'28F004AEy70 '28F400AEy70				'28F004AEy80 '28F400AEy80				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (to V_{CC} at 2.7 V MIN or 3.6 V MAX) (see Note 14)	t_{PL5V} t_{PL3V}	0		0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		150		70		150		80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		800		450		800		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		2		µs
$t_{h(RP3)}$	Hold time, V_{CC} at 2.7 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2		2		2		2		µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F004AEy60 '28F400AEy60				'28F004AEy70 '28F400AEy70				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		110		60		130		70	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		110		60		130		70	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		65		35		80		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	110		60		130		70		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		55		25		70		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		45		25		55		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		800		450		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		45		25		55		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		110		60		130		70	ns

NOTE 15: A_{-1}–A17 for byte-wide

switching characteristics for TMS28F004AEy and TMS28F400AEy over recommended ranges of supply voltage (commercial and extended temperature ranges) (continued)

PARAMETER		ALT. SYMBOL	'28F004AEy80 '28F400AEy80				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		150		80	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		150		80	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		90		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	150		80		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		80		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		60		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		60		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		150		80	ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AEy and TMS28F400AEy

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F004AEy60 '28F400AEy60				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	110		60		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	90		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	200		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	200		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	90		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20		10		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	800		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AEy and TMS28F400AEy (continued)

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F004AEy70 '28F400AEy70				'28F004AEy80 '28F400AEy80				UNIT
			3.0-V V_{CC} RANGE		5-V V_{CC} RANGE		3.0-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	130		70		150		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	105		50		120		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	105		50		120		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	105		50		120		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	200		100		200		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	200		100		200		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	105		50		120		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WLWL}	25		20		30		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	800		450		800		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AEy and TMS28F400AEy

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F004AEy60 '28F400AEy60				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	110		60		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	90		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	90		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	20		10		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	800		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AEy and TMS28F400AEy (continued)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F004AEy70 '28F400AEy70				'28F004AEy80 '28F400AEy80				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	130		70		150		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	105		50		120		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	105		50		120		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	105		50		120		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	200		100		200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	200		100		200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	105		50		120		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	25		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	800		450		800		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

TMS28F004AMy and TMS28F400AMy

The TMS28F004AMy and the TMS28F400AMy configurations offer a 3-V or 5-V memory read with a 12-V program and erase. This configuration is intended for low 3.3-V reads and the fast programming offered with the 12-V V_{PP} = 12 V and 5-V V_{CC}. This configuration is offered in two different temperature ranges: 0°C to 70°C and – 40°C to 85°C.

recommended operating conditions for TMS28F004AMy and TMS28F400AMy

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	3.3-V V_{CC} range	3	3.3	3.6	V
			5-V V_{CC} range	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})	V_{PPL}	0		6.5	V
		During write/erase/erase suspend	12-V V_{PP} range	11.4	12	12.6	
V_{IH}	High-level dc input voltage	3.3 V V_{CC} range	TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
		5 V V_{CC} range	TTL	2		V_{CC} + 0.3	
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage	3.3 V V_{CC} range	TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
		5 V V_{CC} range	TTL	– 0.3		0.8	
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase			0		1.5	V
T_A	Operating free-air temperature		L Suffix	0		70	°C
			E Suffix	– 40		85	

NOTE 7: Mimimum value at T_A = 25°C.

word/byte typical write and block-erase performance for TMS28F004AMy and TMS28F400AMy (see Notes 8 and 9)

PARAMETER	12-V V_{PP} RANGE					
	3.3-V V_{CC} RANGE			5-V V_{CC} RANGE		
	MIN	TYP	MAX	MIN	TYP	MAX
Main block-erase time		1.3			1.1	14
Main block-byte program time		1.6			1.2	4.2
Main block-word program time		0.8			0.6	2.1
Parameter/boot-block erase time		0.44			0.34	7

NOTES: 8. Typical values shown are at T_A = 25°C and nominal conditions.
9. Excludes system-level overhead (all times in seconds)

electrical characteristics for TMS28F004AMy and TMS28F400AMy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	TTL	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -2.5$ mA		2.4		V
		CMOS	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -100$ µA		$V_{CC} - 0.4$		
V_{OL}	Low-level dc output voltage		$V_{CC} = V_{CC}$ MIN, $I_{OL} = 5.8$ mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 10)		$V_{CC} = V_{CC}$ MAX, $V_I = 0$ V to V_{CC}MAX, $\overline{RP} = V_{HH}$			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP} = V_{HH}$			500	µA
I_O	Output current (leakage)		$V_{CC} = V_{CC}$MAX, $V_O = 0$ V to V_{CC}MAX			±10	µA
I_{PPS}	V_{PP} standby current (standby)		$V_{PP} \le V_{CC}$	3.3-V V_{CC} range		15	µA
				5-V V_{CC} range		10	
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V, $V_{PP} \le V_{CC}$	3.3-V V_{CC} range		5	µA
				5-V V_{CC} range		5	
I_{PP1}	V_{PP} supply current (active read)		$V_{PP} \ge V_{CC}$	3.3-V V_{CC} range		200	µA
				5-V V_{CC} range		200	
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 11 and 12)		Programming in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 11 and 12)		Programming in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP4}	V_{PP} supply current (block-erase) (see Notes 11 and 12)		Block-erase in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		15	
I_{PP5}	V_{PP} supply current (erase-suspend) (see Notes 11 and 12)		Block-erase suspended	12-V V_{PP} range, 3.3-V V_{CC} range		200	µA
				12-V V_{PP} range, 5-V V_{CC} range		200	
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$\overline{E} = \overline{RP} = V_{CC}$ MAX, $\overline{E} = \overline{RP} = V_{IH}$	3.3-V V_{CC} range		1.5	mA
				5-V V_{CC} range		2	mA
		CMOS-input level	$\overline{E} = \overline{RP} = V_{CC}$ MAX, $\overline{E} = \overline{RP} = V_{CC} \pm 0.2$ V	3.3-V V_{CC} range		110	µA
				5-V V_{CC} range		130	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V; $V_{CC} = V_{CC}$ MAX	0°C to 70°C		8	µA
				– 40°C to 85°C		8	

NOTES: 10. $DQ15/A_{-1}$ is tested for output leakage only.
11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004AMy and TMS28F400AMy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G} = V_{IH}$	3.3-V V_{CC} range		30	mA
			$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G} = V_{IH}$	5-V V_{CC} range		65	
		CMOS-input level	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 5 MHz, $\overline{G} = V_{CC}$	3.3-V V_{CC} range		30	mA
			$\overline{E} = V_{IL}$, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G} = V_{CC}$	5-V V_{CC} range		60	
I_{CC2}	V_{CC} supply current (active byte-write) (see Notes 11 and 12)		$V_{CC} = V_{CC}$ MAX, Programming in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 11 and 12)		$V_{CC} = V_{CC}$ MAX, Programming in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC4}	V_{CC} supply current (block-erase) (see Notes 11 and 12)		$V_{CC} = V_{CC}$ MAX, Block-erase in progress	12-V V_{PP} range, 3.3-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		30	
I_{CC5}	V_{CC} supply current (erase-suspend) (see Notes 11 and 12)		$V_{CC} = V_{CC}$ MAX, $\overline{E} = V_{IH}$, Block-erase suspended	3.3-V V_{CC} range		8	mA
				5-V V_{CC} range		10	

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F004AMy and TMS28F400AMy over recommended ranges of supply voltage (commercial and extended temperature ranges)(see Notes 11, 12, and 13)

PARAMETER		ALT. SYMBOL	’28F004AMy60 ’28F400AMy60		’28F004AMy70 ’28F400AMy70		’28F004AMy80 ’28F400AMy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (to V_{CC} at 3 V MIN or 3.6 V MAX) (see Note 14)	t_{PL5V} t_{PL3V}	0	0	0	0	0	0	ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}	110	60	130	70	150	80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}	800	450	800	450	800	450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2	2	2	2	2	2	µs
$t_{h(RP3)}$	Hold time, V_{CC} at 3 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2	2	2	2	2	2	µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13 $\overline{E}$ and $\overline{G}$ are switched low after power up.
14 The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F004AMy and TMS28F400AMy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	’28F004AMy60 ’28F400AMy60				’28F004AMy70 ’28F400AMy70				28F004AMy80 ’28F400AMy80				UNIT
			3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		110		60		130		70		150		80	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		110		60		130		70		150		80	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		65		35		80		40		90		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	110		60		130		70		150		80		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		55		25		70		30		80		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		45		25		55		30		60		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		800		450		800		450		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		45		25		55		30		60		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		110		60		130		70		150		80	ns

NOTE 15: A_{-1}–A17 for byte-wide

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timing requirements for TMS28F004AMy and TMS28F400AMy

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F004AMy60 '28F400AMy60				'28F004AMy70 '28F400AMy70				28F004AMy80 '28F400AMy80				UNIT
			3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	110		60		130		70		150		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	90		50		105		50		120		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90		50		105		50		120		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		0		0		0		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AMy and TMS28F400AMy (continued)

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	’28F004AMy60 ’28F400AMy60		’28F004AMy70 ’28F400AMy70		28F004AMy80 ’28F400AMy80		UNIT
			3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	3.3-V V_{CC} RANGE	5-V V_{CC} RANGE	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	200	100	200	100	200	100	ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	200	100	200	100	200	100	ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	90	50	105	50	120	50	ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20	10	25	20	30	30	ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	800	450	800	450	800	450	ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AMy and TMS28F400AMy

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	’28F004AMy60 ’28F400AMy60				’28F004AMy70 ’28F400AMy70				28F004AMy80 ’28F400AMy80				UNIT
			3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	110		60		130		70		150		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	90		50		105		50		120		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90		50		105		50		120		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	200		100		200		100		200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	200		100		200		100		200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	90		50		105		50		120		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	20		10		25		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	800		450		800		450		800		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

TMS28F004AFy and TMS28F400AFy

The TMS28F004AFy and the TMS28F400AFy configurations offer a 5-V memory read with a 5-V or 12-V program and erase. This configuration is intended for systems using a single 5-V power supply and it is offered in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

recommended operating conditions for TMS28F004AFy and TMS28F400AFy

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	5-V V_{CC} range	4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})	V_{PPL}	0		6.5	V
		During write/erase/erase suspend	5-V V_{PP} range	4.5	5	5.5	
			12-V V_{PP} range	11.4	12	12.6	
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.3	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage		TTL	– 0.3		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase			0		1.5	V
T_A	Operating free-air temperature		L Suffix	0		70	°C
			E Suffix	– 40		85	
			Q Suffix	– 40		125	°C

NOTE 7: Mimimum value at T_A = 25°C.

word/byte typical write and block-erase performance for TMS28F004AFy and TMS28F400AFy (see Notes 8 and 9)

PARAMETER	5-V V_{PP} AND 5-V V_{CC} RANGES			12-V V_{PP} AND 5-V V_{CC} RANGES		
	MIN	TYP	MAX	MIN	TYP	MAX
Main block erase time		1.9			1.1	14
Main block byte-program time		1.4			1.2	4.2
Main block word-program time		0.9			0.6	2.1
Parameter/boot-block erase time		0.8			0.34	7

NOTES: 8. Typical values shown are at T_A = 25°C and nominal conditions.
9. Excludes system-level overhead (all times in seconds)

electrical characteristics for TMS28F004AFy and TMS28F400AFy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	TTL	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -2.5$ mA		2.4		V
		CMOS	$V_{CC} = V_{CC}$ MIN, $I_{OH} = -100$ µA		$V_{CC} - 0.4$		
V_{OL}	Low-level dc output voltage		$V_{CC} = V_{CC}$ MIN, $I_{OL} = 5.8$ mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 10)		$V_{CC} = V_{CC}$ MAX, $V_I = 0$ V to V_{CC} MAX, $\overline{RP} = V_{HH}$			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP} = V_{HH}$			500	µA
I_O	Output current (leakage)		$V_{CC} = V_{CC}$ MAX, $V_O = 0$ V to V_{CC} MAX			±10	µA
I_{PPS}	V_{PP} standby current (standby)		$V_{PP} \le V_{CC}$	5-V V_{CC} range		10	µA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V, $V_{PP} \le V_{CC}$	5-V V_{CC} range		5	µA
I_{PP1}	V_{PP} supply current (active read)		$V_{PP} \ge V_{CC}$	5-V V_{CC} range		200	µA
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 5-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 11 and 12)		Programming in progress	5-V V_{PP} range, 5-V V_{CC} range		25	mA
				12-V V_{PP} range, 5-V V_{CC} range		20	
I_{PP4}	V_{PP} supply current (block-erase) (see Notes 11 and 12)		Block-erase in progress	5-V V_{PP} range, 5-V V_{CC} range		20	mA
				12-V V_{PP} range, 5-V V_{CC} range		15	
I_{PP5}	V_{PP} supply current (erase-suspend) (see Notes 11 and 12)		Block-erase suspended	5-V V_{PP} range, 5-V V_{CC} range		200	µA
				12-V V_{PP} range, 5-V V_{CC} range		200	
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = V_{CC}$ MAX, $E = \overline{RP} = V_{IH}$	5-V V_{CC} range		2	mA
		CMOS-input level		5-V V_{CC} range		130	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V	0°C to 70°C		8	µA
				– 40°C to 85°C		8	
				– 40°C to 125°C		40	
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{E} = V_{IL}$, $I_{OUT} = 0$ mA, f = 10 MHz, $\overline{G} = V_{IH}$	5-V V_{CC} range		65	mA
		CMOS-input level	$\overline{E} = V_{SS}$, $I_{OUT} = 0$ mA, f = 10 MHz, $\overline{G} = V_{CC}$	5-V V_{CC} range		60	mA

NOTES: 10. $DQ15/A_{-1}$ is tested for output leakage only.
11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F004AFy and TMS28F400AFy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC2}	V_{CC} supply current (active byte-write) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, Programming in progress	5-V V_{PP} range, 5-V V_{CC} range		50	mA
			12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, Programming in progress	5-V V_{PP} range, 5-V V_{CC} range		50	mA
			12-V V_{PP} range, 5-V V_{CC} range		45	
I_{CC4}	V_{CC} supply current (block-erase) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX V_{PP} = 12 V or 5 V Block-erase in progress	5–V V_{PP} range, 5-V V_{CC} range		35	mA
			12-V V_{PP} range, 5-V V_{CC} range		30	
I_{CC5}	V_{CC} supply current (erase-suspend) (see Notes 11 and 12)	$V_{CC} = V_{CC}$ MAX, $\overline{E} = V_{IH}$, Block-erase suspended	5-V V_{CC} range		10	mA

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F004AFy and TMS28F400AFy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 11, 12, and 13)

PARAMETER		ALT. SYMBOL	'28F004AFy60 '28F400AFy60		'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (see Note 14)	t_{PL5V} t_{PL3V}	0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		60		70		80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		450		450		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

power-up and reset switching characteristics for TMS28F400AFy over recommended ranges of supply voltage (automotive temperature range) (see Notes 11, 12, 13)

PARAMETER		ALT. SYMBOL	'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		'28F004AFy90 '28F400AFy90		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (see Note 14)	t_{PL5V} t_{PL3V}	0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		70		80		90	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		450		450		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F004AFy and TMS28F400AFy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F004AFy60 '28F400AFy60		'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		60		70		80	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		60		70		80	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		35		40		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	60		70		80		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		25		30		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		25		30		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		450		450		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		25		30		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		60		70		80	ns

NOTE 15: A_{-1}–A17 for byte-wide

switching characteristics for TMS28F400AFy over recommended ranges of supply voltage (automotive temperature range)

read operations

PARAMETER		ALT. SYMBOL	'28F400AFy-70 '28F400AFy-70 5-V V_{CC} RANGE		'28F400AFy-80 '28F400AFy-80 5-V V_{CC} RANGE		'28F004AFy-90 '28F400AFy-90 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		70		80		90	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		70		80		90	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		35		40		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	70		80		90		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		25		30		35	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		25		30		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		300		300		300	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		30		30		35	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		70		80		90	ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AFy (commercial and extended temperature ranges)

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	’28F004AFy60 ’28F400AFy60		’28F004AFy70 ’28F400AFy70		’28F004AFy80 ’28F400AFy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	60		70		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	50		50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	10		20		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	450		450		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AFy (automotive temperature range)

write/erase operations — $\overline{W}$-controlled writes (continued)

		ALT. SYMBOL	'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		'28F004AFy90 '28F400AFy90		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	70		80		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		7		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.4		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.4		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.4		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ switching high	t_{PHHWH}	100		100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ switching high	t_{VPWH}	100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	60		60		60		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20		30		40		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	220		220		220		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AFy (commercial and extended temperature ranges)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F004AFy60 '28F400AFy60		'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	60		70		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	50		50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	10		20		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	450		450		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AFy (automotive temperature range)

write/erase operations — $\overline{E}$-controlled writes (continued)

		ALT. SYMBOL	'28F004AFy70 '28F400AFy70		'28F004AFy80 '28F400AFy80		'28F004AFy90 '28F400AFy90		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	70		80		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		7		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.4		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.4		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ valid	t_{DVEH}	50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		50		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		50		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	60		60		60		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	20		30		40		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	300		300		300		ns

NOTE 15: A_{-1}–A17 for byte-wide

TMS28F004AZy and TMS28F400AZy

The TMS28F004AZy and the TMS28F400AZy configurations offer a 5-V memory read with a 12-V program and a 12-V erase for fast programming and erasing times. This configuration is offered in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

recommended operating conditions for TMS28F004AZy and TMS28F400AZy

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	5-V V_{CC} range	4.5	5	5.5	V
V_{PP}	Supply voltage	During read only	V_{PPL}	0		6.5	V
		During write/erase/erase suspend	12-V V_{PP} range	11.4	12	12.6	
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.3	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage		TTL	– 0.3		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase			0		1.5	V
T_A	Operating free-air temperature		L Suffix	0		70	°C
			E Suffix	– 40		85	
			Q Suffix	– 40		125	°C

NOTE 7: Mimimum value at T_A = 25°C.

word/byte typical write and block-erase performance for TMS28F400AZy and TMS28F400AZy (see Notes 8 and 9)

PARAMETER	12-V V_{PP} AND 5-V V_{CC} RANGES		
	MIN	TYP	MAX
Main block-erase time		1.1	14
Main block-byte program time		1.2	4.2
Main block-word program time		0.6	2.1
Parameter/boot-block erase time		0.34	7

NOTES: 8. Typical values shown are at T_A = 25°C and nominal conditions.
9. Excludes system-level overhead (all times in seconds)

electrical characteristics for TMS28F004AZy and TMS28F400AZy over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 9 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	TTL	V_{CC} = V_{CC} MIN, I_{OH} = – 2.5 mA		2.4		V
		CMOS	V_{CC} = V_{CC} MIN, I_{OH} = – 100 µA		V_{CC} – 0.4		
V_{OL}	Low-level dc output voltage		V_{CC} = V_{CC} MIN, I_{OL} = 5.8 mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 10)		V_{CC} = V_{CC} MAX, V_I = 0 V to V_{CC}MAX, $\overline{RP}$ = V_{HH}			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP}$ = V_{HH}			500	µA
I_O	Output current (leakage)		V_{CC} = V_{CC} MAX, V_O = 0 V to V_{CC}MAX			±10	µA
I_{PPS}	V_{PP} standby current (standby)		V_{PP} ≤ V_{CC}	5-V V_{CC} range		10	µA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP}$ = V_{SS} ± 0.2 V, V_{PP} ≤ V_{CC}	5-V V_{CC} range		5	µA
I_{PP1}	V_{PP} supply current (active read)		V_{PP} ≥ V_{CC}	5-V V_{CC} range		200	µA
I_{PP2}	V_{PP} supply current (active byte write) (see Notes 11 and 12)		Programming in progress	12-V V_{PP} range, 5-V V_{CC} range		20	mA
I_{PP3}	V_{PP} supply current (active word write) (see Notes 11 and 12)		Programming in progress	12-V V_{PP} range, 5-V V_{CC} range		20	mA
I_{PP4}	V_{PP} supply current (block erase) (see Notes 11 and 12)		Block erase in progress	12-V V_{PP} range, 5-V V_{CC} range		15	mA
I_{PP5}	V_{PP} supply current (erase suspend) (see Notes 11 and 12)		Block erase suspended	12-V V_{PP} range, 5-V V_{CC} range		200	µA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = V_{CC} MAX, $\overline{E}$ = $\overline{RP}$ = V_{IH}	5-V V_{CC} range		2	mA
		CMOS-input level				130	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP}$ = V_{SS} ± 0.2 V	0°C to 70°C		8	µA
				– 40°C to 85°C		8	
				– 40°C to 125°C		40	
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G}$ = V_{IH}	5-V V_{CC} range		65	mA
		CMOS-input level	$\overline{E}$ = V_{SS}, I_{OUT} = 0 mA, f = 10 MHz, $\overline{G}$ = V_{CC}	5-V V_{CC} range		60	mA
I_{CC2}	V_{CC} supply current (active byte write) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, Programming in progress	12-V V_{PP} range, 5-V V_{CC} range		50	mA
I_{CC3}	V_{CC} supply current (active word write) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, Programming in progress	12-V V_{PP} range, 5-V V_{CC} range		45	mA
I_{CC4}	V_{CC} supply current (block erase) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, Block erase in progress	12-V V_{PP} range, 5-V V_{CC} range		45	mA
I_{CC5}	V_{CC} supply current (erase suspend) (see Notes 11 and 12)		V_{CC} = V_{CC} MAX, $\overline{E}$ = V_{IH}, Block erase suspended	5-V V_{CC} range		10	mA

NOTES: 10. DQ15/A_{-1} is tested for output leakage only.
11. Not 100% tested; characterization data available
12. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F004AZy and TMS28F400AZy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 11, 12, and 13)

PARAMETER		ALT. SYMBOL	'28F004AZy60 '28F400AZy60		'28F004AZy70 '28F400AZy70		'28F004AZy80 '28F400AZy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (see Note 14)	t_{PL5V} t_{PL3V}	0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		60		70		80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		450		450		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

power-up and reset switching characteristics for TMS28F400AZy over recommended ranges of supply voltage (automotive temperature range)

PARAMETER		ALT. SYMBOL	'28F004AZy70 '28F400AZy70		'28F004AZy80 '28F400AZy80		'28F004AZy90 '28F400AZy90		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN (see Note 14)	t_{PL5V} t_{PL3V}	0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		70		80		90	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		450		450		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		µs

NOTES: 11. Characterization data available
12. All ac current values are RMS unless otherwise noted.
13. $\overline{E}$ and $\overline{G}$ are switched low after power up.
14. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F004AZy and TMS28F400AZy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F004AZy60 '28F400AZy60 5-V V_{CC} RANGE		'28F004AZy70 '28F400AZy70 5-V V_{CC} RANGE		'28F004AZy80 '28F400AZy80 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		60		70		80	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		60		70		80	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		35		40		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	60		70		80		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		25		30		30	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		25		30		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		450		450		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		25		30		30	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		60		70		80	ns

NOTE 15: A_{-1}–A17 for byte-wide

switching characteristics for TMS28F400AZy over recommended ranges of supply voltage (automotive temperature range)

read operations

PARAMETER		ALT. SYMBOL	'28F004AZy70 '28F400AZy70 5-V V_{CC} RANGE		'28F004AZy80 '28F400AZy80 5-V V_{CC} RANGE		'28F004AZy90 '28F400AZy90 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17 (see Note 15)	t_{AVQV}		70		80		90	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		70		80		90	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		35		40		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	70		80		90		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		25		30		35	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		25		30		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 15)	t_{AXQX}	0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5	ns

NOTE 15: A_{-1}–A17 for byte-wide

switching characteristics for TMS28F400AZy over recommended ranges of supply voltage (automotive temperature range) (continued)

read operations

PARAMETER		ALT. SYMBOL	'28F004AZy70 '28F400AZy70 5-V V_{CC} RANGE		'28F004AZy80 '28F400AZy80 5-V V_{CC} RANGE		'28F004AZy90 '28F400AZy90 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		300		300		300	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQZ}		30		30		35	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		70		80		90	ns

timing requirements for TMS28F004AZy and TMS28F400AZy (commercial and extended temperature ranges)

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F004AZy60 '28F400AZy60 5-V V_{CC} RANGE		'28F004AZy70 '28F400AZy70 5-V V_{CC} RANGE		'28F004AZy80 '28F400AZy80 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	60		70		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	50		50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	10		20		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	450		450		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AZy (automotive temperature range)

write/erase operations — $\overline{W}$-controlled writes (continued)

		ALT. SYMBOL	’28F004AZy60 ’28F400AZy60		’28F004AZy70 ’28F400AZy70		’28F004AZy80 ’28F400AZy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	70		80		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		7		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		.4		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		.4		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{WHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVWH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	60		60		60		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20		30		40		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	220		220		220		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F004AZy and TMS28F400AZy (commercial and extended temperature ranges)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	’28F004AZy60 ’28F400AZy60		’28F004AZy70 ’28F400AZy70		’28F004AZy80 ’28F400AZy80		UNIT
			5-V V_{CC} RANGE		5-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	60		70		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	50		50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	10		20		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	450		450		450		ns

NOTE 15: A_{-1}–A17 for byte-wide

timing requirements for TMS28F400AZy (automotive temperature range)

write/erase operations — $\overline{E}$-controlled writes (continued)

		ALT. SYMBOL	'28F004AZy70 '28F400AZy70 5-V V_{CC} RANGE		'28F004AZy80 '28F400AZy80 5-V V_{CC} RANGE		'28F004AZy90 '28F400AZy90 5-V V_{CC} RANGE		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	70		80		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		7		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.4		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.4		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17 (see Note 15)	t_{EHAX}	0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 15)	t_{AVEH}	50		50		50		ns
$t_{su(D)}$	Setup time, DQ valid	t_{DVEH}	50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before write operation	t_{WLEL}	0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low	t_{ELEH}	60		60		60		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high	t_{EHEL}	20		30		40		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	300		300		300		ns

NOTE 15: A_{-1}–A17 for byte-wide

PARAMETER MEASUREMENT INFORMATION

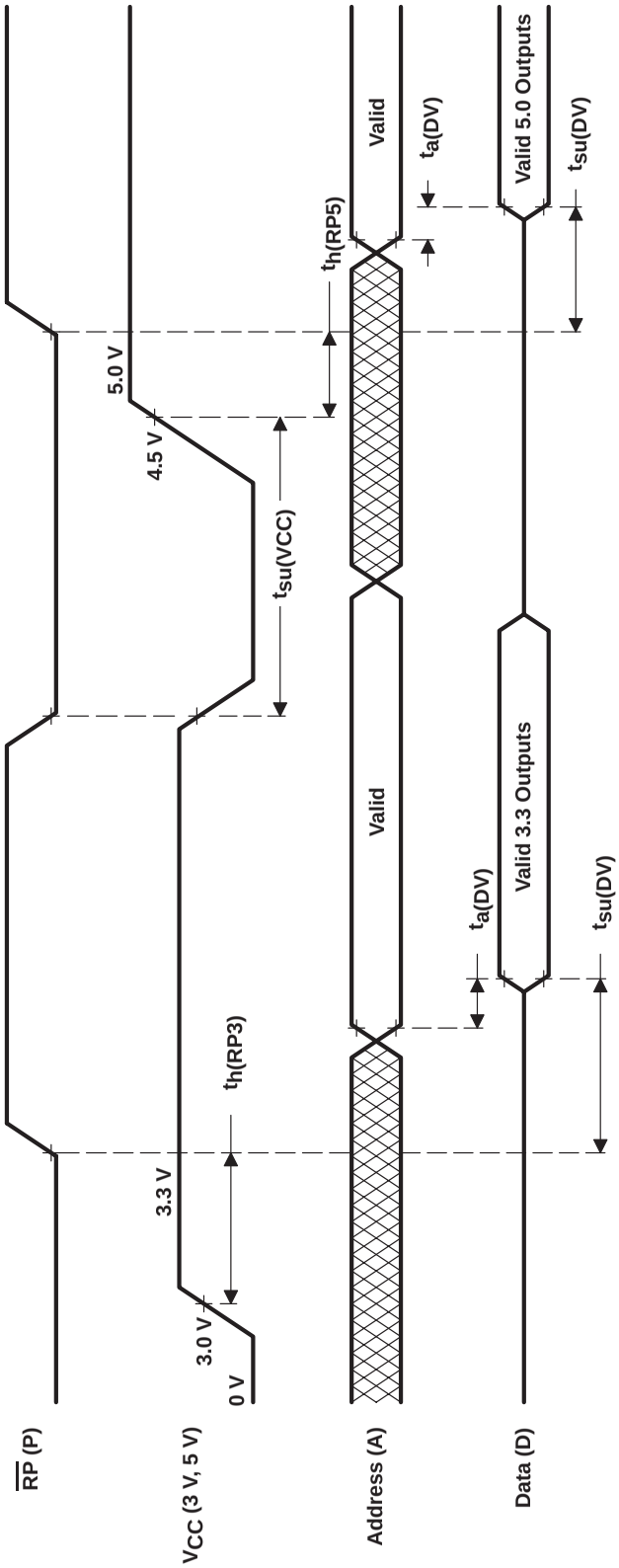


Figure 10. Power-Up Timing and Reset Switching

PARAMETER MEASUREMENT INFORMATION

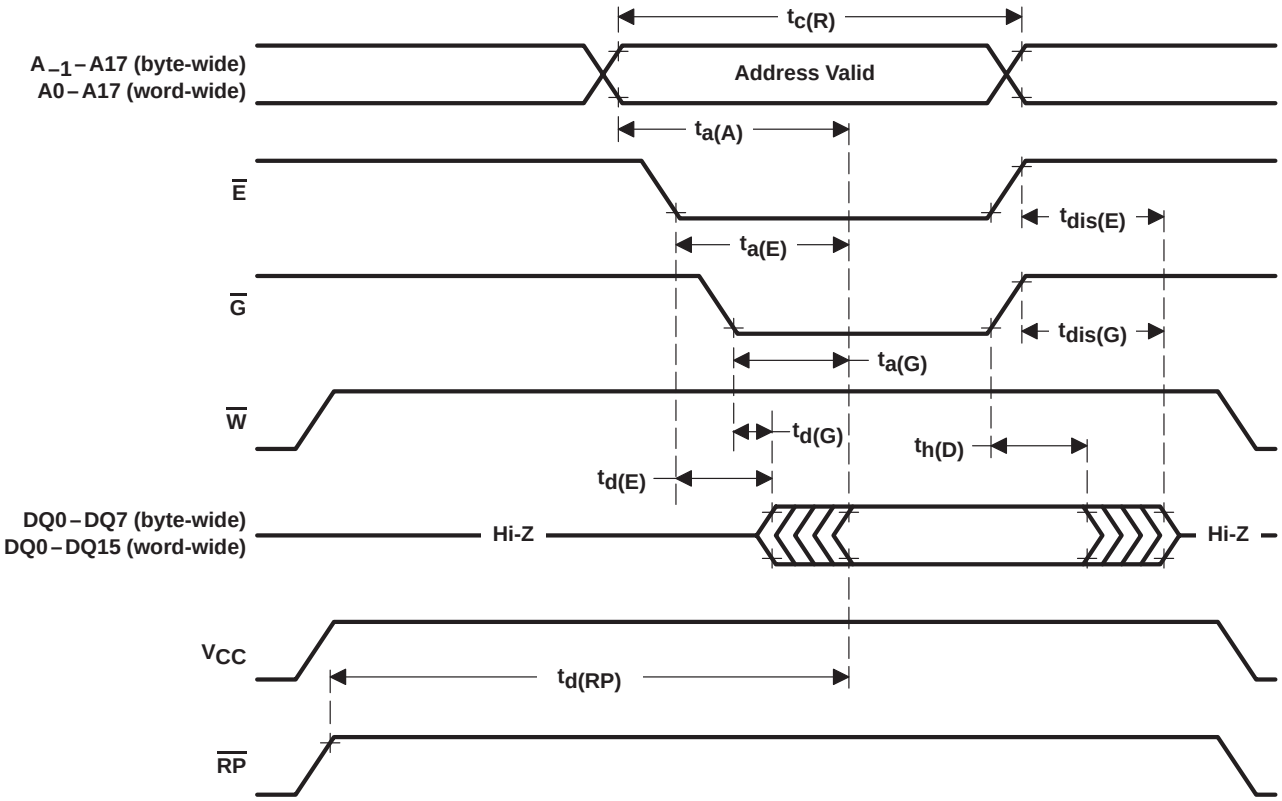


Figure 11. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

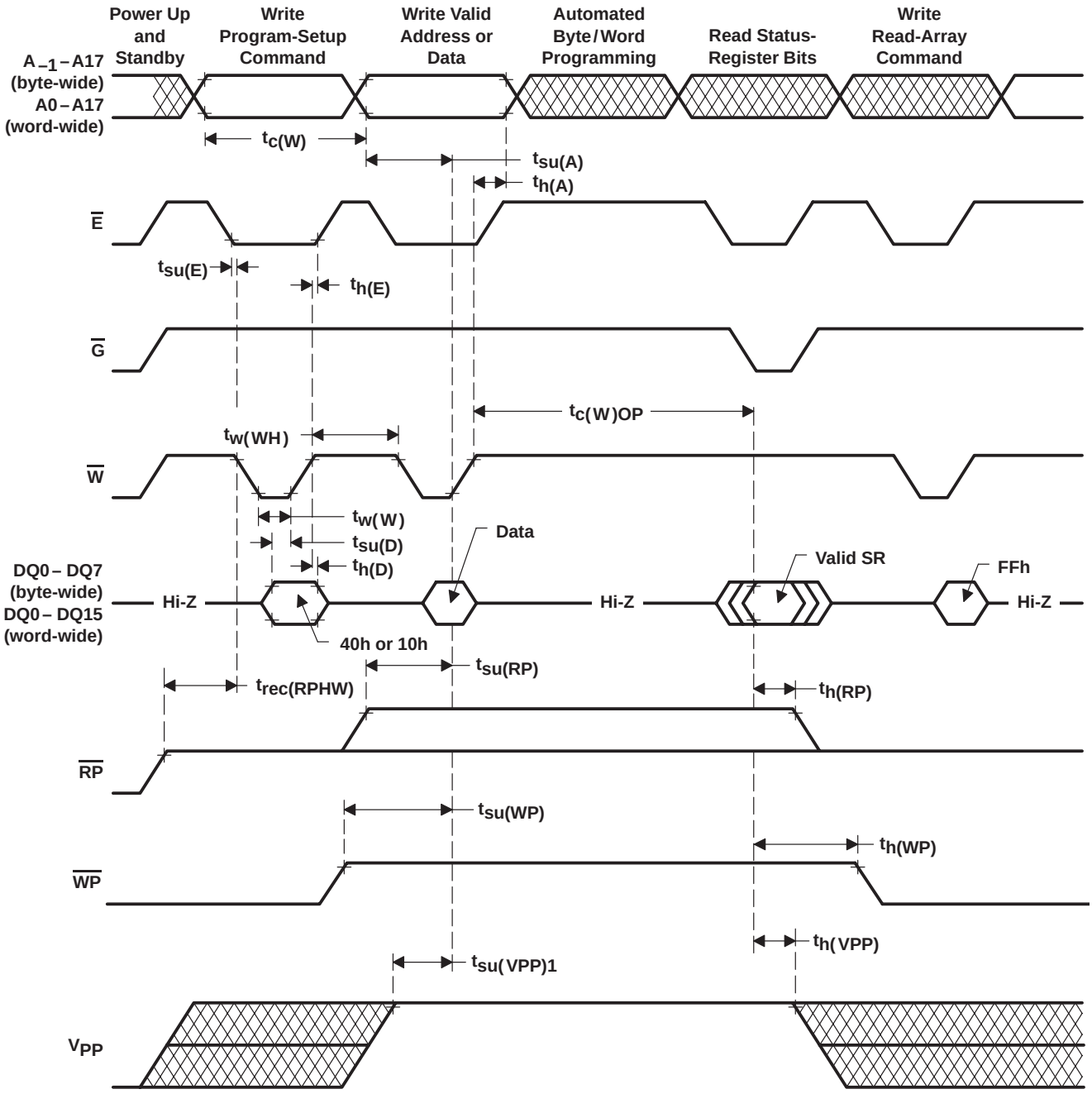


Figure 12. Write-Cycle Timing ($\overline{W}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

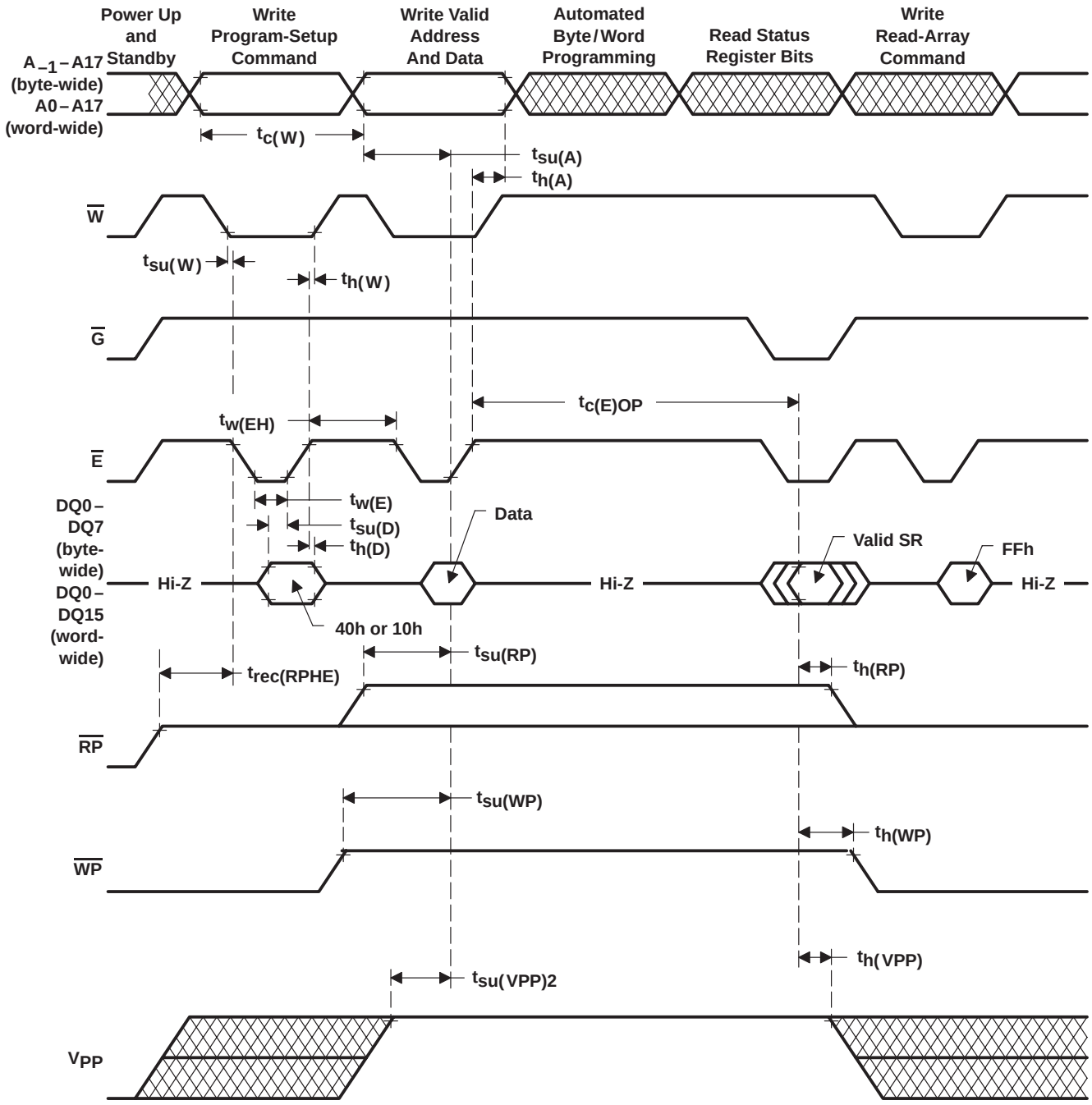


Figure 13. Write-Cycle Timing ($\overline{E}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

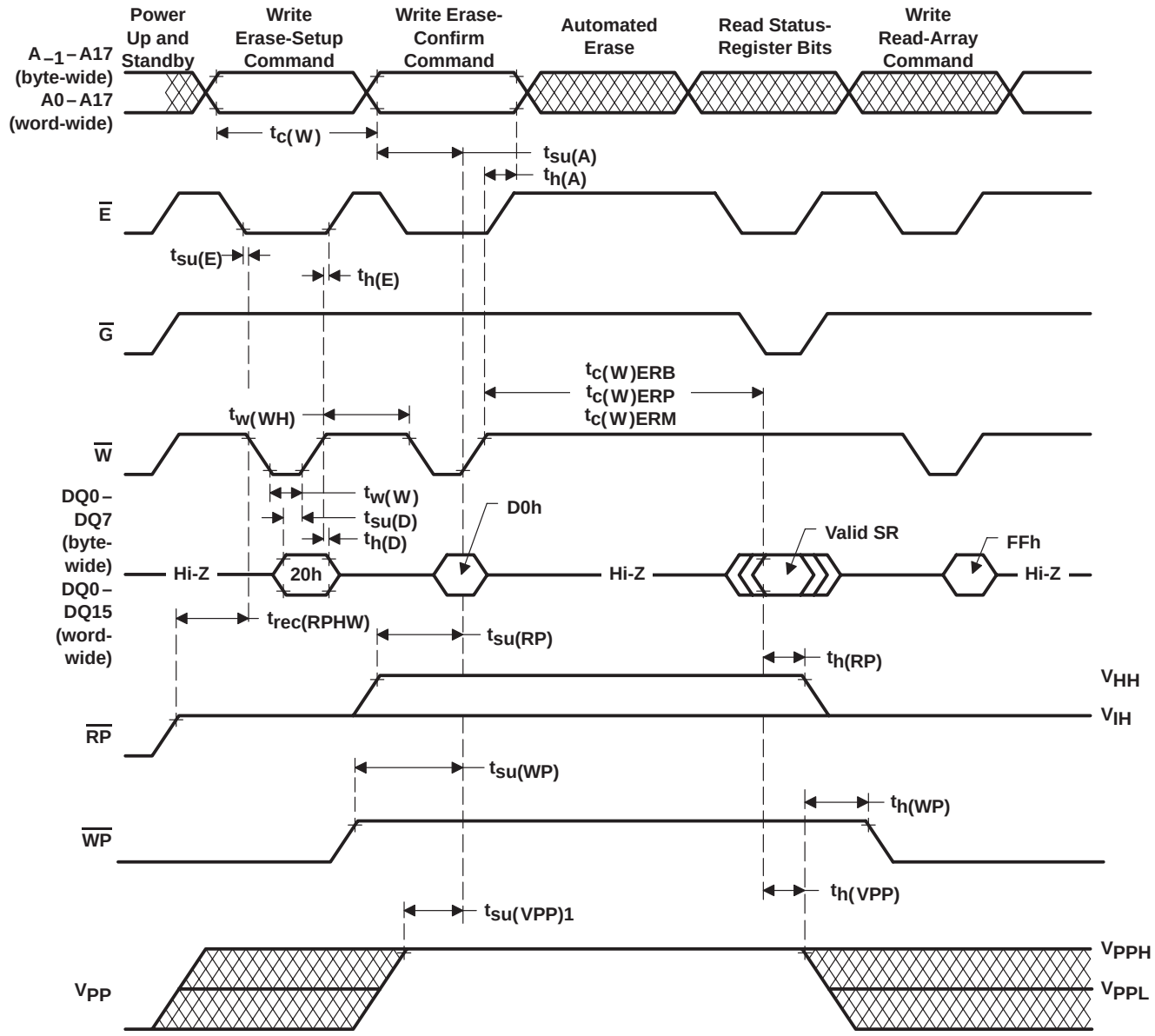


Figure 14. Erase Cycle Timing ($\overline{W}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

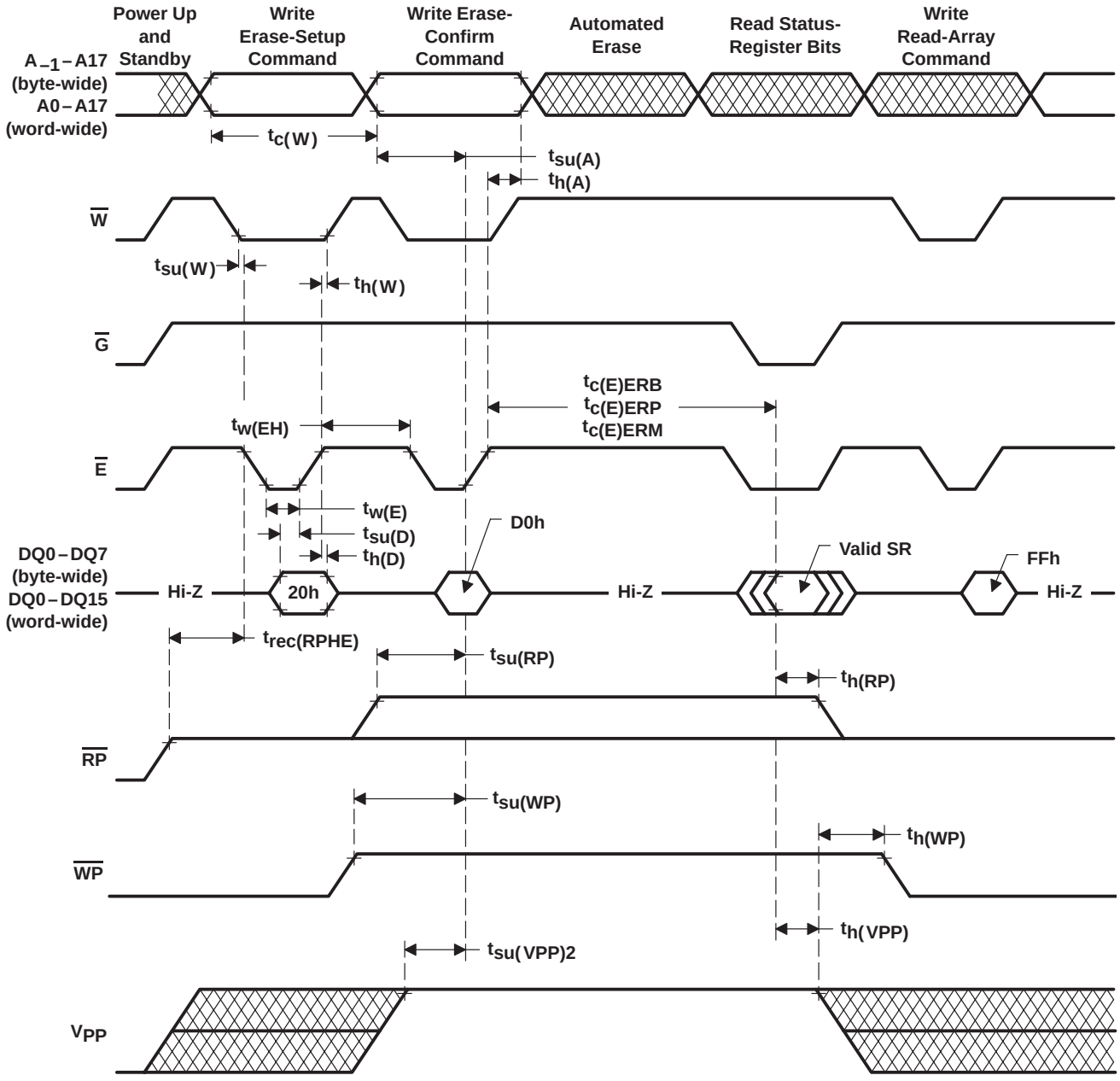


Figure 15. Erase-Cycle Timing ($\overline{E}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

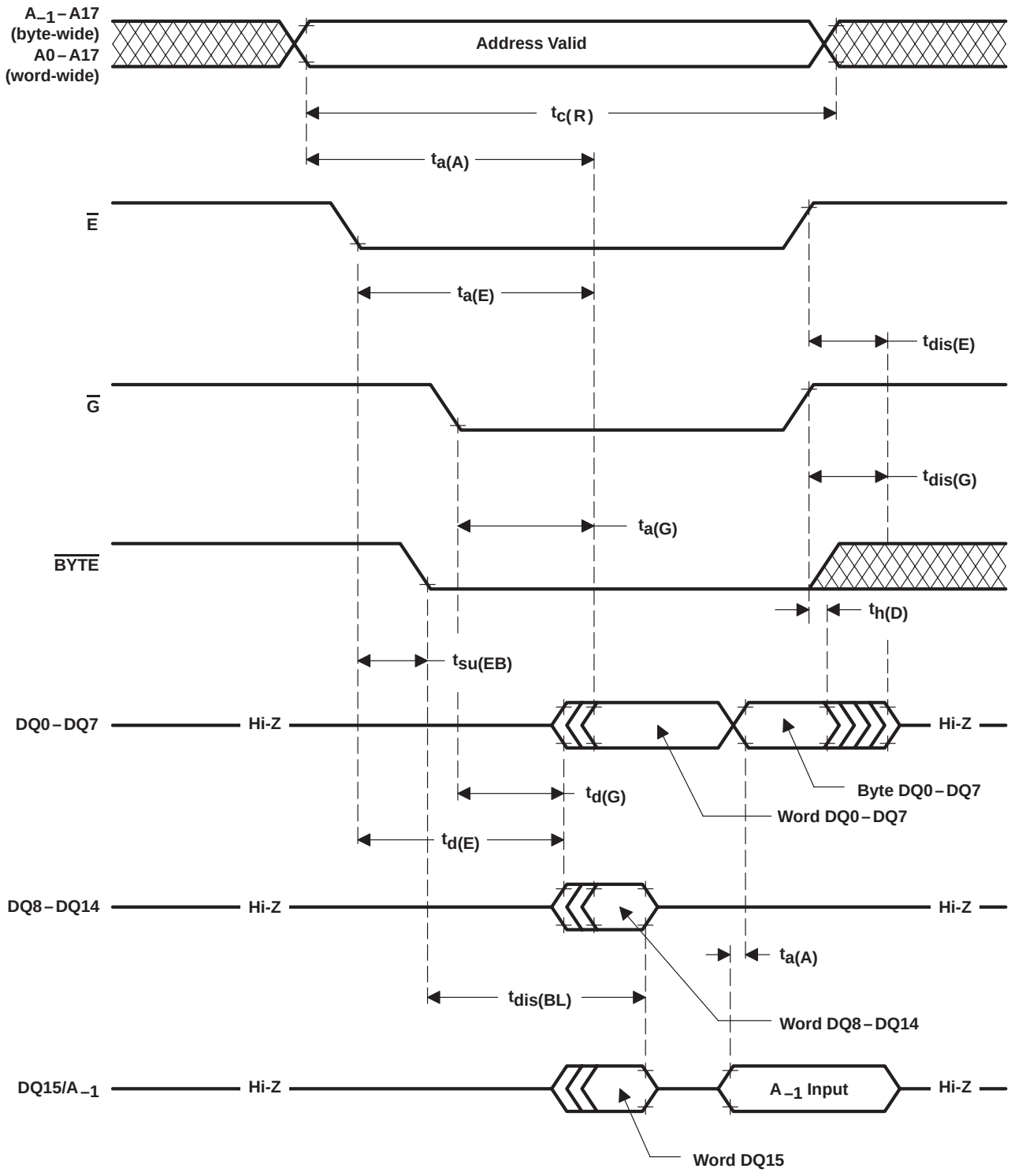


Figure 16. $\overline{\text{BYTE}}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PARAMETER MEASUREMENT INFORMATION

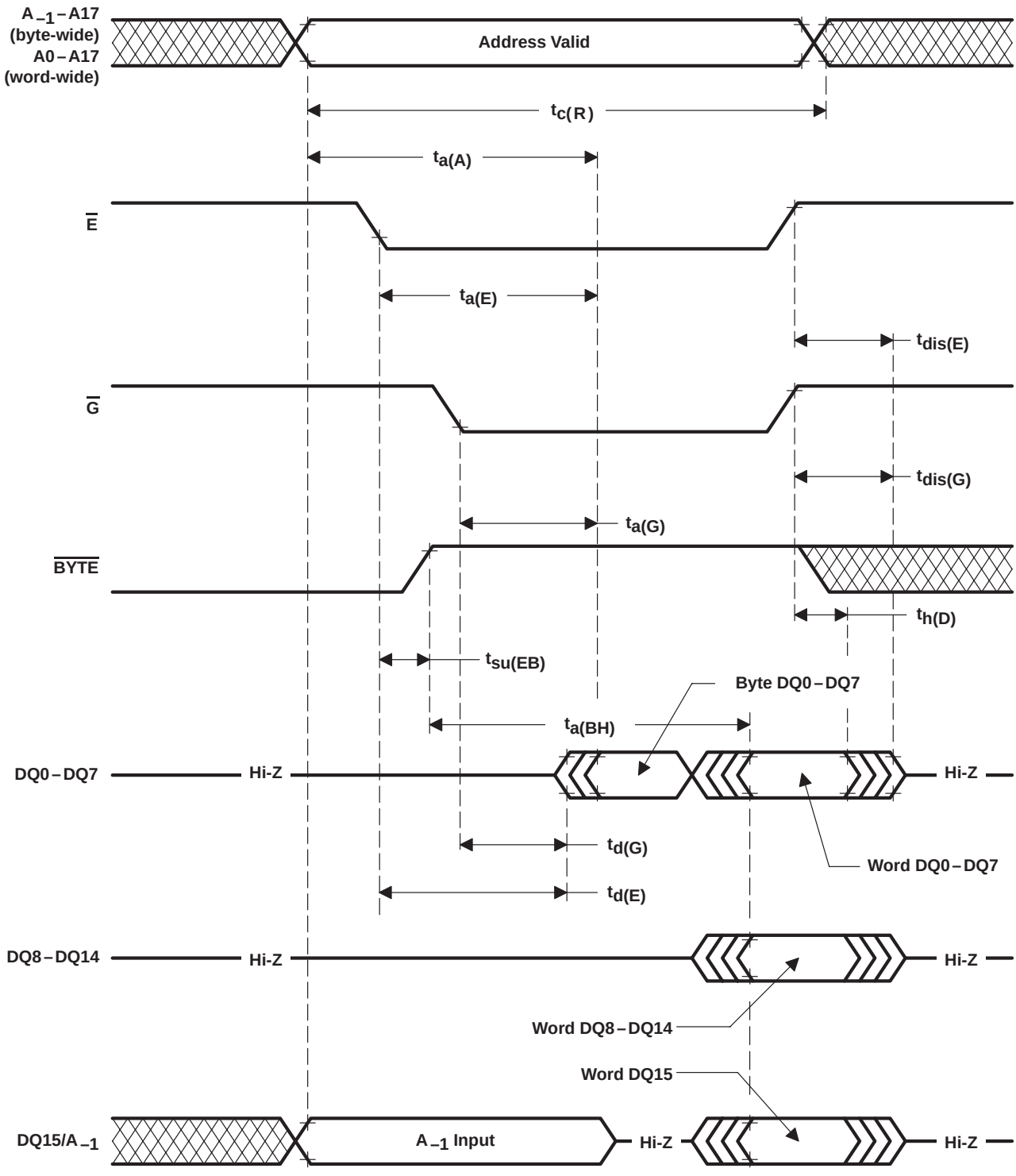
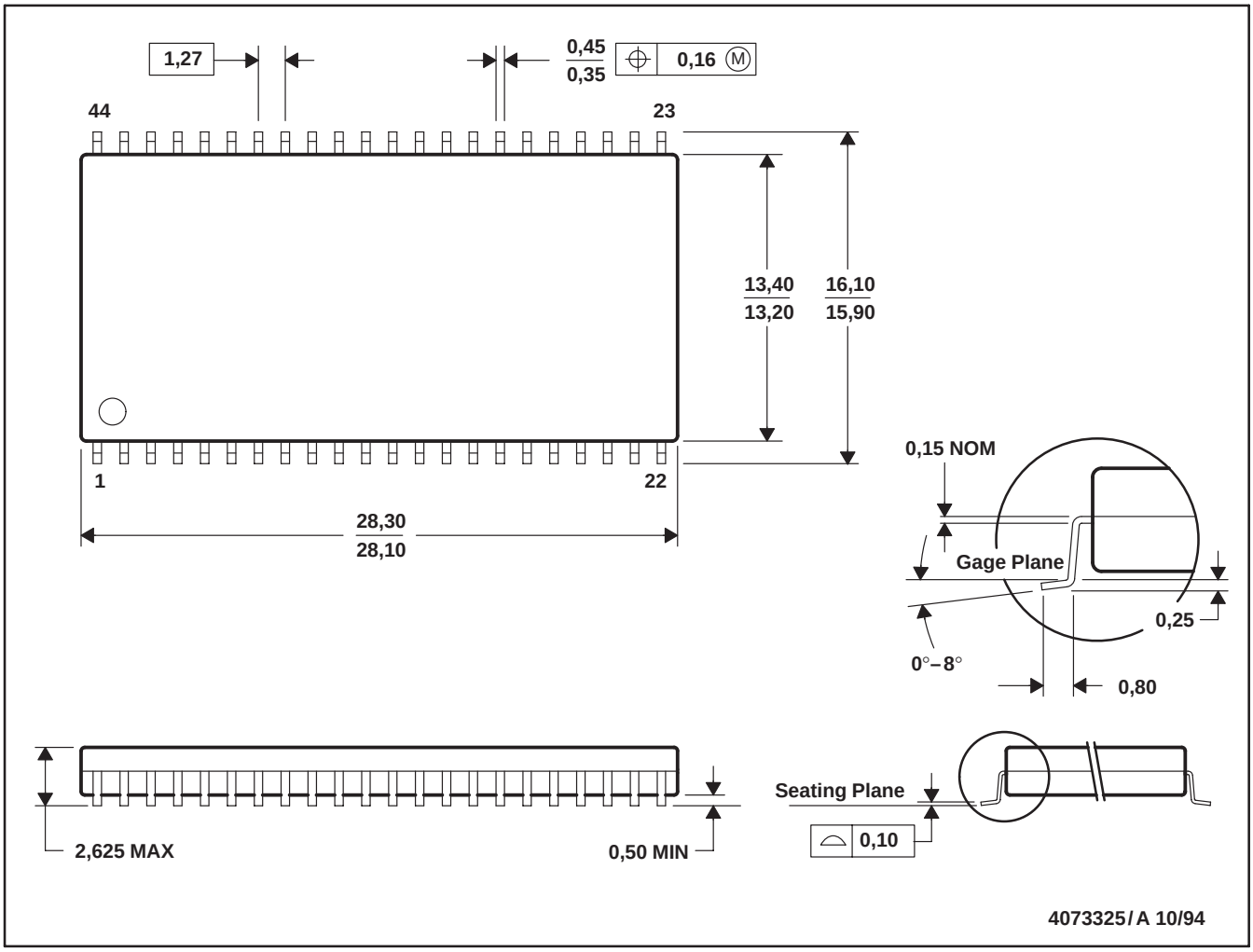


Figure 17. $\overline{\text{BYTE}}$ Timing, Changing From Byte-Wide to Word-Wide Mode

MECHANICAL DATA

DBJ (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE**

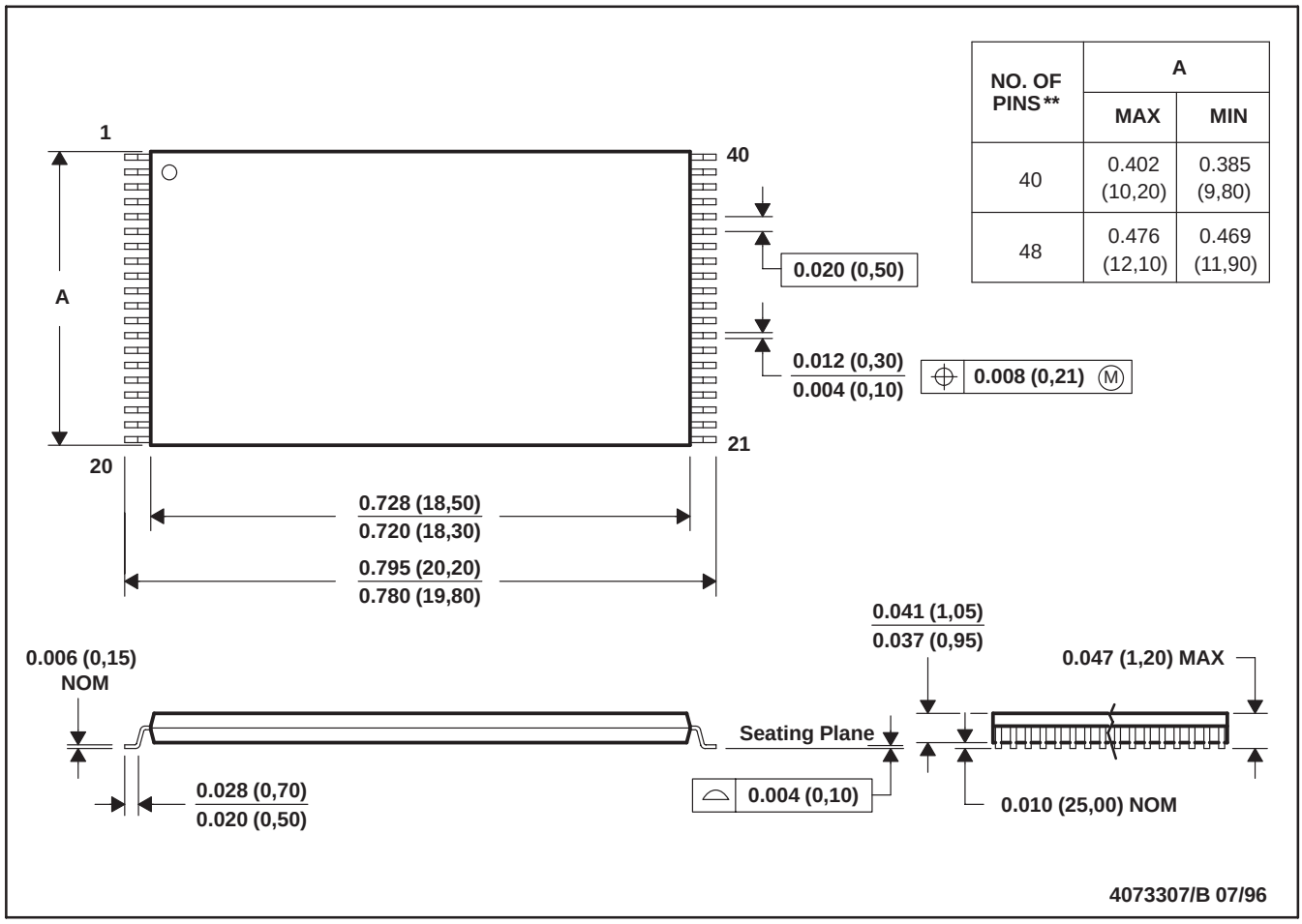


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

DCD (R-PDSO-G)** **PLASTIC DUAL SMALL-OUTLINE PACKAGE**

40 PIN SHOWN



NO. OF PINS**	A	
	MAX	MIN
40	0.402 (10,20)	0.385 (9,80)
48	0.476 (12,10)	0.469 (11,90)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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