

LP38855

1.5A Fast-Response High-Accuracy LDO Linear Regulator with Enable

General Description

The LP38855 is a high-current, fast-response regulator which can maintain output voltage regulation with an extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides power for the internal bias and control circuits, as well as drive for the gate of the N-MOS power transistor, while V_{IN} supplies power to the load. The use of an external bias rail allows the part to operate from ultra low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The LP38855 is available in TO-220 and TO-263 5-Lead packages.

Dropout Voltage: 130 mV (typical) at 1.5A load current.

Low Ground Pin Current: 14 mA (typical) at 1.5A load current.

Shutdown Current: 1 μ A (typical) $I_{IN(GND)}$ when EN pin is low.

Precision Output Voltage: $\pm 1.0\%$ for $T_J = 25^\circ\text{C}$ and $\pm 2.0\%$ for $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, across all line and load conditions

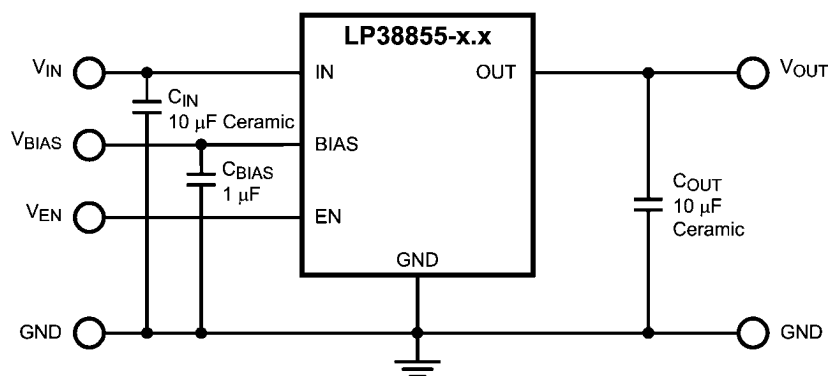
Features

- Standard V_{OUT} values of 0.8V and 1.2V
- Wide V_{BIAS} Supply operating range of 3.0V to 5.5V
- Stable with 10 μ F ceramic capacitors
- Dropout voltage of 130 mV (typical) at 1.5A load current
- Precision Output Voltage across all line and load conditions:
 - $\pm 1.0\%$ for $T_J = 25^\circ\text{C}$
 - $\pm 2.0\%$ for $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
 - $\pm 3.0\%$ for $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
- Over-Temperature and Over-Current protection
- Available in 5 lead TO-220 and TO-263 packages
- Custom V_{OUT} values between 0.8V and 1.2V are available
- -40°C to $+125^\circ\text{C}$ Operating Temperature Range

Applications

- ASIC Power Supplies In:
 - Desktops, Notebooks, and Graphics Cards, Servers
 - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Typical Application Circuit



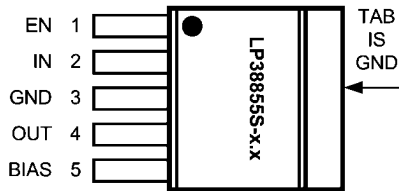
20202601

Ordering Information

V _{OUT} *	Order Number	Package Type	Package Drawing	Supplied As
0.8V	LP38855S-0.8	TO263-5	TS5B	Rail of 45
	LP38855SX-0.8	TO263-5	TS5B	Tape and Reel of 500
	LP38855T-0.8	TO220-5	T05D	Rail of 45
1.2V	LP38855S-1.2	TO263-5	TS5B	Rail of 45
	LP38855SX-1.2	TO263-5	TS5B	Tape and Reel of 500
	LP38855T-1.2	TO220-5	T05D	Rail of 45

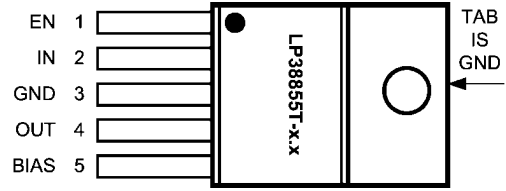
* For custom V_{OUT} values between 0.8V and 1.2V please contact the National Semiconductor Sales Office.

Connection Diagrams



TO-263, Top View

20202602



TO-220, Top View

20202603

Pin Descriptions

TO220-5 and TO263-5 Packages

Pin #	Pin Symbol	Pin Description
1	EN	The device Enable pin.
2	IN	The unregulated input voltage pin
3	GND	Ground
4	OUT	The regulated output voltage pin
5	BIAS	The supply for the internal control and reference circuitry
TAB	TAB	The TAB is a thermal connection that is physically attached to the backside of the die, and is used as a thermal heat-sink connection. See the Application Information section for details

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	-65°C to +150°C
Lead Temperature	
Soldering, 5 seconds	260°C
ESD Rating	
Human Body Model (Note 2)	±2 kV
Power Dissipation (Note 3)	Internally Limited
V _{IN} Supply Voltage (Survival)	-0.3V to +6.0V
V _{BIAS} Supply Voltage (Survival)	-0.3V to +6.0V

V _{EN} Voltage (Survival)	-0.3V to +6.0V
V _{OUT} Voltage (Survival)	-0.3V to +6.0V
I _{OUT} Current (Survival)	Internally Limited
Junction Temperature	-40°C to +150°C

Operating Ratings (Note 1)

V _{IN} Supply Voltage	(V _{OUT} + V _{DO}) to V _{BIAS}
V _{BIAS} Supply Voltage	3.0V to 5.5V
V _{EN} Enable Input Voltage	0.0V to V _{BIAS}
I _{OUT}	0 mA to 1.5A
Junction Temperature Range (Note 3)	-40°C to +125°C

Electrical Characteristics

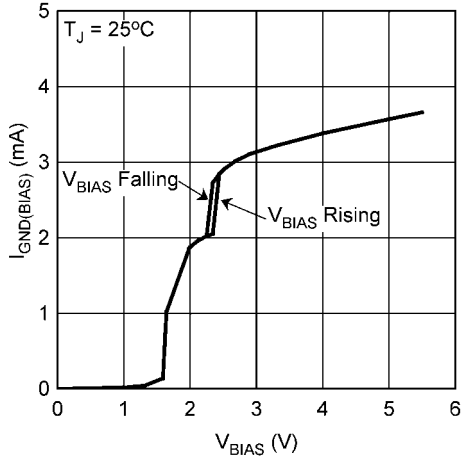
Unless otherwise specified: V_{IN} = V_{OUT(NOM)} + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 μF, C_{BIAS} = 1 μF, V_{EN} = V_{BIAS}. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V _{OUT}	Output Voltage Tolerance	V _{OUT(NOM)} + 1V ≤ V _{IN} ≤ V _{BIAS} , 3.0V ≤ V _{BIAS} ≤ 5.5V, 10 mA ≤ I _{OUT} ≤ 1.5A	-1.0 -3.0	0	+1.0 +3.0	%
		V _{OUT(NOM)} + 1V ≤ V _{IN} ≤ V _{BIAS} , 3.0V ≤ V _{BIAS} ≤ 5.5V, 10 mA ≤ I _{OUT} ≤ 1.5A, 0°C ≤ T _J ≤ 125°C	-2.0	0	+2.0	
ΔV _{OUT} /ΔV _{IN}	Line Regulation, V _{IN} (Note 4)	V _{OUT(NOM)} + 1V ≤ V _{IN} ≤ V _{BIAS}	-	0.04	-	%/V
ΔV _{OUT} /ΔV _{BIAS}	Line Regulation, V _{BIAS} (Note 4)	3.0V ≤ V _{BIAS} ≤ 5.5V	-	0.10	-	%/V
ΔV _{OUT} /ΔI _{OUT}	Output Voltage Load Regulation (Note 5)	10 mA ≤ I _{OUT} ≤ 1.5A	-	0.2	-	%/A
V _{DO}	Dropout Voltage V _{IN} - V _{OUT} (Note 6)	I _{OUT} = 1.5A	-	130	165 180	mV
I _{GND(IN)}	Ground Pin Current Drawn from V _{IN} Supply	LP38855-0.8 10 mA ≤ I _{OUT} ≤ 1.5A	-	7.0	8.5 9.0	mA
		LP38855-1.2 10 mA ≤ I _{OUT} ≤ 1.5A	-	11	12 15	
		V _{EN} ≤ 0.5V	-	1.0	10 300	μA
I _{GND(BIAS)}	Ground Pin Current Drawn from V _{BIAS} Supply	10 mA ≤ I _{OUT} ≤ 1.5A	-	3.0	3.8 4.5	mA
		V _{EN} ≤ 0.5V	-	100	170 200	
UVLO	Under-Voltage Lock-Out Threshold	V _{BIAS} rising until device is functional	2.20 2.00	2.45	2.70 2.90	V
UVLO _(HYS)	Under-Voltage Lock-Out Hysteresis	V _{BIAS} falling from UVLO threshold until device is non-functional	60 50	150	300 350	mV
I _{SC}	Output Short-Circuit Current	V _{IN} = V _{OUT(NOM)} + 1V, V _{BIAS} = 3.0V, V _{OUT} = 0.0V	-	4.5	-	A

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
ENABLE Pin						
I_{EN}	ENABLE pin Current	$V_{EN} = V_{BIAS}$	-	0.01	-	μA
		$V_{EN} = 0.0V, V_{BIAS} = 5.5V$	-19 -13	-30	-40 -51	
$V_{EN(ON)}$	Enable Voltage Threshold	V_{EN} rising until Output = ON	1.00 0.90	1.25	1.50 1.55	V
$V_{EN(HYS)}$	Enable Voltage Hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	50 30	100	150 200	mV
t_{OFF}	Turn-OFF Delay Time	$R_{LOAD} \times C_{OUT} \ll t_{OFF}$	-	20	-	μs
t_{ON}	Turn-ON Delay Time	$R_{LOAD} \times C_{OUT} \ll t_{ON}$	-	15	-	
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT} + 1V,$ $f = 120 \text{ Hz}$	-	80	-	dB
		$V_{IN} = V_{OUT} + 1V,$ $f = 1 \text{ kHz}$	-	65	-	
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT} + 3V,$ $f = 120 \text{ Hz}$	-	58	-	dB
		$V_{BIAS} = V_{OUT} + 3V,$ $f = 1 \text{ kHz}$	-	58	-	
e_n	Output Noise Density	$f = 120 \text{ Hz}$	-	1	-	$\mu V/\sqrt{Hz}$
	Output Noise Voltage	BW = 10 Hz – 100 kHz	-	150	-	μV_{RMS}
		BW = 300 Hz – 300 kHz	-	90	-	
Thermal Parameters						
T_{SD}	Thermal Shutdown Junction Temperature		-	160	-	$^{\circ}C$
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis		-	10	-	
θ_{JA}	Thermal Resistance, Junction to Ambient(Note 3)	TO220-5	-	60	-	$^{\circ}C/W$
		TO263-5	-	60	-	
θ_{JC}	Thermal Resistance, Junction to Case(Note 3)	TO220-5	-	3	-	
		TO263-5	-	3	-	
<p>Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.</p> <p>Note 2: The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114. The HBM rating for device pin 1 (EN) is $\pm 1.5 \text{ kV}$.</p> <p>Note 3: Device power dissipation must be de-rated based on device power dissipation (T_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the Application Information section for details.</p> <p>Note 4: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.</p> <p>Note 5: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.</p> <p>Note 6: Dropout voltage is defined as the input to output voltage differential ($V_{IN} - V_{OUT}$) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.</p>						

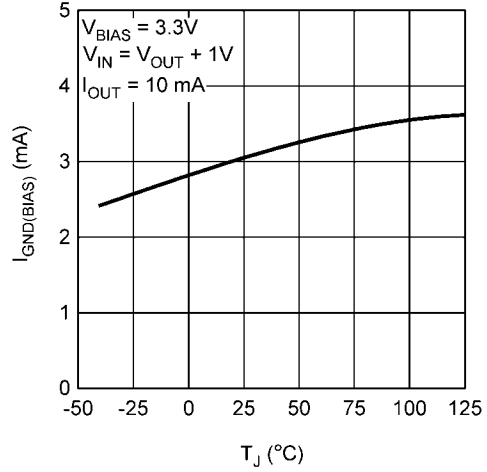
Typical Performance Characteristics Unless otherwise specified: $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{V}$, $V_{BIAS} = 3.0\text{V}$, $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 10\ \mu\text{F}$ Ceramic, $C_{BIAS} = 1\ \mu\text{F}$ Ceramic, $V_{EN} = V_{BIAS}$.

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}



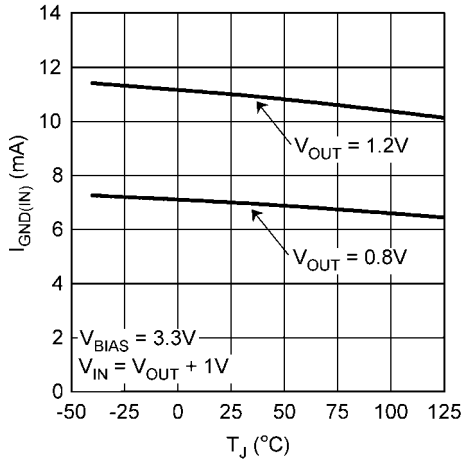
20202687

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature



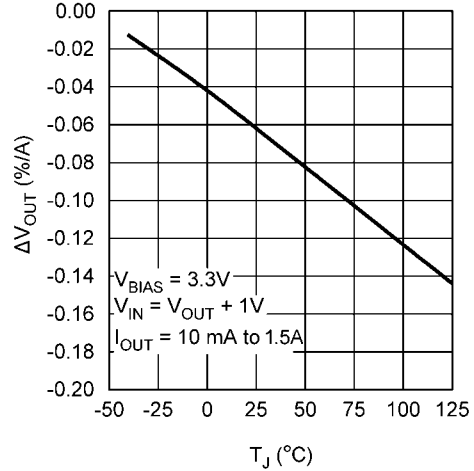
20202661

V_{IN} Ground Pin Current ($I_{GND(IN)}$) vs Temperature



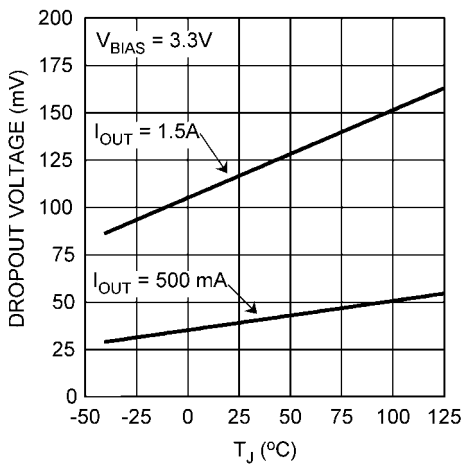
20202662

Load Regulation vs Temperature



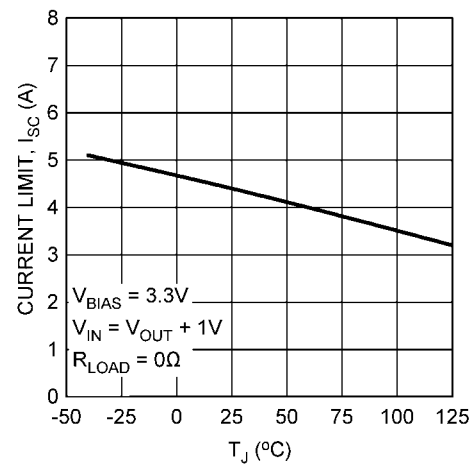
20202663

Dropout Voltage (V_{DO}) vs Temperature

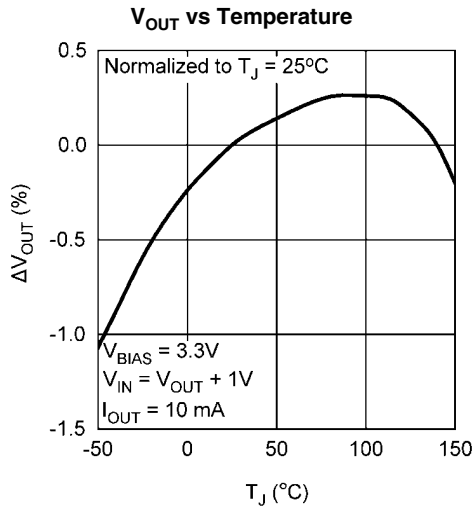


20202665

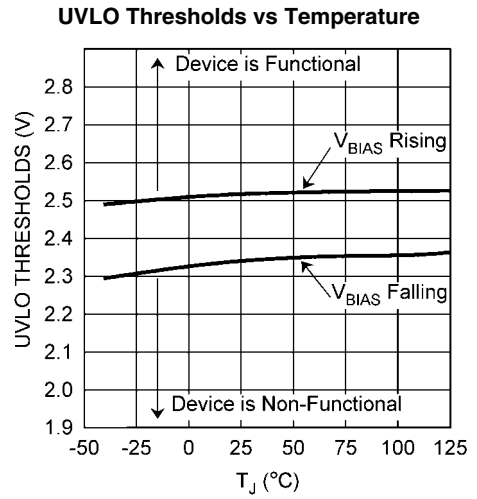
Output Current Limit (I_{SC}) vs Temperature



20202666

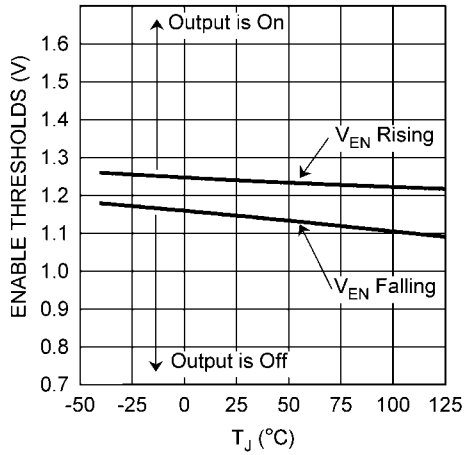


20202667



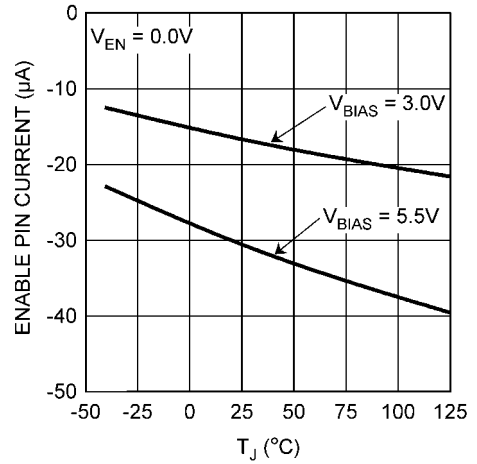
20202668

Enable Thresholds (V_{EN}) vs Temperature



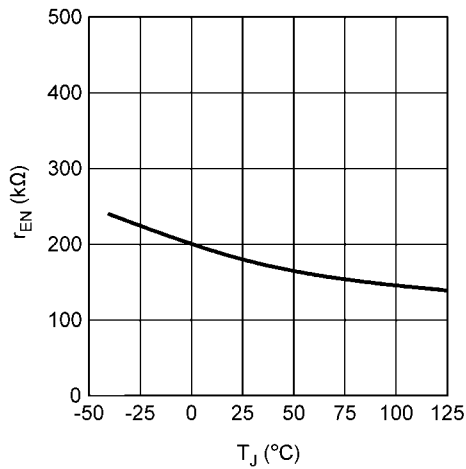
20202672

Enable Pull-Down Current (I_{EN}) vs Temperature



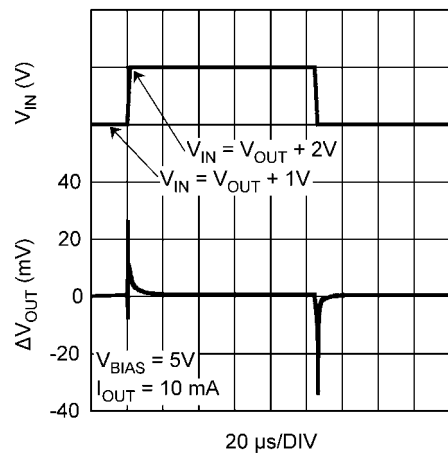
20202673

Enable Pull-Up Resistor (r_{EN}) vs Temperature



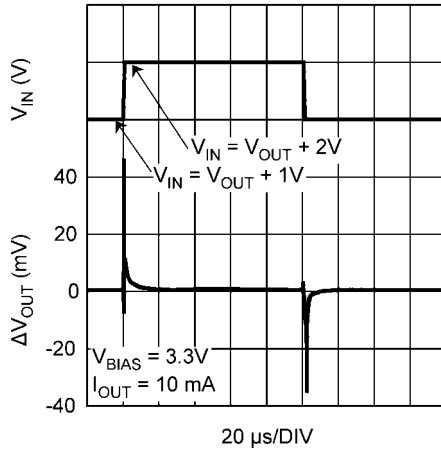
20202674

V_{IN} Line Transient Response



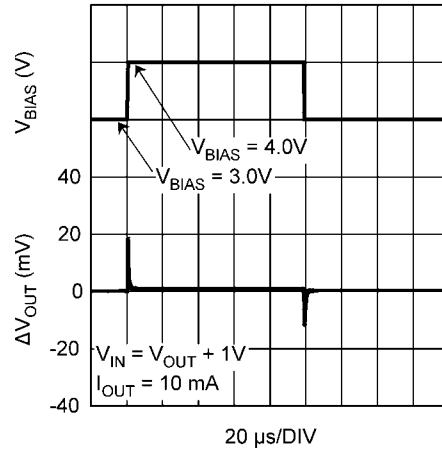
20202677

V_{IN} Line Transient Response



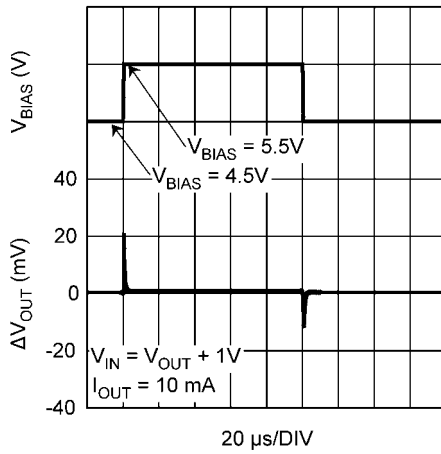
20202678

V_{BIAS} Line Transient Response



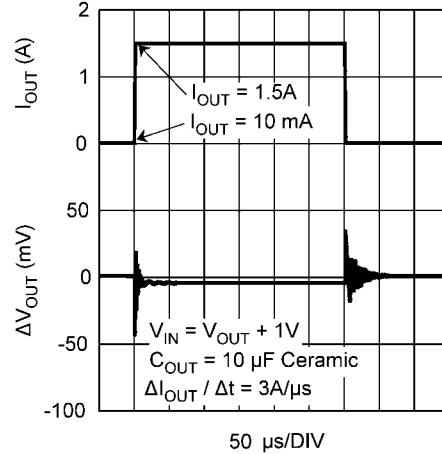
20202679

V_{BIAS} Line Transient Response



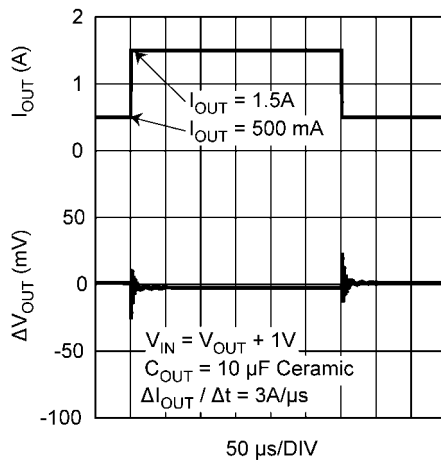
20202680

Load Transient Response, C_{OUT} = 10 μF Ceramic



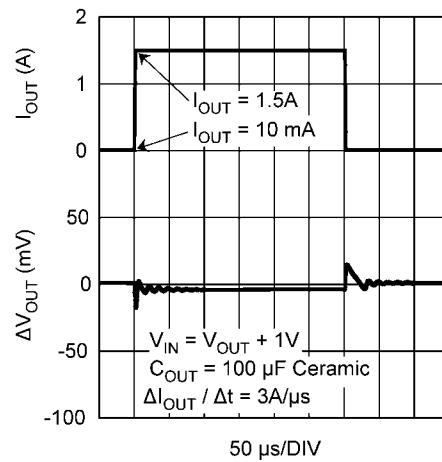
20202681

Load Transient Response, C_{OUT} = 10 μF Ceramic



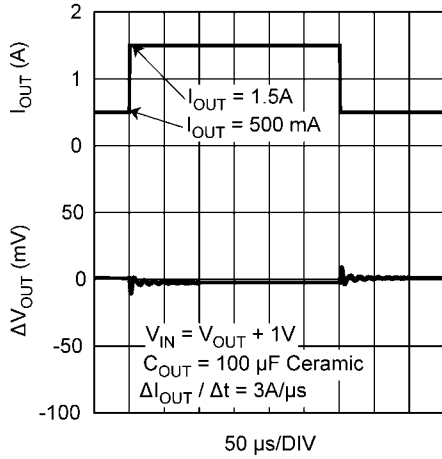
20202682

Load Transient Response, C_{OUT} = 100 μF Ceramic



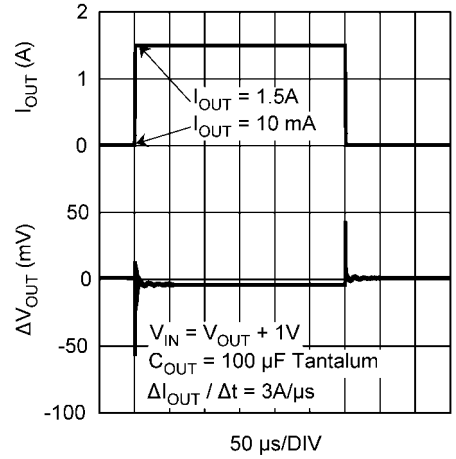
20202683

Load Transient Response, $C_{OUT} = 100 \mu\text{F}$ Ceramic



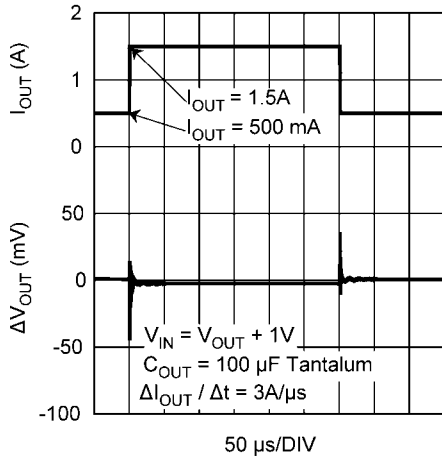
20202684

Load Transient Response, $C_{OUT} = 100 \mu\text{F}$ Tantalum



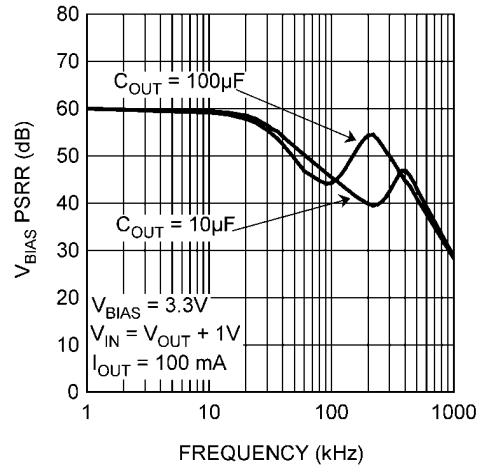
20202685

Load Transient Response, $C_{OUT} = 100 \mu\text{F}$ Tantalum



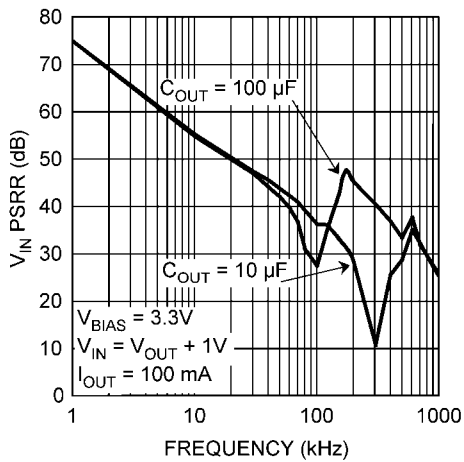
20202686

V_{BIAS} PSRR



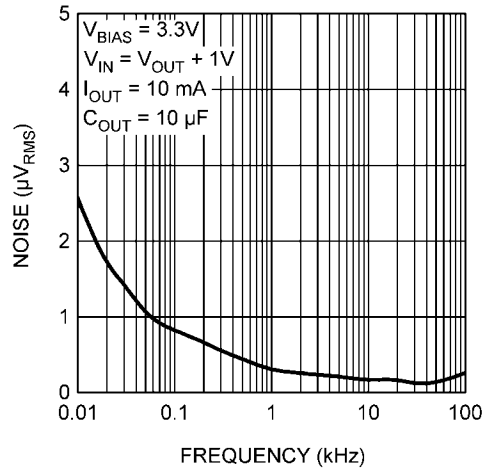
20202670

V_{IN} PSRR



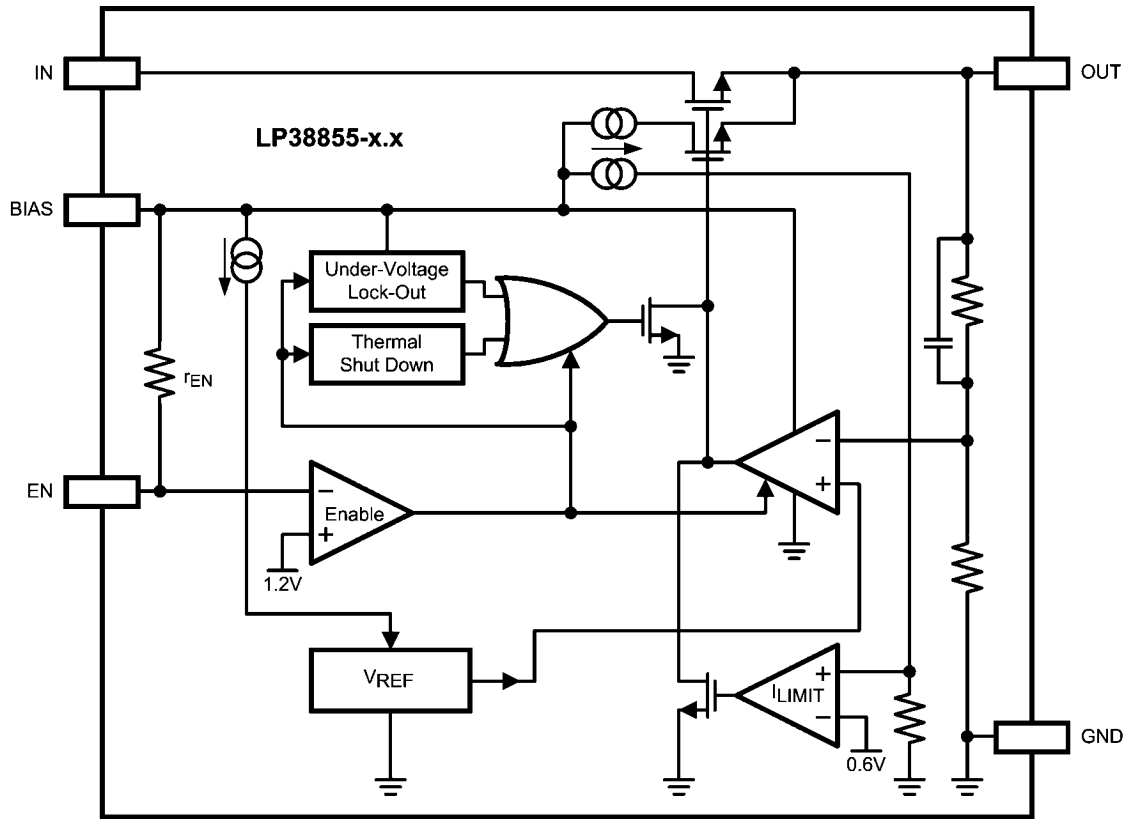
20202671

Output Noise



20202669

Block Diagram



20202605

Application Information

EXTERNAL CAPACITORS

To assure regulator stability, capacitors are required on the input, output and bias pins as shown in the Typical Application Circuit.

Output Capacitor

A minimum output capacitance of 10 μF , ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 μF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

Input Capacitor

The input capacitor must be at least 10 μF , but can be increased without limit. Its purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

Bias Capacitor

The capacitor on the bias pin must be at least 1 μF . It can be any good quality capacitor (ceramic is recommended).

INPUT VOLTAGE

The input voltage (V_{IN}) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least $V_{\text{OUT}} + V_{\text{DO}}$, and no higher than whatever value is used for V_{BIAS} .

BIAS VOLTAGE

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. The bias voltage must be in the range of 3.0V to 5.5V to ensure proper operation of the device.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry become active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the guaranteed limits.

SUPPLY SEQUENCING

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed. However, the output voltage cannot be guaranteed until both V_{IN} and V_{BIAS} are within the range of guaranteed operating values.

If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommend for this diode clamp.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold, or the EN pin is held low.

When V_{BIAS} is above the UVLO threshold, and the EN pin is above the $V_{\text{EN(ON)}}$ threshold, the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{\text{DS(ON)}}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 μF in this manner will not damage the device as the current will decay rapidly. However, continuous reverse current should be avoided.

ENABLE OPERATION

The Enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The Enable pin has an internal pull-up, through a typical 180 k Ω resistor, to V_{BIAS} .

If the Enable pin is actively driven, pulling the Enable pin above the V_{EN} threshold of 1.25V (typical) will turn the regulator output on, while pulling the Enable pin below the V_{EN} threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the Enable threshold provide noise immunity.

If the Enable function is not needed this pin should be left open, or connected directly to V_{BIAS} . If the Enable pin is left open, stray capacitance on this pin must be minimized, otherwise the output turn-on will be delayed while the stray capacitance is charged through the internal resistance (r_{EN}).

POWER DISSIPATION AND HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{\text{D(PASS)}} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} \quad (1)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)} \quad (2)$$

where $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS} .

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)} \quad (3)$$

where $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN} .

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (4)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature ($T_{A(MAX)}$) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (5)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA} , can be calculated using the formula:

$$\theta_{JA} \leq \frac{\Delta T_J}{P_D} \quad (6)$$

Heat-Sinking The TO-220 Package

The TO-220 package has a θ_{JA} rating of 60°C/W, and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat-sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO-263 package.

The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance, θ_{HA} :

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC}) \quad (7)$$

where θ_{JA} is the required total thermal resistance from the junction to the ambient air, θ_{CH} is the thermal resistance from the case to the surface of the heat sink, and θ_{JC} is the thermal resistance from the junction to the surface of the case.

For this equation, θ_{JC} is about 3°C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

Heat-Sinking The TO-263 Package

The TO-263 package has a θ_{JA} rating of 60°C/W, and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The TO-263 package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat-sinking. The graph below shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

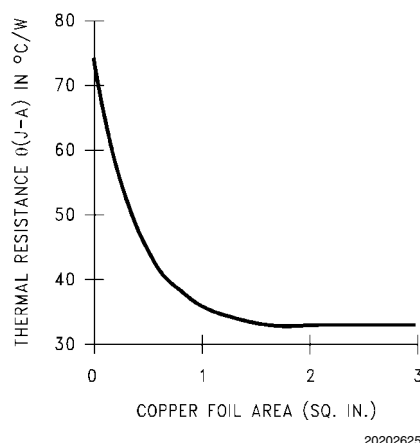


FIGURE 1. θ_{JA} vs Copper (1 Ounce) Area for the TO-263 package

As shown in Figure 1, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 package mounted to a PCB is 32°C/W.

Figure 2 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

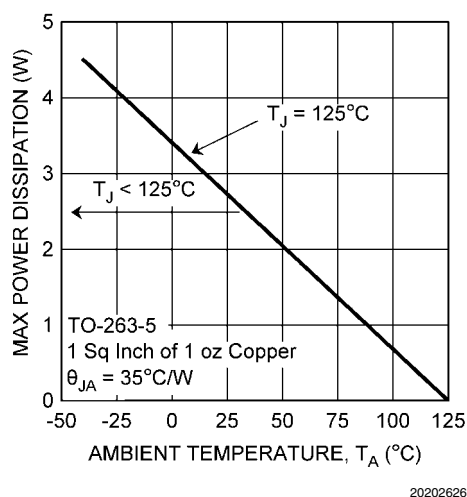
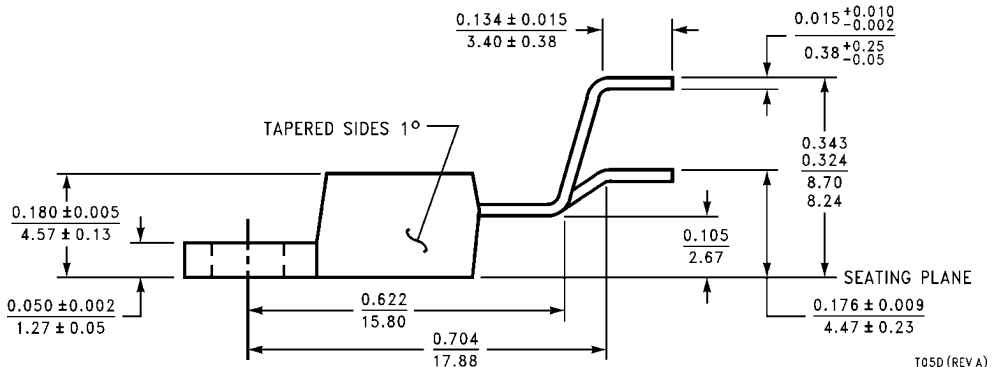
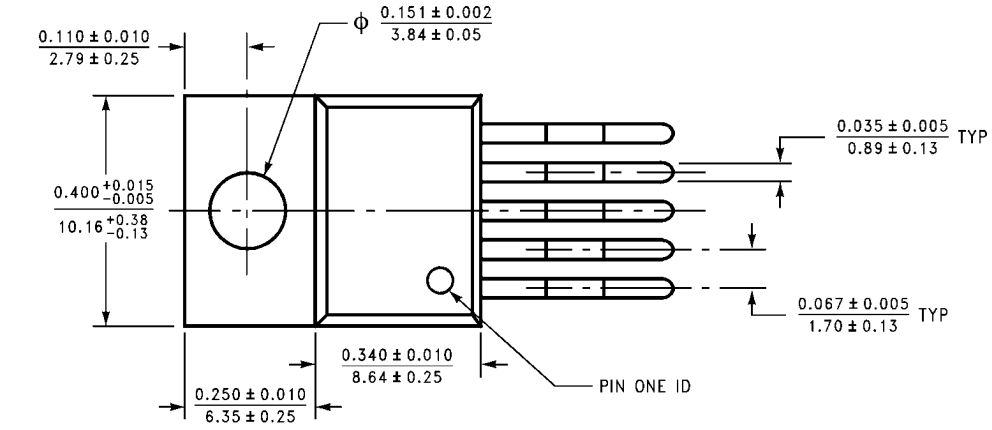


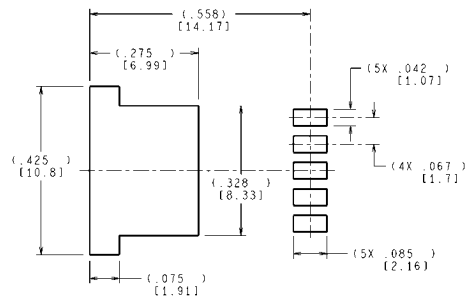
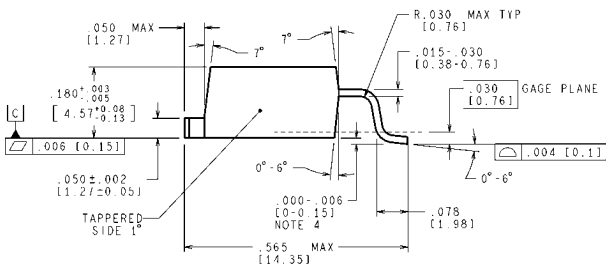
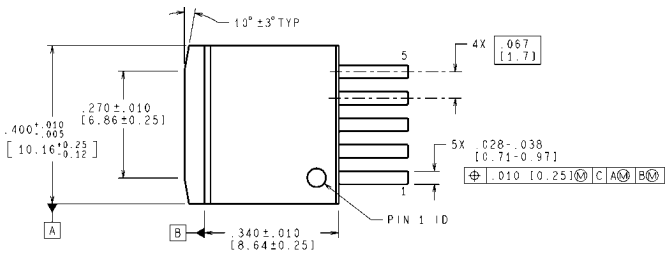
FIGURE 2. Maximum Power Dissipation vs Ambient Temperature for TO-263 package

Physical Dimensions inches (millimeters) unless otherwise noted

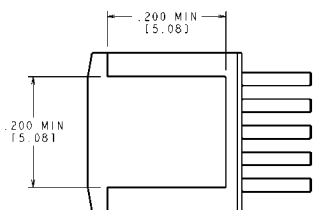


**TO220 5-lead, Molded, Stagger Bend Package (TO220-5)
NS Package Number T05D**

T05D (REV A)



LAND PATTERN RECOMMENDATION



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

**TO263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B**

TS5B (Rev D)

Notes

LP38855

Notes

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2007 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Customer Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
 Fax: +49 (0) 180-530-85-86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +49 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560