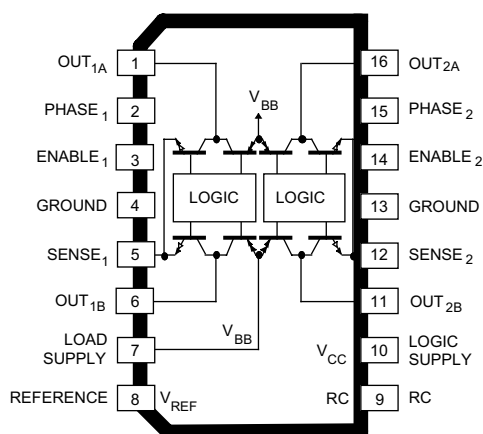


3966

Data Sheet
29319.25G

DUAL FULL-BRIDGE PWM MOTOR DRIVER

A3966SLB (SOIC)



Dwg. PP-066-1

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} **30 V**
Output Current, I_{OUT} (peak) **± 750 mA**
(continuous) **± 650 mA**
Logic Supply Voltage, V_{CC} **7.0 V**
Input Voltage, V_{in} **-0.3 V to $V_{CC} + 0.3$ V**
Sense Voltage, V_S **1.0 V**
Package Power Dissipation ($T_A = 25^\circ\text{C}$), P_D
A3966SA **2.08 W***
A3966SLB **1.87 W***
Operating Temperature Range,
 T_A **-20°C to $+85^\circ\text{C}$**
Junction Temperature,
 T_J **$+150^\circ\text{C}$**
Storage Temperature Range,
 T_S **-55°C to $+150^\circ\text{C}$**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C .

* Per SEMI G42-88 Specification, Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.

The A3966SA and A3966SLB are designed to drive both windings of a two-phase bipolar stepper motor. Each device includes two H-bridges capable of continuous output currents of ± 650 mA and operating voltages to 30 V. Motor winding current can be controlled by the internal fixed-frequency, pulse-width modulated (PWM), current-control circuitry. The peak load current limit is set by the user's selection of a reference voltage and current-sensing resistors. Except for package style and pinout, the two devices are identical.

The fixed-frequency pulse duration is set by a user-selected external RC timing network. The capacitor in the RC timing network also determines a user-selectable blanking window that prevents false triggering of the PWM current-control circuitry during switching transitions.

To reduce on-chip power dissipation, the H-bridge power outputs have been optimized for low saturation voltages. The sink drivers feature the Allegro® patented Satlington® output structure. The Satlington outputs combine the low voltage drop of a saturated transistor and the high peak current capability of a Darlington.

For each bridge, a PHASE input controls load-current polarity by selecting the appropriate source and sink driver pair. For each bridge, an ENABLE input, when held high, disables the output drivers. Special power-up sequencing is not required. Internal circuit protection includes thermal shutdown with hysteresis, ground-clamp and flyback diodes, and crossover-current protection.

The A3966SA is supplied in a 16-pin dual in-line plastic package. The A3966SLB is supplied in a 16-lead plastic SOIC with copper heat sink tabs. The power tab is at ground potential and needs no electrical isolation. The A3966SLB is also available in a lead (Pb) free version, with 100% matte tin leadframe plating.

FEATURES

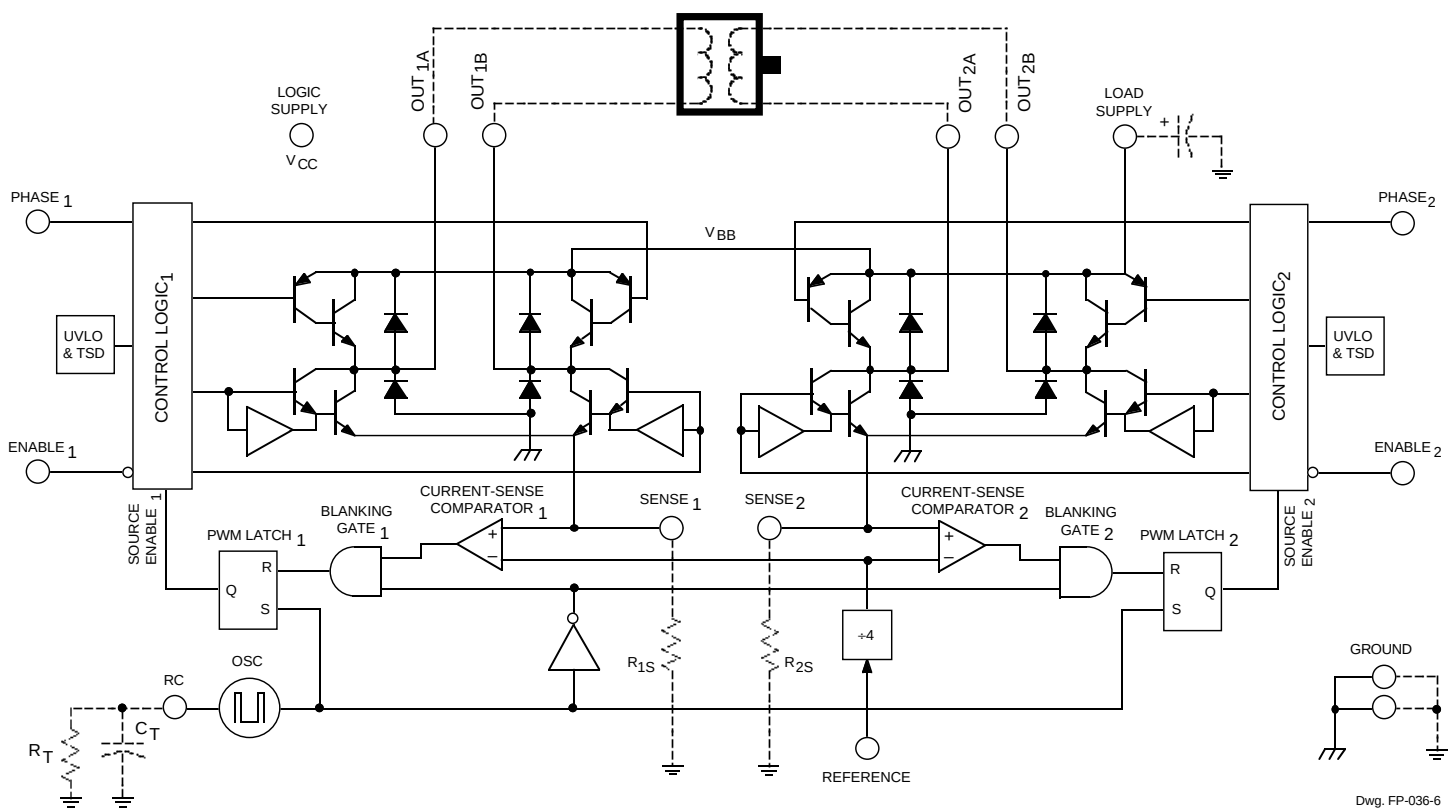
- ± 650 mA Continuous Output Current
- 30 V Output Voltage Rating
- Internal Fixed-Frequency PWM Current Control
- Satlington Sink Drivers
- User-Selectable Blanking Window
- Internal Ground-Clamp & Flyback Diodes
- Internal Thermal-Shutdown Circuitry
- Crossover-Current Protection and UVLO Protection

Part Number	Pb-free*	Package	Packing
A3966SLB-T	Yes	16-Lead SOIC	47 per tube
A3966SLBTR-T	Yes	16-Lead SOIC	1000 per reel

*Pb-based variants are being phased out of the product line. The variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadline for receipt to LAST TIME BUY orders: April 27, 2007. These variants include: A3966SA, A3966SLB, and A3966SLBTR.

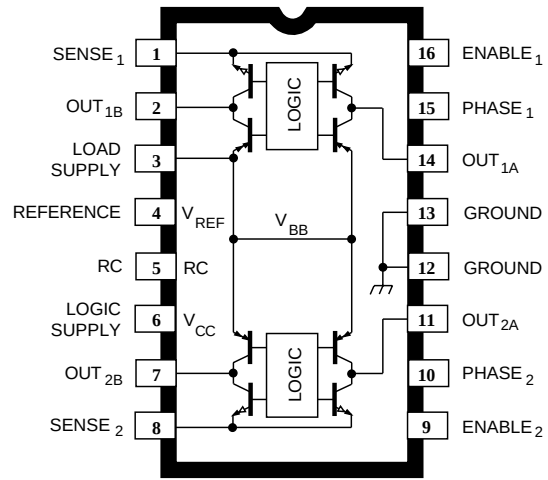
3966 **DUAL FULL-BRIDGE** **PWM MOTOR DRIVER**

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-036-6

A3966SA (DIP)



Dwg. PP-066-2

TRUTH TABLE

PHASE	ENABLE	OUT _A	OUT _B
X	H	Off	Off
H	L	H	L
L	L	L	H

X = Irrelevant

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DUAL FULL-BRIDGE PWM MOTOR DRIVER

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{BB} = 30\text{ V}$, $V_{CC} = 4.75\text{ V to }5.5\text{ V}$, $V_{REF} = 2\text{ V}$, $V_S = 0\text{ V}$, $56\text{ k}\Omega$ & 680 pF RC to Ground (unless noted otherwise)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units

Output Drivers

Load Supply Voltage Range	V_{BB}	Operating, $I_{OUT} = \pm 650\text{ mA}$, $L = 3\text{ mH}$	V_{CC}	—	30	V
Output Leakage Current	I_{CEX}	$V_{OUT} = 30\text{ V}$	—	<1.0	50	μA
		$V_{OUT} = 0\text{ V}$	—	<-1.0	-50	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, $I_{OUT} = -400\text{ mA}$	—	1.7	2.0	V
		Source Driver, $I_{OUT} = -650\text{ mA}$	—	1.8	2.1	V
		Sink Driver, $I_{OUT} = +400\text{ mA}$, $V_S = 0.5\text{ V}$	—	0.3	0.5	V
		Sink Driver, $I_{OUT} = +650\text{ mA}$, $V_S = 0.5\text{ V}$	—	0.7	1.3	V
Clamp Diode Forward Voltage	V_F	$I_F = 400\text{ mA}$	—	1.1	1.4	V
		$I_F = 650\text{ mA}$	—	1.4	1.6	V
Motor Supply Current (No Load)	$I_{BB(ON)}$	$V_{ENABLE1} = V_{ENABLE2} = 0.8\text{ V}$	—	3.0	5.0	mA
	$I_{BB(OFF)}$	$V_{ENABLE1} = V_{ENABLE2} = 2.4\text{ V}$	—	<1.0	200	μA

Control Logic

Logic Supply Voltage Range	V_{CC}	Operating	4.75	—	5.50	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 2.4\text{ V}$	—	<1.0	20	μA
	$I_{IN(0)}$	$V_{IN} = 0.8\text{ V}$	—	<-20	-200	μA
Reference Input Volt. Range	V_{REF}	Operating	0.1	—	2.0	V
Reference Input Current	I_{REF}		-2.5	0	1.0	μA
Reference Divider Ratio	V_{REF}/V_{TRIP}		3.8	4.0	4.2	—
Current-Sense Comparator Input Offset Voltage	V_{IO}	$V_{REF} = 0\text{ V}$	-6.0	0	6.0	mV
Current-Sense Comparator Input Voltage Range	V_S	Operating	-0.3	—	1.0	V
Sense-Current Offset	I_{SO}	$I_S - I_{OUT}$, $50\text{ mA} \leq I_{OUT} \leq 650\text{ mA}$	12	18	24	mA

NOTES: 1. Typical Data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

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DUAL FULL-BRIDGE

PWM MOTOR DRIVER

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{BB} = 30\text{ V}$, $V_{CC} = 4.75\text{ V to } 5.5\text{ V}$, $V_{REF} = 2\text{ V}$, $V_S = 0\text{ V}$, $56\text{ k}\Omega$ & 680 pF RC to Ground (unless noted otherwise) (cont.)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic (continued)						
PWM RC Frequency	f _{osc}	C _T = 680 pF, R _T = 56 kΩ	22.9	25.4	27.9	kHz
PWM Propagation Delay Time	t _{PWM}	Comparator Trip to Source OFF	—	1.0	1.4	μs
		Cycle Reset to Source ON	—	0.8	1.2	μs
Cross-Over Dead Time	t _{codt}	1 kΩ Load to 25 V	0.2	1.8	3.0	μs
Propagation Delay Times	t _{pd}	I _{OUT} = ±650 mA, 50% to 90%: ENABLE ON to Source ON	—	100	—	ns
		ENABLE OFF to Source OFF	—	500	—	ns
		ENABLE ON to Sink ON	—	200	—	ns
		ENABLE OFF to Sink OFF	—	200	—	ns
		PHASE Change to Sink ON	—	2200	—	ns
		PHASE Change to Sink OFF	—	200	—	ns
		PHASE Change to Source ON	—	2200	—	ns
		PHASE Change to Source OFF	—	200	—	ns
Thermal Shutdown Temp.	T _J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT _J		—	15	—	°C
UVLO Enable Threshold	V _{T(UVLO)+}	Increasing V _{CC}	—	4.1	4.6	V
UVLO Hysteresis	V _{T(UVLO)hys}		0.1	0.6	—	V
Logic Supply Current	I _{CC(ON)}	V _{ENABLE 1} = V _{ENABLE 2} = 0.8 V	—	—	50	mA
	I _{CC(OFF)}	V _{ENABLE 1} = V _{ENABLE 2} = 2.4 V	—	—	9.0	mA

NOTES: 1. Typical Data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Internal PWM Current Control. The A3966SA and A3966SLB dual H-bridges are designed to drive both windings of a bipolar stepper motor. Load current can be controlled in each motor winding by an internal fixed-frequency PWM control circuit. The current-control circuitry works as follows: when the outputs of the H-bridge are turned on, current increases in the motor winding. The load current is sensed by the current-control comparator via an external sense resistor (R_S). Load current continues to increase until it reaches the predetermined value, set by the selection of external current-sensing resistors and reference input voltage (V_{REF}) according to the equation:

$$I_{TRIP} = I_{OUT} + I_{SO} = V_{REF}/(4 R_S)$$

where I_{SO} is the sense-current error (typically 18 mA) due to the base-drive current of the sink driver transistor.

At the trip point, the comparator resets the source-enable latch, turning off the source driver of that H-bridge. The source turn off of one H-bridge is independent of the other H-bridge. Load inductance causes the current to recirculate through the sink driver and ground-clamp diode. The current decreases until the internal clock oscillator sets the source-enable latches of both H-bridges, turning on the source drivers of both bridges. Load current increases again, and the cycle is repeated.

The frequency of the internal clock oscillator is set by the external timing components $R_T C_T$. The frequency can be approximately calculated as:

$$f_{osc} = 1/(R_T C_T + t_{blank})$$

where t_{blank} is defined below.

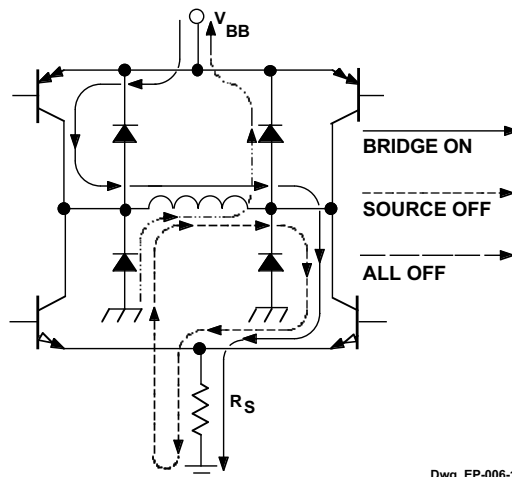
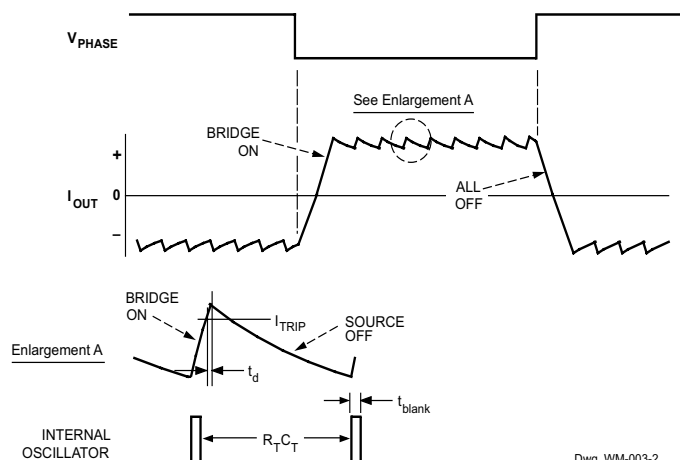
The range of recommended values for R_T and C_T are 20 k Ω to 100 k Ω and 470 pF to 1000 pF respectively. Nominal values of 56 k Ω and 680 pF result in a clock frequency of 25 kHz.

Current-Sense Comparator Blanking. When the source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the current-control comparator output is blanked for a short period of time when the source driver is turned on. The blanking time is set by the timing component C_T according to the equation:

$$t_{blank} = 1900 C_T (\mu s).$$

A nominal C_T value of 680 pF will give a blanking time of 1.3 μs .

The current-control comparator is also blanked when the H-bridge outputs are switched by the PHASE or ENABLE inputs. This internally generated blank time is approximately 1 μs .



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DUAL FULL-BRIDGE PWM MOTOR DRIVER

FUNCTIONAL DESCRIPTION (continued)

Load Current Regulation. Due to internal logic and switching delays (t_d), the actual load current peak will be slightly higher than the I_{TRIP} value. These delays, plus the blanking time, limit the minimum value the current control circuitry can regulate. To produce zero current in a winding, the ENABLE terminal should be held high, turning off all output drivers for that H-bridge.

Logic Inputs. A logic high on the PHASE input results in current flowing from OUT_A to OUT_B of that H-bridge. A logic low on the PHASE input results in current flowing from OUT_B to OUT_A . An internally generated dead time (t_{codd}) of approximately 1 μs prevents cross-over current spikes that can occur when switching the PHASE input.

A logic high on the ENABLE input turns off all four output drivers of that H-bridge. This results in a fast current decay through the internal ground clamp and flyback diodes. A logic low on the ENABLE input turns on the selected source and sink driver of that H-bridge.

The ENABLE inputs can be pulse-width modulated for applications that require a fast current-decay PWM. If external current-sensing circuitry is used, the internal current-control logic can be disabled by connecting the $R_T C_T$ terminal to ground.

The REFERENCE input voltage is typically set with a resistor divider from V_{CC} . This reference voltage is internally divided down by 4 to set up the current-comparator trip-voltage threshold. The reference input voltage range is 0 to 2 V.

Output Drivers. To minimize on-chip power dissipation, the sink drivers incorporate a Satlington structure. The Satlington output combines the low $V_{CE(sat)}$ features of a saturated transistor and the high peak-current capability of a Darlington (connected) transistor. A graph showing typical output saturation voltages as a function of output current is on the next page.

Miscellaneous Information. Thermal protection circuitry turns off all output drivers should the junction temperature reach +165 °C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Normal operation is resumed when the junction temperature has decreased about 15°C.

The A3966 current control employs a fixed-frequency, variable duty cycle PWM technique. As a result, the current-control regulation may become unstable if the duty cycle exceeds 50%.

To minimize current-sensing inaccuracies caused by ground trace I_R drops, each current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the $I \times R$ drops in the printed-wiring board can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_S .

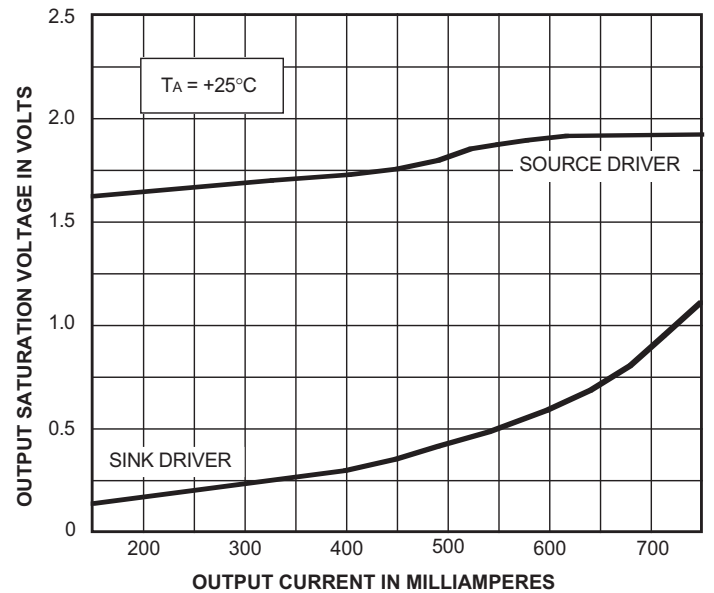
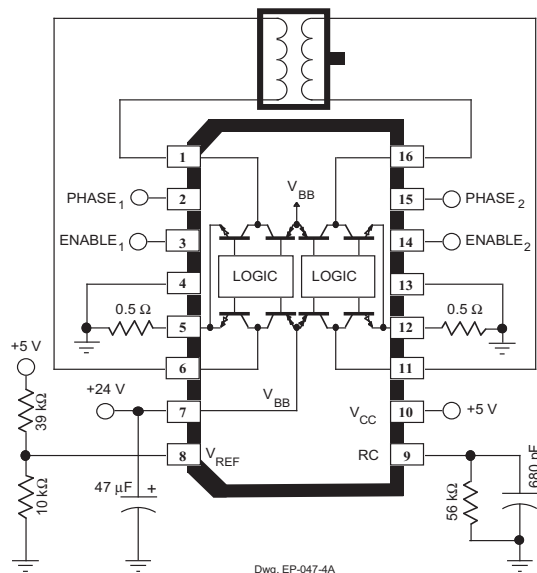
The LOAD SUPPLY terminal, V_{BB} , should be decoupled with an electrolytic capacitor (47 μF recommended) placed as close to the device as physically practical. To minimize the effect of system ground $I \times R$ drops on the logic and reference input signals, the system ground should have a low-resistance return to the load supply voltage.

The frequency of the clock oscillator will determine the amount of ripple current. A lower frequency will result in higher current ripple, but reduced heating in the motor and driver IC due to a corresponding decrease in hysteretic core losses and switching losses respectively. A higher frequency will reduce ripple current, but will increase switching losses and EMI.

3966 DUAL FULL-BRIDGE PWM MOTOR DRIVER

Typical output saturation
voltages showing Satlington
sink-driver operation.

TYPICAL APPLICATION (A3966SLB)



Dwg. GP-064-1A

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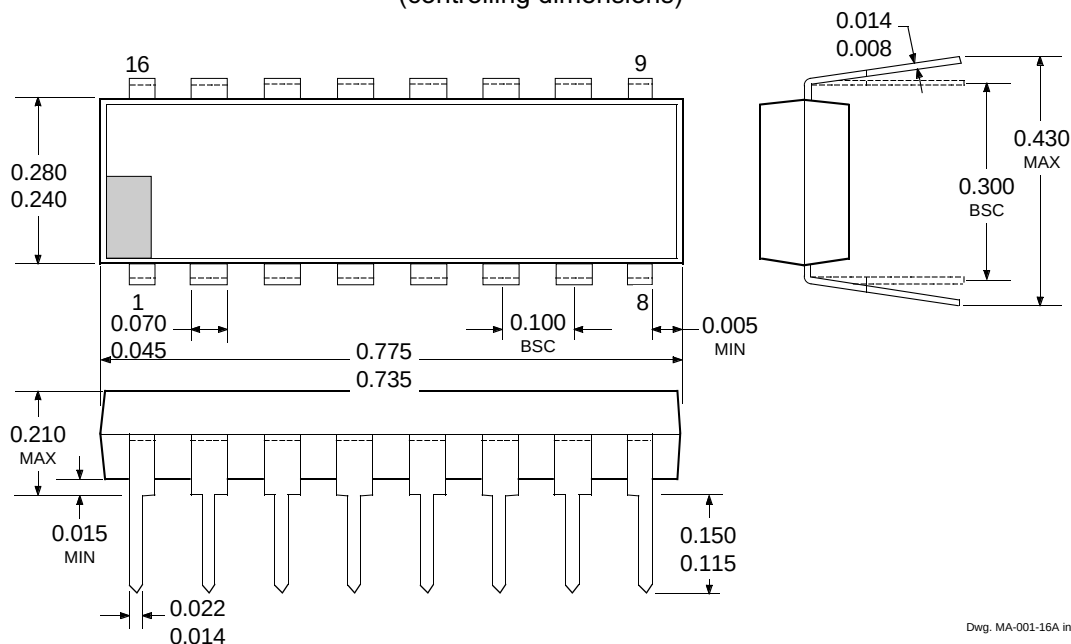
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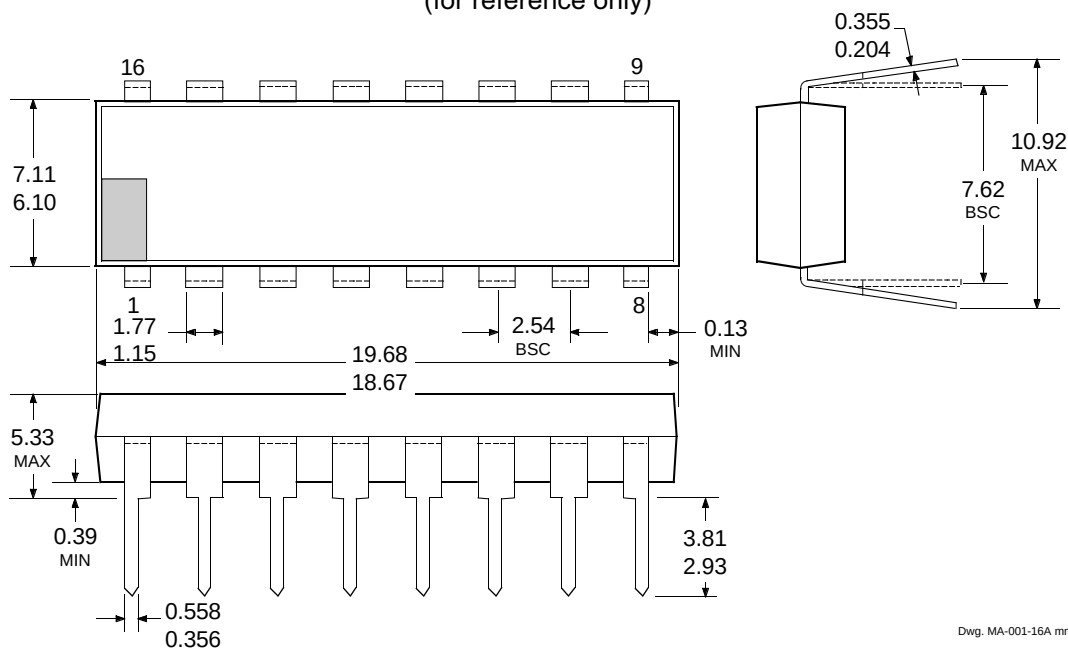
3966 DUAL FULL-BRIDGE PWM MOTOR DRIVER

A3966SA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



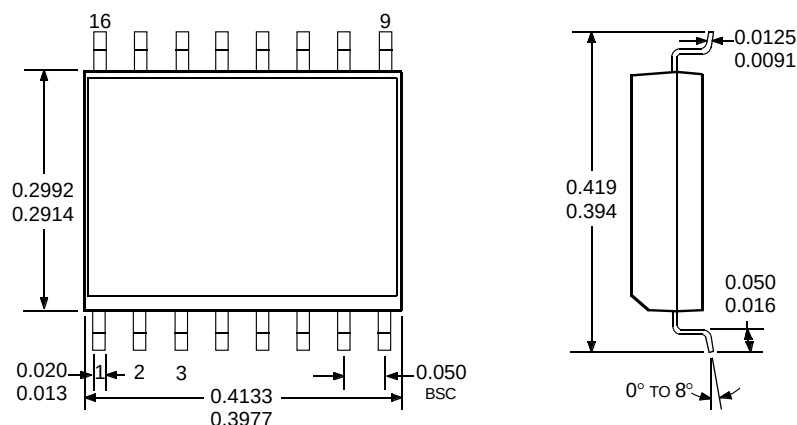
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 25 devices.

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DUAL FULL-BRIDGE PWM MOTOR DRIVER

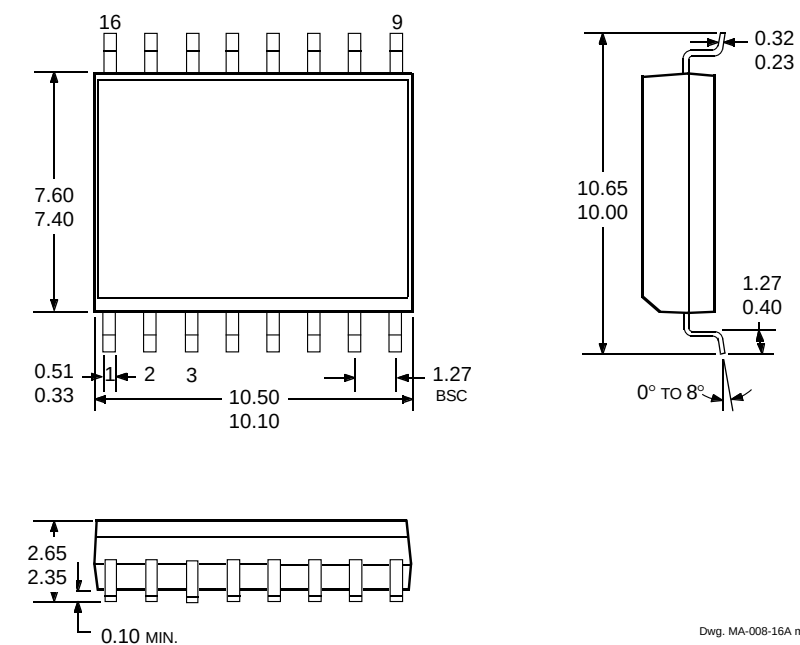
A3966SLB

Dimensions in Inches
(for reference only)



Dwg. MA-008-16A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-16A mm

- NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Webbed lead frame. Leads 4 and 13 are internally one piece.
 4. Supplied in standard sticks/tubes of 47 devices or add "TR" to part number for tape and reel.