64K-bit 2-WIRE SERIAL EEPROM

Description

The EC24C64B provides 65,536 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

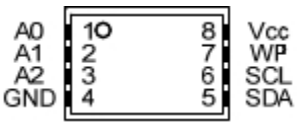
- Low Operation Voltage： V_{CC} = 1.7V to 5.5V
- Internally Organized.. 8192x8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (2.5V~5.5V) and 400 kHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-byte Page Write Modes(Partial Page Writes are Allowed)
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 40 Years
- TDFN-8 packages(RoHS compliant and Halogen-free)

Pin Description

Pin Name	Functions
A0 - A2	Devices Address Inputs
SDA	Serial Data Input / Output
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
Vcc	Power Supply

Pin Configuration

TDFN-8



Top View

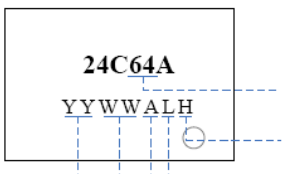
Ordering Information

EC24C64BN XX X X

- R = Tape Reel
- T = Tube
- G = Green
- Package : **F2=TDFN-8**

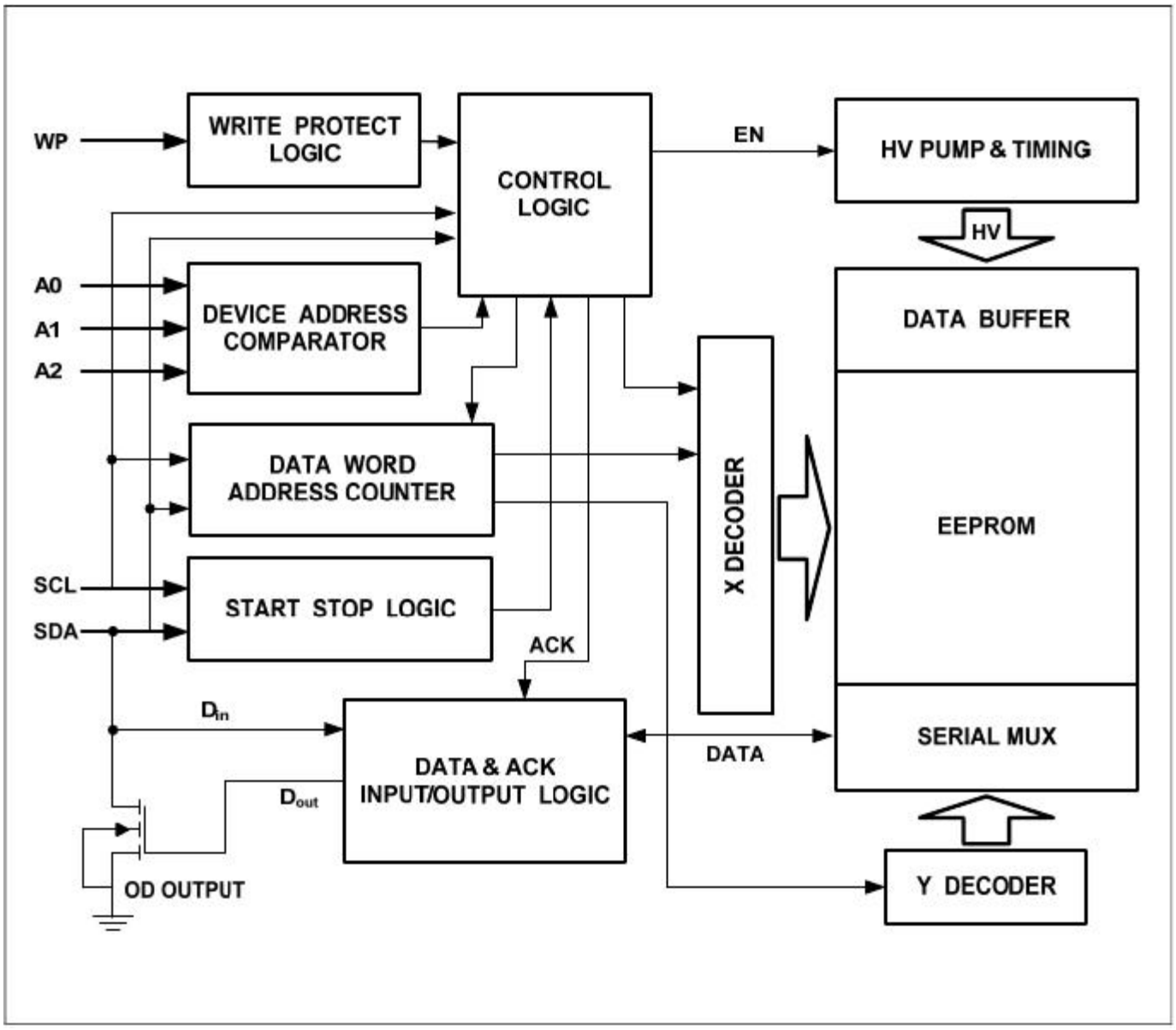
Marking Information

TDFN8



- **Product Density**
- **HSF ID Code**
  G = ROHS Compliant, Halogen-free, Antimony-free
- **Lot Number（just with 0~9、A~Z）**
- **Assembly's Code**
- **Work week during which the products was molded (eg..week 12)**
- **The last two digits of the year In which the products was seal / molded.**

Figure 1. Block Diagram



Pin Descriptions

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other EC24C64B devices. When the pins are hardwired, as many as eight 64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF, if coupling is >3pF, ECMOS recommends connecting the address pins to GND.

WRITE PROTECT (WP): The EC24C64B has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, ECMOS recommends connecting the WP to GND. Switching WP to VCC prior to a write operation creates a software write protected function.

Write Protect Description

WP Pin Status	Part of the Memory Protected
	EC24C64B
WP=V_{CC}	Full (64K) Memory
WP=GND	Normal Read/Write Operations

Memory Organization

EC24C64B, 64K SERIAL EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE: All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

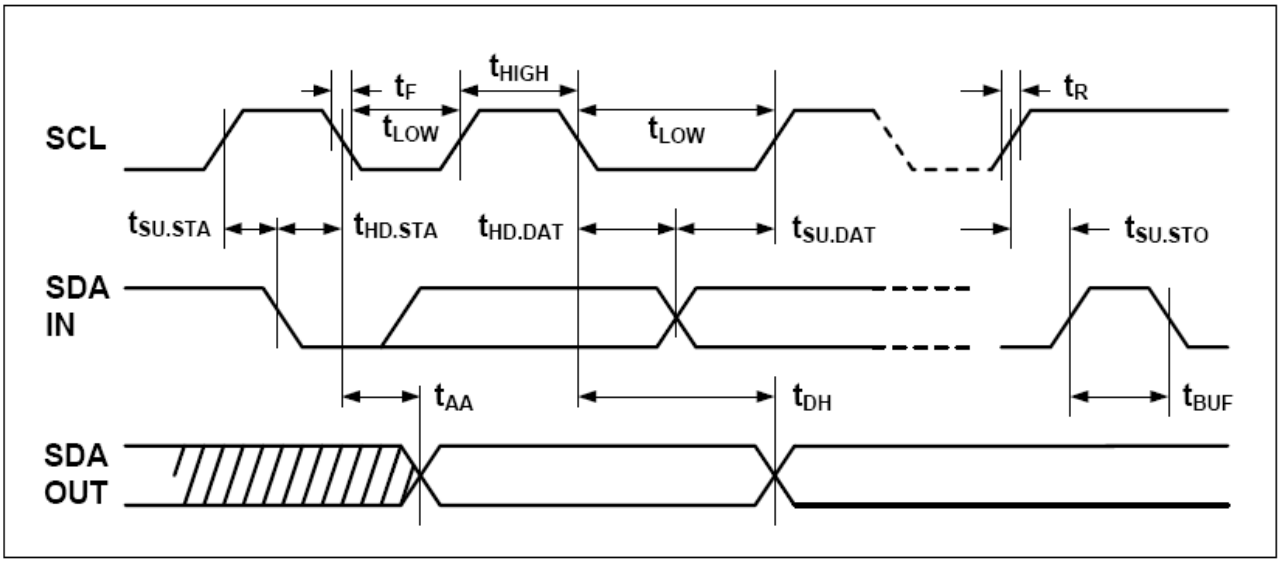
STANDBY MODE: The EC24C64B features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles.
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

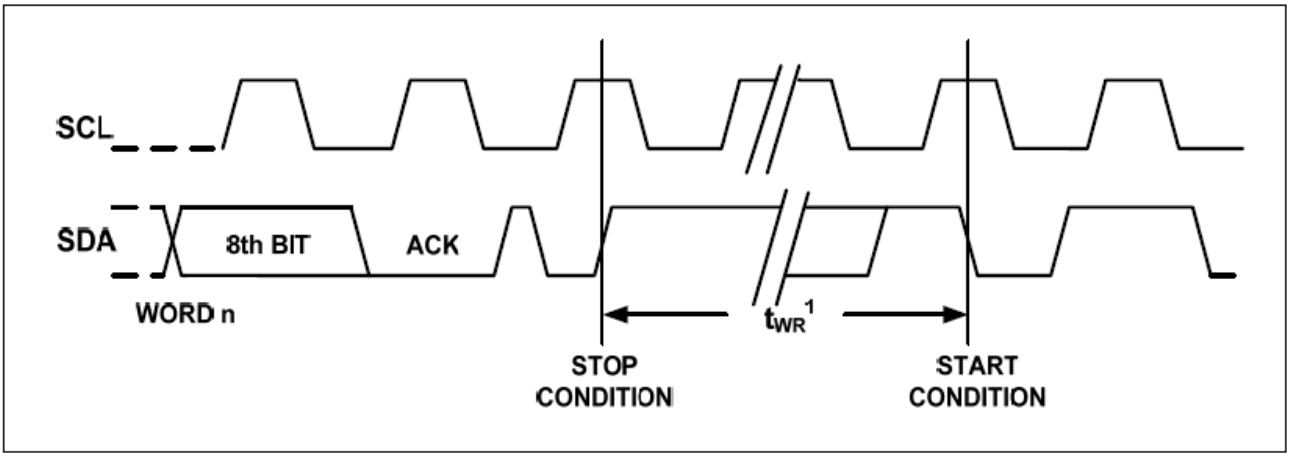
Bus Timing

Figure 2 · SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 3 · SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4 · Data Validity

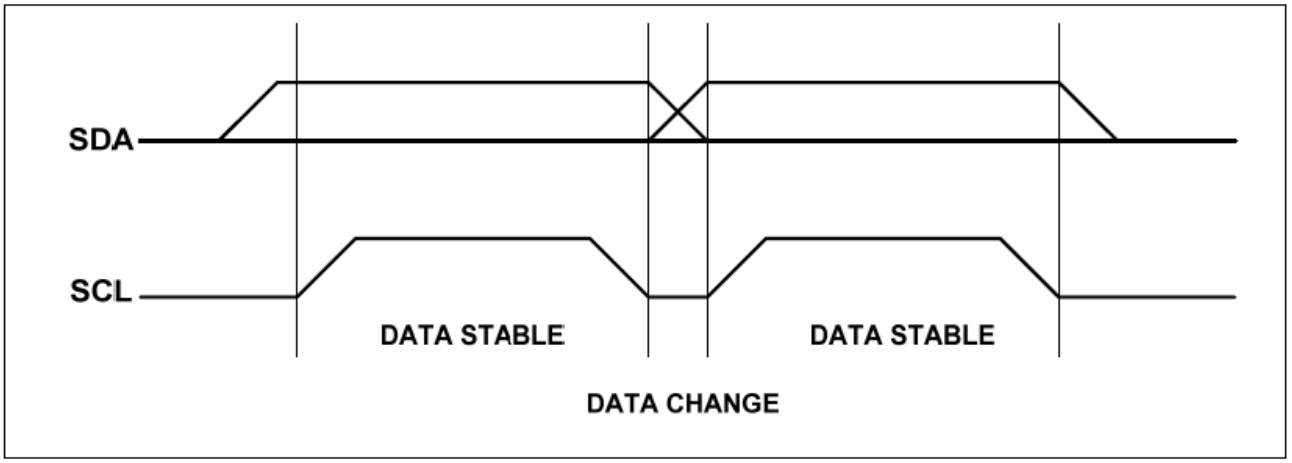


Figure 5 · Start and Stop Definition

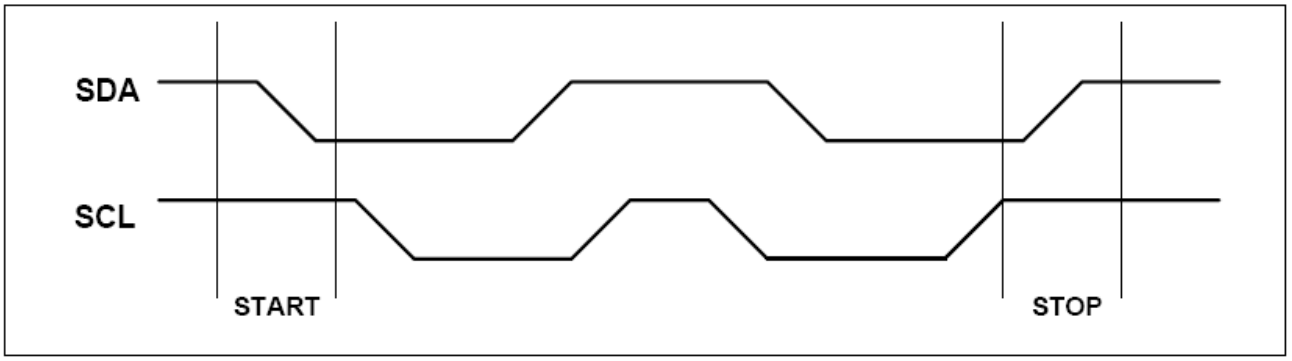
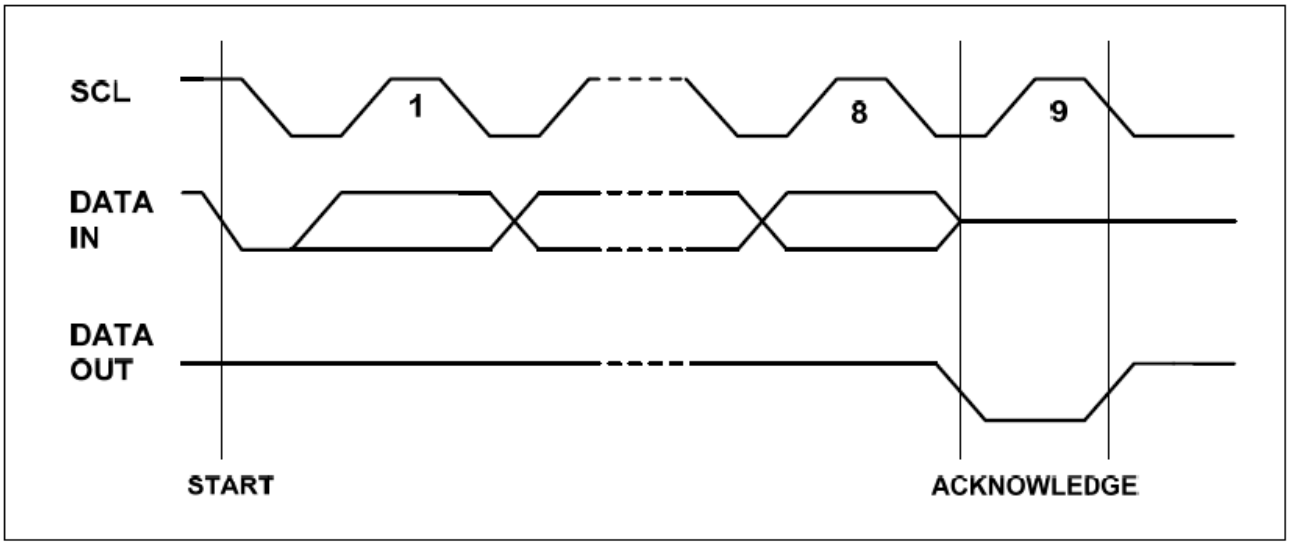


Figure 6 · Output Acknowledge



Device Addressing

The 64K EEPROM device requires a 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 7).
The device address word consists of a mandatory one,zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.
The 64K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard wired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.The Module package device address word also consists of a mandatory one, zero sequence for the first four most significant bits. The next 3 bits are all zero.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: The EC24C64B has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 8).

PAGE WRITE: The 64K EEPROM is capable of 32-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31more data words. The EEPROM will respond with a zero after each data word received.The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 9).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data wordaddressbits are not incremented, retaining the memory page row location.When the word address,internally generated,reaches the page boundary,the following byte is placed at the beginning of the same page.If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word.The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation,incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 10).

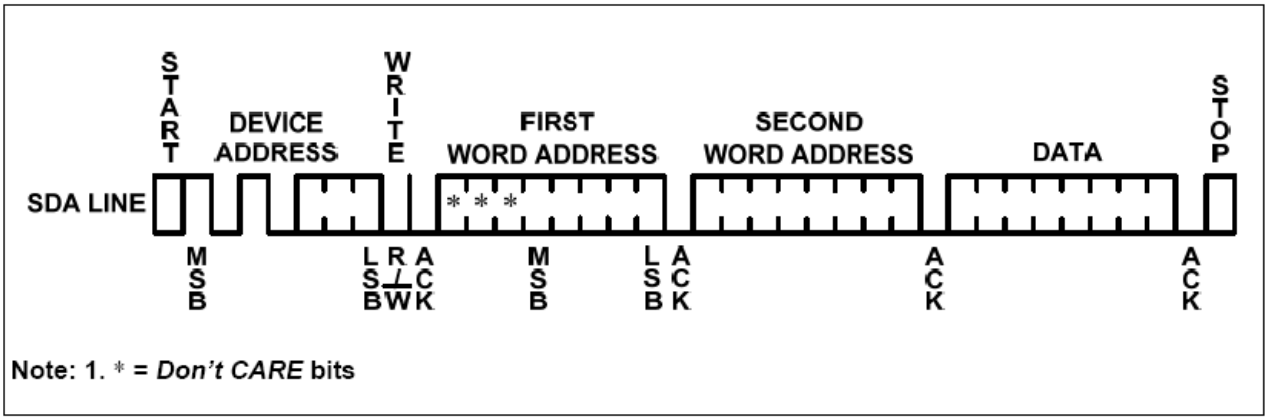
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 12).

Figure 7 · Device Address

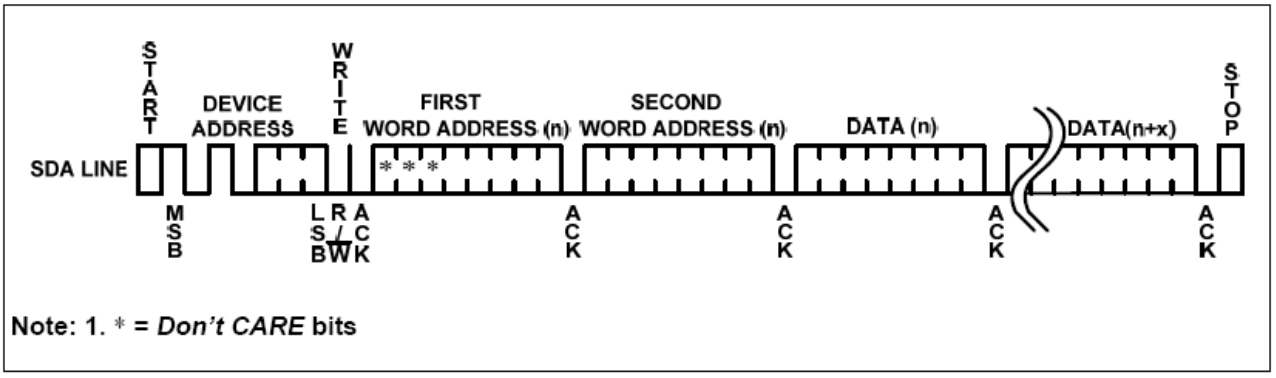
Plastic Package	1	0	1	0	A_2	A_1	A_0	R/W
	MSB							LSB
Module Package	1	0	1	0	0	0	0	R/W

Figure 8 · Byte Write



Note: 1. * = *Don't CARE* bits

Figure 9 · Page Write



Note: 1. * = *Don't CARE* bits

Figure 10 · Current Address Read

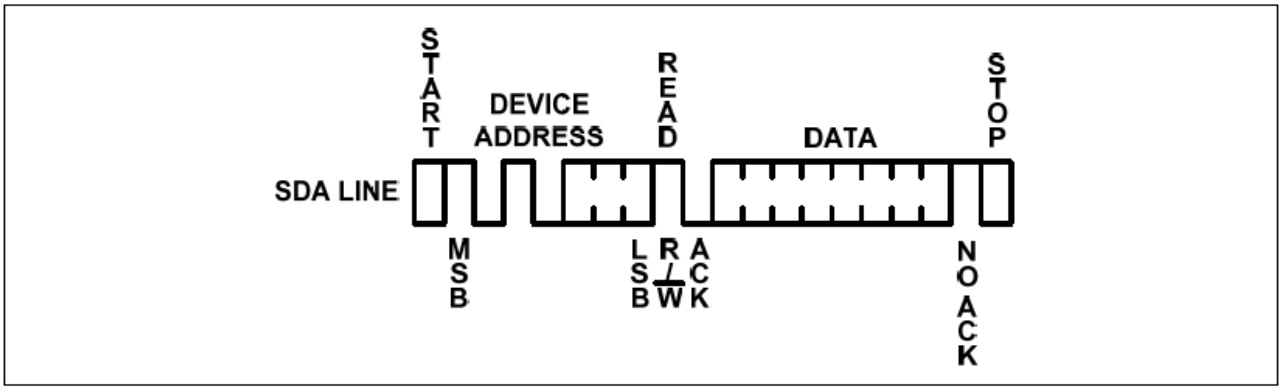
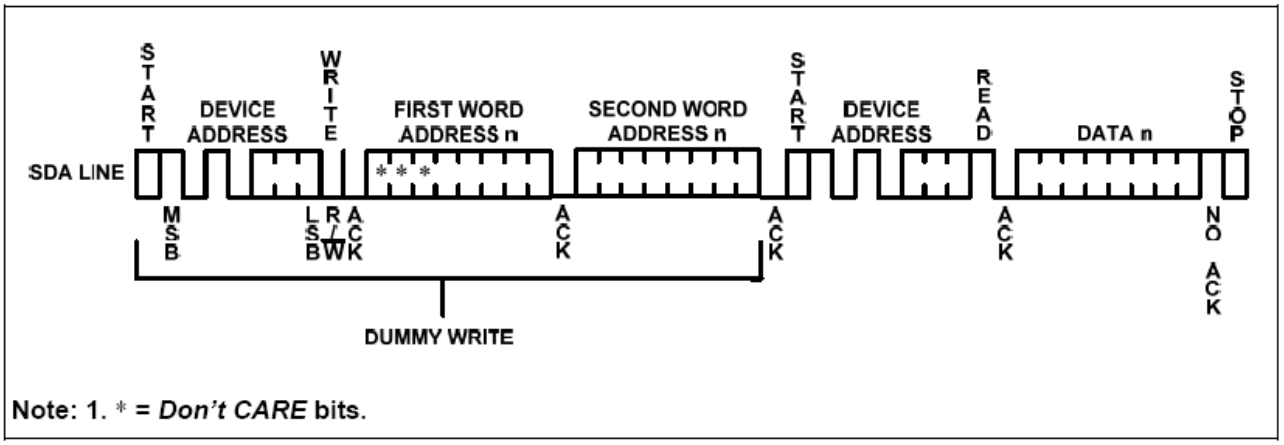
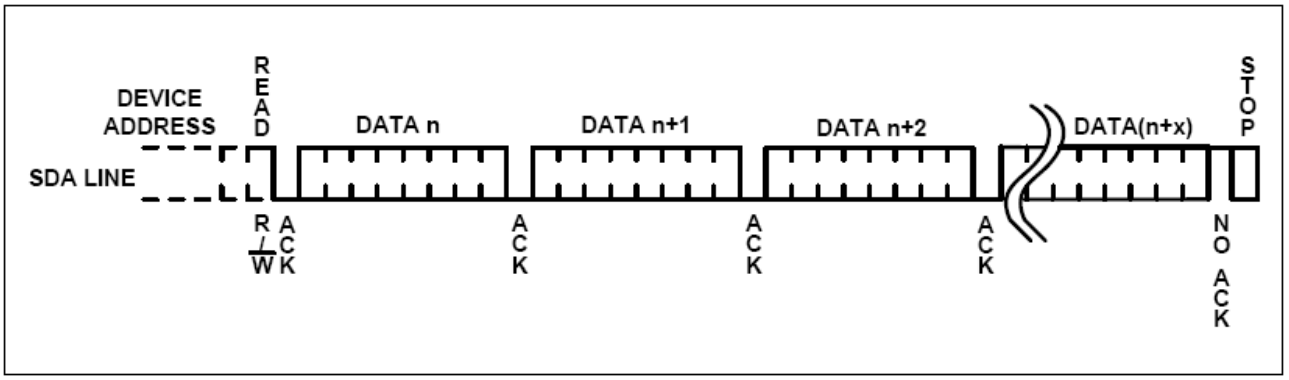


Figure 11 · Random Read



Note: 1. * = *Don't CARE* bits.

Figure 12 · Sequential Read



Electrical Characteristics

Operating Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute MaximumRatings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{CC}	1.7		5.5	V	
Supply Current V_{CC} = 5.0V	I_{CC1}		0.4	1.0	mA	READ at 400 kHz
Supply Current V_{CC} = 5.0V	I_{CC2}		2.0	3.0	mA	WRITE at 400 kHz
Standby Current V_{CC}=1.7V	I_{SB1}			1.0	μA	V_{IN} = V_{CC} or GND
Standby Current V_{CC}=5.5V	I_{SB2}			6.0	uA	V_{IN} = V_{CC} or GND
Input Leakage Current	I_{LI}		0.1	3.0	μA	V_{IN} = V_{CC} or GND
Output Leakage Current	I_{LO}		0.05	3.0	μA	V_{OUT} = V_{CC} or GND
Input Low Level	V_{IL}(1)	-0.6		V_{CC} x 0.3	V	
Input High Level	V_{IH}(1)	V_{CC} x 0.7		V_{CC} + 0.5	V	
Output Low Level V_{CC} =3.0V	V_{OL2}			0.4	V	I_{OL} = 2.1 mA
Output Low Level V_{CC} =1.7V	V_{OL1}			0.2	V	I_{OL} = 0.15 mA

Note (1):V_{IL} min and V_{IH} max are reference only and are not tested

Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.7V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input/Output Capacitance (SDA)	$C_{I/O}$(2)	-	-	8	pF	$V_{I/O}$ = 0V
Input Capacitance (A0, A1, A2, SCL)	C_{IN}(2)	-	-	6	pF	V_{IN} = 0V

Note(2):This parameter is characterized and is not 100% tested.

AC Electrical Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, C_L = 100 pF (unless otherwise noted). Test Condition are listed Note2.

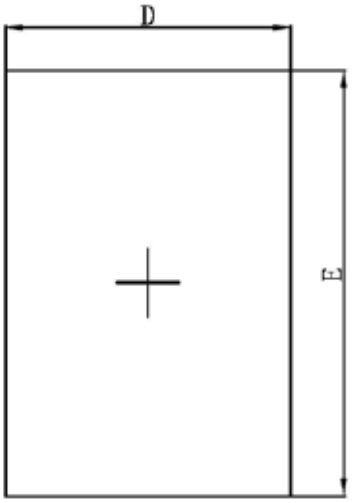
Parameter	Symbol	V_{CC}=1.7V		V_{CC}=2.5V		V_{CC}=5.5V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency, SCL	f_{SCL}	-	400		1000	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.3	-	0.45		0.4	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	0.45		0.4	-	μs
Noise Suppression Time[1]	t_I	-	100		50	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.02	0.9	0.02	0.55	0.02	0.55	μs
Time the bus must be free before a new transmission can start	t_{BUF}[1]	1.3	-	0.5		0.5	-	μs
Start Hold Time	$t_{HD.STA}$	0.6	-	0.25		0.25	-	μs
Start Setup Time	$t_{SU.STA}$	0.6	-	0.25		0.25	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	0		0	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	100		100	-	ns
Inputs Rise Time[1]	t_R	-	0.3		0.3	-	0.3	μs
Inputs Fall Time[1]	t_F	-	300		100	-	100	ns
Stop Setup Time	$t_{SU.STO}$	0.6	-	0.25		0.25	-	μs
Data Out Hold Time	t_{DH}	20	-	20		20	-	ns
Write Cycle Time	t_{WR}	-	5		5	-	5	ms
3.3V, 25°C, Page Mode	Endurance[1]	1M					-	Write Cycles

Note

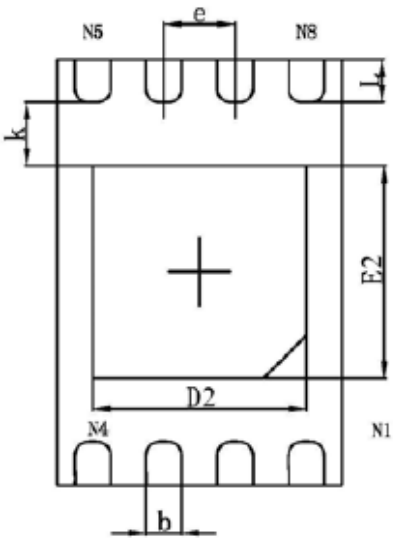
1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3kΩ
   Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   Input rise and fall time: ≦50 ns
   Input and output timing reference voltages: 0.5 x V_{CC}

Mechanical Dimensions

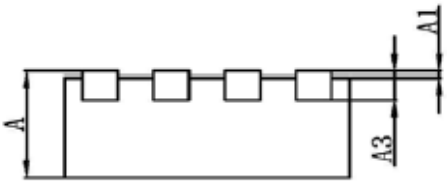
OUTLINE DRAWING TDFN-8



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
A3	0.203(REF)	
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.60
k	0.200(MIN)	
b	0.200	0.300
e	0.500(TYP)	
L	0.200	0.400

NOTE:

1. Dimensions are in Millimeters.