TFP401x TI *PanelBus*™ Digital Receiver

1 Features

- Supports Pixel Rates up to 165 MHz (Including 1080p and WUXGA at 60 Hz)
- Digital Visual Interface (DVI) Specification Compliant (1)
- True-Color, 24-Bit/Pixel, 16.7M Colors at 1 or 2 Pixels per Clock
- Laser Trimmed Internal Termination Resistors for Optimum Fixed Impedance Matching
- Skew Tolerant up to One Pixel-Clock Cycle
- 4× Oversampling
- Reduced Power Consumption – 1.8-V Core Operation With 3.3-V I/Os and Supplies (2)
- Reduced Ground Bounce Using Time-Staggered Pixel Outputs
- Low Noise and Good Power Dissipation Using TI PowerPAD™ Packaging
- Advanced Technology Using TI 0.18-µm EPIC-5 CMOS Process
- TFP401A Incorporates HSYNC Jitter Immunity (3)

(1) The Digital Visual Interface Specification, DVI, is an industry standard developed by the Digital Display Working Group (DDWG) for high-speed digital connection to digital displays. The TPF401 and TFP401A are compliant with the DVI Specification Rev. 1.0.

(2) The TFP401/401A has an internal voltage regulator that provides the 1.8-V core power supply from the external 3.3-V supplies.

(3) The TFP401A incorporates additional circuitry to create a stable HSYNC from DVI transmitters that introduce undesirable jitter on the transmitted HSYNC signal.

2 Applications

- High-Definition TV
- HD PC Monitors
- Digital Video
- HD Projectors
- DVI/HDMI Receivers (HDMI Video-Only)

3 Description

The Texas Instruments TFP401 and TFP401A are TI *PanelBus*™ flat-panel display products, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions. Targeted primarily at desktop LCD monitors and digital projectors, the TFP401/401A finds applications in any design requiring high-speed digital interface.

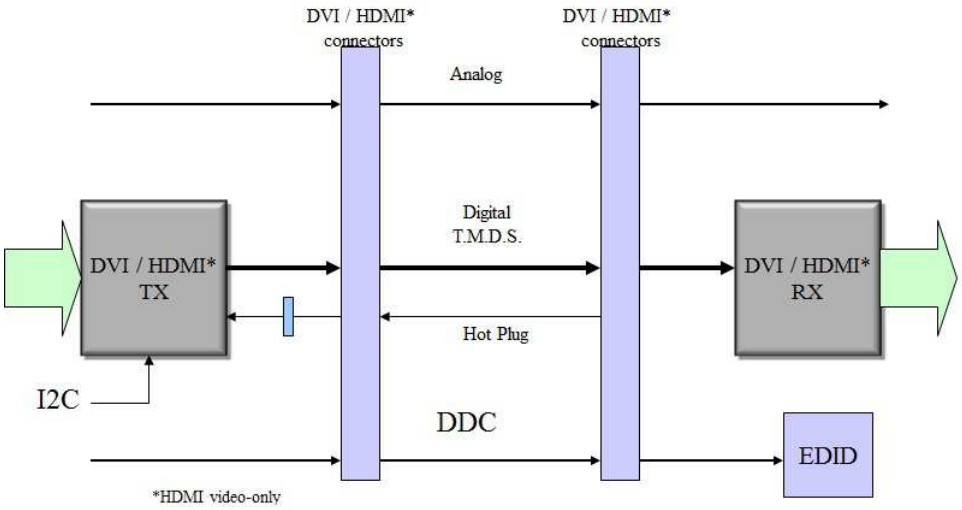
The TFP401 and TFP401A supports display resolutions up to 1080p and WUXGA in 24-bit true-color pixel format. The TFP401/401A offers design flexibility to drive one or two pixels per clock, supports TFT or DSTN panels, and provides an option for time-staggered pixel outputs for reduced ground bounce.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TFP401	HTQFP (100)	14.00 mm × 14.00 mm
TFP401A		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TFP401 Diagram



Copyright © 2016, Texas Instruments Incorporated

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (Continued) ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 6
7.1 Absolute Maximum Ratings ... 6
7.2 ESD Ratings ... 6
7.3 Recommended Operating Conditions ... 6
7.4 Thermal Information ... 6
7.5 DC Digital I/O Electrical Characteristics ... 7
7.6 DC Electrical Characteristics ... 7
7.7 AC Electrical Characteristics ... 7
7.8 Typical Characteristics ... 9
8 Parameter Measurement Information ... 10
9 Detailed Description ... 12
9.1 Overview ... 12
9.2 Functional Block Diagram ... 12
9.3 Feature Description ... 12
9.4 Device Functional Modes ... 15
10 Applications and Implementation ... 17
10.1 Application Information ... 17
10.2 Typical Application ... 17
11 Power Supply Recommendations ... 21
12 Layout ... 21
12.1 Layout Guidelines ... 21
12.2 Layout Example ... 22
13 Device and Documentation Support ... 25
13.1 Related Links ... 25
13.2 Trademarks ... 25
13.3 Electrostatic Discharge Caution ... 25
13.4 Glossary ... 25
14 Mechanical, Packaging, and Orderable Information ... 25
14.1 TI PowerPAD 100-TQFP Package ... 25

4 Revision History

Changes from Revision F (February 2015) to Revision G **Page**

- Added $t_{WL(PDL_MIN)}$ and t_{DEL} to the *AC Electrical Characteristics* table ... 8

Changes from Revision E (July 2013) to Revision F **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Copyright © 2000–2016, Texas Instruments Incorporated

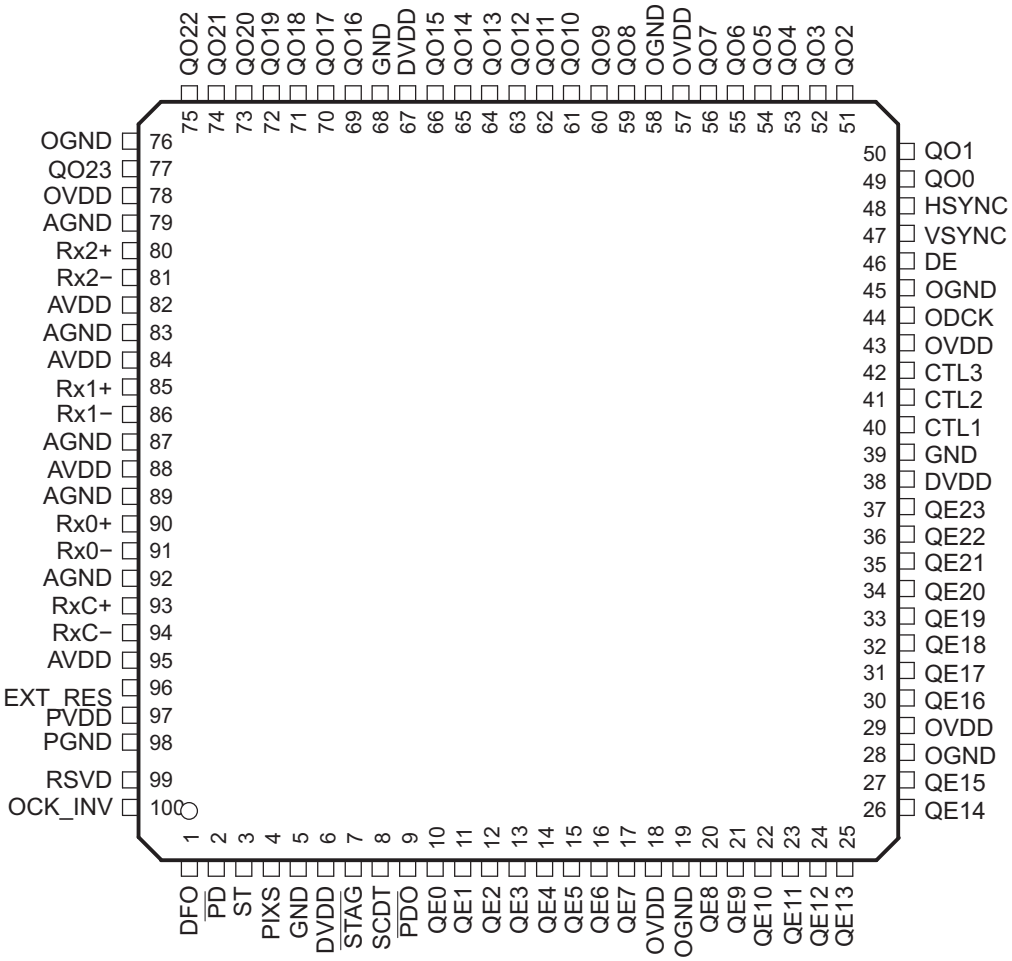
5 Description (Continued)

PowerPAD advanced packaging technology results in best-of-class power dissipation, footprint, and ultralow ground inductance.

The TFP401 and TFP401A combines *PanelBus* circuit innovation with TI's advanced 0.18-µm EPIC-5 CMOS process technology, along with TI PowerPAD package technology to achieve a reliable, low-powered, low-noise, high-speed digital interface solution.

6 Pin Configuration and Functions

PZP Package
100-Pin HTQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	79, 83, 87, 89, 92	GND	Analog ground – Ground reference and current return for analog circuitry
AV_{DD}	82, 84, 88, 95	V_{DD}	Analog V_{DD} – Power supply for analog circuitry. Nominally 3.3 V
CTL[3:1]	42, 41, 40	DO	General-purpose control signals – Used for user-defined control. CTL1 is not powered down via $\overline{PDO}$.
DE	46	DO	Output data enable – Used to indicate time of active video display versus non-active display or blank time. During blank, only HSYNC, VSYNC, and CTL[3:1] are transmitted. During times of active display, or non-blank, only pixel data, QE[23:0], and QO[23:0] are transmitted. High: Active display time Low: Blank time

Copyright © 2000–2016, Texas Instruments Incorporated

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DFO	1	DI	Output clock data format – Controls the output clock (ODCK) format for either TFT or DSTN panel support. For TFT support, the ODCK clock runs continuously. For DSTN support, ODCK only clocks when DE is high; otherwise, ODCK is held low when DE is low. High: DSTN support/ODCK held low when DE = low Low: TFT support/ODCK runs continuously.
DGND	5, 39, 68	GND	Digital ground – Ground reference and current return for digital core
DV_{DD}	6, 38, 67	V_{DD}	Digital V_{DD} – Power supply for digital core. Nominally 3.3 V
EXT_RES	96	AI	Internal impedance matching – The TFP401/401A is internally optimized for impedance matching at 50 Ω. An external resistor tied to this pin has no effect on device performance.
HSYNC	48	DO	Horizontal sync output
RSVD	99	DI	Reserved. Must be tied high for normal operation
OV_{DD}	18, 29, 43, 57, 78	V_{DD}	Output driver V_{DD} – Power supply for output drivers. Nominally 3.3 V
ODCK	44	DO	Output data clock – Pixel clock. All pixel outputs QE[23:0] and QO[23:0] (if in 2-pixel/clock mode), along with DE, HSYNC, VSYNC and CTL[3:1], are synchronized to this clock.
OGND	19, 28, 45, 58, 76	GND	Output driver ground – Ground reference and current return for digital output drivers
OCK_INV	100	DI	ODCK polarity – Selects ODCK edge on which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL[3:1]) are latched. Normal mode: High: Latches output data on rising ODCK edge Low: Latches output data on falling ODCK edge
$\overline{PD}$	2	DI	Power down – An active-low signal that controls the TFP401/401A power-down state. During power down, all output buffers are switched to a high-impedance state. All analog circuits are powered down and all inputs are disabled, except for $\overline{PD}$. If $\overline{PD}$ is left unconnected, an internal pullup defaults the TFP401/401A to normal operation. High : Normal operation Low: Power down
$\overline{PDO}$	9	DI	Output drive power down – An active-low signal that controls the power-down state of the output drivers. During output drive power down, the output drivers (except SCDT and CTL1) are driven to a high-impedance state. When $\overline{PDO}$ is left unconnected, an internal pullup defaults the TFP401/401A to normal operation. High: Normal operation/output drivers on Low: Output drive power down
PGND	98	GND	PLL GND – Ground reference and current return for internal PLL
PIXS	4	DI	Pixel select – Selects between one- and two-pixels-per-clock output modes. During the 2-pixel/clock mode, both even pixels, QE[23:0], and odd pixels, QO[23:0], are output in tandem on a given clock cycle. During 1-pixel/clock, even and odd pixels are output sequentially, one at a time, with the even pixel first, on the even pixel bus, QE[23:0]. (The first pixel per line is pixel-0, the even pixel. The second pixel per line is pixel-1, the odd pixel). High: 2-pixel/clock Low: 1-pixel/clock
PV_{DD}	97	V_{DD}	PLL V_{DD} – Power supply for internal PLL
QE[8:15]	20–27	DO	Even green-pixel output – Output for even and odd green pixels when in 1-pixel/clock mode. Output for even-only green pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE8/pin 20 MSB: QE15/pin 27
QE[16:23]	30–37	DO	Even red-pixel output – Output for even and odd red pixels when in 1-pixel/clock mode. Output for even-only red pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE16/pin 30 MSB: QE23/pin 37
QO[0:7]	49–56	DO	Odd blue-pixel output – Output for odd-only blue pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO0/pin 49 MSB: QO7/pin 56

Copyright © 2000–2016, Texas Instruments Incorporated

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
QO[8:15]	59–66	DO	Odd green-pixel output – Output for odd-only green pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO8/pin 59 MSB: QO15/pin 66
QO[16:23]	69–75, 77	DO	Odd red-pixel output – Output for odd-only red pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO16/pin 69 MSB: QO23/pin 77
QE[0:7]	10–17	DO	Even blue-pixel output – Output for even and odd blue pixels when in 1-pixel/clock mode. Output for even-only blue pixel when in 2-pixel per clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE0/pin 10 MSB: QE7/pin 17
RxC+	93	AI	Clock positive receiver input – Positive side of reference clock. TMDS low-voltage signal differential input pair
RxC–	94	AI	Clock negative receiver input – Negative side of reference clock. TMDS low-voltage signal differential input pair
Rx0+	90	AI	Channel-0 positive receiver input – Positive side of channel-0. TMDS low-voltage signal differential input pair. Channel-0 receives blue pixel data in active display and HSYNC, VSYNC control signals in blank.
Rx0–	91	AI	Channel-0 negative receiver input – Negative side of channel-0. TMDS low-voltage signal differential input pair
Rx1+	85	AI	Channel-1 positive receiver input – Positive side of channel-1 TMDS low-voltage signal differential input pair Channel-1 receives green-pixel data in active display and CTL1 control signals in blank.
Rx1–	86	AI	Channel-1 negative receiver input – Negative side of channel-1 TMDS low-voltage signal differential input pair
Rx2+	80	AI	Channel-2 positive receiver input – Positive side of channel-2 TMDS low-voltage signal differential input pair Channel-2 receives red-pixel data in active display and CTL2, CTL3 control signals in blank.
Rx2–	81	AI	Channel-2 negative receiver input – Negative side of channel-2 TMDS low-voltage signal differential input pair
SCDT	8	DO	Sync detect - Output to signal when the link is active or inactive. The link is considered to be active when DE is actively switching. The TFP401/401A monitors the state of DE to determine link activity. SCDT can be tied externally to $\overline{\text{PDO}}$ to power down the output drivers when the link is inactive. High: Active link Low: Inactive link
ST	3	DI	Output drive strength select – Selects output drive strength for high- or low-current drive. (See dc specifications for I_{OH} and I_{OL} vs ST state). High: High drive strength Low: Low drive strength
$\overline{\text{STAG}}$	7	DI	Staggered pixel select – An active-low signal used in the 2-pixel/clock pixel mode (PIXS = high). Time-staggers the even and odd pixel outputs to reduce ground bounce. Normal operation outputs the odd and even pixels simultaneously. High: Normal simultaneous even/odd pixel output Low: Time-staggered even/odd pixel output
VSYNC	47	DO	Vertical sync output

Copyright © 2000–2016, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
DV_{DD}, AV_{DD}, OV_{DD}, PV_{DD}	Supply voltage		–0.3	4	V
V_I	Input voltage range, logic/analog signals		–0.3	4	V
	Operating ambient temperature		0	70	°C
	Package power dissipation/PowerPAD package	Soldered(2)		4.3	W
		Not soldered(3)		2.7	
	JEDEC latchup (EIA/JESD78)			100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Specified with PowerPAD bond pad on the backside of the package soldered to a 2-oz. (0.071-mm thick) Cu plate PCB thermal plane. Specified at maximum allowed operating temperature, 70°C.
(3) PowerPAD bond pad on the backside of the package is not soldered to a thermal plane. Specified at maximum allowed operating temperature, 70°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD} (DV_{DD}, AV_{DD}, PV_{DD}, OV_{DD})	Supply voltage	3	3.3	3.6	V
t_{pix} (1)	Pixel time	6.06		40	ns
R_t	Single-ended analog-input termination resistance	45	50	55	Ω
T_A	Operating free-air temperature	0	25	70	°C

(1) t_{pix} is the pixel time defined as the period of the RxC clock input. The period of the output clock, ODCK is equal to tpix when in 1-pixel/clock mode and $2t_{pix}$ when in 2-pixel/clock mode.

7.4 Thermal Information

THERMAL METRIC(1)		TFP401, TFP401A PZP (HTQFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2000–2016, Texas Instruments Incorporated

7.5 DC Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level digital input voltage(1)		2		DV_{DD}	V
V_{IL}	Low-level digital input voltage(1)		0		0.8	V
I_{OH}	High-level output drive current(2)	ST = high, V_{OH} = 2.4 V	5	10	14	mA
		ST = low, V_{OH} = 2.4 V	3	6	9	
I_{OL}	Low-level output drive current(2)	ST = high, V_{OL} = 0.8 V	10	13	19	mA
		ST = low, V_{OL} = 0.8 V	5	7	11	
I_{OZ}	Hi-Z output leakage current	$\overline{PD}$ = low or $\overline{PDO}$ = low	–1		1	µA

(1) Digital inputs are labeled DI in I/O column of Terminal Functions table.
(2) Digital outputs are labeled DO in I/O column of Terminal Functions table.

7.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Analog input differential voltage(1)		75		1200	mV
V_{IC}	Analog input common-mode voltage(1)		AV_{DD} – 300		AV_{DD} – 37	mV
$V_{I(OC)}$	Open-circuit analog input voltage		AV_{DD} – 10		AV_{DD} + 10	mV
$I_{DD(2PIX)}$	Normal 2-pix/clock power supply current (2)	ODCK = 82.5 MHz, 2-pix/clock			370	mA
I_{PD}	Power-down current (3)	$\overline{PD}$ = low			10	mA
I_{PDO}	Output drive power-down current(3)	$\overline{PDO}$ = low		35		mA

(1) Specified as dc characteristic with no overshoot or undershoot
(2) Alternating 2-pixel black/2-pixel white pattern. ST = high, $\overline{STAG}$ = high, QE[23:0] and QO[23:0] C_L = 10 pF.
(3) Analog inputs are open circuit (transmitter is disconnected from TFP401/401A).

7.7 AC Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ID(2)}$	Differential input sensitivity(1)		150		1560	mV_{p-p}
t_{ps}	Analog input intra-pair (+ to –) differential skew(2)				0.4	t_{bit}(3)
t_{ccs}	Analog input inter-pair or channel-to-channel skew (2)				1	t_{pix}(4)
t_{ijit}	Worst-case differential input clock jitter tolerance(2)(5)		50			ps
t_{f1}	Fall time of data and control signals(6)(7)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{r1}	Rise time of data and control signals(6)(7)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{r2}	Rise time of ODCK clock(6)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{f2}	Fall time of ODCK clock(6)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	

(1) Specified as ac parameter to include sensitivity to overshoot, undershoot and reflection.
(2) By characterization
(3) t_{bit} is 1/10 the pixel time, t_{pix}
(4) t_{pix} is the pixel time defined as the period of the RxC input clock. The period of ODCK is equal to t_{pix} in 1-pixel/clock mode or $2t_{pix}$ when in 2-pixel/clock mode.
(5) Measured differentially at 50% crossing using ODCK output clock as trigger
(6) Rise and fall times measured as time between 20% and 80% of signal amplitude.
(7) Data and control signals are QE[23:0], QO[23:0], DE, HSYNC, VSYNC. and CTL[3:1].

Copyright © 2000–2016, Texas Instruments Incorporated

AC Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su1}	Setup time, data and control signal to falling edge of ODCK	1 pixel/clock, PIXS = low, OCK_INV = low	1.8			ns
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = low	3.8			
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	0.7			
t_{h1}	Hold time, data and control signal to falling edge of ODCK	1 pixel/clock, PIXS = low, OCK_INV = low	0.6			ns
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	2.5			
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = low	2.9			
t_{su2}	Setup time, data and control signal to rising edge of ODCK	1 pixel/clock, PIXS = low, OCK_INV = high	2.1			ns
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = high	4			
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = high	1.5			
t_{h2}	Hold time, data and control signal to rising edge of ODCK	1 pixel/clock, PIXS = low, OCK_INV = high	0.5			ns
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = high	2.4			
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = high	2.1			
f_{ODCK}	ODCK frequency	PIX = low (1-PIX/CLK)	25		165	MHz
		PIX = high (2-PIX/CLK)	12.5		82.5	
	ODCK duty-cycle		40%	50%	60%	
$t_{pd(PDL)}$	Propagation delay time from $\overline{PD}$ low to Hi-Z outputs				9	ns
$t_{pd(PDOL)}$	Propagation delay time from $\overline{PDO}$ low to Hi-Z outputs				9	ns
$t_{t(HSC)}$	Transition time between DE transition to SCDT low(8)			1e6		t_{pix}
$t_{t(FSC)}$	Transition time between DE transition to SCDT high(8)			1600		t_{pix}
$t_{d(st)}$	Delay time, ODCK latching edge to QE[23:0] data output	$\overline{STAG}$ = low, PIXS = high		0.25		t_{pix}
$t_{WL(PDL_MIN)}$	Minimum time $\overline{PD}$ is asserted low		9			ns
t_{DEL}	Minimum DE low		128			Tpixel

(8) Link active or inactive is determined by amount of time detected between DE transitions. SCDT indicates link activity.

Copyright © 2000–2016, Texas Instruments Incorporated

7.8 Typical Characteristics

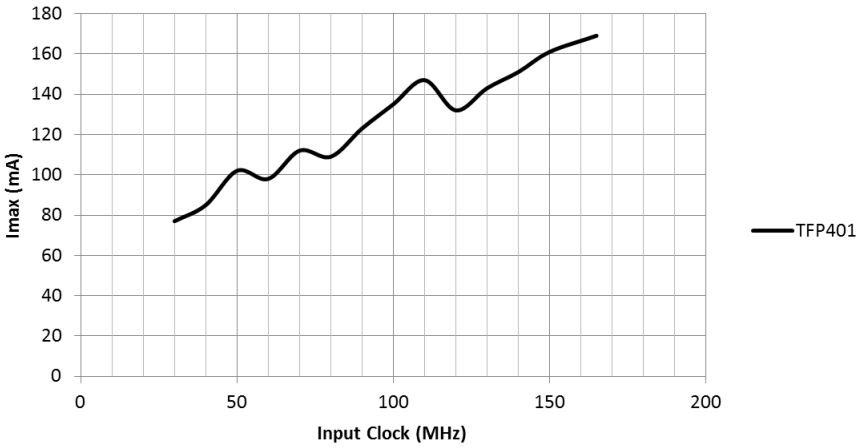


Figure 1. Imax vs Input Frequency

8 Parameter Measurement Information

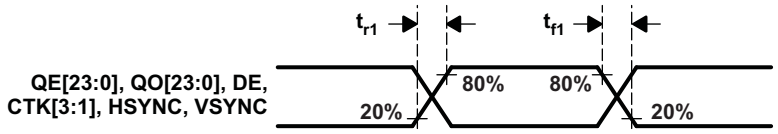


Figure 2. Rise and Fall Times of Data and Control Signals

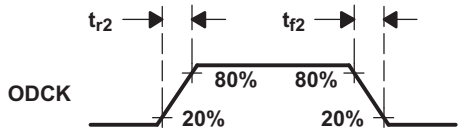


Figure 3. Rise and Fall Times of ODCK

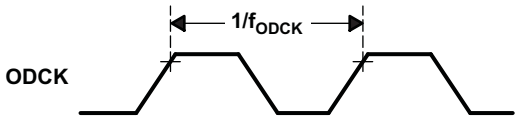


Figure 4. ODCK Frequency

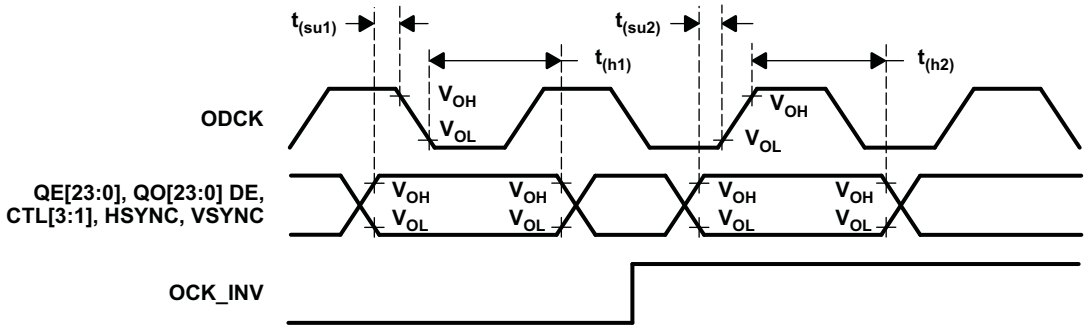


Figure 5. Data Setup and Hold Times to Rising and Falling Edges of ODCK

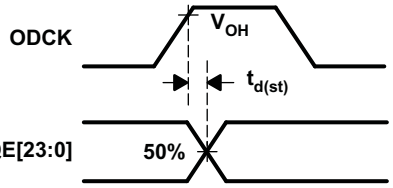


Figure 6. ODCK High to QE[23:0] Staggered Data Output

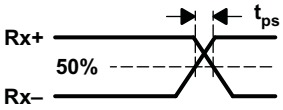


Figure 7. Analog Input Intra-Pair Differential Skew

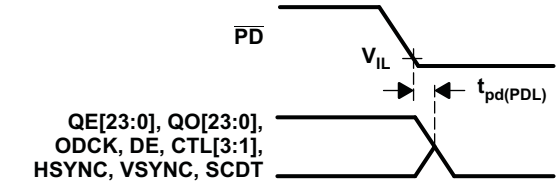


Figure 8. Delay From $\overline{PD}$ Low to Hi-Z Outputs

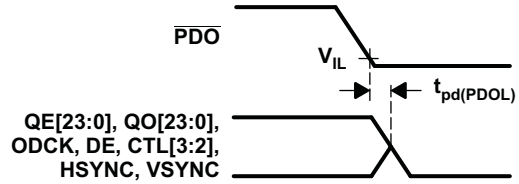


Figure 9. Delay From $\overline{PDO}$ Low to Hi-Z Outputs

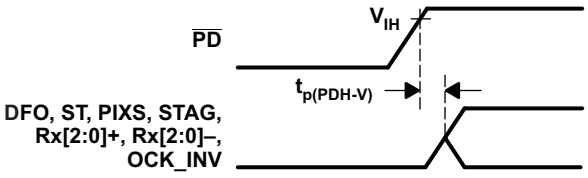


Figure 10. Delay From $\overline{PD}$ Low to High Before Inputs Are Active

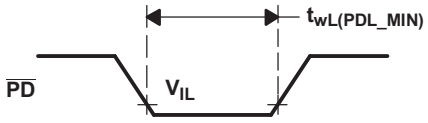


Figure 11. Minimum Time $\overline{PD}$ Low

Copyright © 2000–2016, Texas Instruments Incorporated

Parameter Measurement Information (continued)

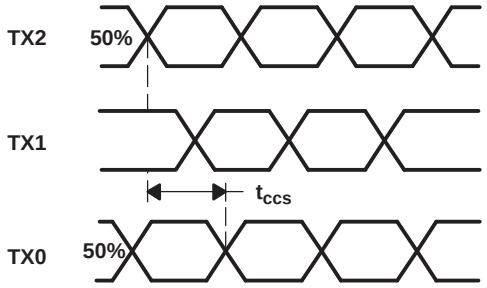


Figure 12. Analog Input Channel-to-Channel Skew

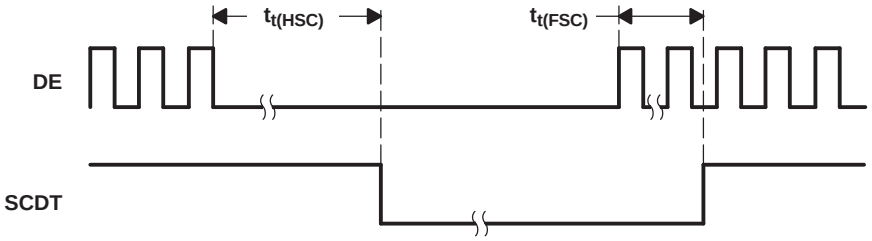


Figure 13. Time Between DE Transitions to SCDT Low and SCDT High

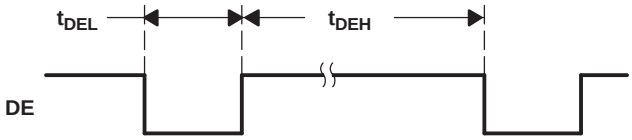


Figure 14. Minimum DE Low and Maximum DE High

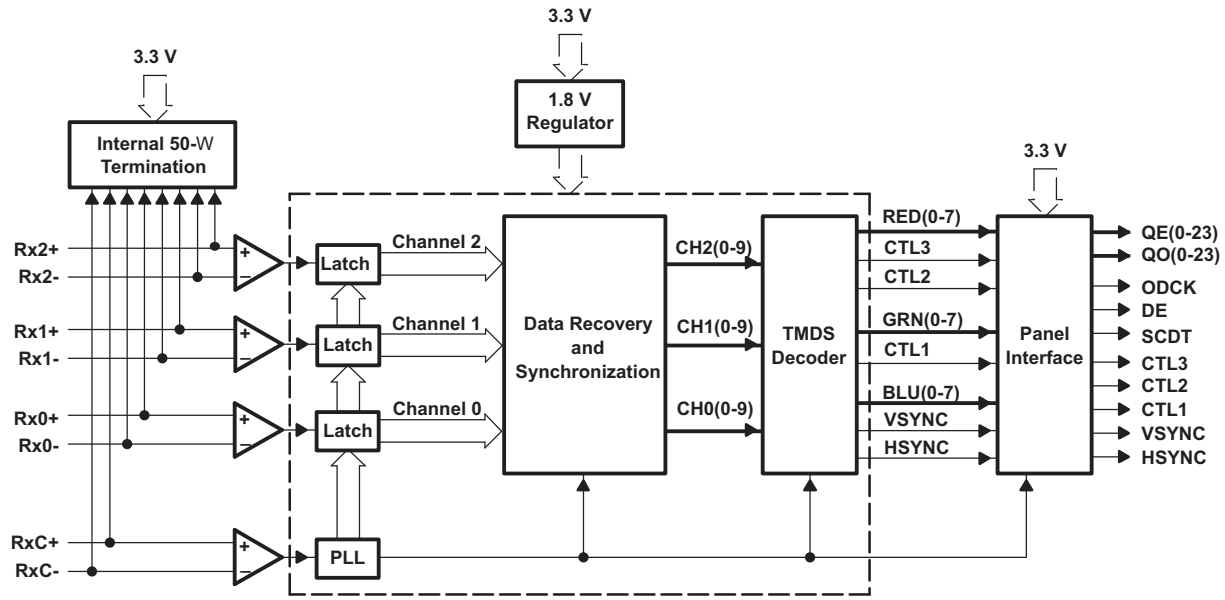
Copyright © 2000–2016, Texas Instruments Incorporated

9 Detailed Description

9.1 Overview

The TFP401/401A is a digital visual interface (DVI)-compliant TMDS digital receiver that is used in digital flat panel display systems to receive and decode TMDS-encoded RGB pixel data streams. In a digital display system a host, usually a PC or workstation, contains a TMDS-compatible transmitter that receives 24-bit pixel data along with appropriate control signals and encodes them into a high-speed low-voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a TMDS-compatible receiver like the TI TFP401/401A to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat-panel drive circuitry to produce an image on the display. Because the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. To support modern display resolutions up to UXGA, a high-bandwidth receiver with good jitter and skew tolerance is required.

9.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

9.3 Feature Description

9.3.1 TMDS Pixel Data and Control Signal Encoding

TMDS stands for transition-minimized differential signaling. Only one of two possible TMDS characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent, and transmits the character that minimizes the number of transitions to approximate a dc balance of the transmission line.

Three TMDS channels are used to receive RGB pixel data during active display time, DE = high. The same three channels also receive control signals, HSYNC, VSYNC, and user-defined control signals CTL[3:1]. These control signals are received during inactive display or blanking-time. Blanking-time is when DE = low. Table 1 maps the received input data to the appropriate TMDS input channel in a DVI-compliant system.

Copyright © 2000–2016, Texas Instruments Incorporated

Table 1. TMDS Pixel Data and Control Signal Encoding

RECEIVED PIXEL DATA ACTIVE DISPLAY DE = HIGH	INPUT CHANNEL	OUTPUT PINS (VALID FOR DE = HIGH)
Red[7:0]	Channel-2 (Rx2 ±)	QE[23:16] QO[23:16]
Green[7:0]	Channel-1 (Rx1 ±)	QE[15:8] QO[15:8]
Blue[7:0]	Channel-0 (Rx0 ±)	QE[7:0] QO[7:0]
RECEIVED CONTROL DATA BLANKING DE = LOW	**INPUT CHANNEL**	**OUTPUT PINS (VALID FOR DE = LOW)**
CTL[3:2]	Channel-2 (Rx2 ±)	CTL[3:2]
CTL[1: 0] (1)	Channel-1 (Rx1 ±)	CTL1
HSYNC, VSYNC	Channel-0 (Rx0 ±)	HSYNC, VSYNC

(1) Some TMDS transmitters transmit a CTL0 signal. The TFP401/401A decodes and transfers CTL[3:1] and ignores CTL0 characters. CTL0 is not available as a TFP401/401A output.

The TFP401/401A discriminates between valid pixel TMDS characters and control TMDS characters to determine the state of active display versus blanking, i.e., the state of DE.

9.3.2 TFP401/401A Clocking and Data Synchronization

The TFP401/401A receives a clock reference from the DVI transmitter that has a period equal to the pixel time, t_{pix}. The frequency of this clock is also referred to as the pixel rate. Because the TMDS encoded data on Rx[2:0] contains 10 bits per 8-bit pixel, it follows that the Rx[2:0] serial bit rate is 10 times the pixel rate. For example, the required pixel rate to support a UXGA resolution with 60-Hz refresh rate is 165 MHz. The TMDS serial bit rate is 10× the pixel rate, or 1.65 Gb/s. Due to the transmission of this high-speed digital bit stream, on three separate channels (or twisted-pair wires) of long distances (3–5 meters), phase synchronization between the data steams and the input reference clock is not assured. In addition, skew between the three data channels is common. The TFP401/401A uses a 4× oversampling scheme of the input data streams to achieve reliable synchronization with up to 1-t_{pix} channel-to-channel skew tolerance. Accumulated jitter on the clock and data lines due to reflections and external noise sources is also typical of high-speed serial data transmission; hence, the TFP401/401A design for high jitter tolerance.

The input clock to the TFP401/401A is conditioned by a phase-locked loop (PLL) to remove high-frequency jitter from the clock. The PLL provides four 10× clock outputs of different phase to locate and sync the TMDS data streams (4× oversampling). During active display, the pixel data is encoded to be transition-minimized, whereas in blank, the control data is encoded to be transition-maximized. A DVI-compliant transmitter is required to transmit in blank for a minimum period of time, 128 t_{pix}, to ensure sufficient time for data synchronization when the receiver sees a transition-maximized code. Synchronization during blank, when the data is transition-maximized, ensures reliable data-bit boundary detection. Phase synchronization to the data streams is unique for each of the three input channels and is maintained as long as the link remains active.

9.3.3 TFP401/401A TMDS Input Levels and Input Impedance Matching

The TMDS inputs to the TFP401/401A receiver have a fixed single-ended termination to AV_{DD}. The TFP401/401A is internally optimized using a laser trim process to precisely fix the impedance at 50 Ω. The device functions normally with or without a resistor on the EXT_RES pin, so it remains drop-in compatible with current sockets. The fixed impedance eliminates the need for an external resistor while providing optimum impedance matching to standard 50-Ω DVI cables.

Figure 15 shows a conceptual schematic of a DVI transmitter and TFP401/401A receiver connection. A transmitter drives the twisted-pair cable via a current source, usually achieved with an open-drain type output driver. The internal resistor, which is matched to the cable impedance at the TFP401/401A input, provides a pullup to AV_{DD}. Naturally, when the transmitter is disconnected and the TFP401/401A DVI inputs are left unconnected, the TFP401/401A receiver inputs pull up to AV_{DD}. The single-ended differential signal and full-differential signal is shown in Figure 16. The TFP401/401A is designed to respond to differential signal swings ranging from 150 mV to 1.56 V with common-mode voltages ranging from (AV_{DD} – 300 mV) to (AV_{DD} – 37 mV).

Copyright © 2000–2016, Texas Instruments Incorporated

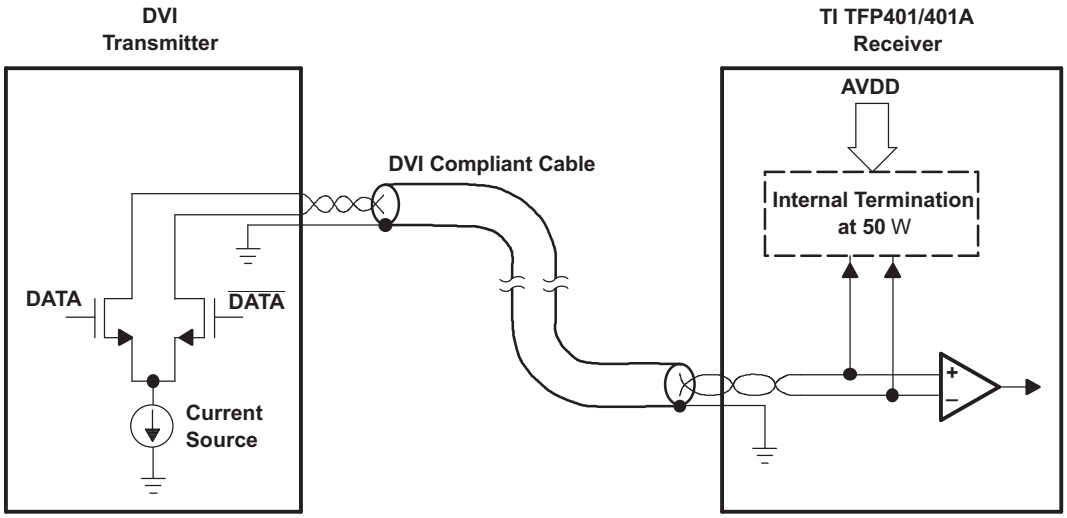


Figure 15. TMDS Differential Input and Transmitter Connection

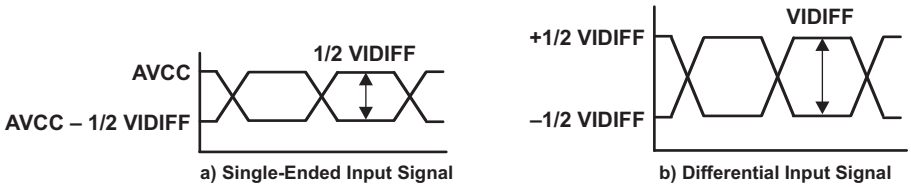


Figure 16. TMDS Inputs

9.3.4 TFP401A Incorporates HSYNC Jitter Immunity

Several DVI transmitters available in the market introduce jitter on the transmitted HSYNC and VSYNC signals during the TMDS encryption process. The HSYNC signal can shift by one pixel position (one clock) from nominal in either direction, resulting in up to two cycles of HSYNC shift. This jitter carries through to the DVI receiver, and if the position of HSYNC shifts continuously, the receiver can lose track of the input timing, causing pixel noise to occur on the display. For this reason, a DVI-compliant receiver with HSYNC jitter immunity should be used in all displays that could be connected to host PCs with transmitters that have this HSYNC jitter problem.

The TFP401A integrates HSYNC regeneration circuitry that provides a seamless interface to these noncompliant transmitters. The position of the data enable (DE) signal is always fixed in relation to data, irrespective of the location of HSYNC. The TFP401A receiver uses the DE and clock signals to recreate stable vertical and horizontal sync signals. The circuit filters the HSYNC output of the receiver, and HSYNC is shifted to the nearest eighth bit boundary, producing a stable output with respect to data, as shown in Figure 17. This ensures accurate data synchronization at the input of the display timing controller.

This HSYNC regeneration circuit is transparent to the monitor and need not be removed even if the transmitted HSYNC is stable. For example, the PanelBus line of DVI 1.0 compliant transmitters, such as the TFP6422 and TFP420, do not have the HSYNC jitter problem. The TFP401A operates correctly with either compliant or noncompliant transmitters. In contrast, the TFP401 is ideal for customers who have control over the transmit portion of the design, such as bundled system manufacturers and for internal monitor use (the DVI connection between monitor and panel modules).

Copyright © 2000–2016, Texas Instruments Incorporated

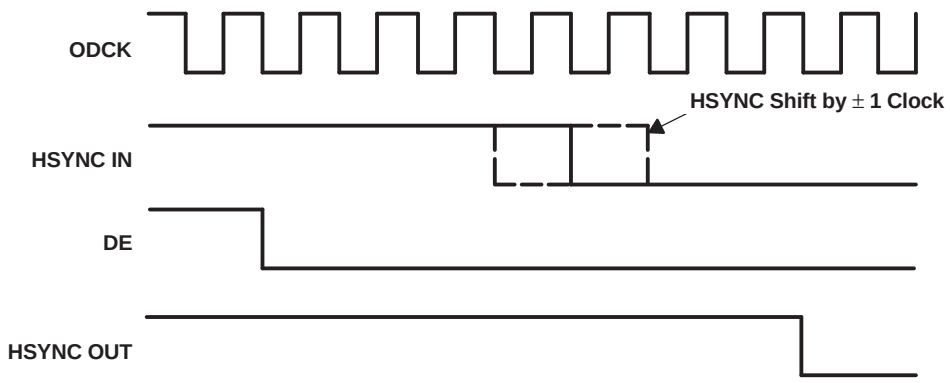


Figure 17. HSYNC Regeneration Timing Diagram

9.4 Device Functional Modes

9.4.1 TFP401/401A Modes of Operation

The TFP401/401A provides system design flexibility and value by providing the system designer with configurable options or modes of operation to support varying system architectures. Table 2 outlines the various panel modes that can be supported, along with appropriate external control pin settings.

Table 2. TFP401/401A Modes of Operation

PANEL	PIXEL RATE	ODCK LATCH EDGE	ODCK	DFO	PIXS	OCK_INV
TFT or 16-bit DSTN	1 pix/clock	Falling	Free run	0	0	0
TFT or 16-bit DSTN	1 pix/clock	Rising	Free run	0	0	1
TFT	2 pix/clock	Falling	Free run	0	1	0
TFT	2 pix/clock	Rising	Free run	0	1	1
24-bit DSTN	1 pix/clock	Falling	Gated low	1	0	0
NONE	1 pix/clock	Rising	Gated low	1	0	1
24-bit DSTN	2 pix/clock	Falling	Gated low	1	1	0
24-bit DSTN	2 pix/clock	Rising	Gated low	1	1	1

9.4.2 TFP401/401A Output Driver Configurations

The TFP401/401A provides flexibility by offering various output driver features that can be used to optimize power consumption, ground bounce, and power-supply noise. The following sections outline the output driver features and their effects.

9.4.2.1 Output Driver Power Down

($\overline{\text{PDO}}$ = low). Pulling $\overline{\text{PDO}}$ low places all the output drivers, except CTL1 and SCDT, into a high-impedance state. The SCDT output, which indicates link-disabled or link-inactive, can be tied directly to the $\overline{\text{PDO}}$ input to disable the output drivers when the link is inactive or when the cable is disconnected. An internal pullup on the $\overline{\text{PDO}}$ pin defaults the TFP401/401A to the normal nonpower-down output drive mode if left unconnected.

9.4.2.2 Drive Strength

(ST = high for high drive strength, ST = low for low drive strength). The TFP401/401A allows for selectable output drive strength on the data, control, and ODCK outputs. See the *DC Electrical Characteristics* table for the values of I_{OH} and I_{OL} current drives for a given ST state. The high output drive strength offers approximately two times the drive as the low-output drive strength.

Copyright © 2000–2016, Texas Instruments Incorporated

9.4.2.3 Time-Staggered Pixel Output

This option works only in conjunction with the 2-pixel/clock mode (PIXS = high). Setting $\overline{\text{STAG}}$ = low time-staggers the even- and odd-pixel outputs so as to reduce the amount of instantaneous current surge from the power supply. Depending on the PCB layout and design, this can help reduce the amount of system ground bounce and power-supply noise. The time stagger is such that in 2-pixel/clock mode, the even pixel is delayed from the latching edge of ODCK by 0.25 t_{cip}. (t_{cip} is the period of ODCK. The ODCK period is 2 t_{pix} when in 2-pixel/clock mode).

Depending on system constraints of output load, pixel rate, panel input architecture, and board cost, the TFP401/401A drive-strength and staggered-pixel options allow flexibility to reduce system power-supply noise, ground bounce, and EMI.

9.4.2.4 Power Management

The TFP401/401A offers several system power-management features.

The output driver power down ($\overline{\text{PDO}}$ = low) is an intermediate mode which offers several uses. During this mode, all output drivers except SCDT and CTL1 are driven to a high-impedance state while the rest of the device circuitry remains active.

The TFP401/401A power down ($\overline{\text{PD}}$ = low) is a complete power down in that it powers down the digital core, the analog circuitry, and output drivers. All output drivers are placed into a Hi-Z state. All inputs are disabled except for the $\overline{\text{PD}}$ input. The TFP401/401A does not respond to any digital or analog inputs until $\overline{\text{PD}}$ is pulled high.

Both $\overline{\text{PDO}}$ and $\overline{\text{PD}}$ have internal pullups, so if left unconnected they default the TFP401/401A to normal operating modes.

9.4.2.5 Sync Detect

The TFP401/401A offers an output, SCDT, to indicate link activity. The TFP401/401A monitors activity on DE to determine if the link is active. When 1 million (1e6) pixel clock periods pass without a transition on DE, the TFP401/401A considers the link inactive, and SCDT is driven low. While SCDT is low, if two DE transitions are detected within 1600 pixel clock periods, the link is considered active, and SCDT is pulled high.

SCDT can be used to signal a system power management circuit to initiate a system power down when the link is considered inactive. The SCDT can also be tied directly to the TFP401/401A $\overline{\text{PDO}}$ input to power down the output drivers when the link is inactive. It is not recommended to use SCDT to drive the $\overline{\text{PD}}$ input, because once in complete power-down, the analog inputs are ignored and the SCDT state does not change. An external system power-management circuit to drive $\overline{\text{PD}}$ is preferred.

Copyright © 2000–2016, Texas Instruments Incorporated

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TFP401 is a DVI (Digital Visual Interface) compliant digital receiver that is used in digital flat panel display systems to receive and decode TMDS encoded RGB pixel data streams. A digital display system a host, usually a PC or workstation, contains a DVI compliant transmitter that receives 24-bit pixel data along with appropriate control signals and encodes them into a high-speed low voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, will require a DVI compliant receiver like the TI TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. The TFP401 will support resolutions up to UXGA.

10.2 Typical Application

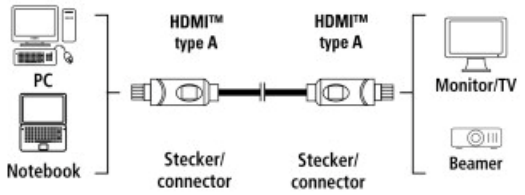


Figure 18. Typical Application

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	VALUE
Power supply	3.3 V-DC @ 1 A
Input clock	Single-ended
Input clock frequency range	25 MHz – 165 MHz
Output format	24 bits/pixel
Input clock latching	Rising edge
I^2C EEPROM support	No
De-skew	No

Copyright © 2000–2016, Texas Instruments Incorporated

10.2.2 Detailed Design Procedure

10.2.2.1 Data and Control Signals

The trace length of data and control signals out of the receiver should be kept as close to equal as possible. Trace separation should be ~5X Height. As a general rule, traces also should be less than 2.8 inches if possible (longer traces can be acceptable).

Delay = 85 × SQRT ER

where

- ER = 4.35
- Relative permittivity of 50% resin FR-4 @ 1 GHz
- Delay = 177 pS/inch (1)

Length of rising edge = TR(picoseconds) ÷ Delay

where

- TR = 3 nS
- = 3000 ps ÷ 177 ps per inch
- = 16.9 inches (2)

Length of rising edge ÷ 6 = Max length of trace for lumped circuit

where

- 16.9 ÷ 6 = 2.8 inches (3)

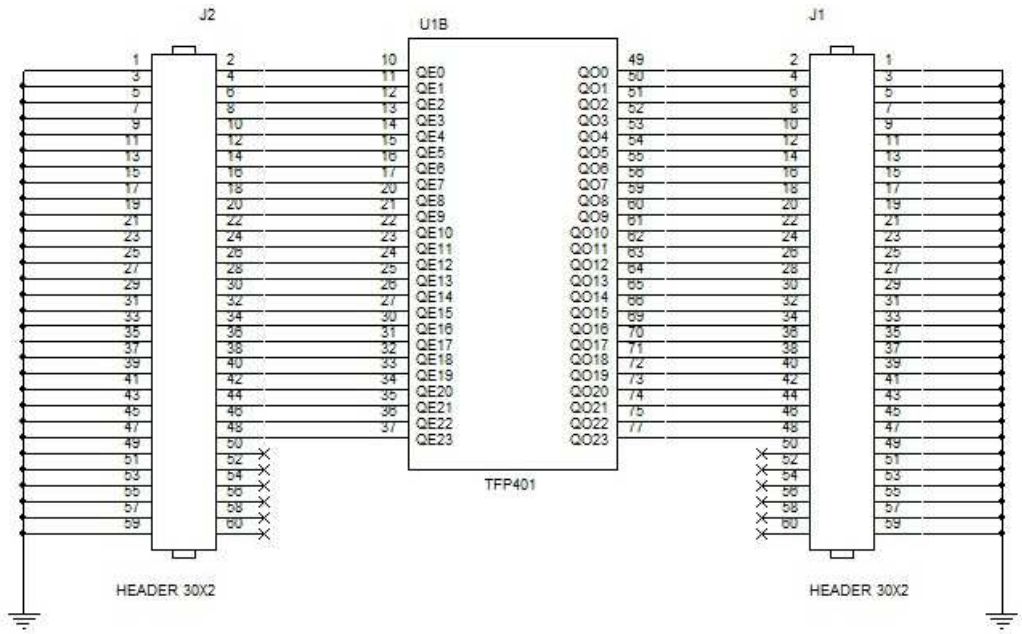


Figure 19. Data and Control Signals Design

Copyright © 2000–2016, Texas Instruments Incorporated

10.2.2.2 Configuration Options

The TFP401 can be configured in several modes depending on the required output format, for example 1-byte/clock, 2-bytes/clock, falling/rising clock edge. You can leave place holders for future configuration changes.

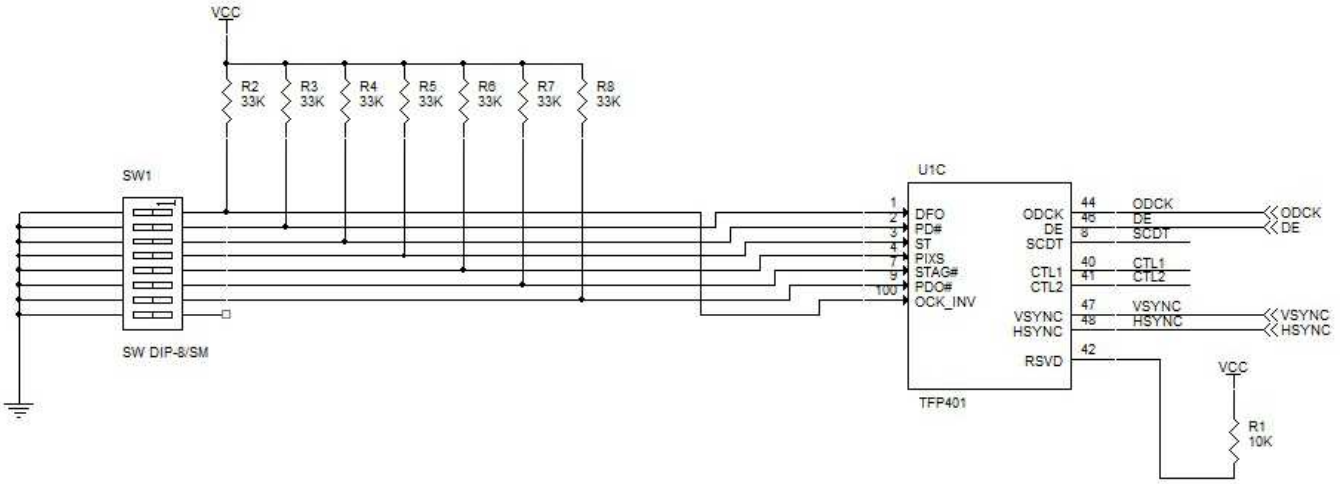


Figure 20. Configuration Options Design

10.2.2.3 Power Supplies Decoupling

Digital, analog, and PLL supplies must be decoupled from each other to avoid electrical noise on the PLL and the core.

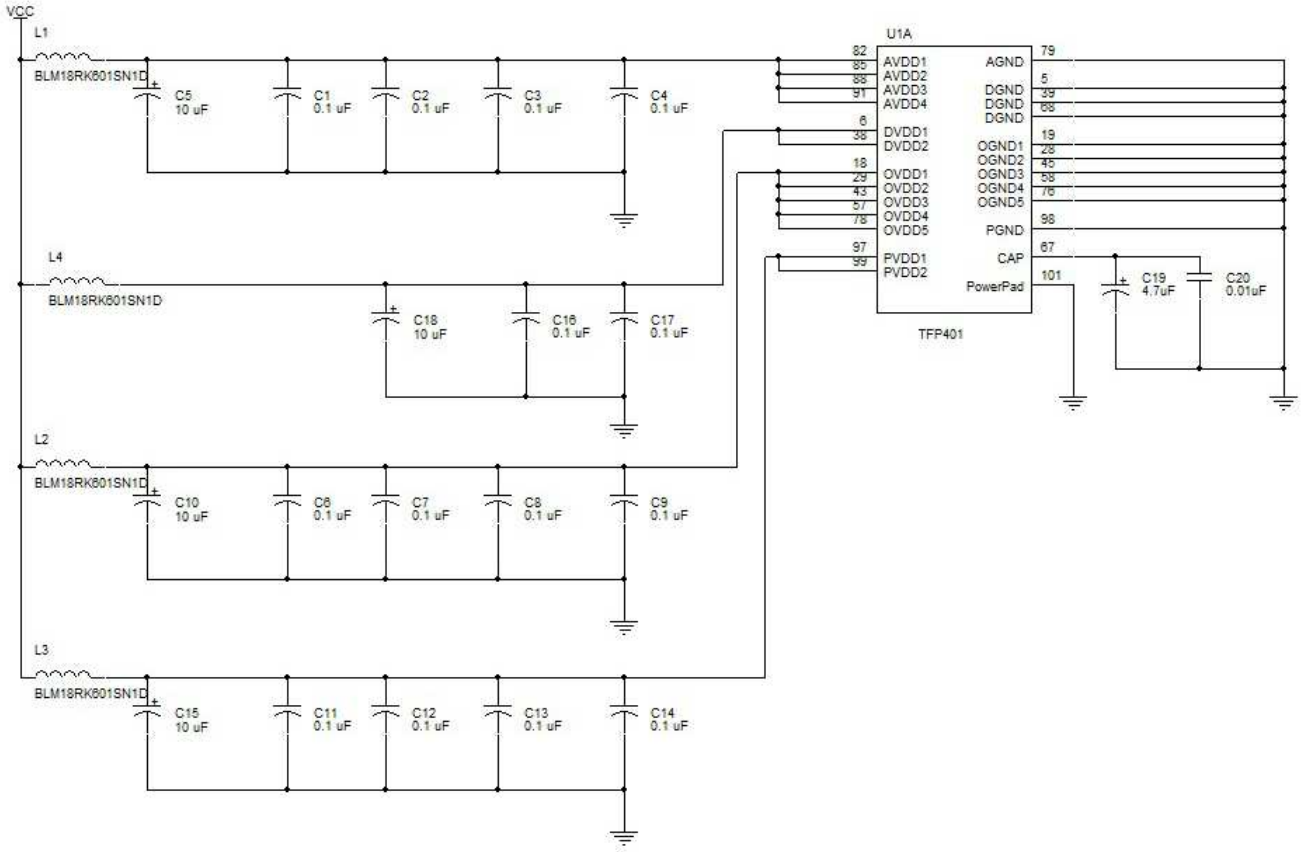


Figure 21. Power Supplies Decoupling Design

10.2.3 Application Curve

Sometimes the panel does not support the same format as the graphics processor unit (GPU). In these cases the user must decide how to connect the unused bits. Figure 22 and Figure 23 plots show the mismatches between the 18-bit GPU and a 24-bit LCD where “x” and “y” represent the 2 LSB of the panel.

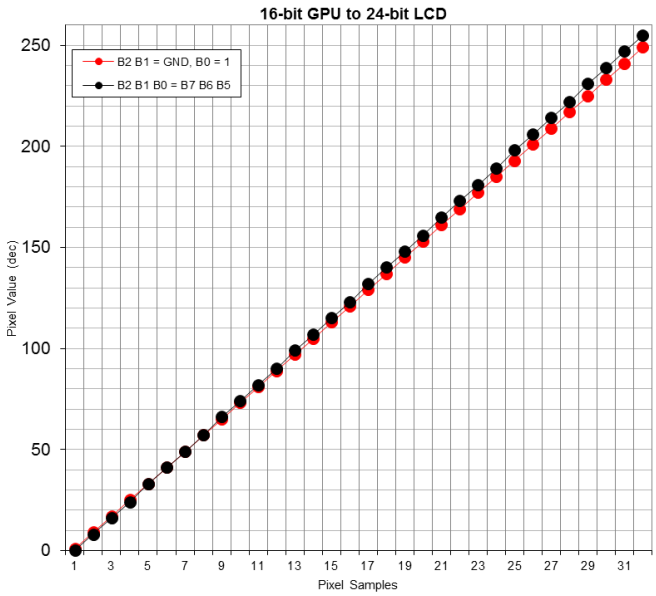


Figure 22. 16-bit GPU to 24-bit LCD

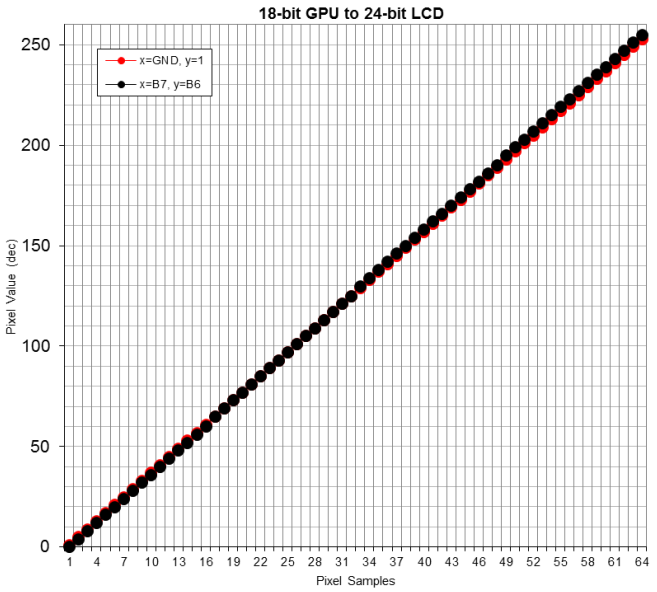


Figure 23. 18-bit GPU to 24-bit LCD

Copyright © 2000–2016, Texas Instruments Incorporated

11 Power Supply Recommendations

Use solid ground planes and tie ground planes together with as many vias as is practical. This will provide a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus receiver power and ground pins and all bypass caps to appropriate power or ground plane with via. Vias should be as fat and short as practical, the goal is to minimize the inductance.

- **DVDD:** Place one 0.01 uF capacitor as close as possible between each DVDD device pin (Pins 6, 38, 67) and ground. A 22 uF tantalum capacitor should be placed between the supply and 0.01 uF capacitors. A ferrite bead should be used between the source and the 22 uF capacitor.
- **OVDD:** Place one 0.01 uF capacitor as close as possible between each OVDD device pin (Pins 18, 29, 43, 57, 78) and ground. A 22 uF tantalum capacitor should be placed between the supply and 0.01 uF capacitors. A ferrite bead should be used between the source and the 22 uF capacitor.
- **AVDD:** Place one 0.01 uF capacitor as close as possible between each AVDD device pin (Pins 82, 84, 88, 95) and ground. A 22 uF tantalum capacitor should be placed between the supply and 0.01 uF capacitors. A ferrite bead should be used between the source and the 22 uF capacitor.
- **PVCC:** Place three 0.01 uF capacitors in parallel as close as possible between the PVDD device pin (Pin 97) and ground. A 22 uF tantalum capacitor should be placed between the supply and 0.01 uF capacitors. A ferrite bead should be used between the source and the 22 uF capacitor.

12 Layout

12.1 Layout Guidelines

12.1.1 Layer Stack

The pinout of Texas Instruments High Speed Interface (HSI) devices features differential signal pairs and the remaining signals comprise the supply rails, V_{CC} and ground, and lower speed signals such as control pins. As an example, consider a device X which is a repeater/re-driver, so both its inputs and outputs are high-speed differential signals. These guidelines can be applied to other high-speed devices such as drivers, receivers, multiplexers, etc. A minimum of four layers is required to accomplish a low EMI PCB design. Layer stacking should be in the following order (top-to-bottom): high-speed differential signal layer, ground plane, power plane and control signal layer.

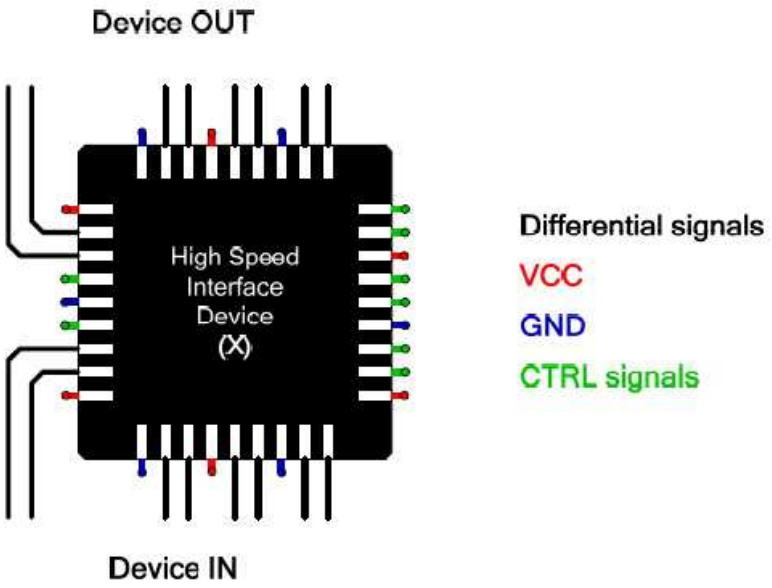


Figure 24. Layer Stack

Layout Guidelines (continued)

12.1.2 Routing High-Speed Differential Signal Traces (RxC–, RxC+, Rx0–, Rx0+, Rx1–, Rx1+, Rx2–, Rx2+)

Trace impedance should be controlled for optimal performance. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2X to 4X Height. A differential trace separation of 4X Height yields about 6% cross-talk (6% effect on impedance). It is recommended that differential trace routing should be side by side, though it is not important that the differential traces be tightly coupled together because tight coupling is not achievable on PCB traces. Typical ratios on PCBs are only 20-50%, and 99.9% is the value of a well-balanced twisted pair cable.

Each differential trace should be as short as possible (<2" preferably) with no 90" angles. These high-speed transmission traces should be on Layer 1 (top layer). RxC–, RxC+, Rx0–, Rx0+, Rx1–, Rx1+, Rx2–, Rx2+ signals all route directly from the DVI connector pins to the device, no external components are needed.

12.1.3 DVI Connector

Clear-out holes for connector pins should leave space between pins to allow continuous ground through the pin field. Allow enough spacing in ground plane around signal pins vias however, keep enough copper between vias to allow for ground current to flow between the vias. Avoid creating a large ground plane slot around the entire connector, minimizing the via capacitance is the goal.

12.2 Layout Example

DVI connector trace matching:

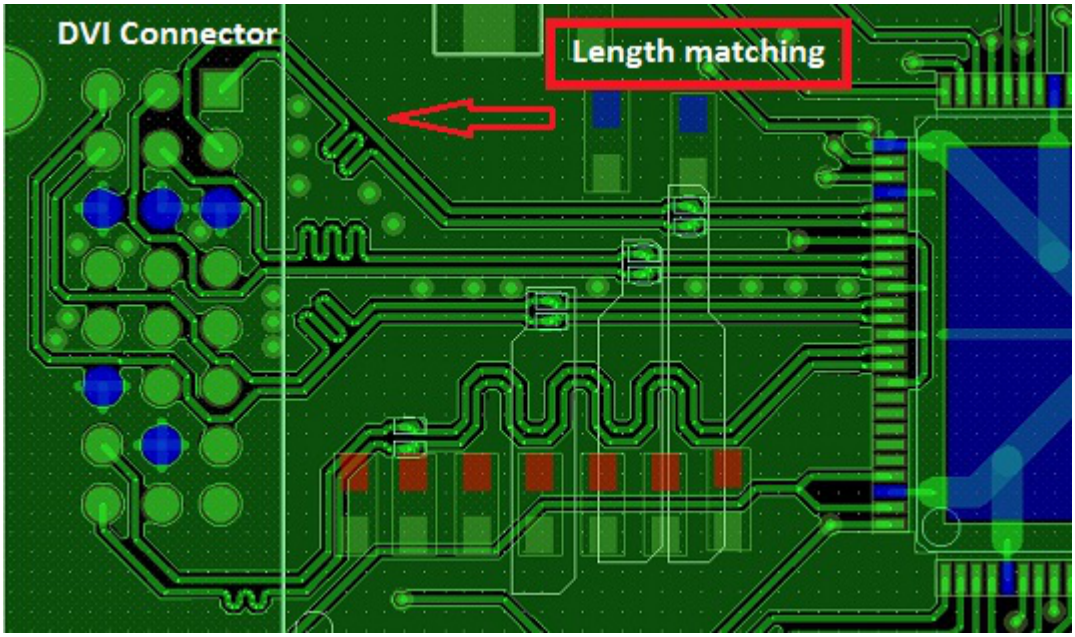


Figure 25. DVI Connector Routing

Copyright © 2000–2016, Texas Instruments Incorporated

Layout Example (continued)

Keep data lines as far as possible from each other.

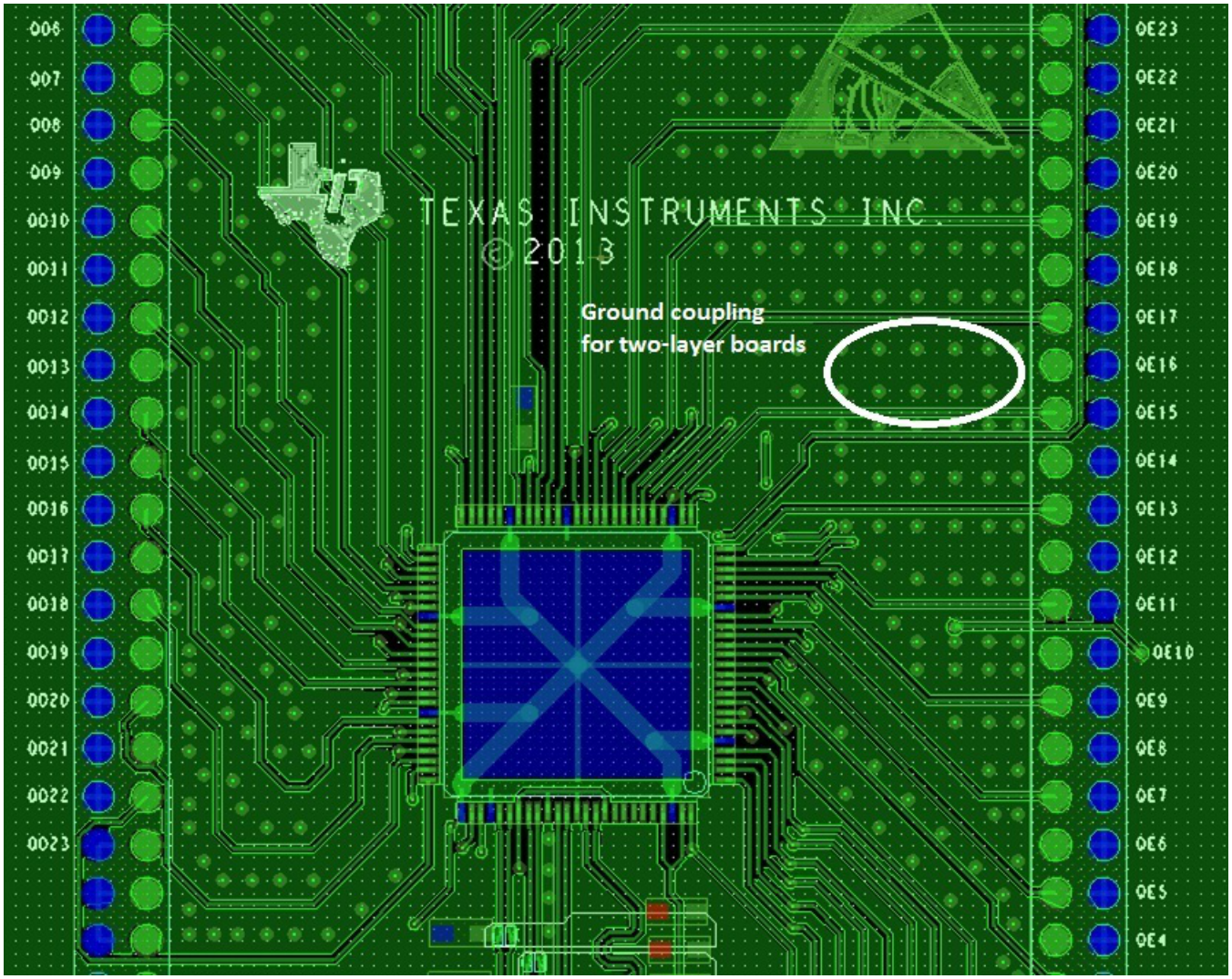


Figure 26. Data Lines Routing

Layout Example (continued)

Connect the thermal pad to ground.

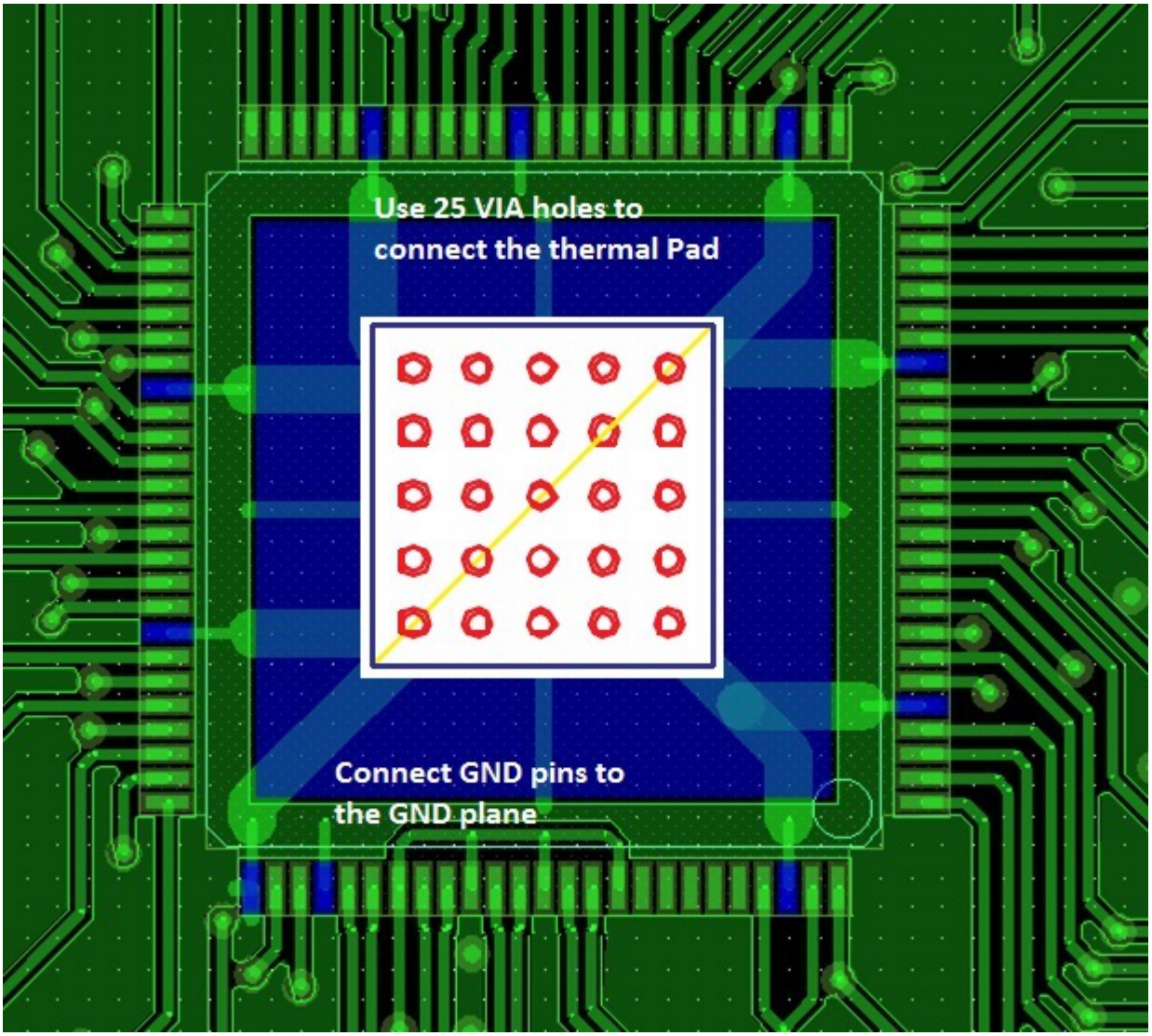


Figure 27. Ground Routing

Copyright © 2000–2016, Texas Instruments Incorporated

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TFP401	Click here	Click here	Click here	Click here	Click here
TFP401A	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

PowerPAD, *PanelBus* are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 TI PowerPAD 100-TQFP Package

The TFP401/401A is packaged in TI's thermally enhanced PowerPAD 100-TQFP packaging. The PowerPAD package is a 14-mm × 14-mm × 1-mm TQFP outline with 0.5-mm lead pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 100-TQFP PowerPAD package offers a back-side solder plane that connects directly to the die mount pad for enhanced thermal conduction. Soldering the back side of the TFP401/401A to the application board is not required thermally, because the device power dissipation is well within the package capability when not soldered.

Soldering the back side of the device to the PCB ground plane is recommended for electrical considerations. Because the die pad is electrically connected to the chip substrate and hence to chip ground, connection of the PowerPAD back side to a PCB ground plane helps to improve EMI, ground bounce, and power-supply noise performance.

Table 5 outlines the thermal properties of the TI 100-TQFP PowerPAD package. The 100-TQFP non-PowerPAD package is included only for reference.

Copyright © 2000–2016, Texas Instruments Incorporated

TI PowerPAD 100-TQFP Package (continued)

Table 5. TI 100-TQFP (14 mm × 14 mm × 1 mm) / 0.5-mm Lead Pitch

PARAMETER	WITHOUT PowerPAD™ Package	PowerPAD™ Package, NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ Package, CONNECTED TO PCB THERMAL PLANE(1)
Theta-JA(1)(2)	45°C/W	27.3°C/W	17.3°C/W
Theta-JC(1)(2)	3.11°C/W	0.12°C/W	0.12°C/W
Maximum power dissipation(1)(2)(3)	1.6 W	2.7 W	4.3 W

(1) Specified with 2-oz. (0.071 mm thick) Cu PCB plating
(2) Airflow is at 0 LFM (0 m/s) (no airflow).
(3) Measured at ambient temperature, T_A = 70°C

Copyright © 2000–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TFP401APZP	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP401APZP	Samples
TFP401APZPG4	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP401APZP	Samples
TFP401APZPR	PREVIEW	HTQFP	PZP	100	1000	TBD	Call TI	Call TI	0 to 70		
TFP401PZP	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP401PZP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

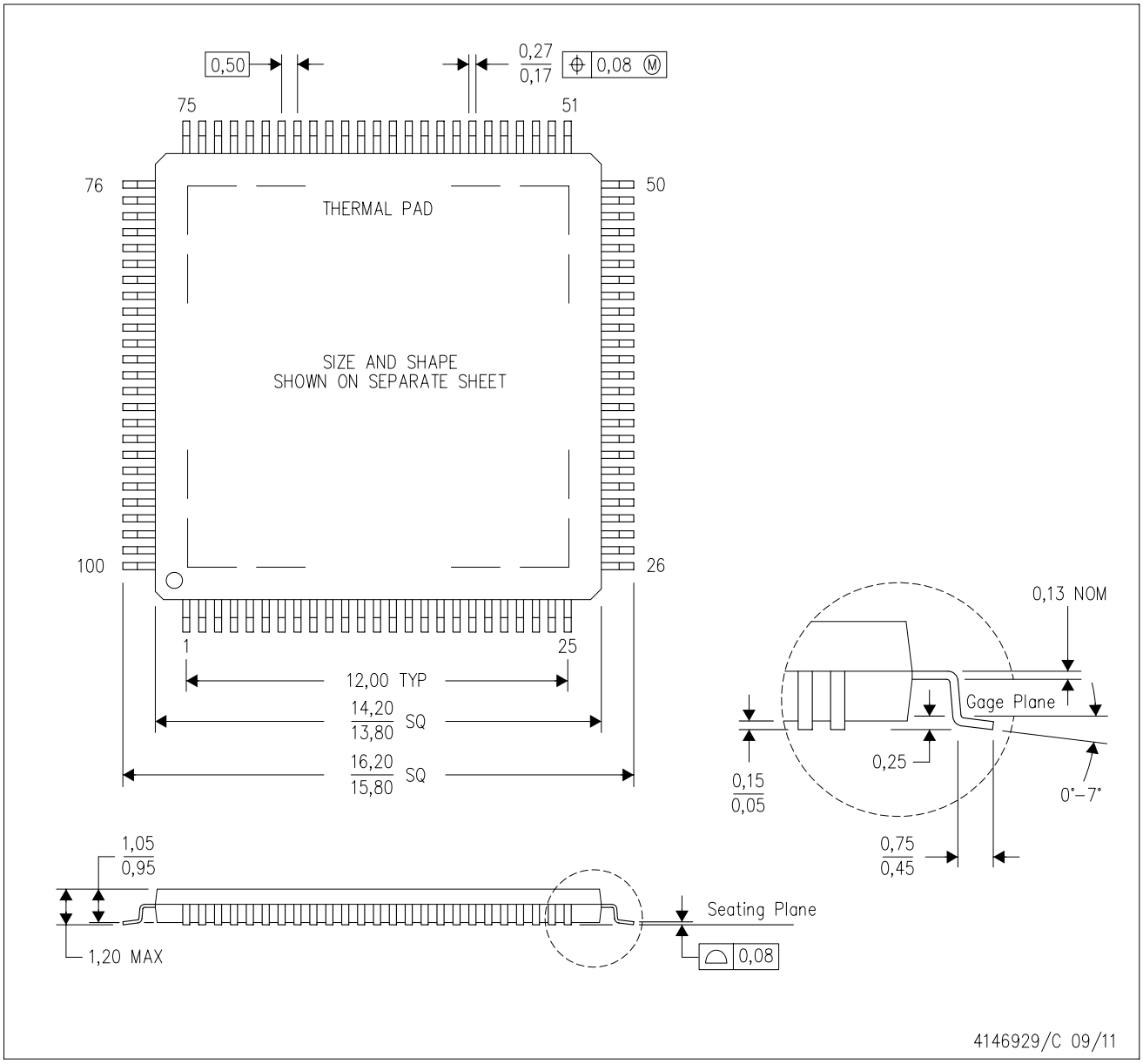
OTHER QUALIFIED VERSIONS OF TFP401A :

- Automotive: TFP401A-Q1
- Enhanced Product: TFP401A-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

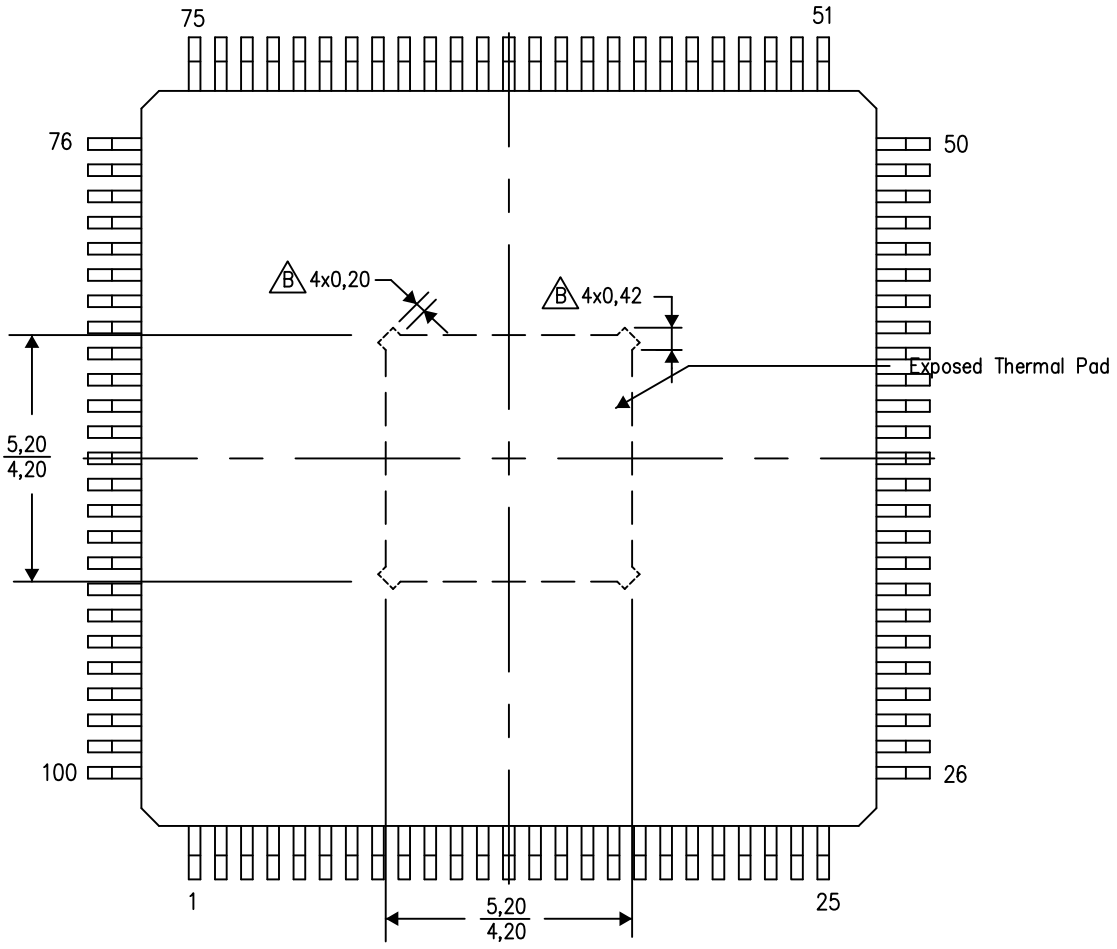
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

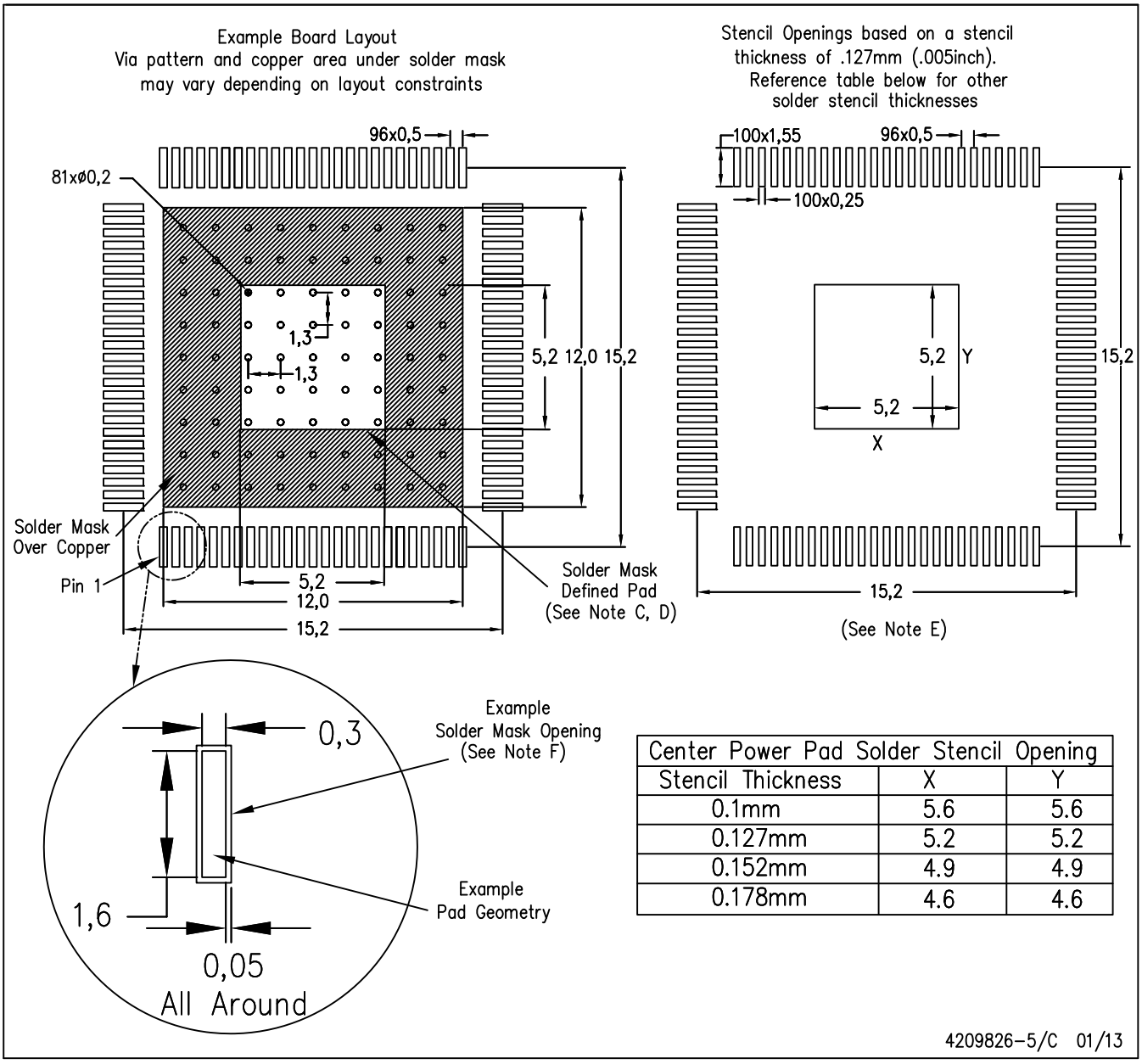
4206333–2/L 05/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	5.6
0.127mm	5.2	5.2
0.152mm	4.9	4.9
0.178mm	4.6	4.6

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated