Sup*IR*Buck™

USER GUIDE FOR IR3837 EVALUATION BOARD

DESCRIPTION

The IR3837 ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3837 a space-efficient solution, providing accurate power delivery for low output voltage applications.

IR3837 is a versatile regulator which offers programmability of switching frequency and current limit while operates in wide input and output voltage range.

The switching frequency is programmable from 250kHz to 1.5MHz for an optimum solution.

Key features includes: Internal LDO, Pre-Bias startup, protection functions, such as hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions. An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3837 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3837 is available in the IR3837 data sheet.

BOARD FEATURES

- V_{in} = +12V
- V_{out} = +1.8V @ 0 – 14A
- F_s = 600kHz
- L = 0.51uH
- C_{in}= 4x10uF (ceramic 1206) + 1x330uF (electrolytic)
- C_{out}=7x47uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 14A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3837 has only one input supply, the input voltage (Vin). Internal LDO circuitry generates Vcc voltage (=5.2V).

One option for using a separate +5V supply for Vcc voltage, as required in a certain application, is to remove R15 (zero Ohm resistor), which disables the internal LDO circuit. In this case Vcc input should be a well regulated 4.5V-7.5V supply and it would be connected to Vcc+ and Vcc-.

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
VOUT+	V_{out} (+1.8V)
VOUT-	Ground of Vout
Vref	Internal Reference-Voltage
SEQ	Sequence input
Vcc+	VCC/LDO_out pin
Vcc-	Connected to PGND
Sync	Synchronous input

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3837 and other components are mounted on the top and bottom side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3837. The feedback resistors are connected to the output voltage at the point of regulation and are located close to IR3837. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

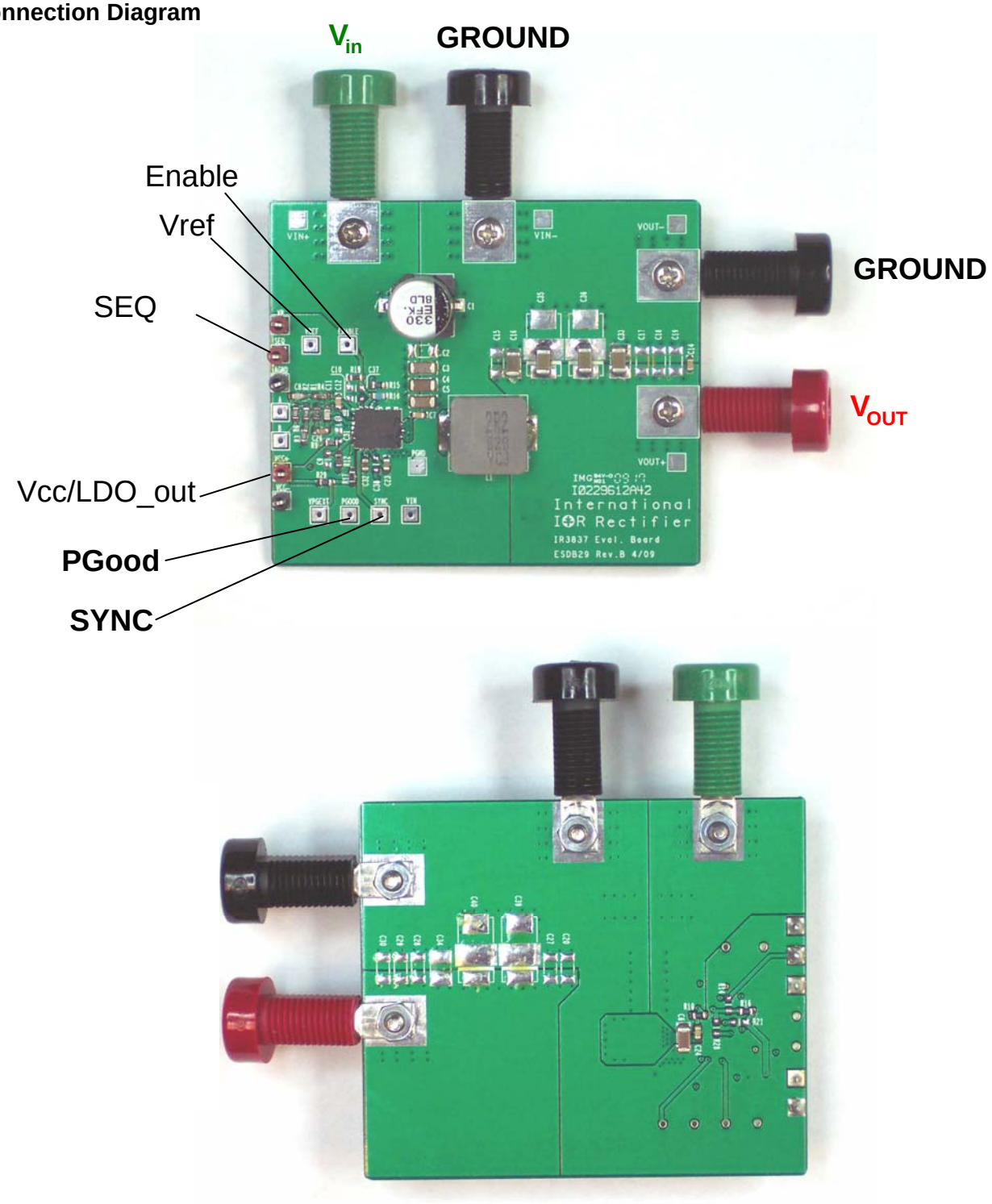


Fig. 1: Connection diagram of IR3838 evaluation board (top and bottom)

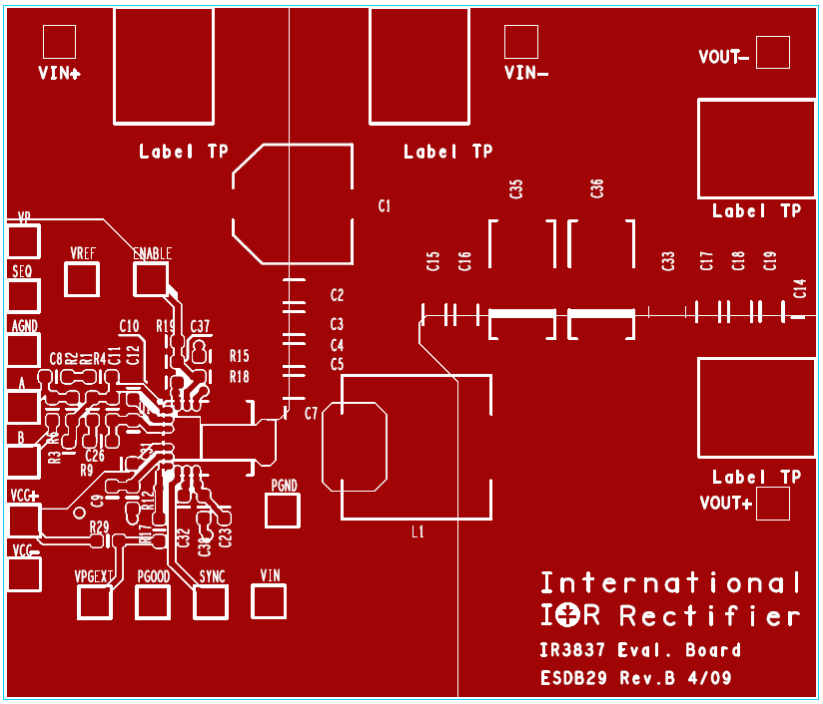


Fig. 2: Board layout, top layer

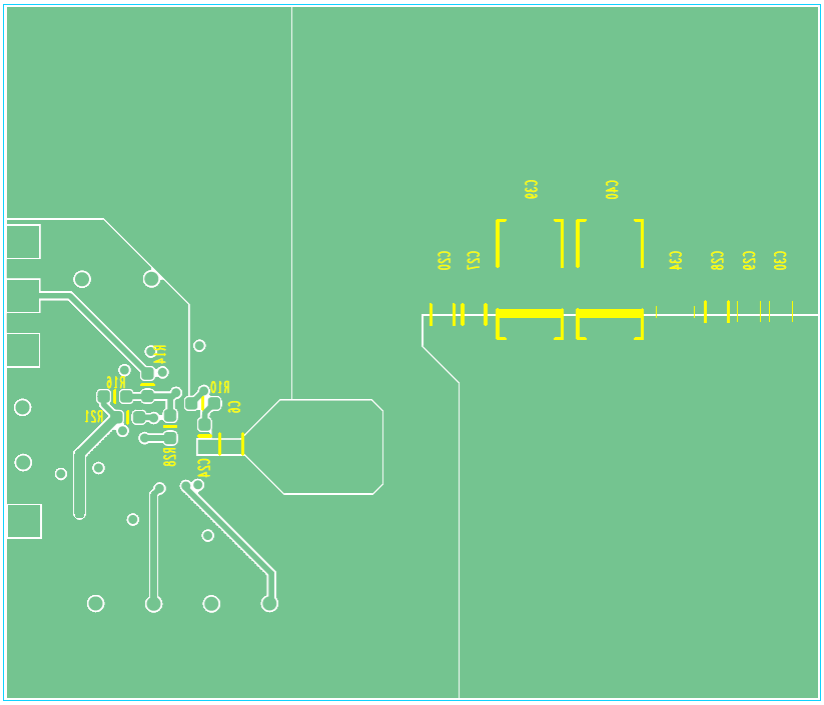


Fig. 3: Board layout, bottom layer

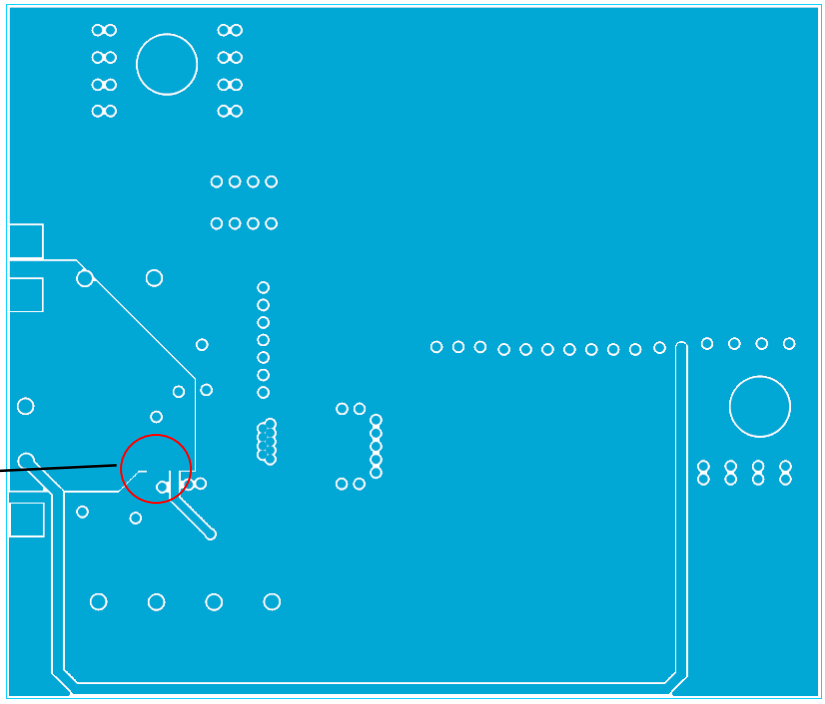


Fig. 4: Board layout, mid-layer I

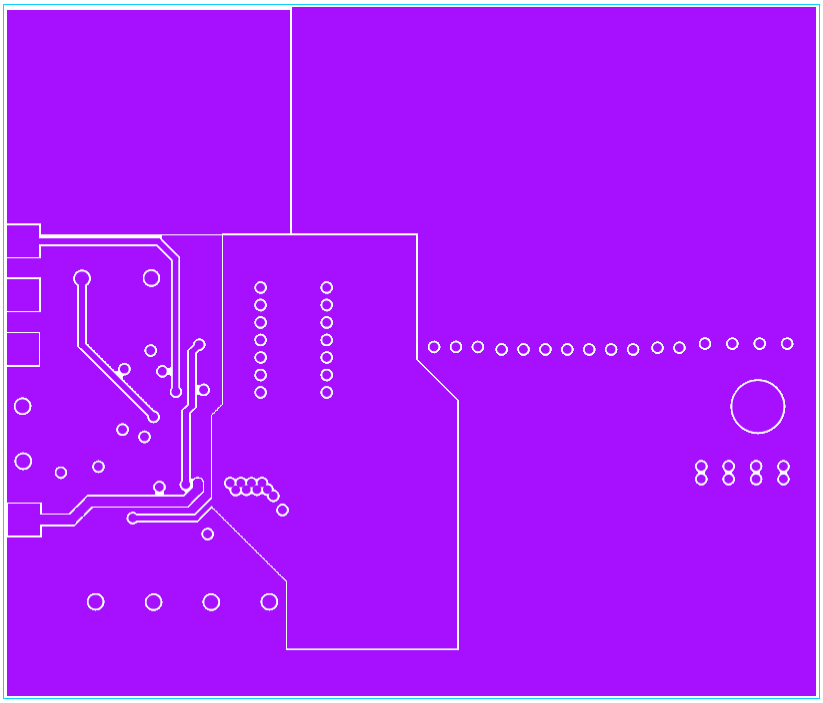


Fig. 5: Board layout, mid-layer II

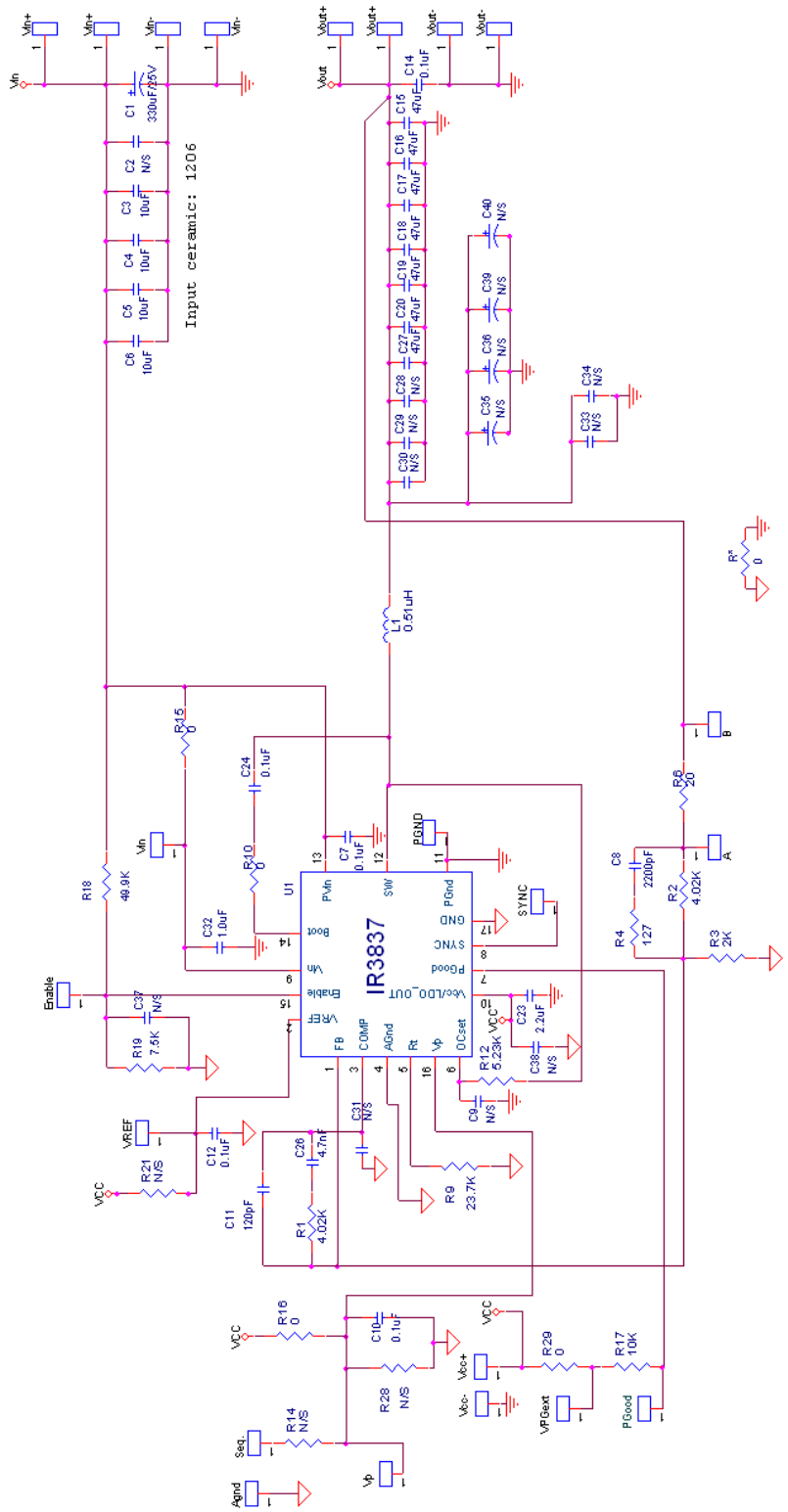


Fig.8: Schematic of the IR3837 evaluation board

Bill of Materials

Item Nun	Quantity	Part Reference	Value	Description	Manufacturer	Manufacturer Part Number
1	1	C1	330uF/25V	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEE-FK1E331P
2	4	C3 C4 C5 C6	10uF	Ceramic,16V,1206,X7R,20%	Panasonic - ECG	ECJ-3YX1C106K
3	5	C7 C10 C12 C14 C24	0.1uF	0603-50V-X7R-10%	Panasonic	ECJ-1VB1H104K
4	1	C8	2200pF	Ceramic,50V,0603,C0G,5%	TDK Corporation	C1608C0G1H222J
5	1	C11	120pF	Ceramic,50V,0603,NP0	Kemet	C0603C121J5GACTU
6	1	C23	2.2uF	Ceramic, 16V, 0603, X5R, 20%	AVX Corporation	0603YD225MAT2A
7	1	C26	4.7nF	Ceramic,25V,0603,C0G,5%	TDK Corporation	C1608C0G1E472J
8	1	C32	1.0uF	Ceramic,25V,0603,X5R,10%	Murata Electronics	GRM188R61E105KA12D
9	7	C15 C16 C17 C18 C33 C35 C36	47uF	CAP, Ceramic, 6.3V X5R 0805	Taiyo Yuden	JMK212BJ476MG-T
10	14	C2 C9 C19 C20 C27 C28 C29 C30 C31 C34 C37 C38 C39 C40	N/S	No Stuff		
11	1	L1	0.51uH	SMT-Inductor,0.29mOhms,11x7.2x7.5mm	VITEC	59PR9876N
12	4	R10 R15 R16 R29	0	Thick-film,0603,1/10W,5%	Vishay/Dale	CRCW06030000Z0EA
13	2	R1 R2	4.02K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX4021
14	1	R3	2K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX2001
15	1	R4	127	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX1270
16	1	R6	20	Thick-film,0603,1/10 W,5%	Vishay/Dale	CRCW060320R0FKEA
17	1	R9	23.7K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX2372
18	1	R12	5.23K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX5231
19	1	R17	10K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX1002
20	1	R18	49.9K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX4992
21	1	R19	7.5K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX7501
22	3	R14 R21 R28	N/S	No Stuff		
23	1	U1	IR3837	IR3837 PQFN	IR	IR3837MBF

TYPICAL OPERATING WAVEFORMS

Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=0-14A, Room Temperature, No Air Flow

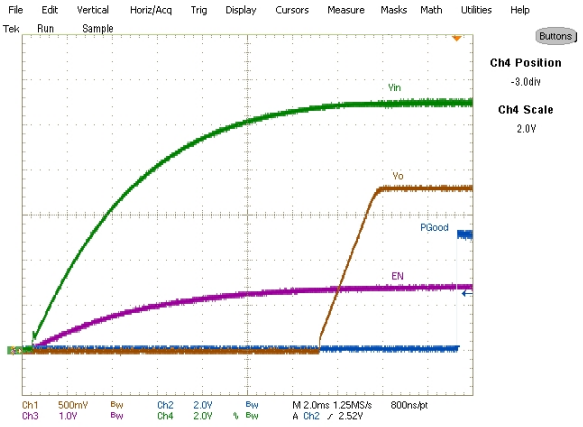


Fig. 9: Start up at 14A Load (Note 1)
Ch_1:V_{out} Ch_2:PGood Ch_3:EN Ch_4: V_{in}

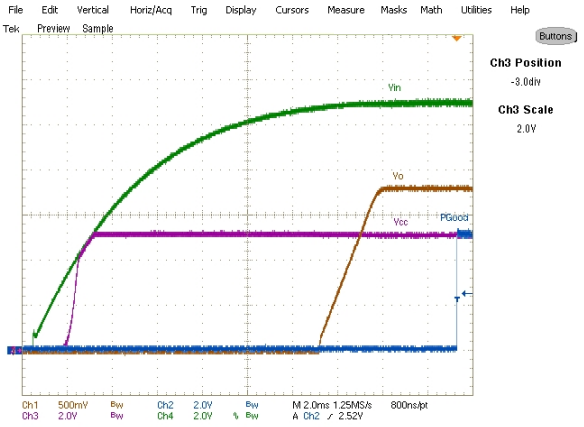


Fig. 10: Start up at 14A Load (Note 1)
Ch_1:V_{out} Ch_2:PGood Ch_3:Vcc Ch_4: V_{in}

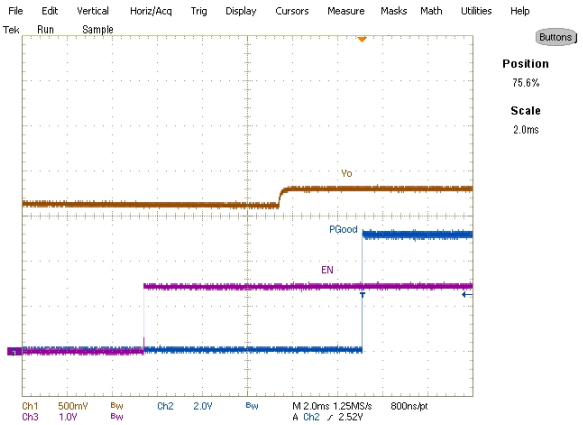


Fig. 11: Start up with 1.62V Prebias,
0A Load, Ch_1:V_{out} Ch_2: PGood Ch_3: EN

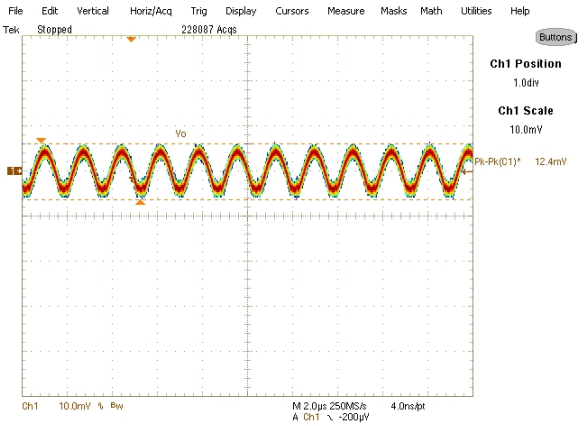


Fig. 12: Output Voltage Ripple, 14A load
(Note2) Ch_1: V_{out}

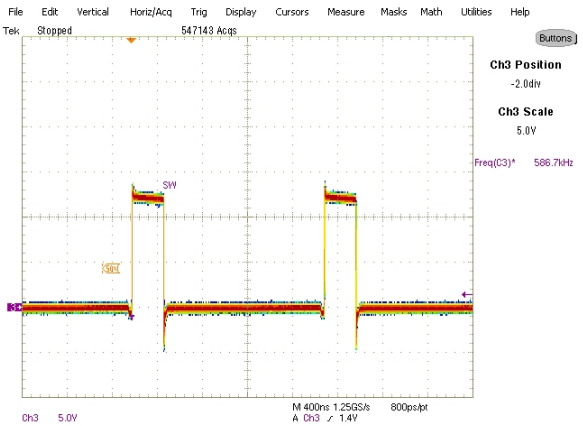


Fig. 13: Inductor node at 14A load
Ch_3:SW

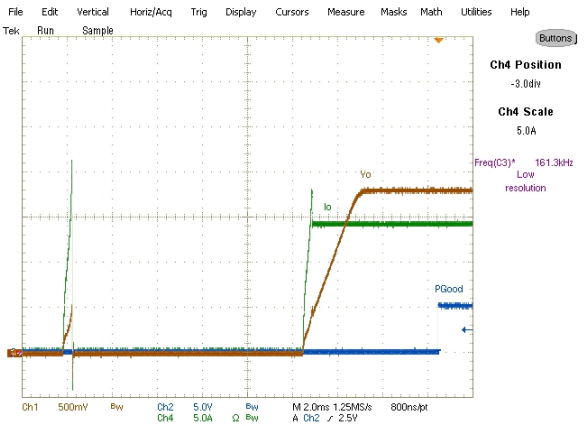


Fig. 14: Short (Hiccup) Recovery
Ch_1:V_{out}, Ch_2:PGood , Ch_4:Iout

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Room Temperature, No Air Flow

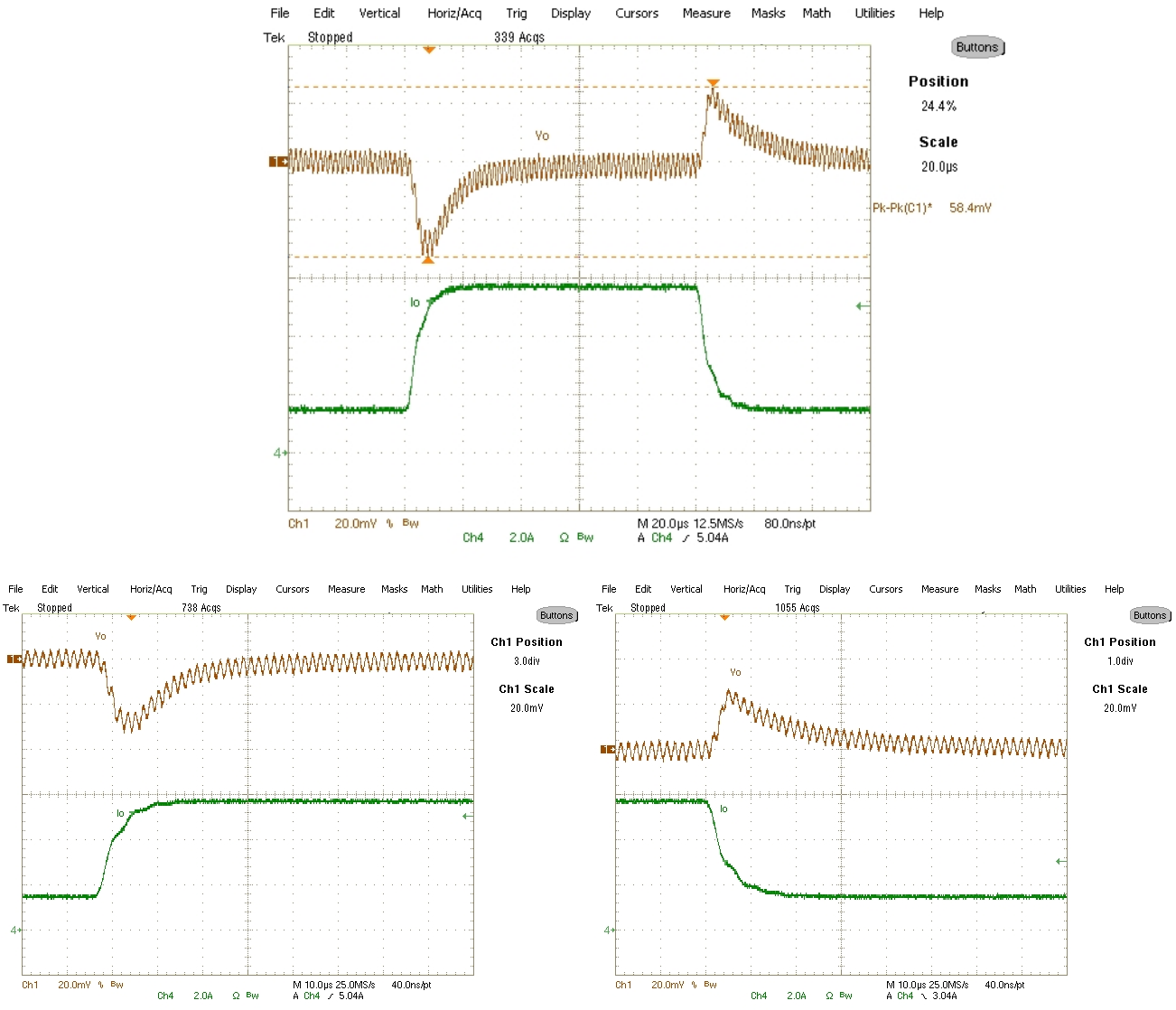


Fig. 15: Transient Response
1.4A(10%)-5.6A(40%) load (0.5A/us) Ch_1:V_{out}, Ch_4:I_o

Note1: Enable is tied to Vin via a resistor divider and triggered when Vin is exceeding above 10.2V.
Note2: Vo ripple signal is taken across C17 cap.

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=0-14A, Room Temperature, No Air Flow

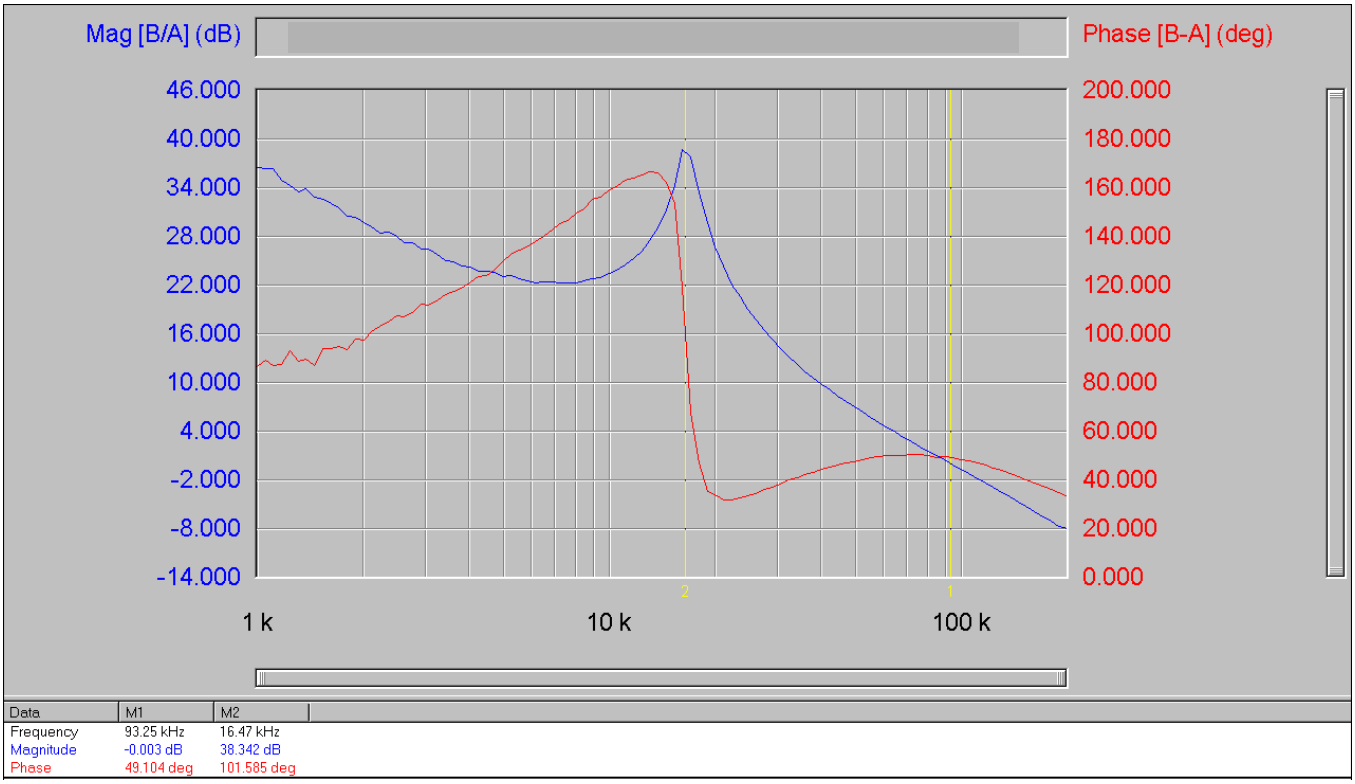
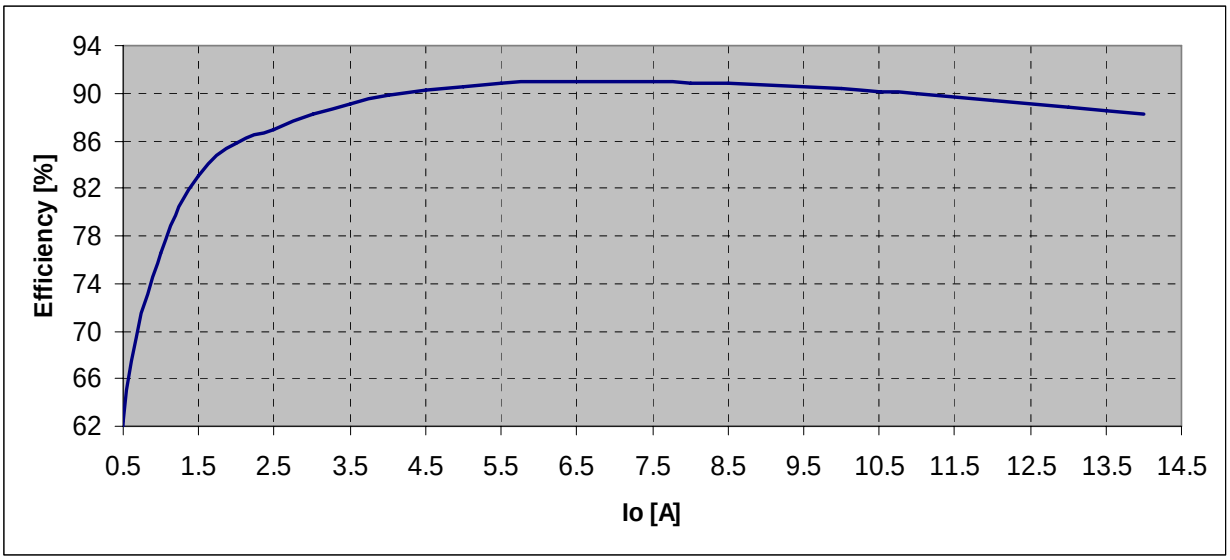


Fig.16: Bode Plot at 10A load shows a bandwidth of 93kHz and phase margin of 49 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=0-14A, Room Temperature, No Air Flow



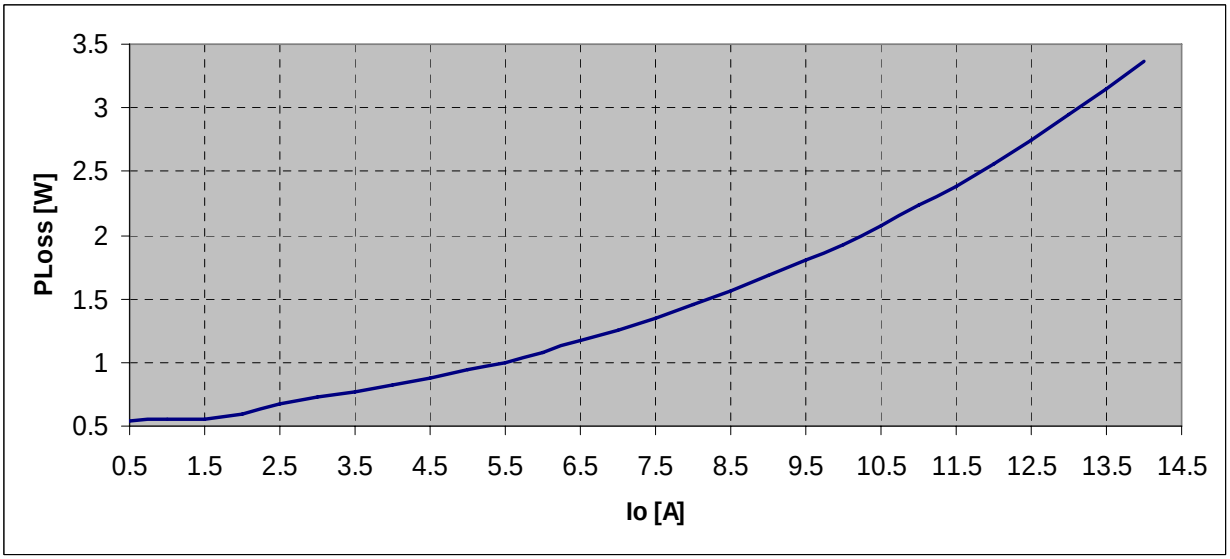


Fig.17: Efficiency and power loss vs. load current

THERMAL IMAGES
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=14A, Room Temperature, No Air Flow

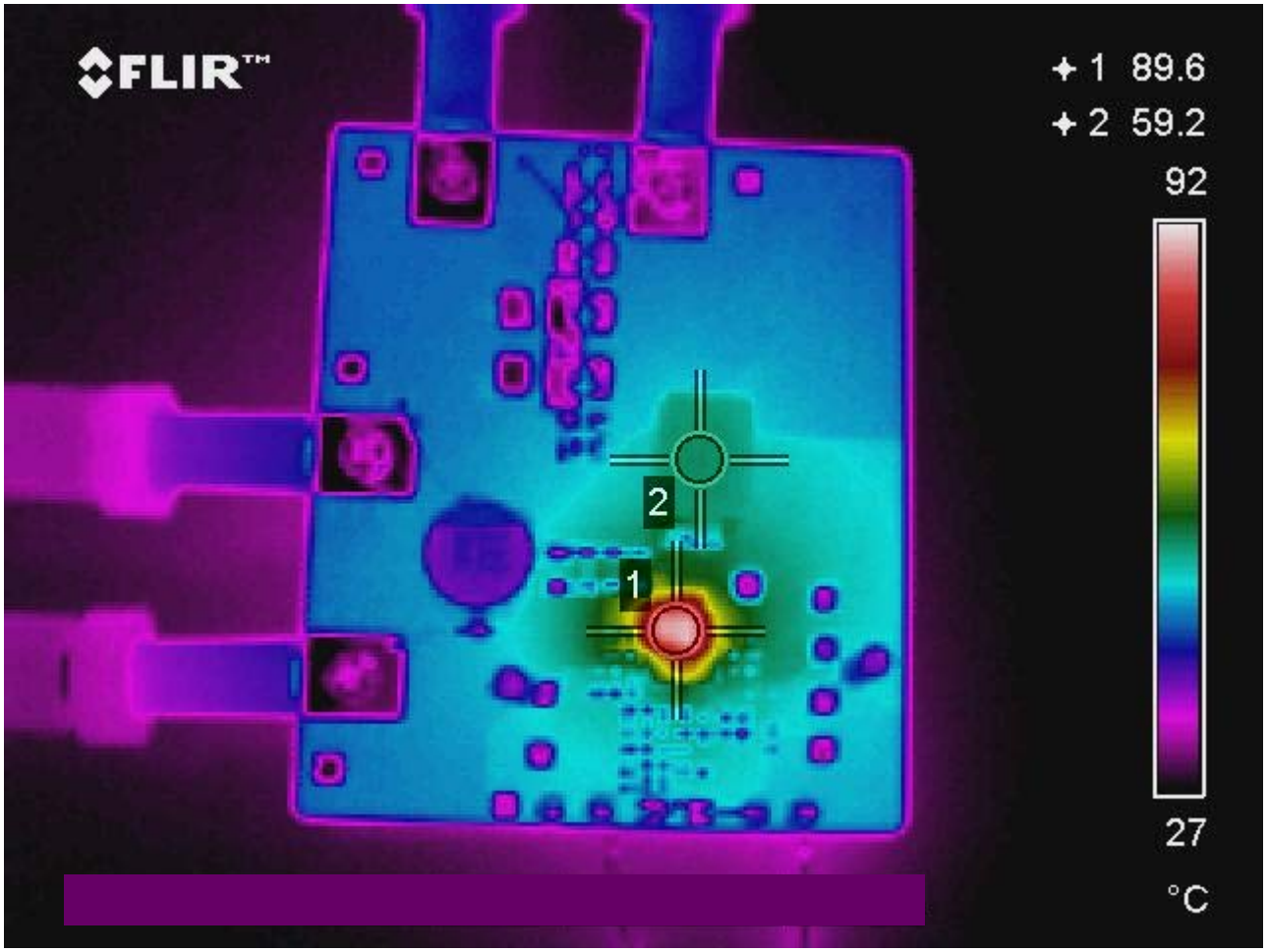


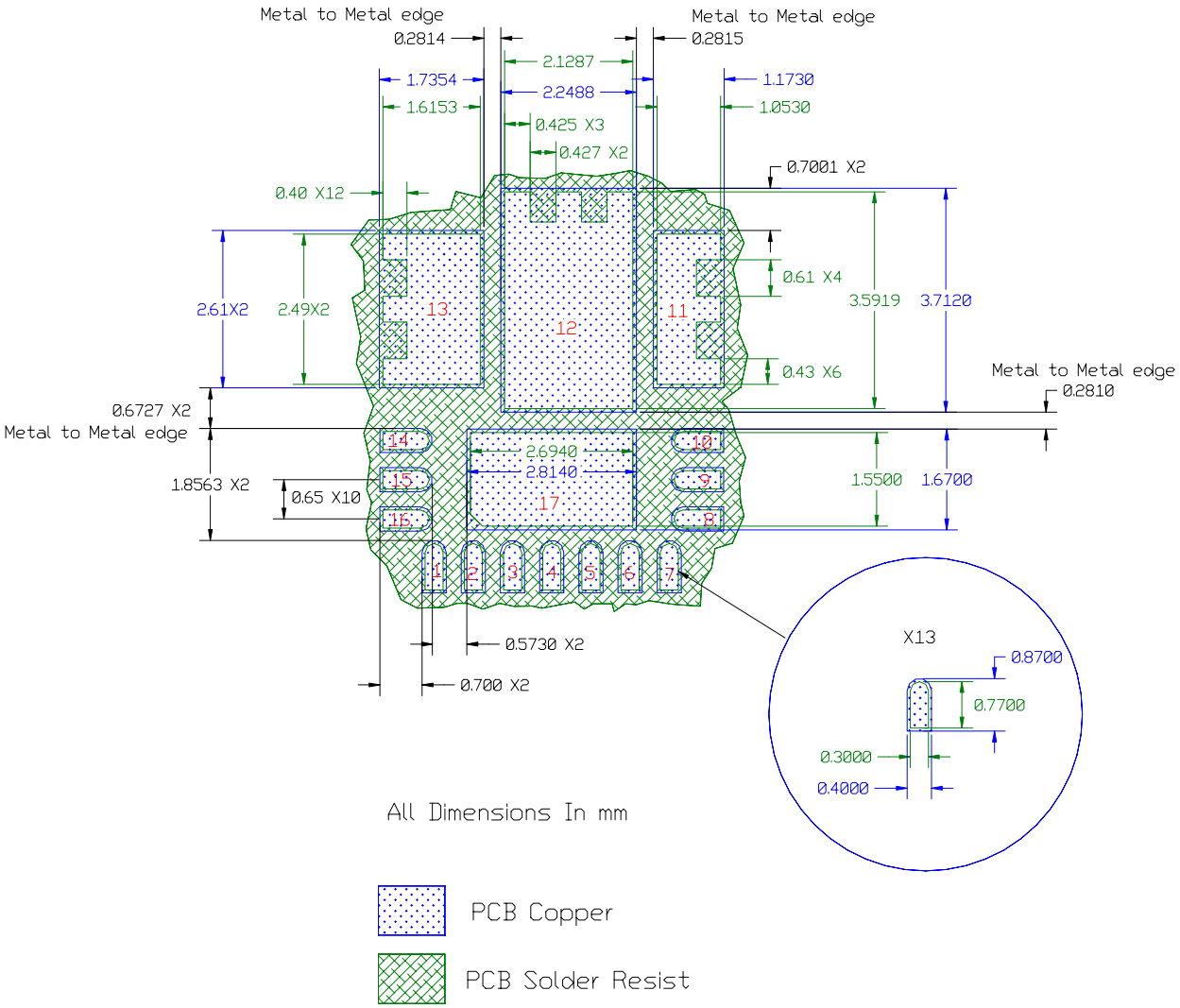
Fig.18: Thermal Image at 14A load
Test Point 1: IR3837, Test Point 2: Inductor

PCB Metal and Components Placement

The lead lands (the 13 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 13 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

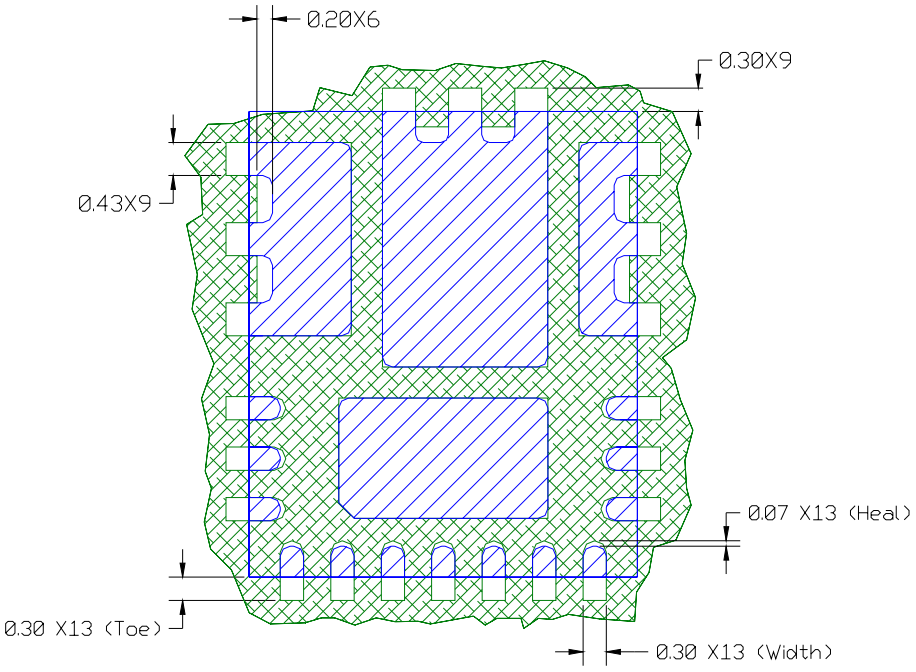


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.



All Dimensions In mm

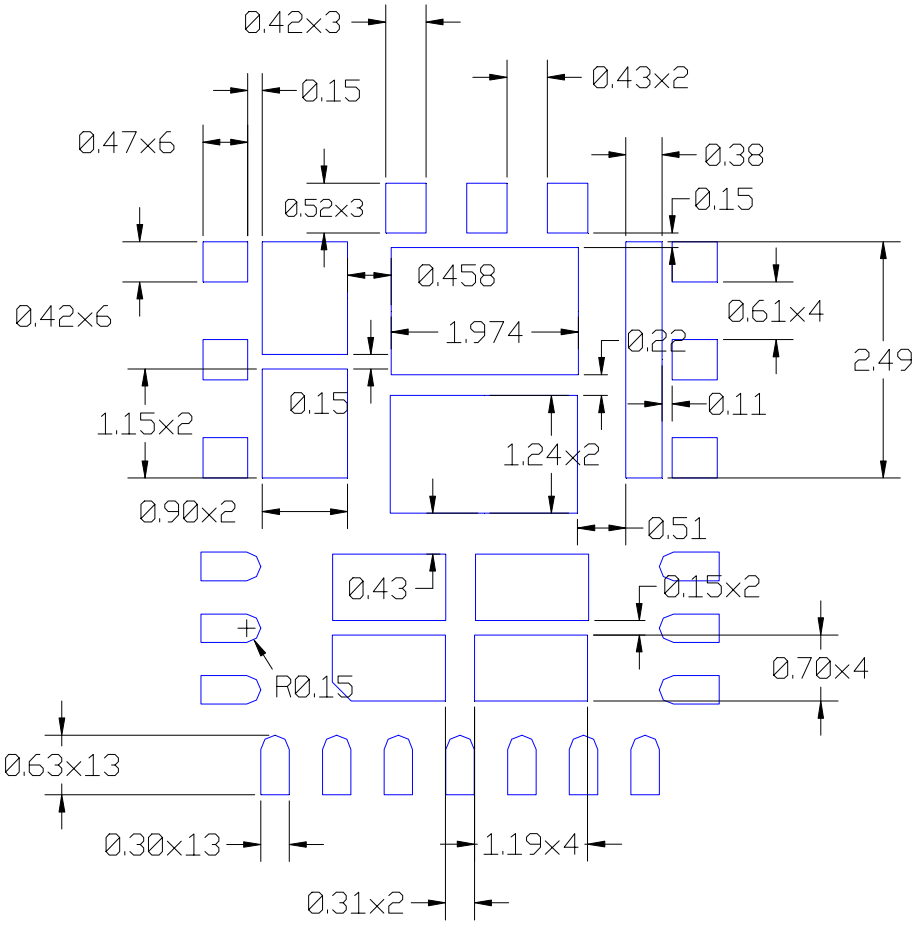
All Pads are Solder Mask Defined

PCB Solder Resist

Component Pad

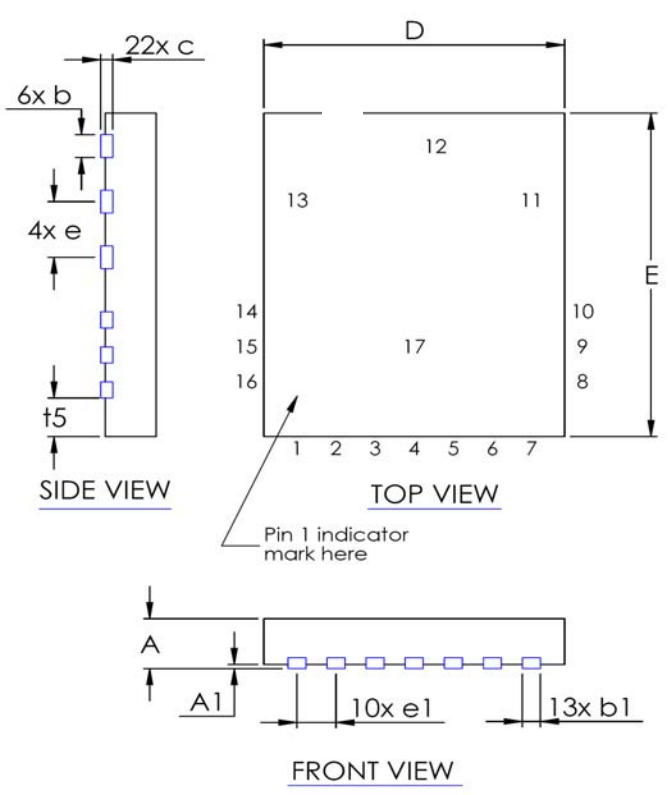
Stencil Design

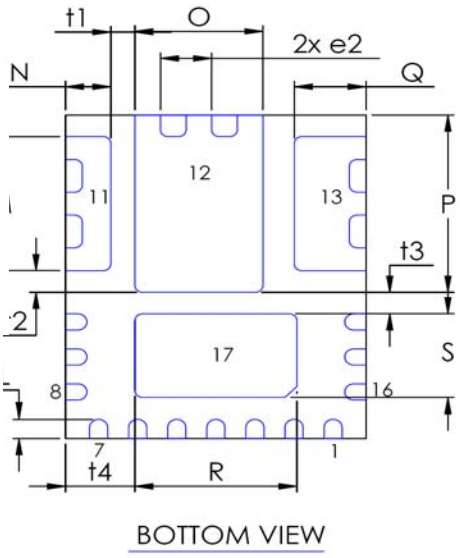
- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.800	1.000	0.0315	0.0394	L	0.350	0.450	0.0138	0.0177
A1	0.000	0.050	0.0000	0.0020	M	2.441	2.541	0.0961	0.1000
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0316
b1	0.250	0.350	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.969 BASIC		Q	1.265	1.365	0.0498	0.0537
E	6.000 BASIC		2.362 BASIC		R	2.644	2.744	0.1041	0.1080
e	1.033 BASIC		0.0407 BASIC		S	1.500	1.600	0.0591	0.0630
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0335 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	





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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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